

TECHNICAL MANUAL

**OPERATOR'S, UNIT AND INTERMEDIATE
DIRECT SUPPORT, AND GENERAL SUPPORT
MAINTENANCE MANUAL**

**MICROWAVE FREQUENCY COUNTER TD-1225A(V)2/U
(HEWLETT-PACKARD MODEL 5342A/H16)
(NSN 6625-01-121-6934)**

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HEADQUARTERS, DEPARTMENT OF THE ARMY

1 OCTOBER 1988



5

SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK

1

DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL

2

IF POSSIBLE, TURN OFF THE ELECTRICAL POWER

3

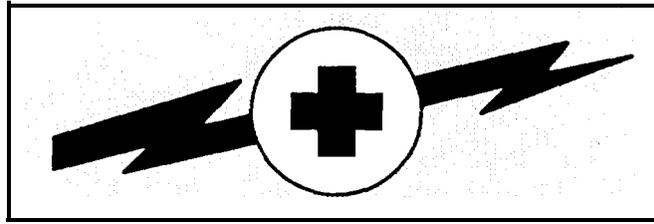
IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH, OR LIFT THE PERSON TO SAFETY USING A DRY WOODEN POLE OR A DRY ROPE OR SOME OTHER INSULATING MATERIAL

4

SEND FOR HELP AS SOON AS POSSIBLE

5

AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESPIRATION



WARNING

HIGH VOLTAGE

is used in the operation of this equipment

DEATH ON CONTACT

may result if personnel fail to observe safety precautions

Never work on electric equipment unless there is another person nearby who is familiar with the operation and hazards of the equipment and who is competent in administering first aid. When technicians are aided by operators, they must be warned about dangerous areas.

Be careful not to contact high-voltage connections of 115-volt ac input when installing or operating this equipment.

Whenever the nature of the operation permits, keep one hand away from the equipment to reduce the hazard of current flowing through vital organs of the body.



Do not be misled by the term "LOW VOLTAGE". Potentials as low as 50 volts may cause death under adverse conditions,

For Artificial Respiration refer to FM 21-11.

CAUTION



**THIS EQUIPMENT CONTAINS PARTS
AND ASSEMBLIES SENSITIVE TO
DAMAGE BY ELECTROSTATIC DISCHARGE (ESD).
USE ESD PRECAUTIONARY PROCEDURES WHEN TOUCHING,
REMOVING OR INSETING PRINTED CIRCUIT BOARDS.**

ESD CLASS 1

NOTE

The symbol for static sensitive devices in military inventory is as depicted in the caution block above

GENERAL HANDLING PROCEDURES FOR ESDS ITEMS

- .USE WRIST GROUND STRAPS OR MANUAL GROUNDING PROCEDURES
- .KEEP ESDS ITEMS IN PROTECTIVE COVERING WHEN NOT IN USE
- .GROUND ALL ELECTRICAL TOOLS AND TEST EQUIPMENT
- .PERIODICALLY CHECK CONTINUITY AND RESISTANCE OF GROUNDING SYSTEM
- .USE ONLY METALIZED SOLDER SUCKER HANDLING
- .ESDS ITEMS ONLY IN PROTECTED AREAS

MANUAL GROUNDING PROCEDURES

- . MAKE CERTAIN EQUIPMENT IS POWERED DOWN
- . TOUCH GROUND PRIOR TO REMOVING ESDS ITEMS
- . TOUCH PACKAGE OF REPLACEMENT ESDS ITEM TO GROUND BEFORE OPENING
- . TOUCH GROUND PRIOR TO INSERTING REPLACEMENT ESDS ITEMS

ESD PROTECTIVE PACKAGING AND LABELING

- INTIMATE COVERING OF ANTISTATIC MATERIAL WITH AN OUTER WRAP OF EITHER TYPE 1 ALUMINIZED MATERIAL OR CONDUCTIVE PLASTIC FILM OR HYBRID LAMINATED BAGS HAVING AN INTERIOR OF ANTISTATIC MATERIAL WITH AN OUTER METALIZED LAYER
- LABEL WITH SENSITIVE ELECTRONIC SYMBOL AND CAUTION NOTE

CAUTION

Devices such as CMOS, NMOS, MNOS, VMOS, HMOS, thin-film resistors PMOS, and MOSFET used in many equipments can be damaged by static voltages present in most repair facilities. Most of the components contain internal gate protection circuits that are partially effective, but sound maintenance practice and the cost of equipment failure in time and money dictate careful handling of all electrostatic sensitive components.

The following precautions should be observed when handling all electrostatic sensitive components and units containing such components.

CAUTION

Failure to observe all of these precautions can cause permanent damage to the electrostatic sensitive device. This damage can cause the device to fail immediately or at a later date when exposed to an adverse environment.

- STEP 1 Turn off and/or disconnect all power and signal source and loads used with the unit.
- STEP 2 Place the unit on grounded conductive work surfaces.
- STEP 3 Ground the repair operator using a conductive wrist strap or other device using a 1 -M series resistor to protect the operator.
- STEP 4 Ground any tools (including soldering equipment) that will contact the unit. Contact with the operator's hand provides a sufficient ground for tools that are otherwise electrically isolated.
- STEP 5 All electrostatic sensitive replacement components are shipped in conductive foam or tubes and must be stored in the original shipping container until installed,
- STEP 6 When these devices and assemblies are removed from the unit, they should be placed in the conductive work surface or in conductive containers.
- STEP 7 When not being worked on, wrap disconnected circuit boards in aluminum foil or in plastic bags that have been coated or impregnated with a conductive material.
- STEP 8 Do not handle these device unnecessarily or remove from their packages until actually used or tested.

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Technical Manual

No. 11-6625-3014-14-1

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, DC, 1 October 1988

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MICROWAVE FREQUENCY COUNTER TD 1225A(V)2/U
(HEWLETT-PACKARD MODEL 5342A/H16)
(NSN 6625-01-121-6934)**

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028, (Recommended Changes to Publications and Blank Forms) or 2028-2 located in back of this manual direct to: Commander, U.S. Army Communications-Electronics Command, ATTN: AMSEL-LC-ME-PS, Fort Monmouth, New Jersey 07703-5000,

In either case, a reply will be furnished to you.

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This manual is an authentication of the manufacturer's commercial literature which, through usage, has been found to cover the data required to operate and maintain this equipment, Since the manual was not prepared in accordance with military specifications, the format has not been structured to consider levels of maintenance.

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Section 0 INTRODUCTION

0-1. SCOPE.

This manual contains instructions for the operation and maintenance of Microwave Frequency Counter TD-1225A(V)2/U. Throughout this manual, the Microwave Frequency Counter TD-1225A(V)2/U is referred to as either the Instrument, Frequency Counter, 5342A, or 5342A/H16.

0-2. CONSOLIDATED INDEX OF ARMY PUBLICATIONS AND BLANK FORMS.

Refer to the latest issue of DA Pam 25-30 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

0-3. MAINTENANCE FORMS, RECORDS, AND REPORTS.

a. *Reports of Maintenance and Unsatisfactory Equipment.* Department of the Army forms and procedures used for equipment maintenance will be those prescribed by DA Pam 738-750 as contained in Maintenance Management Update.

b. *Reporting of Item and Packaging Deficiencies.* Fill out and forward SF 364 Report of Discrepancy (ROD) as prescribed in AR 735-11-2/DLAR 4140.55 /SECNAVINST 4355.18/AFR 400-54/MCO 4430.3J.

c. *Transportation Discrepancy Report (TDR) (SF 36D)* Fill out and forward Transportation Discrepancy in Report (TDR) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33C/AFR 75-18/MCO P4610.19D/DLAR 4500.15.

0-4. REPORTING EQUIPMENT IMPROVEMENT RECOMMENDATIONS (EIR'S).

If your TD-1225A(V)2/U needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design or performance. Put it on an SF 368 (Product Quality Deficiency Report). Mail it to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-PA-MA-D, Fort Monmouth, New Jersey 07703-5000. We'll send you a reply.

0-5. ADMINISTRATIVE STORAGE,

Administrative storage of equipment issued to and used by Army activities will have preventive maintenance performed in accordance with the PMCS charts before storing. When removing the equipment from administrative storage the PMCS should be performed to assure operational readiness.

0-6. DESTRUCTION OF ARMY ELECTRONICS MATERIEL.

Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2.

0-7. WARRANTY INFORMATION.

The TD-1225A(V)2/U is warranted by Hewlett-Packard Company for one year. Warranty starts on the date of shipment to the original buyer. Report all defects in material or workmanship to your supervisor who will take appropriate action.

0-8. SAFETY CONSIDERATIONS.

This product is a Safety Class I instrument; that is, one provided with a protective earth terminal. Before operating or servicing the TD-1225A(V)2/U, personnel should familiarize themselves with both the safety markings on the equipment and the safety information presented at the beginning of this manual.

0-9. TOOLS AND TEST EQUIPMENT CROSS REFERENCE.

The following is a cross-reference of test equipment from table 1-4 to Appendix B MAC test equipment.

Table 1-4 Model Number/Name	Appendix B MAC Tool Number/Name
AE 705-0048 Isolation Transformer HP 10842A Extender Kit HP 11667A Power Splitter HP 11048B 50 Ω Termination HP 1400-0734 AP Clips, 4 each HP 141T/8552A/8554B Spectrum Analyzer HP 1607A Logic State Analyzer HP 1740A Oscilloscope HP 3406A AC Voltmeter HP 3465A DC Voltmeter HP 436A Power Meter HP 5004A Signature Analyzer HP 5345A Frequency Counter HP 545A Logic Probe HP 546A Logic Pulser HP 547A Current Tracer HP 59401A Bus System Analyzer HP 651 B Signal Generator HP 8481A Power Sensor HP 8495B Step Attenuator HP 8620C/86222A Signal Generator HP 8620C/86290A Signal Generator HP 909A/012 50 Ω Termination	GIS-1000 Isolation Transformer HP 10842A Service Accessory Kit AN/USM-281C Oscilloscope System ME-416/U Voltmeter, Sampling HP 3490A and AN-PSM-45 Multimeter SG-763/U or SG-1121 (A)1/U Signal Generator HP 8620C/86222A Mainframe with Plug-in HP 8620C/86290A Mainframe with Plug-in

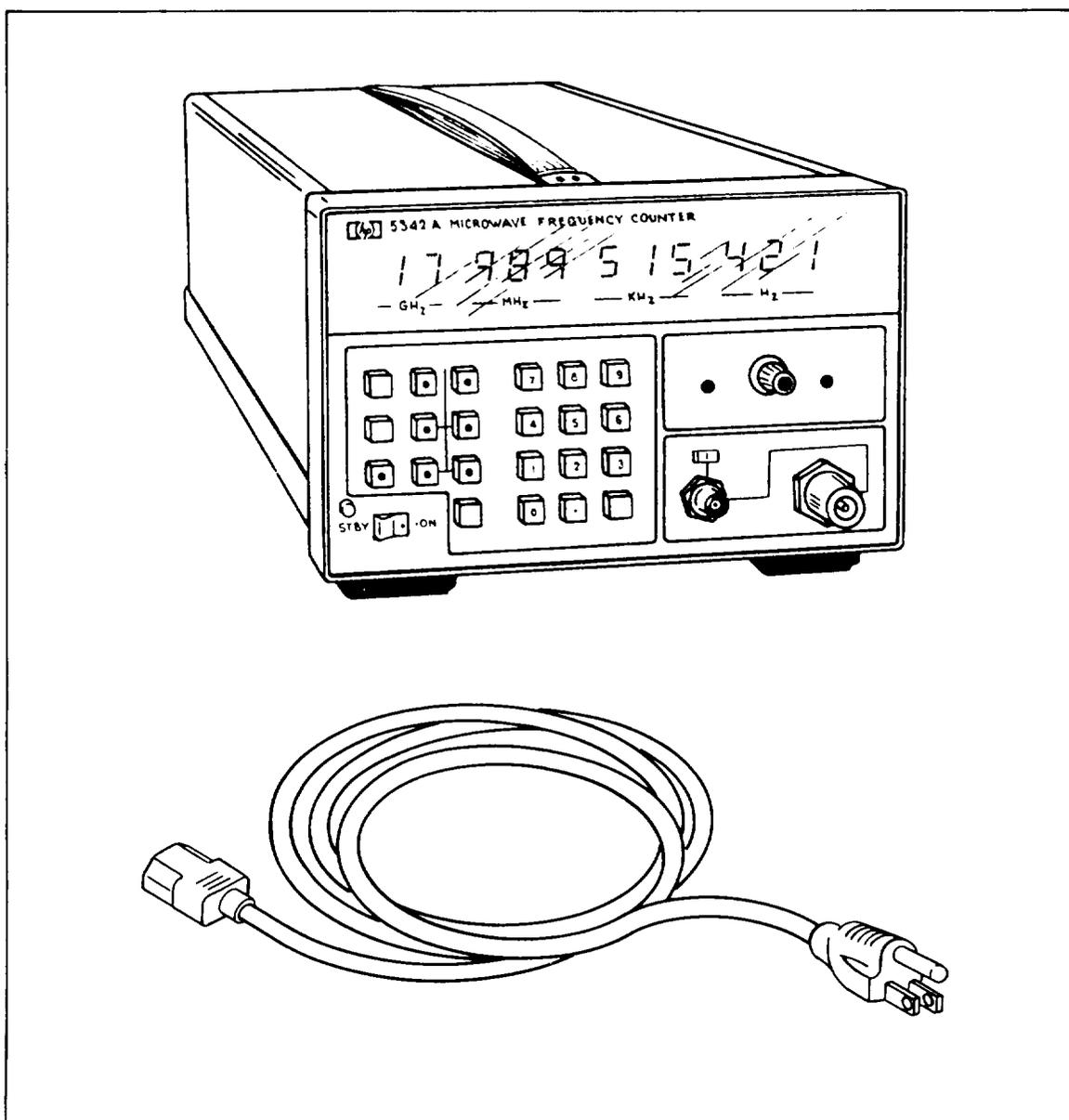
SECTION I GENERAL INFORMATION

1-1. INTRODUCTION

1-2. This manual provides operating and service information for the Hewlett-Packard Model 5342A Microwave Frequency Counter, shown in Figure 1-1.

1-3. SPECIFICATIONS

1-4. Specifications of the 5342A are listed in Table 1-1.



CE1LG001

Figure 1-1. Model 5342A Microwave Frequency Counter

Table 1-1. Model 5342A/H16 Specifications

INPUT CHARACTERISTICS**INPUT 1:****Frequency Range:** 500 MHz to 18 GHz**Sensitivity:** 500 MHz to 12.4 GHz -25 dBm. 12.4 GHz to 18 GHz -20 dBm.**Maximum Input:** +7 dBm**Dynamic Range:** 500 MHz to 12.4 GHz 32 dB. 12.4 GHz to 18 GHz 27 dB.**Impedance:** 50 ohms, nominal**Connector:** Precision Type N female**Damage Level:** +25 dBm, peak**Coupling:** dc to load, ac to instrument**SWR:** <2:1, 500MHz—10GHz Typical. <3:1, 10GHz—18GHz Typical.**FM Tolerance:** Switch selectable (rear panel)**FM (wide):** 50 MHz p-p worst case.**CW (normal):** 20 MHz p-p worst case. For modulation rates from dc to 10 MHz.**AM Tolerance:** Any modulation index, provided the minimum signal level is not less than the sensitivity specification.**Automatic Amplitude Discrimination:** Automatically measures the largest of all signals present, providing that signal is 6 dB above any signal within 500 MHz; 20 dB above any signal, 500 MHz—18 GHz.**Modes of Operation:****Automatic:** Counter automatically acquires and displays highest level signal within sensitivity range.**Manual:** Center frequency entered to within ± 40 MHz TYPICAL of true value; ± 25 MHz TYPICAL for frequencies below 825 MHz.**Acquisition Time:****Automatic mode:** Normal FM 530 ms worst case, wide FM 2.4 s worst case.**Manual Mode:** 80 ms after frequency entered.**INPUT 2:****Frequency Range:** 10 Hz to 520 MHz direct count.**Sensitivity:** 50 Ω 10 Hz to 520 MHz 25 mV rms. 1 M Ω 10 Hz to 25 MHz 50 mV rms.**Coupling:** ac**Connector:** Type BNC female.**Maximum Input:** 50 Ω 3.5V rms (+24 dBm) or 5V dc fuse protected; 1 M Ω 200V dc +5.0V rms.**TIME BASE (10811-60111)****Crystal Frequency:** 10 MHz**Stability:****Aging Rate:** $<5 \times 10^{-10}$ /day after 24-hour warm-up.**Temperature:** $<7 \times 10^{-9}$ over the range 0°C to 50°C.**Short Term:** $<5 \times 10^{-10}$ for 1 second average time.**Line Variation:** $<1 \times 10^{-10}$ over specified line voltage range.**External Time Base:** Requires 10 MHz, 3.0V (2.4V TYPICAL) peak-to-peak sine wave or square wave into 1 K Ω via rear panel BNC connector. Switch selects either internal or external time base.**Output:** 1V rms across 50 Ω available at the rear panel FREQ STD OUT (10 MHz).

Table 1-1. Model 5342A/H16 Specifications (Continued)

<p>GENERAL</p> <p>Accuracy: ±1 count ± time base error.</p> <p>Resolution: Front panel pushbuttons select 1 Hz to 1 MHz.</p> <p>Residual Stability: When counter and source use common time base or counter uses higher stability external time base, $<4 \times 10^{-11}$ rms TYPICAL.</p> <p>Display: 11-digit LED display, sectionalized to read GHz, MHz, kHz, and Hz.</p> <p>Self-Check: Selected from front panel pushbuttons. Measures 75 MHz for resolution chosen.</p> <p>Frequency Offset: Selected from front panel pushbuttons. Displayed frequency is offset by entered value to 1 Hz resolution.</p> <p>Sample Rate: Variable from less than 20 ms between measurements to HOLD which holds display indefinitely.</p> <p>IF Out: Rear panel BNC connector provides 25 MHz to 125 MHz output of down-converted microwave signal.</p> <p>Operating Temperature: 0°C to 50°C.</p> <p>Power Requirements: 100 +5, -10%, 48-66 Hz. 115 ±10%, 47-63 Hz and 380-420 Hz. 230 ±10%, 47-63 Hz. 240 +5, -10%, 48-66 Hz 100 VA max.</p> <p>Accessories Furnished: Power cord, 229 cm (7½-ft.)</p> <p>Size: 133 mm H × 213 mm W × 498 mm D (5¼" × 8¾" × 19⅝").</p> <p>Weight: Net 9.1 kg (20 lbs.). Shipping 12.7 kg (28 lbs.).</p>
--

1-5. SAFETY CONSIDERATIONS

1-6. This product is a Safety Class I instrument (provided with a protective earth terminal). Safety information pertinent to the operation and servicing of this instrument is included in appropriate sections of this manual.

1-7. INSTRUMENT IDENTIFICATION

1-8. Hewlett-Packard instruments have a 2-section, 10-character serial number (0000A00000), which is located on the rear panel. The four-digit serial prefix identifies instrument changes. If the serial prefix of your instrument differs from that listed on the title page of this manual, there are differences between this manual and your instrument. Instruments having higher serial prefixes are covered with a "Manual Changes" sheet included with this manual. If the change sheet is missing, contact the nearest Hewlett-Packard Sales and Service Office listed at the back of this manual. This manual covers serial number prefix 2746A and above.

1-9. ACCESSORIES

1-10. Table 1-2 lists accessory equipment supplied and Table 1-3 lists accessories available.

Table 1-2. Equipment Supplied

DESCRIPTION	HP PART NUMBER
Detachable Power Cord 229 cm (7½ feet long)	8120-1378

Table 1-3 Accessories Available

DESCRIPTION	HP PART NUMBER
Bail Handle Kit	5061-2002
Rack Mounting Adapter Kit	5061-9677
Rack Mounting Adapter Kit with slot for access to front connectors from rear.	K70-59992A
Transit Case	9211-2682
Service Accessory Kit (refer to paragraph 1-16)	Model 10842A
Microwave Attenuators	Model 8491B, 8494/5/6H
Signature Analyzer	Model 5004A

1-11. DESCRIPTION

1-12. The 5342A Microwave Frequency Counter measures the frequency of signals in the range of 10 Hz to 18 GHz, with a basic sensitivity of -25 dBm. Signals in the frequency range of 10 Hz to 500 MHz are measured by the direct count method. Signals in the frequency range of 500 MHz to 18 GHz are down-converted to an IF by a heterodyne conversion technique for application to the counter circuits. The unique conversion technique employed results in high sensitivity and FM tolerance in addition to automatic amplitude discrimination. The counted IF is added to the local oscillator frequency to determine the unknown frequency for display.

1-13. Deleted

1-14. Deleted

1-15. SERVICE EQUIPMENT AVAILABLE

1-16. Extender boards are available for servicing printed circuit assemblies while extended from the instrument. The extender boards allow assemblies to be extended from their plug-in connectors for monitoring with appropriate test equipment. Extender boards for each assembly are supplied in Service Accessory Kit 10842A as described in paragraph 8-46.

1-17. RECOMMENDED TEST EQUIPMENT

1-18. The test equipment listed in Table 1-4 is recommended for use during performance tests, adjustments, and troubleshooting. Substitute test equipment may be used if it meets the required characteristics listed in the table.

Table 1-4. Recommended Test Equipment

INSTRUMENT	REQUIRED CHARACTERISTICS	USE*	RECOMMENDED MODEL
Oscilloscope	100 MHz bandwidth	T,A,OV,P	HP 1740A
Signal Generator	10 Hz—10 MHz 10 MHz—2.4 GHz 2 GHz—18 GHz	T,A,OV,P	HP 651B HP 8620C/86222A HP 8620C/86290A
Spectrum Analyzer	RF inputs from 1MHz – 500MHz RES BW 100kHz	T,A,P	HP 141T/8552A/8554B
DC Voltmeter	20V Range, 0.05V Resolution	T,A	HP 3465A
AC Voltmeter	10 MHz-350 MHz	T,A	HP 3406A
Frequency Counter	100MHz to 400MHz, 50Ω 100kHz MIN resolution	T	HP 5345A
Logic State Analyzer	HP 1740A compatibility	T	HP 1607A (use with HP 1740A)
Signature Analyzer	5342A compatibility	T	HP 5004A
Power Splitter	DC—18 GHz	OV,P	HP 11667A
Logic Pulser	TTL compatibility	T	HP 546A
Current Tracer	1 mA—1 A range	T	HP 547A
Logic Probe	TTL compatibility	T	HP 545A
Step Attenuator	DC—18 GHz 10 dB steps	OV,P	HP 8495B
AP Clips (4)	Clip for 14 pin/16 pin IC's	T	HP P/N 1400-0734
Isolation Transformer	120V IN — Isolated 120V OUT	T	Allied Electronics P/N 705-0048
Extender Boards	2 × 10 pin 2 × 12 pin 2 × 15 pin 2 × 18 pin (2) 2 × 22 pin (2) 2 × 24 pin A 14 Extender A15 Extender	T	HP P/N 05342-60030 HP P/N 05342-60031 HP P/N 05342-60032 HP P/N 05342-60033 HP P/N 05342-60034 HP P/N 05342-60035 HP P/N 05342-60036 HP P/N 05342-60039
Power Meter	10MHz to 18GHz ±0.1dBm	A,OV,P	HP 436A
Power Sensor	10 MHz—18 GHz -30 dBm to +20 dBm	A,OV,P	HP 8481A
50Ω Termination	DC—18 GHz	P	HP 909A (Option 012)
Power Supply	480 mA @ 20V (2 required)		6215A
Feedthru Termination	50 ohms		11048B
Signal Generator Mainframe	(Two Microwave sources needed for automatic amplitude discrimination test — see paragraph 4-35)	P	HP 8620C Mainframe
Bus System Analyzer	Control HP-IB lines		HP 59401A

*T = Troubleshooting
A = Adjustments

OV = Operational Verification
P = Full Performance Testing

SECTION II INSTALLATION

2-1. INTRODUCTION

2-2. This section contains information for unpacking, inspection, storage, and installation.

2-3. UNPACKING AND INSPECTION

2-4. If the shipping carton is damaged, inspect the instrument for visible damage (scratches, dents, etc.). If the instrument is damaged, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately (offices are listed at the back of this manual). Keep the shipping carton and packing material for the carrier's inspection. The Hewlett-Packard Sales and Service Office will arrange for repair or replacement of your instrument without waiting for the claim against the carrier to be settled.

2-5. INSTALLATION REQUIREMENTS

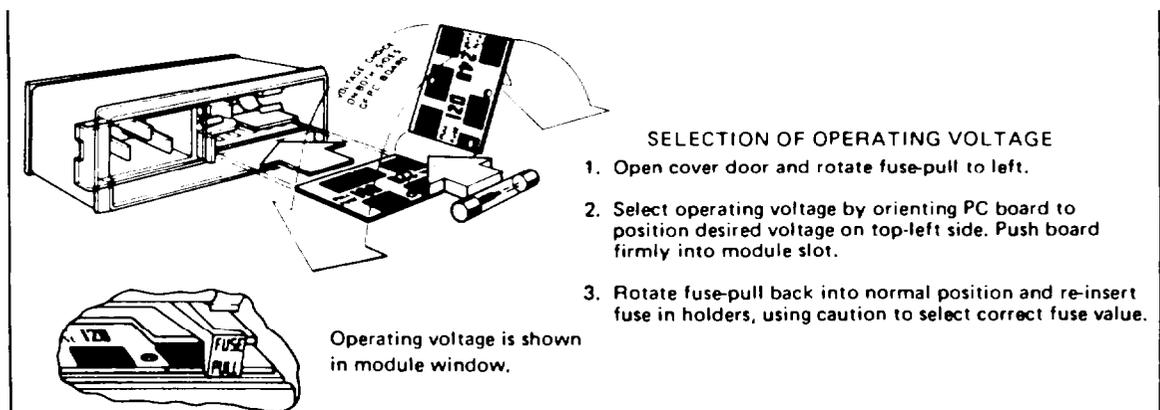
CAUTION

**Before connecting the instrument to ac power lines,
be sure that the voltage selector is properly
positioned as described below.**

2-6. **LINE VOLTAGE REQUIREMENTS.** The 5342A is equipped with a power module that contains a printed-circuit line voltage selector to select 100-, 120-, 220-, or 240-volt ac operation. Before applying power, the pc selector must be set to the correct position and the correct fuse must be installed as described below.

2-7. Power line connections are selected by the position of the plug-in circuit card in the module. When the card is plugged into the module, the only visible markings on the card indicate the line voltage to be used. The correct value of line fuse, with a 250-volt rating, must be installed after the card is inserted. This instrument uses a 1.00A fuse (HP Part No. 2110-0007) for 100/120-volt operation; a 0.500A fuse (HP Part No. 2110-0202) for 220/240-volt operation.

2-8. To convert from one line voltage to another, the power cord must be disconnected from the power module before the sliding window covering the fuse and card compartment can be moved to expose the fuse and circuit card. See Figure 2-1.

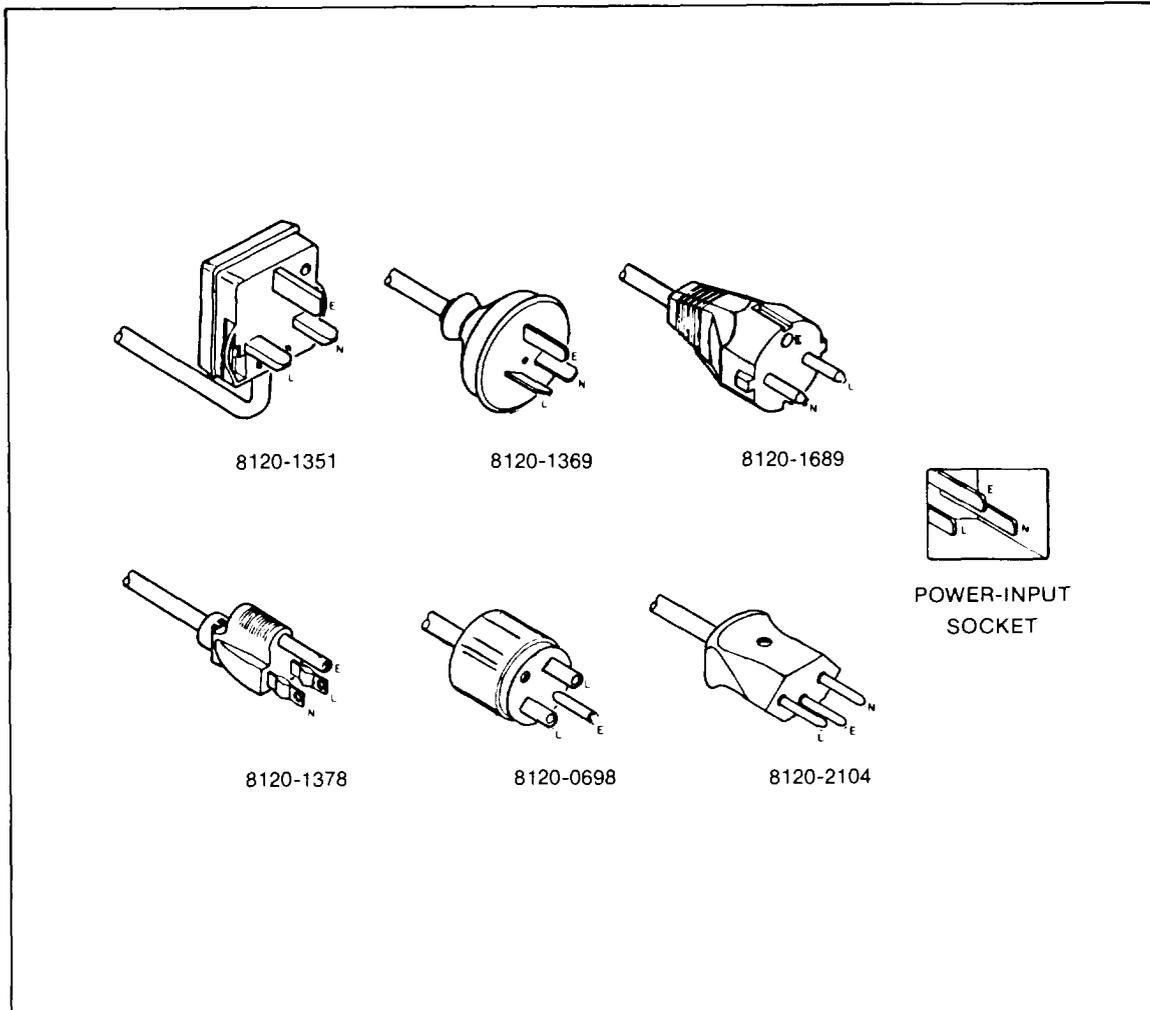


CE1LG002

Figure 2-1. Line Voltage Selection

2-9. Power Cable

2-10. The 5342A is shipped with a three-wire power cable. When the cable is connected to an appropriate ac power source, this cable connects the chassis to earth ground. The type of power cable plug shipped with each instrument depends on the country of destination. Refer to Figure 2-2 for the part numbers of the power cable and plug configurations available.



CE1LG003

Figure 2-2. Power Cable HP Part Numbers versus Mains Plugs Available

WARNING

BEFORE SWITCHING ON THIS INSTRUMENT, THE PROTECTIVE EARTH TERMINALS OF THIS instrument MUST BE CONNECTED TO THE PROTECTIVE CONDUCTOR OF THE (MAINS) POWER CORD. THE MAINS PLUG SHALL ONLY BE INSERTED IN A SOCKET OUTLET PROVIDED WITH A PROTECTIVE EARTH CONTACT. THE PROTECTIVE ACTION MUST NOT BE NEGATED BY THE USE OF AN EXTENSION CORD (POWER CABLE) WITHOUT A PROTECTIVE CONDUCTOR (GROUNDING).

2-11. Operating Environment

2-12. TEMPERATURE. The 5342A may be operated in temperatures from 0°C to +55°C.

2-13. HUMIDITY. The 5342A may be operated in environments with humidity up to 95%. However, it should be protected from temperature extremes which cause condensation in the instrument.

2-14. ALTITUDE. The 5342A may be operated at altitudes up to 4,600 metres (15,000 feet).

2-15. STORAGE AND SHIPMENT

2-16. Environment

2-17. The instrument may be stored or shipped in environments within the following limits:

TEMPERATURE	-40 °C to +75°C
HUMIDITY	up to 95%
ALTITUDE	7,620 metres (25,000 feet)

2-18. The instrument should also be protected from temperature extremes which cause condensation within the instrument.

2-19. Packaging

2-20. ORIGINAL PACKAGING. Containers and materials identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is being returned to Hewlett-Packard for servicing, attach a tag indicating the type of service required, return address, model number, and full serial number. Also, mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

2-21. OTHER PACKAGING. The following general instructions should be used for repacking with commercially available materials:

- a. Wrap instrument in heavy paper or plastic. (If shipping to Hewlett-Packard office or service center, attach tag indicating type of service required, return address, model number, and full serial number.)
- b. Use strong shipping container. A double-wall carton made of 350-pound test material is adequate.
- c. Use a layer of shock-absorbing material 70 to 100 mm (3- to 4-inch) thick around all sides of the instrument to provide firm cushioning and prevent movement inside container. Protect control panel with cardboard.
- d. Seal shipping container securely.
- e. Mark shipping container FRAGILE to ensure careful handling.
- f. In any correspondence, refer to instrument by model number and full serial number.

2-22 through 2-35. Deleted.

2-36. HP-IB Interconnections

2-37. HEWLETT-PACKARD INTERFACE BUS. Interconnection data concerning the rear panel HP-IB connector is provided in Figure 2-3. This connector is compatible with the HP 10631A/B/C/D HP-IB cables. The HP-IB system allows interconnection of up to 15 (including the controller) HP-IB compatible instruments. The HP-IB cables have identical "piggy back" connectors on both ends so that several cables can be connected to a single source without special adapters or switch boxes. System components and devices may be connected in virtually any configuration desired. There must, of course, be a path from the calculator (or other controller) to every device operating on the bus. As a practical matter, avoid stacking more than three or four cables on any one connector. If the stack gets too large, the force on the stack produces great leverage which can damage the connector mounting. Be sure each connector is firmly (finger tight) screwed in place to keep it from working loose during use.

2-38. CABLE LENGTH RESTRICTIONS. To achieve design performance with the HP-IB, proper voltage levels and timing relationship must be maintained. If the system cable is too long, the lines cannot be driven properly and the system will fail to perform properly. Therefore, when interconnecting an HP-IB system, it is important to observe the following rules:

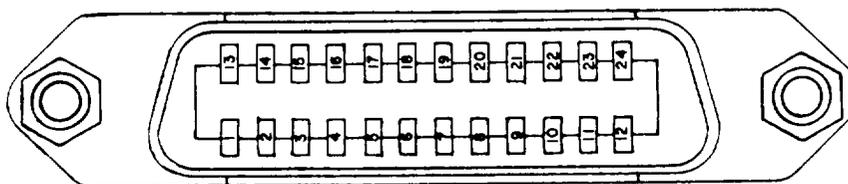
- a. The total cable length for the system must be less than or equal to 20 metres (65 feet).
- b. The total cable length for the system must be equal to or less than 2metres (6.6 feet) times the total number of devices connected to the bus.
- c. The total number of instruments connected to the bus must not exceed 15.

2-39. 5342A Listen Address

2-40. The 5342A contains a rear panel HP-IB Instrument address selection switch. There are five switches designated (A5, A4, A3, A2, A1) which are used to select the address. Instructions for setting and changing the listen address are provided in Section III of this manual along with programming codes.

2-41. HP-IB Descriptions

2-42. A description of the HP-IB is provided in Section III of this manual. A study of this information is necessary if the user is not familiar with the HP-IB concept. Additional information concerning the design criteria and operation of the bus is available in IEEE Standard 488-1975, titled "IEEE Standard Digital Interface for Programmable Instrumentation".

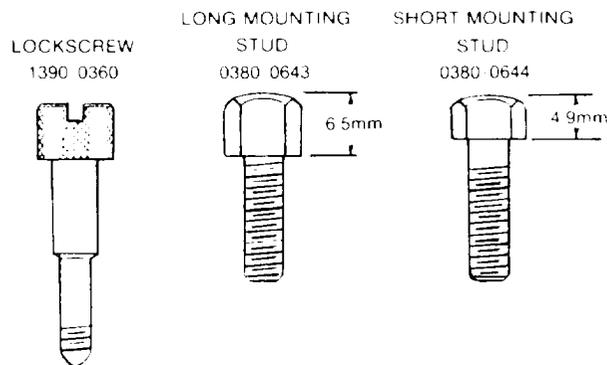


PIN	LINE
1	DIO1
2	DIO2
3	DIO3
4	DIO4
13	DIO5
14	DIO6
15	DIO7
16	DIO8
5	EO1
17	REN
6	DAV
7	NRFD
8	NDAC
9	IFC
10	SRQ
11	ATN
12	SHIELD-CHASSIS GROUND
18	P O TWISTED PAIR WITH PIN 6
19	P O TWISTED PAIR WITH PIN 7
20	P O TWISTED PAIR WITH PIN 8
21	P O TWISTED PAIR WITH PIN 9
22	P O TWISTED PAIR WITH PIN 10
23	P O TWISTED PAIR WITH PIN 11
24	ISOLATED DIGITAL GROUND

THESE PINS ARE INTERNALLY GROUNDED

CAUTION

The 5342A contains metric threaded HP-IB cable mounting studs as opposed to English threads. Metric threaded HP 10631A, B, C, or D HP-IB cable lock screws must be used to secure the cable to the instrument. Identification of the two types of mounting studs and lock screws is made by their color. English threaded fasteners are colored silver and metric threaded fasteners are colored black. DO NOT mate silver and black fasteners to each other or the threads of either or both will be destroyed. Metric threaded HP-IB cable hardware illustrations and part numbers follow.



Logic Levels

The Hewlett-Packard Interface Bus logic levels are TTL compatible, i.e., the true (1) state is 0.0V dc to 0.4V dc and the false (0) state is +2.5V dc to +5.0V dc.

Programming and Output Data Format

Refer to Section III, Operation

Mating Connector

HP 1251-0293; Amphenol 57-30240.

Mating Cables Available

- HP 10631A, 0.9 metres (3 ft.), HP 10631B, 1.8 metres (6 ft.)
- HP 10631C, 3.7 metres (12 ft.)
- HP 10631D, 0.5 metres (1.5 ft.)

Cabling Restrictions

1. A Hewlett-Packard Interface Bus System may contain no more than 1.8 metres (6 ft.) of connecting cable per instrument
2. The maximum accumulative length of connecting cable for any Hewlett-Packard Interface Bus System is 20.0 metres (65.6 ft.).

CE1LG004

Figure 2-3. Hewlett-Packard Interface Bus Connection

SECTION III OPERATION

3-1. INTRODUCTION

3-2. This section contains operating information including operating characteristics, descriptions of controls and indicators, and operating procedures.

3-3. OPERATING CHARACTERISTICS

3-4. The following paragraphs describe the operating ranges and modes, resolution, sample rate, AM and FM characteristics, and auto-amplitude discrimination. Front panel controls and indicators are described in Figure 3-1, rear panel controls and connectors are described in Figure 3-2. Operating procedures are explained in Figure 3-3.

3-5. Operating Ranges

3-6. There are two basic operating ranges: 10 Hz to 500 MHz and 500 MHz to 18 GHz. Frequencies in the lower range are measured directly while measurements in the 500 MHz to 18 GHz range are made indirectly by a harmonic heterodyne down-conversion technique. Provision is made to select either range by a front-panel slide switch. A separate input connector is provided for each range. When the range switch is in the 10Hz—500 MHz position, the signal at the BNC connector is routed to the direct count circuits of the 5342A. In this range, input impedance is selectable via the 50 Ω – 1 M Ω) switch. When the range switch is in the 500 MHz—18 GHz range, the input signal is applied via the front-panel type N connector to the down-conversion circuits of the 5342A.

3-7. Resolution Keys

3-8. The best case resolution is the value represented by the least significant digit (LSD) in the display. In the 5342A, a maximum resolution of 1 Hz can be selected (by the pushbutton keys on the front panel labeled in blue, preceded by the blue key being pressed). The display is divided into four sections for ease of determining GHz, MHz, kHz, and Hz resolution. Half-sized \square 's are used as space fillers within a section to improve interpretation of the display. For example, a signal measured to 100 kHz resolution will be displayed thus:



 — GHz — — MHz — — kHz — — Hz —

The two filler \square 's in the kHz section indicate immediately that the \square represents hundreds of kilohertz. The Hz section is blanked.

3-9. The pushbutton keys on the front panel under the RESOLUTION label are used for other purposes when the blue key is not in effect (has not been pressed). When the blue key has not been pressed, the keys are defined by the black number on the keys and are used to enter frequency offsets, manual center frequencies, and amplitude offsets as described in Figure 3-1.

3-10. CHECK, DAC, and ENTER keys

3-11. The CHECK, DAC, and ENTER keys are used as described in Figure 3-1.

3-12. FREQ Keys

3-13. Two of the pushbutton keys on the front panel under the FREQ label are used to select the automatic or manual mode of operation. The other keys in this section of the keyboard control the use of the RESOLUTION keys. Use of these keys is described in detail in Figure 3-7.

3-14. Automatic Mode

3-15. The automatic mode of operation is selected by pressing the AUTO key. Input signals in the 500 MHz—18 GHz range are acquired, measured, and displayed automatically. When power is initially turned on, the 5342A goes into this mode automatically.

3-16. Manual Mode

3-17. The manual mode of operation is selected by pressing the MAN (MHz) key. To operate in this mode, input signals in the 500 MHz—18GHz range must be known to within 50 MHz and this frequency (called the manual center frequency) must be entered into the display prior to the measurement. Use of the manual mode is described in detail in Figure 3-3.

3-17a. The manual mode of operation is generally selected when the acquisition time during automatic operation is longer than desired. Acquisition time is the time involved to acquire the signal to be measured and determine the harmonic number, and is typically 450ms. Manual operation reduces this dead-time between measurements and provides faster updates of the measured signal.

3-17b. One disadvantage of manual operation is that the frequency to be measured must typically be within 40 MHz (25 MHz for frequencies below 825 MHz) of the manual center frequency selected. If the input signal drifts beyond this limit, signal dropout may occur and the display will read zero. Two forms of corrective action exist once the manual center frequency has been entered and the 5342A has failed to measure the signal.

1. Press the 5342A front panel AUTO key. After the measured signal is displayed, press the MAN (MHz) key. This procedure automatically produces the correct manual center frequency.
2. Reenter the manual center frequency which is closer to the actual frequency of the signal to be measured. Refer to figure 3-3 on page 3-9.

3-18. Offset Frequencies

3-19. It is sometimes desirable to add or subtract a constant to/from a frequency measurement. For example, by measuring a radio IF and knowing the LO, the counter can display the RF input when the LO frequency is entered as a positive offset. It may be easier to tune an oscillator to a specific frequency if the desired frequency is entered as a negative offset and the oscillator tuned until the counter reads zero. Frequency offsets are described in Figure 3-3.

3-20. Deleted

3-21. Deleted

3-22. Deleted

3-23. Deleted

3-24. SET, RESET, RECALL, and CHS Keys

3-25. The SET, RESET, RECALL, and CHS keys allow offsets and center frequencies to be entered, reset the measurement process, recall previous values, and change the sign of offsets as described in Figure 3-3.

3-26. SAMPLE RATE, GATE, and REMOTE

3-27. The SAMPLE RATE control adjusts the deadtime between the end of one measurement and the start of the next measurement. The duration of the measurement is determined by the resolution selected. The SAMPLE RATE is variable between <20 ns and HOLD. In HOLD position the display will hold the measurement displayed indefinitely.

3-28. The GATE indicator is lit during the measurement interval (gate time) when the counter's gate is open and accumulating counts.

3-29. The REMOTE indicator is lit when the 5342A is in remote operation.

3-30. AM Tolerance

3-31. The 5342A will measure carrier frequencies containing amplitude modulation to any modulation index provided the minimum voltage of the signal is not less than the sensitivity specification of the 5342A.

3-32. FM Tolerance

3-33. The 5342A will measure carrier frequencies which are modulated in frequency such as a microwave radio carrier. The FM tolerance is the worst case FM deviation which can be present without affecting the counters ability to acquire the signal. If the deviations about the carrier are symmetrical, then the counter averages out the deviations to measure the actual carrier frequency. The FM tolerance is determined by the position of the CW-FM switch on the rear panel. The CW position provides FM tolerance of 20 MHz peak-to-peak. The FM position provides a tolerance of 50 MHz peak-to-peak but results in slower acquisition time (2.4 seconds compared to 530 milliseconds for CW position).

NOTE

Most measurements should be made with the rear panel FM/CW switch in CW position. The FM position should be used only when the input signal has significant amounts of FM (>20 MHz p-p). Incorrect measurements may result if the FM position is used with a stable input (non-FM) signal which has been locked to the counter's time base.

3-34. Automatic Amplitude Discrimination

3-35. The automatic amplitude discrimination feature allows the 5342A to acquire and display the highest level signal within its sensitivity range. The highest level signal must be 20 dB greater in amplitude than any other signal present. Typical operation is approximately 10dB. This feature is useful for discriminating against spurious signals and harmonics.

3-36. MAXIMUM INPUT SIGNAL POWER**CAUTION**

Do not exceed +25 dBm (peak) of input power at the type N connector (500 MHz–18 GHz). Damage to the internal sampler may occur. Refer to paragraph 3-37 for detailed explanation.

3-37. The 5342A will function within specifications for 500 MHz—18 GHz signal inputs up to +7dBm (standard unit). Under no circumstances should the input level to the 5342A exceed +25 dBm. If the input power exceeds this level, damage to the internal sampler may occur and the sampler is expensive to replace. Measurements from +7 to +25 dBm are not recommended as false readings may occur. When signal levels exceed +7dBm external attenuators should be used to attenuate the signal.

3-38. The 10 Hz—500 MHz direct count input BNC connector is fuse-protected for a maximum input level of 3.5V rms (+24 dBm).

3-39. INPUT CABLE CONSIDERATIONS

3-40. Consideration should be given to input cable losses at higher frequencies. For example, a 6-foot section of RG-214/U coaxial cable has about 15 dB loss at 18 GHz. Such losses must be taken into consideration along with the sensitivity specifications given in Tab/e 1-1.

3-41. CONTROLS, INDICATORS, AND CONNECTORS

3-42. Figure 3-7 describes the front panel controls, indicators, and connectors. Figure 3-2 describes the rear panel connectors and controls.

WARNING

BEFORE THE INSTRUMENT IS SWITCHED ON, ALL PROTECTIVE EARTH TERMINALS, EXTENSION CORDS, AUTOTRANSFORMERS AND DEVICES CONNECTED TO IT SHOULD BE CONNECTED TO A PROTECTIVE EARTH GROUNDED SOCKET. ANY INTERRUPTION OF THE PROTECTIVE EARTH GROUNDING WILL CAUSE A POTENTIAL SHOCK HAZARD THAT COULD RESULT IN PERSONAL INJURY.

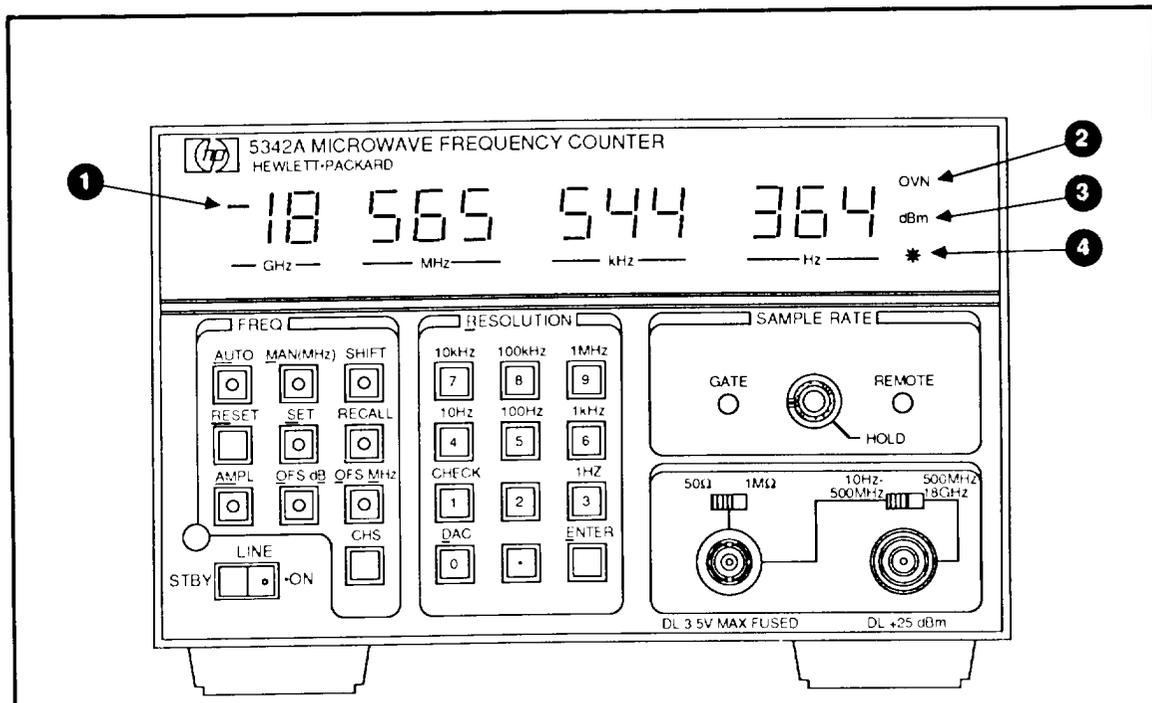
ONLY FUSES WITH THE REQUIRED RATED CURRENT AND SPECIFIED TYPE SHOULD BE USED. DO NOT USE REPAIRED FUSES OR SHORT CIRCUITED FUSEHOLDERS. TO DO SO COULD CAUSE A SHOCK OR FIRE HAZARD.

CAUTION

Before the instrument is switched on, it must be set to the voltage of the power source, or damage to the instrument may result. (Refer to paragraph 2-6.)

3-43. OPERATING PROCEDURES

3-44. Figure 3-3 illustrates operating procedures for the standard 5342A. Self-check procedures are also given in Figure 3-3. An operators keyboard check is given in paragraph 3-45.



CE1LG005

DISPLAY

Digits:

The display contains 11 digit positions, two digits for frequencies in GHz and three digits each for MHz, kHz, and Hz.

Annunciators:

– Sign ① When lighted, indicates a negative frequency offset has been entered into display (MHz).

OVN indicator ② Oven monitor indicates when crystal oscillator oven is on (warming). When warmed-up, light goes out

dBm indicator ③ Not used.

* indicator ④ When lighted, indicates the rear panel CW-FM switch is in FM position. This selects the wide-band mode which provides wider FM (50 MHz p-p) tolerance.

FREQ Keys

The FREQ keys select the mode of operation and control the display.

NOTE

Some keys are equipped with center indicator lights that serve as “prompters” to the user. A blinking indicator light states a “ready” condition for the key function that was selected and the instrument is waiting for a mode or number to be entered. A steady indicator light states that the key function that was selected is in operation.

AUTO key. Selects the automatic mode of operation to acquire and display input signal frequencies in the 500 MHz—18 GHz range. The instrument goes into this mode when power is turned on.

MAN (MHz) key. Selects manual mode for input signal frequencies in the 500 MHz—18 GHz range. Input signal frequency must be known (within 50 MHz) and entered into display via the black-numbered keys.

Figure 3-1. front Panel Controls and Indicators

Blue key. Pressing this key activates the blue-labeled functions of the RESOLUTION keys.

RESET key. Clears the display and restarts a measurement. Clears any blinking lights in key center indicators.

SET key. Must be pressed prior to selecting OFS dB, OFS MHz or MAN (MHz). The SET condition is indicated by lighted segments $\equiv \equiv$ in the GHz digits of the display. This indicates that a center frequency, offset frequency, or amplitude offset may be entered into the display.

RECALL key. Recalls stored memory information into display. The MAN (MHz), OFS dB, or OFS MHz keys, if **held in** after RECALL is pressed, will result in a display of previously entered or computed information.

NOTE

Information stored in memory (by digit keys) after MAN (MHz) key is pressed is available for display until AUTO mode is selected. Then the center frequency determined by the automatic measurement overrides the manual information.

AMPL key. Not used.

OFS dB key. Not used.

OFS MHz key. After pressing the SET key, the OFS MHz key is pressed prior to entering an offset value via the digit keys. (Digit keys are labeled in black numbers under RESOLUTION.) Indicates selection of frequency offset mode when lighted and adds frequency offset to measured frequency.

RESOLUTION keys:

The resolution keys select the display resolution (according to the blue labeling above each key) after the blue key is pressed. The keys are defined by the black number labeled on the key when entering offsets and manual center frequencies.

CHECK key. After pressing the blue key, the CHECK key is pressed to perform a self-check of the instrument. The display will indicate 75 MHz for proper operation. Press RESET to exit self-check.

NOTE

The instrument must not have an **input signal connected** at the 500 MHz—18 GHz input to perform the self-check.

ENTER key. Used to enter digits for manual center frequencies or offsets into memory via black-numbered keys. After the digits have been selected, ENTER key is pressed to signal the end of the digit sequence.

LINE switch. In ON position, applies power to all circuits except the crystal oven. The crystal oven connects through a separate transformer, a thermal circuit breaker and fuse directly to the ac line. This allows the oven to maintain its operating temperature and accuracy when the LINE switch is in STBY position, thereby eliminating warmup delays.

SAMPLE RATE control. Adjusts the interval between measurements from 20 ms to HOLD. When rotated to HOLD will hold display indefinitely.

GATE indicator. Indicates when counters main gate is open and a measurement is in progress.

REMOTE indicator. Illuminates when counter is in remote operation.

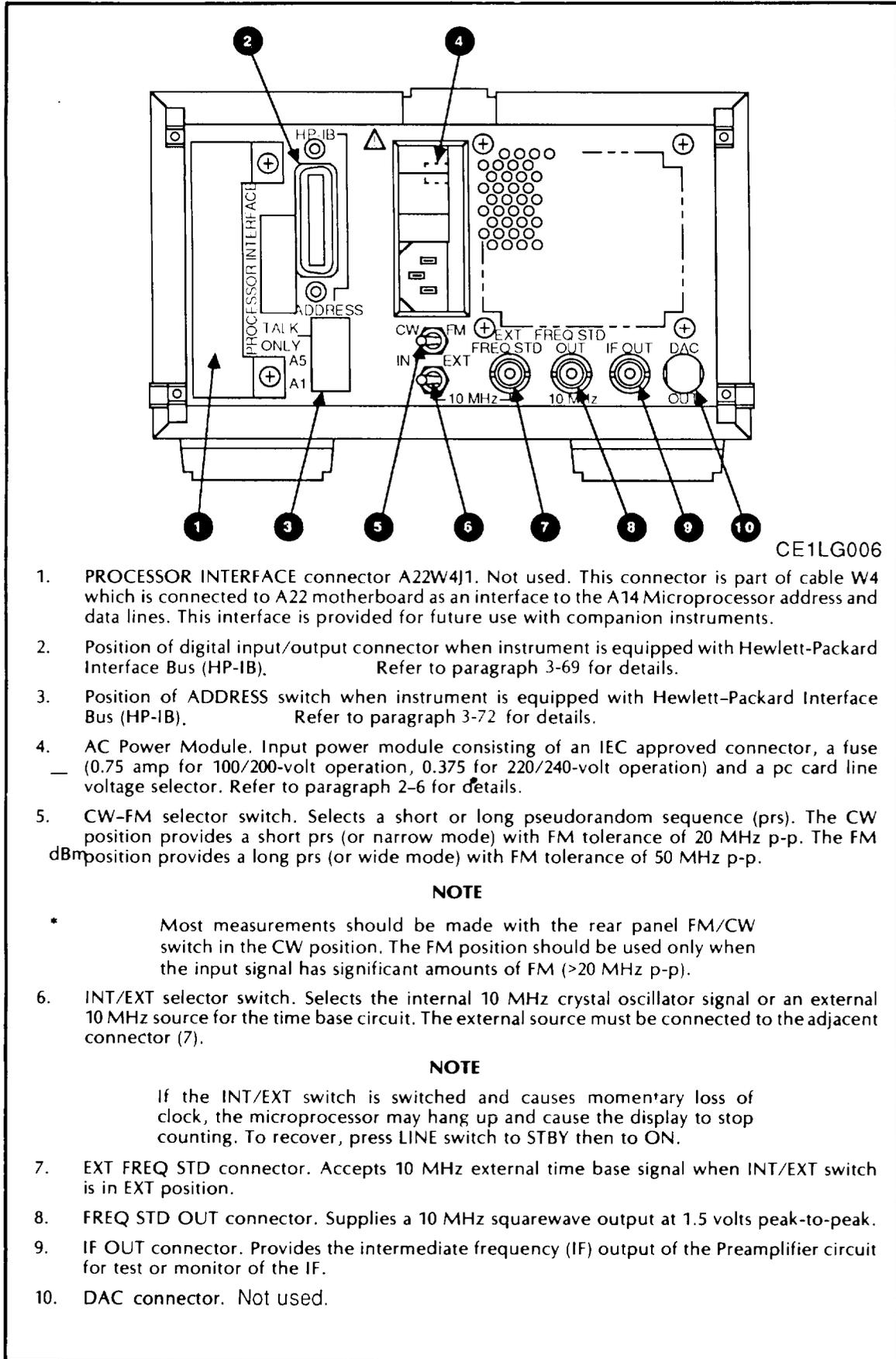
50 Ω —1 M Ω switch. Selects input impedance for adjacent 10 Hz—500 MHz input connector.

10 Hz—500 MHz, 500 MHz—18 GHz switch. Selects either low or high frequency range input connector.

BNC Input Connector. Accepts 10 Hz—500 MHz input for direct count measurements. Measurements made at this input require that the range switch is set to the 10 Hz—500 MHz position. Sensitivity is listed in *Table 1-1*.

Type N Input Connector. Input for measurements in the 500 MHz—18 GHz range. Measurements made at this input require that the range switch is set to the 500 MHz—18 GHz position. Sensitivity is listed in *Table 1-1*.

Figure 3-1. Front Panel Controls and indicators (Continued)



1. PROCESSOR INTERFACE connector A22W4J1. Not used. This connector is part of cable W4 which is connected to A22 motherboard as an interface to the A14 Microprocessor address and data lines. This interface is provided for future use with companion instruments.
2. Position of digital input/output connector when instrument is equipped with Hewlett-Packard Interface Bus (HP-IB). Refer to paragraph 3-69 for details.
3. Position of ADDRESS switch when instrument is equipped with Hewlett-Packard Interface Bus (HP-IB). Refer to paragraph 3-72 for details.
4. AC Power Module. Input power module consisting of an IEC approved connector, a fuse (0.75 amp for 100/200-volt operation, 0.375 for 220/240-volt operation) and a pc card line voltage selector. Refer to paragraph 2-6 for details.
5. CW-FM selector switch. Selects a short or long pseudorandom sequence (prs). The CW position provides a short prs (or narrow mode) with FM tolerance of 20 MHz p-p. The FM position provides a long prs (or wide mode) with FM tolerance of 50 MHz p-p.

NOTE

- * Most measurements should be made with the rear panel FM/CW switch in the CW position. The FM position should be used only when the input signal has significant amounts of FM (>20 MHz p-p).

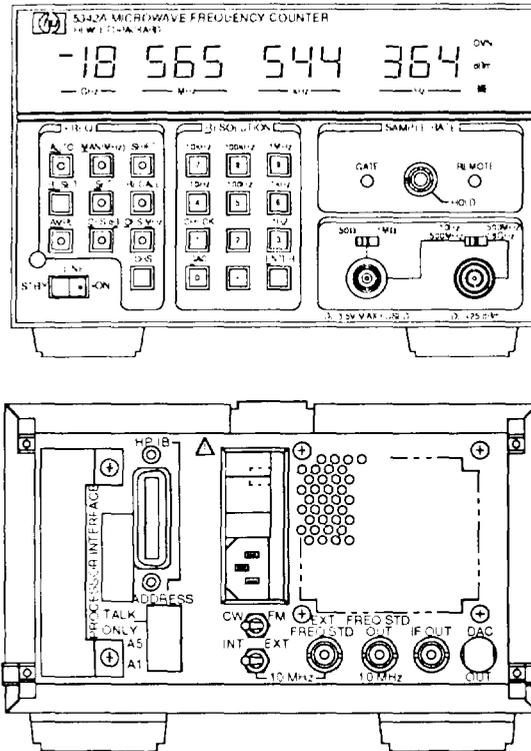
6. INT/EXT selector switch. Selects the internal 10 MHz crystal oscillator signal or an external 10 MHz source for the time base circuit. The external source must be connected to the adjacent connector (7).

NOTE

If the INT/EXT switch is switched and causes momentary loss of clock, the microprocessor may hang up and cause the display to stop counting. To recover, press LINE switch to STBY then to ON.

7. EXT FREQ STD connector. Accepts 10 MHz external time base signal when INT/EXT switch is in EXT position.
8. FREQ STD OUT connector. Supplies a 10 MHz squarewave output at 1.5 volts peak-to-peak.
9. IF OUT connector. Provides the intermediate frequency (IF) output of the Pre-amplifier circuit for test or monitor of the IF.
10. DAC connector. Not used.

Figure 3-2. Rear Panel Controls and Connectors



PRELIMINARY PROCEDURES

CE1LG007

1. On rear panel:
 - a. Set INT/EXT to INT position.
 - b. Set CW/FM switch to CW. Refer to paragraph 3-33 for detailed description.
 - c. On ac power module, check for proper fuse (1.0 amp for 100/120-volt operation, 0.5000 amp for 220/240-volt operation) and check position of pc line voltage selector (refer to paragraph 2-6 for detailed description).
 - d. For remote operation, refer to paragraph 3-69 for explanation of HP-IB programming and address switch settings on rear panel.
2. On front panel, set LINE switch to ON position.

CAUTION

Do not exceed +25 dBm peak of input power at the type N connector (500 MHz—18 GHz). Damage to the internal sampler may occur.

CAUTION

The 10 Hz—500 MHz direct count input BNC connector is fuse-protected for a maximum input level of 3.5V rms (+24 dBm).

NOTE

The fuse for the 10 Hz—500 MHz input is located on the A3 Direct Count Amplifier assembly.

Figure 3-3. Operating Procedures

3. Connect input signal to appropriate input connector according to frequency requirements (BNC for 10—500 MHz, type N for 500 MHz—18 GHz) and set frequency range switch accordingly.
4. For input signals connected to BNC connector (10—500 MHz): set the 50Ω—1 MΩ switch as required. This switch has no effect on input signals connected to the type N connector (500 MHz—18 GHz).
5. Press blue key, then press blue-labeled RESOLUTION key for desired resolution.

NOTE

Half-sized □'s are used as fillers in the display to facilitate display interpretation.

6. Adjust SAMPLE RATE control for desired interval between measurements.

KEY INDICATORS

Indicator LED's in the center of some keys are used as "prompters" by the operator, as follows:

Blinking Indicator

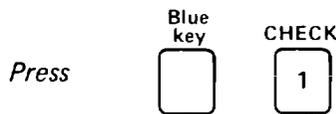
A blinking LED in a key is a "ready" condition for that key function. It indicates it is waiting for an entry via the keyboard. To clear the condition, press RESET.

Steady Indicator

A steady "on" LED in a key is an indication that the key function is in effect. To clear the condition, press the key. (The AUTO Key is cleared by pressing MAN (MHz) and vice versa.)

SELF-CHECK PROCEDURE

Perform the self-check as follows (no input signal connected and SAMPLE RATE full ccw):



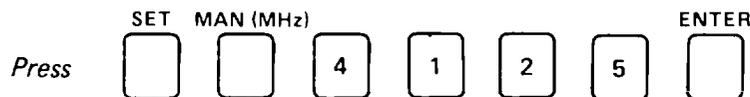
Counter Display:



(To exit from CHECK mode, press RESET)

TO SET MANUAL CENTER FREQUENCY

Example — To measure a 4.125 (±0.050) GHz signal in manual mode, connect signal to type N connector and:



NOTE

The manual center frequency is entered (and displayed) with 1 MHz resolution and must be within 50 MHz of the input signal frequency (connected to 500 MHz—18 GHz connector).

Figure 3-3. Operating Procedures (Continued)

TO ENTER OFFSET FREQUENCY

Example — To add 12.5 MHz to the measured frequency:

Press

Example — To subtract 12.5 MHz from the measured frequency:

Press

TO RECALL OFFSETS OR CENTER FREQUENCY

Example — To recall a center frequency:

Press *Press and hold*

(Displays center frequency to 1 MHz resolution)

Example — To recall an offset frequency:

Press *Press and hold*

(Displays offset)

TO REMOVE OFFSETS

Example — To remove offset from display:

Press

LED in key goes out, function is off and display shows actual measured frequency. (Offset is still stored in memory and can be added to the measurement by pressing OFS MHz again.)

Figure 3-3. Operating Procedures (Continued)

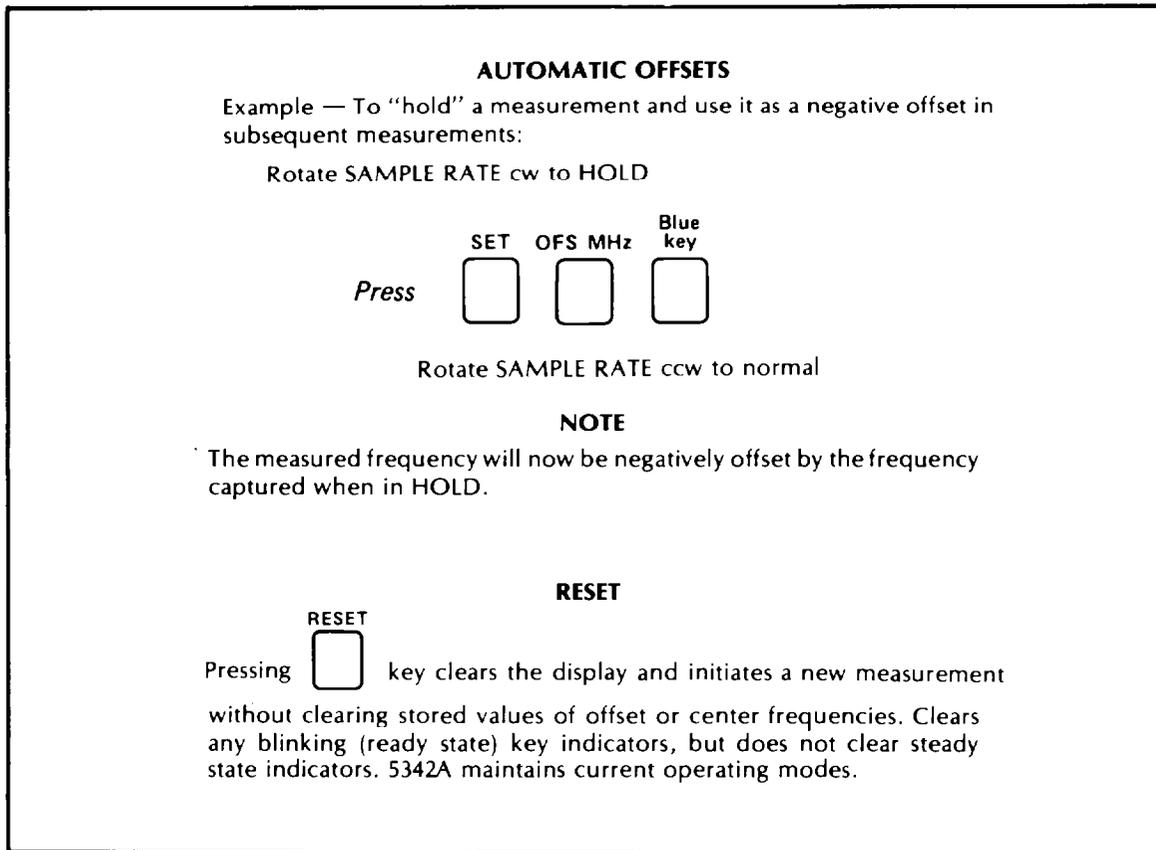


Figure 3-3. Operating Procedures (Continued)

Figure 3-4. Deleted

Figure 3-5. Deleted

3-45. OPERATOR KEYBOARD CHECK

3-46. Check for proper operation of the keyboard and display by pressing the keys listed and observing display. To exit from keyboard check mode, press RESET.

Press	Display
SET <input type="checkbox"/> SET <input type="checkbox"/> 8 <input type="checkbox"/>	 --- GHz --- --- MHz --- --- kHz --- --- Hz ---
AUTO <input type="checkbox"/>	
MAN (MHz) <input type="checkbox"/>	
Blue key <input type="checkbox"/>	

NOTE

Do not press RESET key or procedure will need to be started over.

SET <input type="checkbox"/>	
RECALL <input type="checkbox"/>	
AMPL <input type="checkbox"/>	
OFS dB <input type="checkbox"/>	
OFS MHz <input type="checkbox"/>	
CHS <input type="checkbox"/>	

Press

Display

7

77 777 777 777

8

88 888 888 888

9

99 999 999 999

4

44 444 444 444

5

55 555 555 555

6

66 666 666 666

1

11 111 111 111

2

22 222 222 222

3

33 333 333 333

0

00 000 000 000

.

.

ENTER

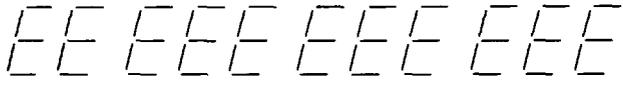
rr rrr rrr rrr

3-47. ERROR CODE DISPLAYS

3-48. Error codes are displayed by the 5342A to indicate circuit malfunctions in the instrument and to indicate operator (procedure) errors.

3-49. Instrument Error Displays

3-50. When power is applied to the 5342A, check-sum routines are automatically performed. If a routine fails, an error code is displayed to indicate the circuit fault area as follows:

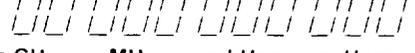
Display	Fault Area
 — GHz — — MHz — — kHz — — Hz —	RAM A14U12
	ROM A14U7
	ROM A14U4
	ROM A14U1
	PROM A16U3
	No Conversion complete signal from A16U8(36)

NOTE

If any of the above codes are displayed, refer to the troubleshooting procedures in Table 8-5.

3-51. Operator Error Displays

3-52. The display indicates when the applied signal is insufficient or excessive in level or limits, as follows:

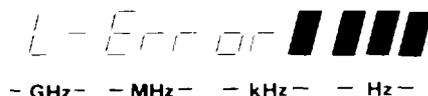
Operating Mode	Range Switch	Insufficient Signal Level Display
*Frequency	10 Hz—500 MHz	 - GHz - - MHz - - kHz - - Hz -
*Frequency	500 MHz—18 GHz	 - GHz - - MHz - - kHz - - Hz -

NOTES:

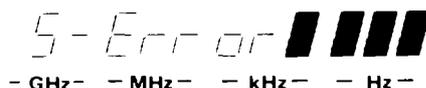
*† Shown for 1 Hz resolution. Digit shifts one position to left for each step decrease in resolution.

3-53. Limit Errors and Sequence Errors

3-54. A limit error (for example, setting a manual center frequency less than 500 MHz) will be displayed as:



3-55. A sequence error (for example, pressing a digit key before pressing a function key) will be displayed as:



3-56. For detailed descriptions of error codes, refer to Table 8-5.

3-57. Deleted

3-58. Deleted

3-59. Time Base

3-60. Provides for an oven-controlled crystal oscillator time base (model 1081 1-60111) that results in higher accuracy and longer periods between calibration (refer to Table 1-1). The oven temperature is maintained when the 5342A LINE switch is in either the ON or the STBY position (provided the instrument is connected to the power mains). When the OVN indicator in the display is lit, the oven is on (warming]. When the oven is at the proper temperature, the OVN indicator goes out.

3-61. Deleted

3-62. Deleted

3-63. Deleted

3-64. Deleted

3-65. HP-IB Interface

3-66. The Hewlett-Packard Interface Bus (HP-IB) allows the functions of the 5342A to be controlled remotely and allows measurement data to be output to the bus. Programming information for is given in paragraphs 3-69 through 3-80.

3-67. Deleted

3-68. Deleted

3-69. HP-IB PROGRAMMING

3-70. The capability of a device connected to the HP-IB is specified by its interface functions. Table 3-7 lists the interface functions of the 5342A using the terminology of IEEE Standard 488-1975 (Appendix C). Interface functions provide the means for a device to receive, process, and send messages over the HP-IB. Procedures for verification of proper operation of HP-IB are contained in paragraphs 4-19 through 4-26.

Table 3-1. HP-1B Interface Capability

Interface Function Subset Identifier	Interface Function Description
SH1	Complete source handshake capability.
AH1	Complete acceptor handshake capability.
T1	Talker (basic talker, serial poll, talk only mode, does not unaddress to talk if addressed to listen).
L2	Listener (basic listener, no listen only mode, doe not unaddress to listen if addressed to talk).
SR1	Service request capability.
RL1	Complete remote/local capability.
PPØ	No parallel poll capability.
DC1	Device clear capability.
DT1	Device Trigger capability.
CØ	No controller capability.
E1	One unit load.

3-71. There are 12 basic messages which can be sent over the interface. Table 3-2 lists each bus message, a description of the m&sage, how the 5342A uses that message, and examples of 9825A implementation of the messages.

3-72. The 5342A must be assigned a bus address. Tab/e 3-3 gives the allowable address switch settings.

3-73. Table 3-4 gives the program code set for the 5342A. Frequency and amplitude mode selection, manual center frequency setting, frequency and amplitude offset mode selection, frequency and amplitude offset setting, resolution selection, range selection, FM/CW mode selection, and automatic offsets are all analogous to the corresponding front panel operations described previously.

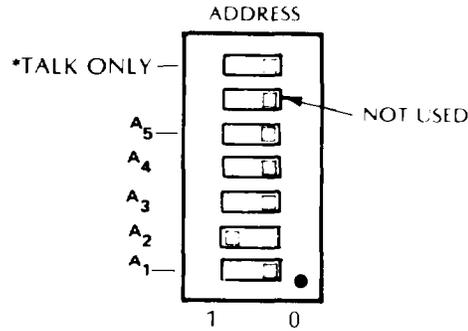
3-74. There are four sample rate modes TØ-T3. In TØ, the sample rate is determined by the setting of the front panel SAMPLE RATE control. In T1, the counter is in hold. To trigger a measurement, a trigger message must be sent. In T2, the counter ignores any sample rate run-down and initiates a new measurement as soon as the previous measurement is over. In T3, the counter takes a measurement and holds until the next T3 or trigger message.

Table 3-2. 5342A Bus Message Usage

Message	Description	5342A Use	Sample 9825 Statements (5342A set to Address 02)
Data	Transfers device-dependent information from one device to one or more devices on the bus.	Sends measurement data. See paragraph 3-77 for output format. Accepts program codes. See Table 3-4 for code set.	red 702, A wrt 702, "AUSR4"
Trigger	Causes a group of selected devices to simultaneously initiate a set of device-dependent actions	Starts a new measurement.	trg 7 or trg 702
Clear	Causes an instrument to be set to a predefined state (a certain range, function, etc.).	Same as front panel RESET. Clears internal count and starts new measurement.	clr 7 or clr 702
Remote	Permits selected devices to be set to remote operation, allowing parameters and device characteristics to be controlled by Bus Messages.	5342A goes to remote if REN is true and addressed to listen. In absence of program data, remote operation is according to the state of the front panel settings just prior to going to remote.	rem 702
Local	Causes selected devices to return to local (front panel) operation.	Goes to local front panel control. In absence of front panel data, local operation is according to the state of the remote data just prior to going to local.	lcl 702
Local Lockout	Disables local (front panel) controls of selected devices.	Disables front panel RESET. 5342A remains in remote.	llo 7
Clear Lockout and local	Returns all devices to local (front panel) control and simultaneously clears the Local Lockout Message.	Local lockout cleared and returns to local front panel control	lcl 7
Require Service	Indicates a device's need for interaction with the controller.	Pulls on SRQ to indicate end of a measurement.	rds(7)→A if bit (7, A) (bit 7=1 if SRQ true)
Status Byte	Presents status information of a particular device; one bit indicates whether or not the device currently requires service, the other 7 bits (optional) are used to indicate the type of service required.	In serial poll mode, 5342A outputs decimal 80 (01010000) to indicate end of measurement.	rds (702)→A (if A=80, then 5342A is ready to output)
Status Bit	A single bit of device-dependent status information which may be logically combined with status bit information from other devices by the controller.	Does not use	—
Pass Control	Passes bus controller responsibilities from the current controller to a device which can assume the Bus supervisory role.	Does not use	—
Abort	Unconditionally terminates Bus communications and returns control to the system controller.	Clears Talk, Listen, Serial Poll Enable registers on 5342A HP-IB interface. Front panel annunciators do not change, however.	cli 7

Table 3-3. Address Selection

Read panel address switch:



(Shown in addressable mode, and address 02)

*If the 5342A is in TALK ONLY mode and It is desired to return to the addressable mode, set TALK ONLY switch to 0 and press RESET on front panel

ASCII CODE CHARACTER		ADDRESS SWITCHES					5-BIT DECIMAL CODE
LISTEN	TALK	A ₅	A ₄	A ₃	A ₂	A ₁	
SP	@	0	0	0	0	0	00
!	A	0	0	0	0	1	01
"	B	0	0	0	1	0	02
#	c	0	0	0	1	1	03
\$	D	0	0	1	0	0	04
%	E	0	0	1	0	1	05
&	F	0	0	1	1	0	06
'	G	0	0	1	1	1	07
(H	0	1	0	0	0	08
)	I	0	1	0	0	1	09
*	J	0	1	0	1	0	10
+	K	0	1	0	1	1	11
,	L	0	1	1	0	0	12
-	M	0	1	1	0	1	13
.	N	0	1	1	1	0	14
/	O	0	1	1	1	1	15
0	P	1	0	0	0	0	16
1	Q	1	0	0	0	1	17
2	R	1	0	0	1	0	18
3	s	1	0	0	1	1	19
4	T	1	0	1	0	0	20
5	u	1	0	1	0	1	21
6	v	1	0	1	1	0	22
7	w	1	0	1	1	1	23
8	x	1	1	0	0	0	24
9	Y	1	1	0	0	1	25
:	Z	1	1	0	1	0	26
;	[1	1	0	1	1	27
<	\	1	1	1	0	0	28
=]	1	1	1	0	1	29
>	~	1	1	1	1	0	30

Table 3-4. HP-IBProgram Code Set

1. FREQUENCY MODE SELECT	
AUTOAU
MANUALM
2. SET MANUAL CENTER FREQUENCY	
SMXXXXXE	(X's represent nonfixed length data string of up to 5 characters. Decimal points cause entire string to be ignored. +signs and spaces are allowable. Number is in MHz and must be less than 18 GHz or will be ignored.)
Example:	SM10000E for 10 GHz center frequency SM775E for 775 MHz center frequency SM+5250E for 5.25 GHz center frequency
3. AMPLITUDE MODE SELECT	
Not used.	
4. FREQUENCY OFFSET MODE SELECT	
Frequency Offset of fOM0
Frequency Offset onOM1
5. SET FREQUENCY OFFSET	
SOM±XXXXX.XXXXXXE	(X's represent nonfixed length data string representing offset frequency in MHz. Spaces are ignored.)
Example:	SOM10.7E for 10.7 MHz positive offset SOM-4000.25E for 4.00025 GHz negative offset.
6. AMPLITUDE OFFSET MODE	
Not used.	
7. SET AMPLITUDE OFFSET	
Not used.	
8. RESOLUTION	
1 Hz	SR3
10 Hz	SR4
100 Hz	SR5
1kHz	SR6
10 kHz	SR7
100 kHz	SR8
1 MHz	SR9
9. RANGE	
10 Hz—500 MHzL
500 MHz—18GHzH
10. FM/CW MODE	
CW modeC
FM modeF

Table 3-4. HP-18 Program Code Set (Continued)

11. SAMPLE RATE	
Front panel sample rate	T0
Hold	T1 *
Fast sample (no delay)	T2
Sample then hold	T3
* Send trigger command (trg 7 or trg 702) to start measurement. If 5342A is in remote and addressed to listen and other than Hold (T1), the trigger command causes the 5342A to automatically go to Sample then Hold (T3).	
12. OUTPUT MODE	
Output only when addressed.	ST1
Wait until addressed	ST2
13. RESET	
RE (display is blanked and new measurement initiated. If in Hold (T1), then measurement is not completed but stays in Hold. Does not return control to local.)	
14. AUTOMATIC OFFSETS	
Automatic frequency offset.	SOMB
15. CHECK MODE	
SR1 (No input can be present at RF connector. Counter must be in SAMPLE RATE full ccw. Be sure to send RESET command (RE) before making other measurements.)	

3-75. In the “output only when addressed” mode, the counter pulls SRQ at the end of a measurement and then checks to see if it has been addressed to talk. If not, SRQ is cleared and it starts the next measurement. If it has been addressed to talk, it outputs the measurement, clears SRQ, and starts the next measurement. In the “wait until addressed” output mode, the counter pulls SRQ at the end of a measurement and waits in a loop until it has been addressed to talk. When it is addressed to talk, it outputs the measurement, clear SRQ and starts the next measurement.

NOTE

If the counter is placed in the HOLD (T1) mode, triggered, then addressed to talk, be sure to use the Wait Until Addressed (ST2) output mode, If not, then for short gate times the measurement may be completed before the controller addresses the counter to talk and the counter will discard the measurement result and hang up the bus.

3-76. The 5342A executes each complete program code as it is received just as if the microprocessor were receiving the data from the front panel keyboard. Program code strings should be in the same order as they would be if being entered from the front panel. When a data byte is sent to the 5342A HP-IB, the HP-IB interface stores the byte and sends an interrupt to the microprocessor which reads in the byte. If the byte does not complete a program code, then the microprocessor waits for the next byte(s) until a complete code is sent (for example, SR5 is a complete code but SR is not). After a complete code is received, the microprocessor executes the code and begins the measurement. If more codes are in the string, another interrupt is generated. For example, if the string “SR5AU” is sent by the controller, the “S” is the first byte received and stored by the 5342A HP-IB interface. The interface generates an interrupt to the microprocessor and the “S” is read by the MPU. Since S is not a complete code, the microprocessor

waits until the complete code is sent and received. After "R" and then "5" are sent, the microprocessor sets the resolution accordingly and then goes to the beginning of the measurement. When the controller sends "A", an interrupt is generated and "A" is read by the microprocessor. It then waits for the complete code to be sent which in this case is "AU". The microprocessor again goes to the start of the measurement cycle.

NOTE

The following output formats pertain to input signals of specified sensitivity (Table 1-1). For less sensitive input signals, refer to paragraph 3-82,

3-77. The 5342A outputs measurement data in the following fixed length formats:

- a. NO OFFSET, FREQUENCY ONLY

SP F SP SP XXXX.XXXXXX E + 06 CR LF

frequency ↗
space ↗
carriage return ↗
line feed ↗

- b. Deleted

- c. OFFSET in FREQUENCY

SP FS ±XXXXX.XXXXXX E + 06, CR LF

offset ↗

- d. OVERLOAD

SP F SP SP 99999.999999 E + 09 CR LF
(caused by excessive input level)

- e. DISPLAY OVERFLOW

SP F SP SP 99999.999999 E + 06 CR LF
(caused by offset which makes display overflow)

- f. Deleted

- g. Deleted

- h. INSUFFICIENT SIGNAL

SP F SP SP 00000.000000 E + 06, CR LF

- i. Deleted

3-78. When the 5342A is in remote, the front panel REMOTE annunciator lights. When the 5342A is addressed to talk, the front panel RECALL pushbutton lamp will light.

3-79. 9825A PROGRAM EXAMPLES

3-80. The following 9825A program examples are illustrative of 5342A programming:

EXAMPLE 1

```
0: wrt 702,"AUSR
   7T18T2"
1: tra 702;red
   702,A;dsp A;
   wait 500
2: ato 1
3: end
*3802
```

This program assumes the range switch was set to 0.5—18GHz before the program was executed. The program puts the 5342A in AUTO, 10 kHz resolution, HOLD, and "wait until addressed" output mode. Program takes a measurement (trg 702) and reads it into the A register. After waiting 500 ms, the program loops back to the next trigger, then read statement.

EXAMPLE 2

```
0: wrt 702,"AUSR
   4T2ST1      "
1: red 702,A;
   cmd 7,"_";dsp
   A;wait 500
2: ato 1
3: end
*6699
```

This program also assumes the range switch was previously set to the 0.5—18 GHz position. The program puts the counter in AUTO mode, 10 Hz resolution, fast sample, and "only if addressed" output mode. The program takes a measurement, unaddressed the 5342A as a talker (cmd 7," — ") so that the counter will continue making measurements at a fast rate, and waits 500 ms until reading the next measurement.

EXAMPLE 3

```
0: wrt 702,"SM10
   000ESR3HFT0ST1"
1: red 702,A;
   prt A
2: ato 1
3: end
*1870
```

This program sets a manual center frequency of 10 GHz (input frequency = 10.03 GHz), 1 Hz resolution, 0.5—18 GHz range, FM mode, front panel sample rate control, and "output only if addressed". Each reading is printed on the 9825A printer.

```
10030069548.00
10030069544.00
10030069539.00
10030069529.00
10030069524.00
10030069514.00
10030069512.00
```

EXAMPLE 4

```
0: wrt 702,"AUSR
  3T25T1AM1"
1: red 702,A,B;
  prt A;prt B
2: rto 1
3: end
*32729
```

This program selects AUTO mode, 1 Hz resolution, fast sample, "(output only if addressed", and amplitude "on". The frequency is read into the A register and the amplitude is read into the B register. Notice that although the frequency is displayed only to 1 MHz resolution on the counter, the full 1 Hz resolution is output to the calculator.

```
4230028373.00
  -5.30
4230028373.00
  -5.30
4230028367.00
  -5.30
4230028370.00
  -5.30
```

EXAMPLE 5 Deleted

EXAMPLE 6 Deleted

3-81. HP-IB PROGRAMMING NOTES

3-82. The HP-IB output is affected by input signal level as follows:

- a. For input signal levels greater than or equal to specified sensitivity, the 5342A outputs measurement data as described in paragraph 3-77.
- b. For input signal levels less than the actual sensitivity by 0.1 dB or more (or for no input), the counter outputs zeros when addressed to talk.
- c. For input signal levels just on the edge of the counter's actual sensitivity (approximately a 0.1 dB band) the detectors which indicate sufficient signal level for counting may become intermittent resulting in very long acquisition times. The counter's display holds the previous reading during the prolonged acquisition but the counter will not output any data when addressed to talk. This will hang up the program at the read statement.
- d. With the 9825A, use the "time" statement and "on err" statement to branch around the read statement if it takes longer than a specified number of milliseconds to complete an I/O operation. The following example program can be used when there is more than one read statement in the program. If there is only one read statement, then statement 2 could be deleted and the end of statement 7 could simply cause the program to go to the statement after the read (in this case, "gto 6"):

EXAMPLE

```

0: dev "ctr";702
1: gto "begin"
2: "er ret":jmp
  er1-1
3: "begin":time
  1000:on err
  "er"
4: wrt "ctr";
  "AUSR4HCT1"
5: tra "ctr";
  red "ctr":A
6: wait 500:ert
  A:jmp -1
7: "er":if ern=4
  10+A:time 1000:
  on err "er";
  gto "er ret"
8: end
*29627

```

Since this statement is in line 2, the program jumps to the statement after the read statement.

Error 4 is time out error. Reset time and error jump.

```

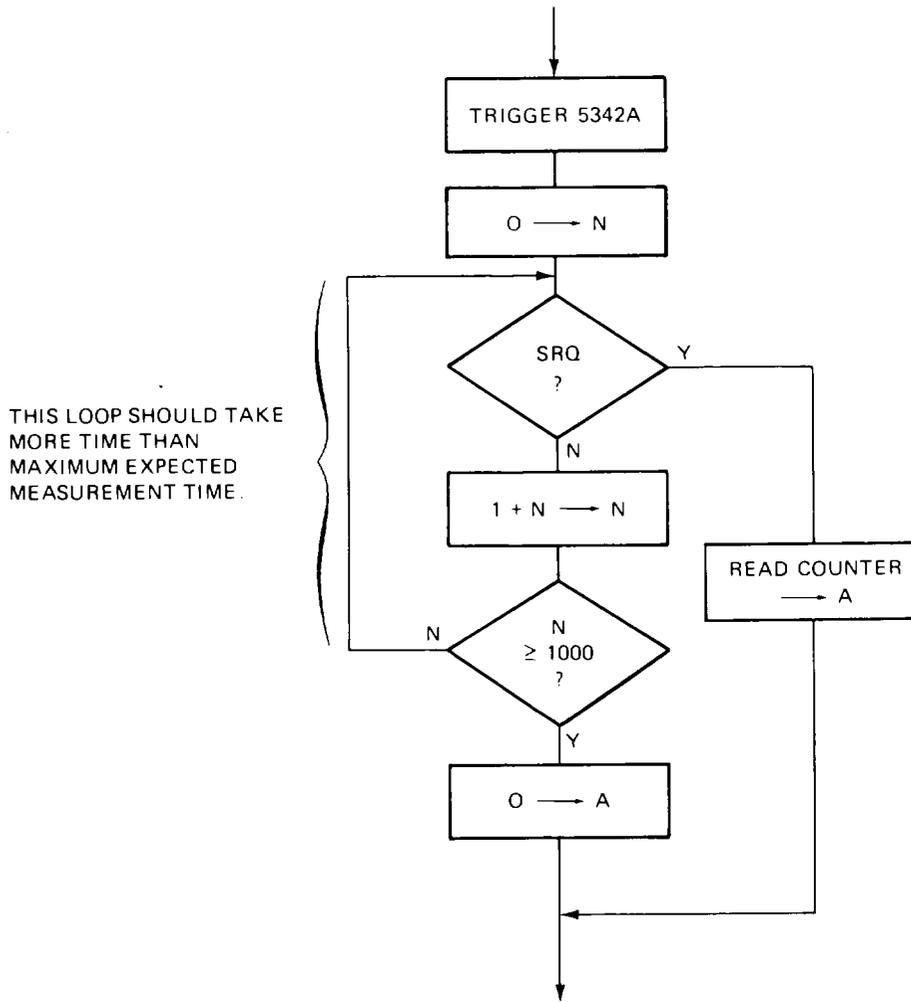
6.200093550e 09
6.200093540e 09
6.200093540e 09
6.200093550e 09
      0.000000
      0.000000
      0.000000
      0.000000
6.200093530e 09
6.200093530e 09
6.200093540e 09
6.200093540e 09

```

} When the 5342A took more time than 1 second to make the measurement, zeroes are output.

NOTE

For any controller, check SRQ to see if a measurement has been completed. Allow an adequate number of iterations on the SRQ check to permit the counter to complete the measurement and pull SRQ. A flow diagram of such an algorithm is:



3-83. Deleted.

3-84. Deleted.

SECTION IV PERFORMANCE TESTS

4-1. INTRODUCTION

4-2. The procedures in this section test the electrical performance of the 5342A using the specifications in Table 1-1 as performance standards. Those specifications which are inherent to the design (obvious during operation) are not covered in these tests. For example, worst case acquisition time is determined by the period of the sweep and the length of the pseudo-random sequence. If the counter acquires the signal, it must have acquired it in a time less than specified.

4-3. OPERATIONAL VERIFICATION

4-4. The abbreviated checks given in paragraphs 4-12 through 4-18 can be performed to give a high degree of confidence that the 5342A is operating properly without performing the complete performance test. The operational verification should be useful for incoming QA, routine maintenance, and after instrument repair. The HP-IB Verification Program is described in paragraphs 4-19 through 4-26.

4-5. COMPLETE PERFORMANCE TEST

4-6. The complete performance test is given in paragraphs 4-28 through 4-40. All tests can be performed without access to the inside of the instrument.

4-7. EQUIPMENT REQUIRED

4-8. Equipment required for the complete test and operation verification is listed in Table 7-4. Any equipment which satisfies the critical specifications given in the table may be substituted for the recommended model numbers.

4-9. TEST RECORD

4-10. Results of the operational verification may be tabulated on the Operational Verification Record, Table 4-7. Results of the performance test may be tabulated on the Performance Test Record, Table 4-5.

4-10.1. INPUT CABLE CONSIDERATIONS

Consideration should be given to input cable losses at higher frequencies. For example, a 6-foot section of RG-214/U coaxial cable has about 15dB loss at 18GHz. Such losses must be taken into consideration along with the sensitivity specifications given in Table 1-1.

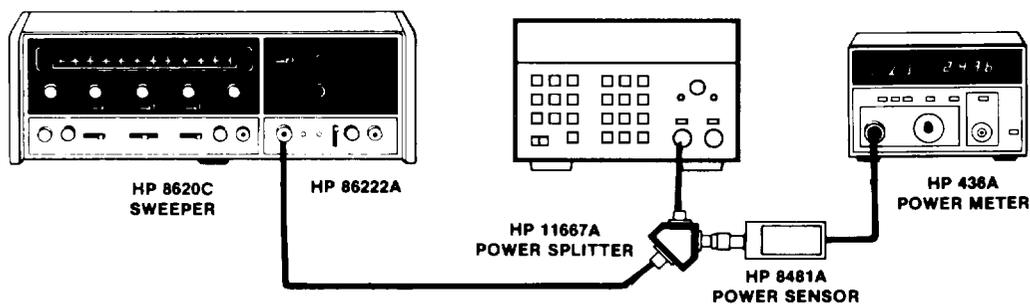
4-11. OPERATIONAL VERIFICATION PROCEDURES

4-12. Self-Check

- a. Select 1 Hz resolution, AUTO mode, and 500 MHz—18 GHz range. Set self-check mode and verify counter displays 75.000000 MHz \pm 1 count.
- b. Set 5342A to 10 Hz—500 MHz range. Connect rear panel FREQ STD OUTPUT to front panel BNC input. Select 50 Ω impedance. Reset the 5342A. Verify that the 5342A counts 10.000 000 MHz \pm 1 count.

4-13. 10 Hz—500 MHz Input Sensitivity Test, 50 Ω /1 M Ω)

Setup:

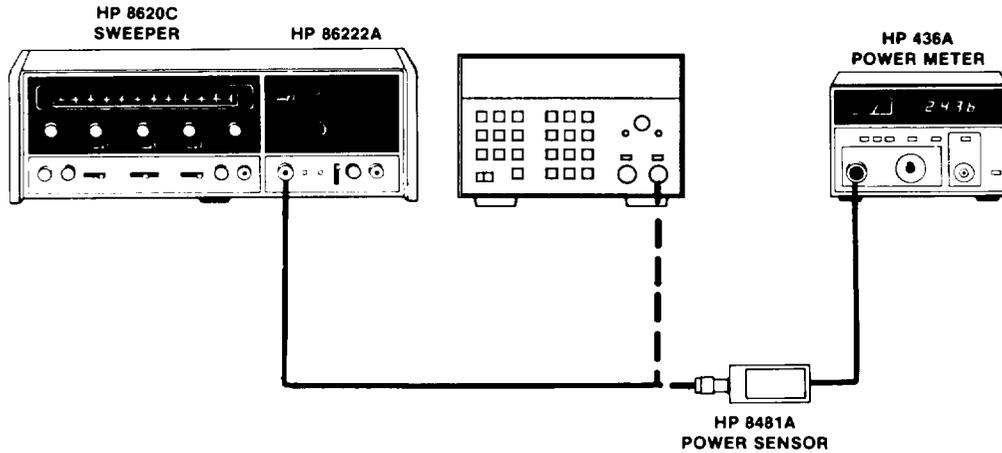


- Set the 5342A to 10 Hz—500 MHz range and 50 Ω
- Set 8620C to 10 MHz and a level of -19.3dBm (25 mV rms) as measured on the 436A Power Meter. Measure actual sensitivity and verify that the 5342A counts at 10 MHz, 100 MHz, 520 MHz, and record on operational verification record (Table 4-1).
- Disconnect 11667A and connect 8481A directly to 86222A output. Set 8620C to 25 MHz at a level of -19.3 dBm (25 mV rms).
- Disconnect 8481A from 86222A output. Switch 5342A to the 1 M Ω position. Connect 86222A output to 5342A 10 Hz—500 MHz input (86222A supplies 25 mV rms into 50 Ω or 50 mV rms into 1 M Ω).
- Verify that the 5342A counts 25 MHz at 50 mV rms and record on operational verification record (Table 4-1).

4-14. Deleted

4-15. Deleted

4-18. 500 MHz—18 GHz High Level Test



For Standard Instrument:

- Set the 8620C to 1 GHz at +5.0 dBm as measured by the 436A Power Meter. Connect the 8620C output to the 5342A and verify that the counter counts 1 GHz.

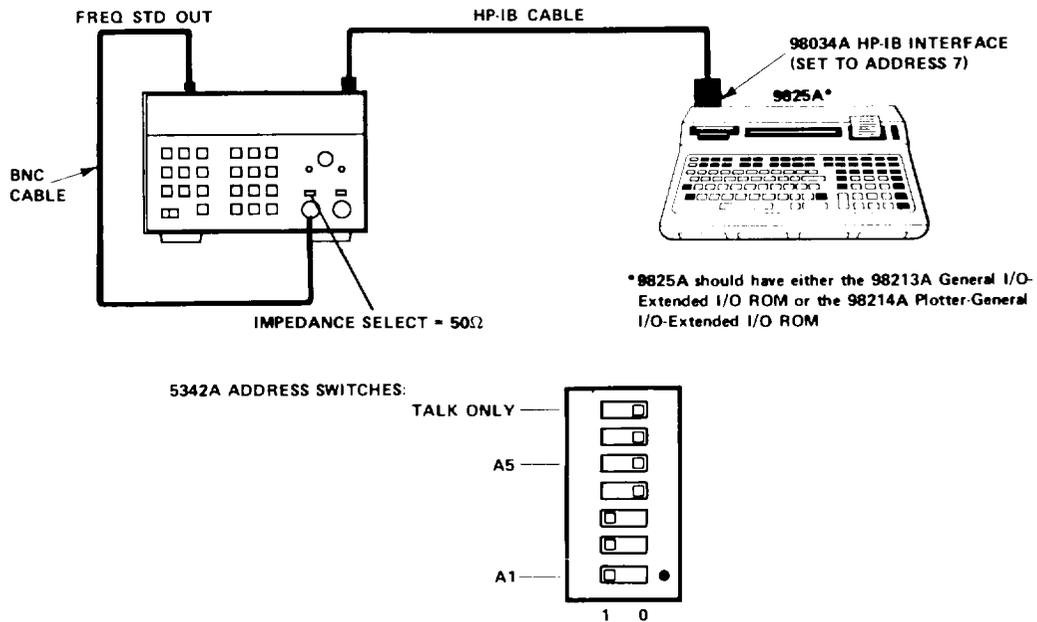
4-19. HP-IB VERIFICATION PROGRAM

4-20. The 9825A program listed in Table 4-2 exercises the 5342A through various operating modes, described below, via its HP-IB Interface. If the 5342A successfully completes all phases of the verification program, then there is a high probability that the HP-IB Interface (A15 assembly) is working properly. If the 5342A does not respond as described, refer to HP-IB troubleshooting in Section VIII.

NOTE

Prior to conducting the performance test, check the A15 board revision letter (adjacent to the board part number). If the revision letter is D or later, check the LSRQ line to pin 13 be sure the jumper is installed as shown in Figure 8-38.

4-21. To perform the verification, set up the 5342A as shown and set its rear panel address switches to address 07.



*9825A should have either the 98213A General I/O-Extended I/O ROM or the 98214A Plotter-General I/O-Extended I/O ROM

4-22. The program listed in Table 4-2 may be keyed into the 9825A or may be loaded from a HP-IB Verification Cassette, HP P/N 59300-10001, (Revision B or later) which also contains HP-IB verification programs for the 59300 series of instruments. To run the program on the cassette, insert the cassette into the 9825A, load file Ø, and press RUN. Enter "5342" when the instrument mode number is requested and select code "707" when select code is requested. The 9825A will then load the 5342A verification program into memory.

4-23. Apply power to the 5342A and verify that the counter powers up in AUTO mode and REMOTE off. Verify that when the range switch is placed in the 10 Hz—500 MHz position and impedance select to 50 Ω), the counter counts its 10 MHz time base.

4-24. The program goes through 14 check points. The information in Table 4-3 tells what occurs during each test and what should be observed by the operator if the test has been successfully completed. At the conclusion of each test, the program stops and displays the current check point. To advance to the next test, simply press CONTINUE. If it is desired to repeat a test, set the variable L to 1 via the keyboard (1 → L EXECUTE). To go on to the next test after looping, set L back to 0 when the program halts (Ø → L EXECUTE). Record on operational verification record (Table 4-71).

4-25. When the 9825A displays "AMPL OPT?" at the end of check point 14, enter "NO".

4-26. Table 4-4 is a sample printout from the 9825A.

4-27. Deleted

Table 4-7. Operational Verification Record

5342 SIN _____		Date _____	
PARAGRAPH NUMBER	TEST	RESULTS	
		PASS	FAIL
4-12	Self-Test		
-13	10 Hz—500 MHz Input Sensitivity Test 15 Ω/1 MΩ): 50Ω: 10 MHz 50Ω: 100 MHz 50Ω: 520 MHz 1 MΩ: 25 MHz		
4-14 Deleted			
4-15 Deleted			
-16	500 MHz—18 GHz Input Sensitivity Test: Sensitivity @ 1 GHz 12.4 GHz 18 GHz		
4-17 Deleted			
4-18	500 MHz—18 GHz High Level Test: 1 GHz Display.		
4-19 through 4-26	HP-IB Verification		
4-27 Deleted			

Table 4-2. Model 9825A Program

```

0: dim C$(40); dsp "MODEL 5342A Frequency Counter"; wait 2000
1: "code" :ent "select code?", S
2: if S=721; dsp "error: calculator address"; wait 1000; gto "code"
3: if S>730; dsp "out of address range →high"; wait 1000; gto "code"
4: if S<700; dsp "out of address range →low"; wait 1000; gto "code"
5: dev "ctr", S; prt "5342A HP-IB TEST"; spc 2
6: prt "-----", "CHECK POINT 1"
7: rem "ctr"; beep
8: prt " *REMOTE ", " *AUTO "; spc 2
9: dsp "CHECK POINT 1--Press Continue"
10: Stp
11: if L=1; gto 7
12: prt "-----", "CHECK POINT 2"
13: wrt "ctr", 'M'; beeper
14: dsp "MANUAL MODE"; wait 5000
15: wrt "ctr", 'A'; beeper
16: prt " *MANUAL off", " *AUTO on"; spc 2
17: dsp "CHECK POINT 2--Press CONTINUE"
18: stp
19: if L=1; gto 13
20: prt "-----", "CHECK POINT 3"
21: wrt "ctr", 'OM1'; beep; dspdsp "FREQ OFFSET mode"; wait 5000
22: wrt "ctr", 'OMO'; beeper
23: prt " *OFS(MHZ) off"; spc 2
24: dsp "CHECK POINT 3--Press CONTINUE"
25: stp
26: if L=1; gto 21
27: prt "-----", "CHECK POINT 4"
28: wrt "ctr", 'L'; beep; dspdsp "Low Range"; wait 5000
29: wrt "ctr", 'H'; beeper
30: prt "Low Range 10MHz", " High Range", " 000000000000"; spc 2
31: dsp "CHECK POINT 4--Press Continue"
32: stp
33: if L=1; gto 28
34: prt "-----", "CHECK POINT 5"
35: wrt "ctr", 'F'; beep; dspdsp "FM Mode"; wait 5000
36: wrt "ctr", ''; beeper
37: prt " *ASTERISK off"
38: dsp "CHECK POINT 5--Press Continue"; spc 2
39: Stp
40: if L=1; gto 35

```

Table 4-2. Model 9825A Program (Continued)

```

41: prt "-----", "CHECK POINT 6"
42: 3 → x
43: fmt 1," SR",f.0, "SR1"; wrt; "ctr.1", X; beep
44: X+1 → X;wait 2000;if X=10;gto +2
45: gto -2
46: prt "*RES 1MHZ"
47: dsp "CHECK POINT 7--Press Continue"
48: spc 2;stp
49: if L=1;gto 42
50: prt "-----", "CHECK POINT 7","Enter Manual ", "center Freq"
51: ent X;fmt3,"SM",f.0,"E"
52: if<X 5e2 or X>1.8e4;prt "LIMIT ERROR";gto -2
53: wrt "ctr.3",X
54: spc 1;prt "Recall Center"," freq";spc 1;fxd 0;prt "Does Center Freq=", X
55: dsp "CHECK POINT 8--Press Continue" ;spc 2;stp
56: if L=1;gto 51
57: prt "-----", "CHECK POINT 8","Enter Frequency","Offset(MHZ)"
58: ent X;fmt 4,"SOM",f.6,"E" ;wrt "ctr.4",X
59: fxd 6;prt "Recall OFS(MZ)";spc 1;prt "Does OFS(MHZ)=", X
60: dsp "CHECK POINT 9--Press Continue";spc 2;stp
61: if L=1;gto 58
62: prt "-----", "CHECK POINT 9"
63: wrt "ctr","AUHOMOSR3SR1' ";red "ctr",A
64: prt "check=", A,"*RECALL
65: dsp "CHECK POINT 10--Press CONTINUE";SpC 2;stp
66: if L=1;gto 63
67: prt "-----", "CHECK POINT 10"
68: wrt "ctr","RELSR3T1"
69: trg "ctr"; wait 4000;trg "ctr";beep;wait 4000;trg "ctr";beep
70: prt "2 Measurements--HOLD"
71: wrt "ctr","RESR9T0";spc 2;prt "Vary SR Pot" ;dsp "Press Continue";stp
72: wrt "ctr","T2"
73: spc 2;prt "Fast Sample";dsp "Press Continue";stp
74: wrt "ctr","T3";beep;wait 4000;wrt "ctr", "T3";beep;wait 4000
75: wrt "ctr","T";bee peep
76: spc 2;prt "3 measurements--sample then HOLD"
77: dsp "CHECK POINT n--Press CONTINUE";spc 2;stp
78: if L=1;gto 68
79: prt "-----", "CHECK POINT 11"
80: wrt "ctr","LSR6TOST1";dsp "Only If Addressed";wait 5000
81: red "ctr", A;beep;prt "freq= ",A
82: wrt "ctr","ST2"
83: dsp "Wait Until Addressed";wait 5000;beep
84: red "ctr",A;prt "freq= ",A

```

Table 4-2. Model 9825A Program (continued)

```

85: dsp "CHECK POINT 12--Press Continue" ;spc 2;stp
86: if L=1; gto 80
37: prt "-----", "CHECK POINT 12" ;1 → X
88: wrt "ctr", "T1"
89: X+1 → X;if X=500;trg "ctr"; beep
90: rds("ctr")+A;dsp A
91: if X=1000;prt "status= ",A;gto +2
92: gto -3
93: dsp "CHECK POINT 12--Press Continue";stp
94: if L=1;gto 88
95: prt "-----", "CHECK POINT 13"
96: 1c1 "ctr";beep
97: spc 2;prt "REMOTE 0ff";dsp "CHECK POINT 13--Press Continue";stp
98: if L=1;gto -2
99: prt "-----". "CHECK POINT 14"
100: rem "ctr";dsp "REMOTE"
101: 11o 7;beep;prt "LOCAL LOCKOUT";dsp "Press Continue" ;stp
102: 1c1 7;prt "Return to LOCAL"
103: spc 1;prt "REMOTE off";dsp "CHECK POINT 14--Press Continue";stp
104: rem 7
105: if L=1;gto -5
106: ent "AMPL OPT ?","C$;if C$=YES";gto +2
107: dsp END;prt "END";stp
108: spc 4;prt "AMPL OPT 002";spc 2
109: prt "-----", 'CHECK POINT 1"
110: wrt "ctr", "AM1";beep;wait 5000
111: wrt "ctr", "AM0";beep
112: prt "*AMPL off"
113: dsp "CHECK POINT 1--Press Continue";spc 2;stp
114: if L=1;gto 110
115: prt "-----", "CHECK POINT 2"
116: wrt "ctr", "AM1031";beep;wait 5000;wrt "ctr", "0B0"
117: prt "*OFS(DB) off"
118: dsp "CHECK POINT 2--Press Continue";spc 2;stp
119: if L=1;gto 116
120: prt "-----", "CHECK POINT3";spc 1;prt "Enter AMP OFFSET"
121: ent X
122: if X<-99.9 or X>99.9;prt "LIMIT ERROR";gto -2
123: fmt 5, "SOB",f.1, "E" ;wrt "ctr.5",X
124: fxd 1;prt "Recall OFS(DB)","Does OFS(DB)=",X
125: dsp "CHECK POINT 3--Press Continue";spc 2;stp
126: if L=1;gto 120
127: prt "-----", "CHECK POINT 4"
128: dsp "Press Continue ";stp

129: wrt "ctr", "RELSR3ST2T3AM1050"
130: red "ctr",C$;prt C$;prt "END"
131: dsp "CHECK POINT 4-Press Continue";stp
132: if L=1;gto 129
133: end
*4993

```

Table 4-3. Model 9825A Program Description

CHECK POINT	TEST	OBSERVE ON 5342A
1	Remote	Front panel REMOTE should light.
2	Manual/Auto	Front panel MANUAL should light for approximately 5 seconds (AUTO goes off for 5 seconds). At conclusion of test, AUTO light should be on.
3	Frequency Offset-On/OFF	Front panel OFS (MHz) should light for approximately 5 seconds then go off.
4	Range - Low/High	The counter should display 10 MHz for approximately 5 seconds and then all 0's (high range - no input).
5	FM mode - On/Off	Front panel asterisk should light for approximately 5 seconds.
6	Resolution - 1 Hz to 1 MHz	The counter should display the 75 MHz check frequency with resolution from 1 Hz to 1 MHz. Each beep from calculator decreases resolution by one decade. There is approximately a 2-second wait between each change.
7	Set Manual Center Frequency	When the 9825A displays X?, enter a manual center frequency in MHz, no decimal points between 500 (MHz) and 18000 (MHz). Press CONTINUE. Verify that the counter was set to this manual center frequency by pressing RESET, RECALL, MANUAL. For example, if 12345 is entered (12.345 GHz manual frequency), then 12.345 GHz should be displayed by the counter when the manual center frequency is recalled.
8	Set Offset Frequency	When the 9825A displays X?, enter a frequency offset in MHz, decimal points allowed. Press CONTINUE, Verify that the counter was set to this frequency offset by pressing RESET, RECALL, OFS (MHz). For example, if 12345.678987 is entered, then 12.345678987 GHz should be displayed by the counter when the fequency offset is recalled.
9	Talk	The 9825A should print 75 MHz, which is the output of the 5342A in check mode. The 5342A RECALL light should flash on during output, indicating that it has been addressed as a talker.
10	Sample Rate — Hold, Front Panel Control, Fast Sample, Sample and Hold	In the first part of the test, the 5342A is placed in HOLD and a trg 722 is executed. For each beep of the calculator, observe that the 5342A GATE lights. After the second measurement, the 5342A is programmed for front panel control. Vary the front panel sample rate pot and observe the change in GATE delay. Press CONTINUE and the 5342A is programmed for fast sample. Verify that the front panel pot has no effect and that there is minimum time between measurements. Press CONTINUE and the 5342A is programmed for sample and HOLD. Before each beep from the 9825A, the 5342A is sent T3 which takes one measurement and holds.

Table 4-3. Model 9825A Program Description (Continued)

CHECK POINT	TEST	OBSERVE ON 5342A
11	Only If/Wait Until Addressed	At the start of this test, the 5342A is placed in the ONLY IF addressed mode. The GATE light should continually light, indicating that measurements are continually being made until the 5342A is addressed to talk. The counter is addressed to talk and the value is printed. The counter is then placed in WAIT UNTIL addressed. The GATE light should go out after the first measurement and remain out, indicating that the first measurement is being saved until the counter is addressed to talk. It is then addressed to talk and the value is printed by the printer.
12	Status Byte	The 5342A is put in HOLD and serial poll mode. Its status byte is displayed by the 9825A. After approximately 5 seconds, the 5342A is triggered and a measurement is taken. The status byte displayed by the 9825A should change from 0 to 80, indicating that the 5342A has taken a measurement.
13	Go To Local	LCL 722 is issued. The front panel REMOTE light should go off.
14	Local Lockout	The 5342A is returned to remote control and the local lockout command is issued. When the 9825A displays "press CONTINUE", press RESET on the 5342A and verify that the counter remains in REMOTE. Press CONTINUE on the 9825A and lcl 7 is issued. Verify that the 5342A goes to local.

Table 4-4. Sample Printout

5342A HP-IB TEST		
----- CHECK POINT 1 *REMOTE on *AUTO on -----	----- CHECK POINT 8 Enter Frequency Offset [MHZ] Recall OFS[MZ] -----	----- CHECK POINT 12 status= 80.000000000 -----
----- CHECK POINT 2 *MANUAL off *AUTO on -----	Does OFS[MHZ]= 12345.678987000 -----	----- CHECK POINT 13 REMOTE Off -----
----- CHECK POINT 3 *OFS[MHZ] off -----	----- CHECK POINT 9 CHECK= 7.500000000e 07 *RECALL on -----	----- CHECK POINT 14 LOCAL LOCKOUT Return to LOCAL REMOTE Off -----
----- CHECK POINT 4 Low Range 10MHz High Range 00000000000 -----	----- CHECK POINT 10 3 Measurements-- HOLD -----	----- AMPL OPT 002 -----
----- CHECK POINT 5 *ASTERISK off -----	Vary SR Pot ----- Fast Sample -----	----- CHECK POINT 1 *AMPL Off -----
----- CHECK POINT 6 *RES 1MHZ -----	3 measurements-- sample then HOLD -----	----- CHECK POINT 2 *OFS(DB) Off -----
----- CHECK POINT 7 Enter Manual Center Freq Recall Center Freq -----	----- CHECK POINT 11 freq= 1.000000000e 07 freq= 1.000000000e 07 -----	----- CHECK POINT 3 Enter AMP OFFSET Recall OFS(DB) Does OFS(DB)= 10.100000000 -----
Does Center Freq = 12345.00		----- CHECK POINT 4 F 00010.000000E +06, A +12.0E+0 END

4-28. PERFORMANCE TEST PROCEDURES

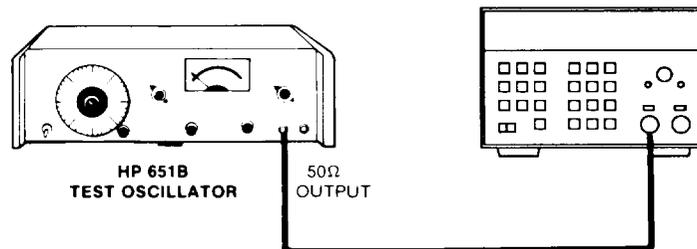
4-29. 10 Hz—500 MHz Input Sensitivity Test, 50 Ω .

Specification: 50 Ω position, sensitivity \approx 25 mV rms for frequencies from 10 Hz—520 MHz.

Description: The 5342A is set to the 10 Hz—500 MHz range and a signal at the rated sensitivity is applied to the BNC input. The frequency is slowly swept up to 10 MHz at constant level and the 5342A reading is checked for the proper count. For the range of 10 MHz to 520 MHz, a different generator is used.

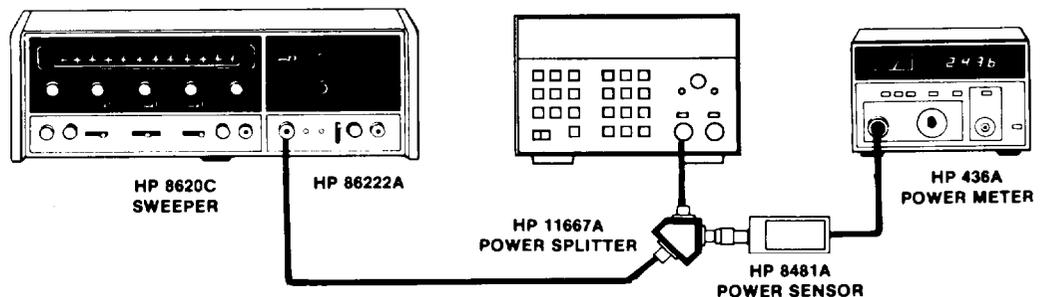
Setup:

a. 10 Hz—10 MHz



- Set the 5342A to 50 Ω , 10 Hz—500 MHz range, 1 Hz resolution.
- Set 651B to 10 Hz and 25 mV rms.
- Increase the frequency of the 651B and verify that the 5342A counts proper frequency from 10 Hz to 10 MHz.
- Measure actual sensitivity by decreasing the 651B level until the 5342A gives an unstable count at these frequencies: 10 Hz, 1 kHz, 500 kHz, 5 MHz, 10 MHz. Enter on performance test record (Table 4-1).

b. 10 MHz—520 MHz



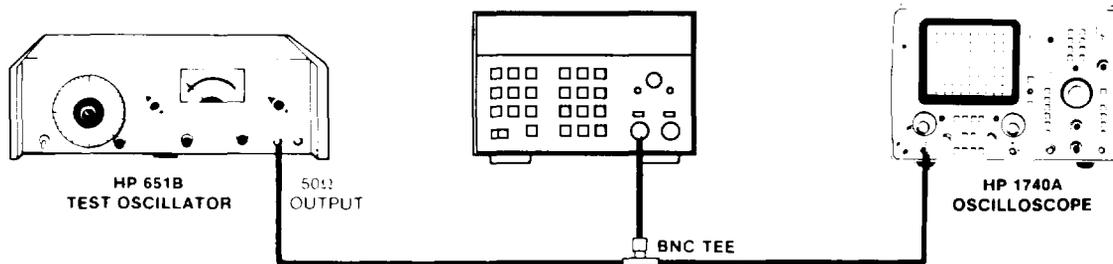
- 5342A settings remain unchanged.
- Set 436A power meter for AUTO range and dBm mode.
- Set the 86222A for INT leveling and adjust the output power level for a 436A reading of -19.3 dBm (25 mV rms into 50 Ω).
- Increase the frequency of the 8620C over the range of 10 MHz to 520 MHz and verify that the 5342A counts proper frequency. Use 436A to verify input power.
- Measure actual sensitivity at 50 MHz, 250 MHz, 520 MHz, and enter on performance test record (Table 4-5).

4-30. 10 Hz—500 MHz Input Sensitivity Test, 1 M Ω)

Specifications: 1 M Ω position, sensitivity = 50 mV rms for frequencies from 10 Hz—25 MHz.

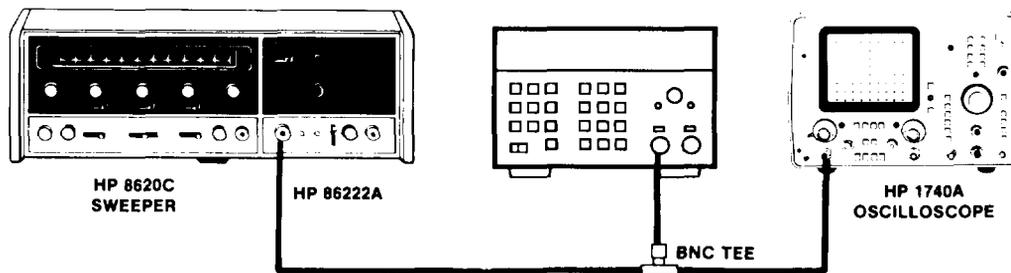
Setup:

a. 10 Hz—10 MHz



- Set the 5342A to 1 M Ω , 10 Hz—500 MHz range.
- Set the 651B to 10 Hz and adjust level for 141 mV p-p signal (50 mV rms).
- Increase the frequency of the 651B and verify that the 5342A counts proper frequency from 10 Hz to 10 MHz.
- Measure actual sensitivity at 10 Hz, 1kHz,500kHz,5MHz, and 10 MHz by monitoring p-p voltage on oscilloscope. Enter on performance test record (Table 4-5).

b. 10 MHz—25 MHz



5342A settings remain unchanged.

Adjust 86222A output for a 141 mV p-p (50 mV rms) reading on the 1740A.

Increase the frequency of the 8620C from 10 MHz—25 MHz and verify that the counter counts properly. Monitor the output level on the oscilloscope for 141 mV p-p (50 mV rms) over the range.

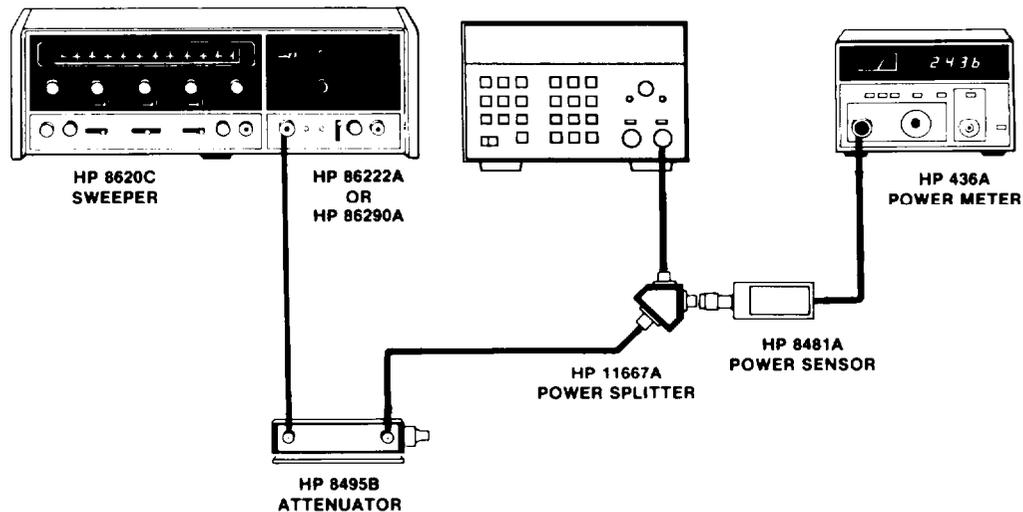
Measure actual sensitivity at 15 MHz, 25 MHz, and enter on performance test record (Table 4-5).

4-31. 500 MHz—18 GHz Input Sensitivity Test

Specification: Sensitivity = -25 dBm, 500 MHz—12.4 GHz
 = -20 dBm, 12.4 GHz—18 GHz

Description: The 5342A is set to the 500 MHz—18 GHz range and a signal at the rated sensitivity is applied to the type N connector. The frequency is slowly varied over the range of 500 MHz to 12.4 GHz and the 5342A is checked for proper counting. The output level of the test generator is increased to the second value, the frequency is slowly varied from 12.4 GHz to 18 GHz, and the 5342A checked for proper counting.

Setup:



- Set the 5342A to the 500 MHz—18 GHz range, AUTO mode.
- Connect the 11667A power splitter directly to the 5342A type N connector. Connect the 8481A power sensor directly to the other output port of the 11667A power splitter.
- Set the 8620C with the appropriate plug-in (86222A for 500 MHz to 2GHz, 86290A for 2 GHz—18 GHz) and the 8495B step attenuator to the rated sensitivity as measured on the 436A.
- Slowly increase the 8620C frequency over the range and verify that the 5342A counts properly.
- Measure actual sensitivity at 500 MHz, 1 GHz, 5GHz, 10 GHz, 12.4 GHz, 15 GHz, 17 GHz, and 18 GHz. Enter on performance test record (Table 4-5).

4-32 through 4-33. Deleted.

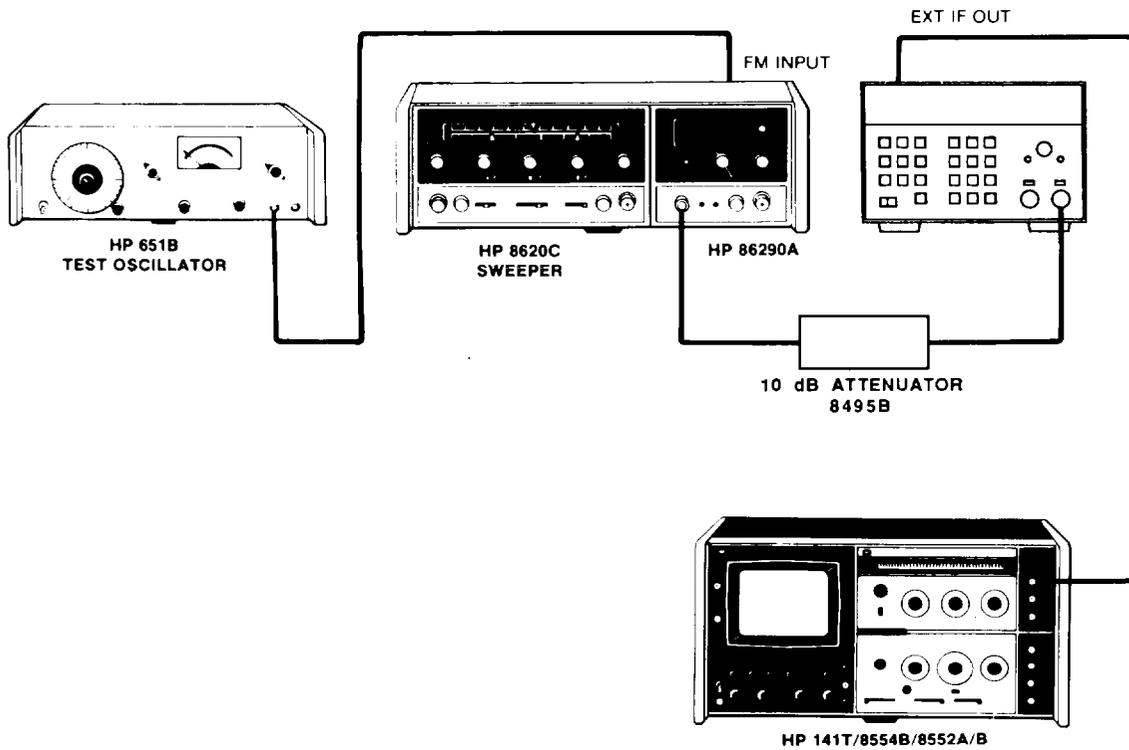
4-34. FM Tolerance Test

Specification: 20 MHz peak-to-peak (CW mode)
50 MHz peak-to-peak (FM mode)

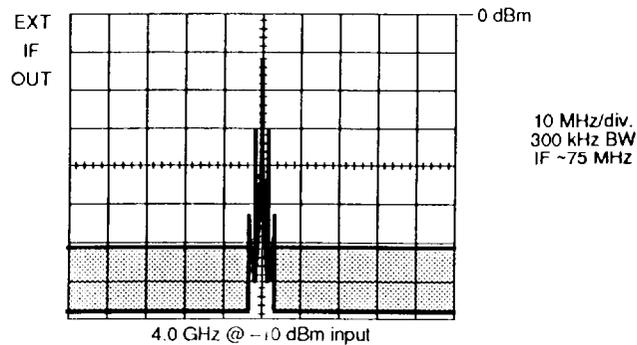
Description: The FM tolerance specification indicates the worst case FM deviation which can be present on a carrier that the counter can acquire and count. If the deviations are symmetrical about the carrier, then the counter averages out the deviations and displays the carrier frequency, A rear panel switch controls the CW mode and FM mode.

In this test, a function generator is used to FM them 8620C and the output is examined on a spectrum analyzer to measure the peak-to-peak deviation. The amplitude of the modulating waveform is adjusted for a 20 MHz p-p deviation and then a 50 MHz-p-p deviation.

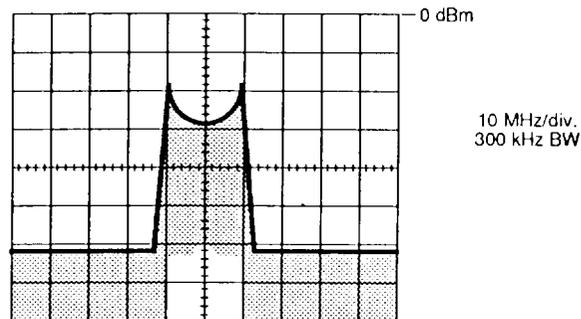
Setup:



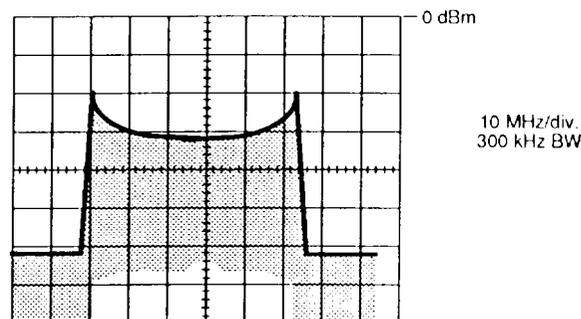
- Set 86290A to 4 GHz at -10 dBm.
- Put 5342A in 500 MHz—18 GHz range and AUTO mode. Observe IF OUT on the spectrum analyzer. Set 5342A to manual mode to setup peak-to-peak deviation.



- Apply modulating signal to EXT FM input on the rear panel of 86290A. Use a 100 kHz sine wave of sufficient amplitude to give 20 MHz p-p FM deviation as shown. (Modulating rate for this photo was 100 kHz.) Record on performance test record (Table 4-5).
- Switch the counter from manual to AUTO to verify that the counter will acquire and count the signal.



- If deviations are symmetrical about center frequency, the 5342A will average out the deviations and display the 4.0 GHz center frequency.
- Return the MAN mode. Increase amplitude of modulating waveform to produce a 50 MHz p-p deviation as shown below (fm = 100 kHz). Record on performance test record (Table 4-5).



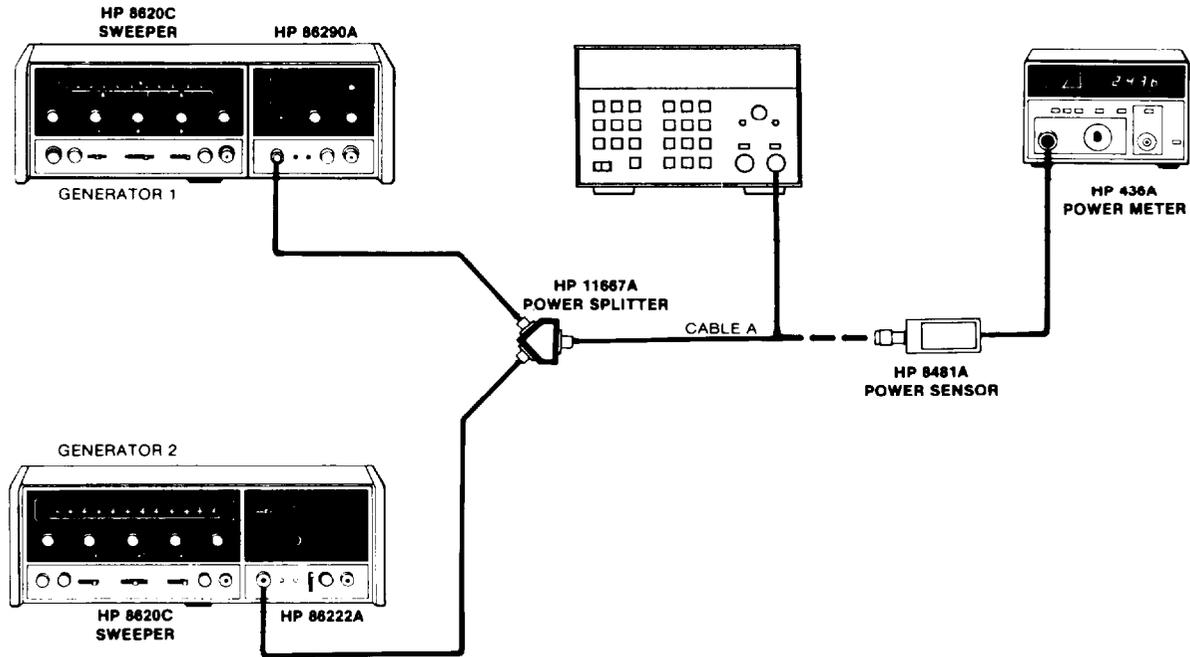
- Switch rear panel switch to FM. Switch counter from MAN to AUTO. Verify that the counter will acquire and count the signal,
- If deviations are symmetrical about the center frequency, the 5342A will average out the deviations and display the 4.0 GHz center frequency. For this case, the deviation is not symmetrical about the center frequency. To verify that the counter has passed the test, check that the displayed frequency is within 300 MHz of 4 GHz (if then N number computed is off by 1 due to excessive FM, then the displayed frequency will be off by 300 to 350 MHz).

4-35. Automatic Amplitude Discrimination Test

Specification: The 5342A measures the largest of all signals present, providing that the signal is 6 dB above any signal within 500 MHz; 20 dB above any signal, 500 MHz—18 GHz.

Description: In this test, two microwave generators are used to provide two signals into the 5342A. The relative level of the two signals is adjusted to the specification and the 5342A must count the higher amplitude signal.

Setup:



- Set generator 1 to 18 GHz and at a level to deliver -5 dBm to the 5342A. To set this level, disconnect generator 2 from the 11667A and terminate that input port of the 11667A with a 909A (Option 012) 50 termination. Connect the 8481A to the 5342A end of cable A and adjust the 86290A output for a -5 dBm reading.
- Set generator 2 to 500 MHz and at a level to deliver -25 dBm to the 5342A. To set this level, disconnect generator 1 from the 11667A (reconnect generator 2 to 11667A) and terminate the generator 1 input of the 11667A with a 909A 500 termination. Connect the 8481A to the 5342A end of cable A and adjust 86222A for a -25 dBm reading.
- Connect both generators to the 11667A inputs. Connect cable A to the 5342A. Verify that the 5342A counts 18 GHz. Record 20 dB (the algebraic difference between the 2 signal generator output levels) on the test record.
- Set generator 1 to 2.5 GHz at a level to deliver -5dBm to the 5342A using the technique described above. Set generator 2 to 2.0 GHz at a level to deliver -11 dBm to the 5342A using the technique described above. Connect both generators to the 11667A, and cable to the 5342A. Verify that the 5342A counts 2.5 GHz. Record -6dB on the test record.

4-36 through 4-40. Deleted

Table 4-5. Performance test Record

5342A S/N _____		Date _____		
PARA. NO.	TEST	MIN.	RESULTS	
			ACTUAL	MAX.
4-29	10 Hz—500 MHz Input Sensitivity (50 Ω): 10 Hz 1 kHz 500 kHz 5 MHz 10 MHz 50 MHz 250 MHz 520 MHz			25 mV rms I
4-30	10 Hz—500 MHz Input Sensitivity (1 M Ω): 10 Hz 1 kHz 500 kHz 5 MHz 10 MHz 15 MHz 25 MHz			50 mV rms (141 mV p-p) I
4-31	500 MHz—18 GHz Input Sensitivity: 500 MHz 1 GHz 5 GHz 10 GHz 12.4 GHz 15 GHz 17 GHz 18 GHz			Standard -25 dBm -20 dBm t
4-32 Deleted				
4-33 Deleted				
4-34	FM Tolerance: CW Mode	20 MHz p-p	Pass	
	FM mode	50 MHz p-p	Pass	
4-35	Automatic Amplitude Discrimination: 17.5 GHz separation 500 MHz separation			20 dB 6 dB

SECTION V ADJUSTMENTS

5-1. INTRODUCTION

5-2. This section describes the adjustments required to maintain the 5342A's operating characteristics within specifications. Adjustments should be made when required, such as after a performance test failure or when components are replaced that may affect an adjustment.

5-3. Table 5-1 is a list of all adjustable components in the 5342A and indicates the order in which adjustments should be performed.

5-4. EQUIPMENT REQUIRED

5-5. The test equipment required for the adjustment procedures is listed in Table 1-4, Recommended Test Equipment. Substitute instruments may be used if they meet the critical specifications.

5-5.1. CIRCUIT CARD REMOVAL

Remove power from the 5342A when installing or removing extender boards, and remove all extender boards when reinstalling the assemblies at the completion of the adjustment procedure, unless otherwise instructed. Refer to figure 8-21 for assembly location. Refer to figures 8-24 through 8-46 for adjustment locations. Refer to figure 8-43 (A22) for XA3 through XA24 location.

5-5.2. INPUT CABLE CONSIDERATIONS

Consideration should be given to input cable losses at higher frequencies. For example, a 6-foot section of RG-214/U coaxial cable has about 15dB loss at 18GHz. Such losses must be taken into consideration along with the sensitivity specifications given in Table 1-1.

5-6. FACTORY SELECTED COMPONENTS

5-7. Factory selected components are identified by an asterisk (*) in parts lists and schematic diagrams. Refer to paragraph 8-36 for replacement information.

5-8. ADJUSTMENT LOCATIONS

5-9. Adjustment locations are identified in the component locators in the Section VIII schematic diagrams and in the top view of the instrument, Figure 8-21.

5-10. SAFETY CONSIDERATIONS

5-11. This section contains warnings that must be followed for your protection and to avoid damage to the equipment.

Table 5-7. Adjustments

NAME	REFERENCE DESIGNATOR	NAME	POWER	ORDER
1. Power Supply Adjustments	A21R27	—	Set frequency of switching regulator to 37 kHz,	(1)
	A21R17	—	Sets reference voltage against which +5v (p) is compared.	(2)
	A19R5	—	Sets current level at which shutdown occurs.	(3)
2. Main Synthesizer Adjustment	A8R22	—	Sets free-run frequency of A8 Main VCO.	Can be done anytime
3. Offset Synthesizer Adjustments	A4R1	—	Sets free-run frequency of A4 OFFSET VCO.	(1)
	A6R1, A6R2	—	Set center and extremes of triangular search waveform on A6.	(2)
4. IF Adjustments	A25R28	"BAL"	Maximizes gain through A25U2.	(1)
	A25C11	—	Sets attenuation at 175 MHz	(2)
	A11R1	"AMP"	Maximize gain through A11U2.	(3)
	412R2	"B1"	Maximize gain through A12U2,	(4)
	A12R12	"B2"	Maximize gain through A12U4,	(5)
	A12R7	"OFS"	Sets level detector so counter counts 1 GHz, -130 dBm	(6)
	A25R31	"OFST"	Adjust detector to dash 5342A display at overload.	(7)
5. Direct Count Adjustment	A3R8		Adjust for maximum sensitivity.	Can be done anytime

WARNING

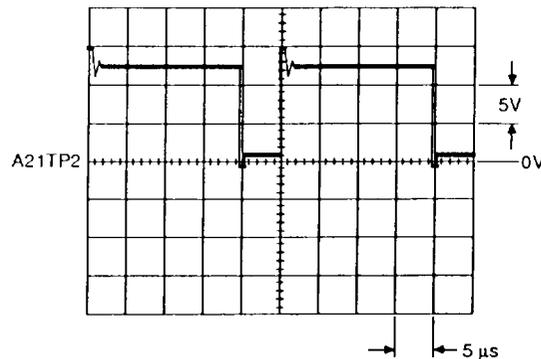
MAINTENANCE DESCRIBED HEREIN IS PERFORMED WITH POWER SUPPLIED TO THE INSTRUMENT, AND PROTECTIVE COVERS REMOVED. SUCH MAINTENANCE SHOULD BE PERFORMED ONLY BY SERVICE-TRAINED PERSONNEL WHO ARE AWARE OF THE HAZARDS INVOLVED (FOR EXAMPLE, FIRE AND ELECTRICAL SHOCK). WHERE MAINTENANCE CAN BE PERFORMED WITHOUT POWER APPLIED, THE POWER SHOULD BE REMOVED.

BEFORE ANY REPAIR IS COMPLETED, ENSURE THAT ALL SAFETY FEATURES ARE INTACT AND FUNCTIONING, AND THAT ALL NECESSARY PARTS ARE CONNECTED TO THEIR PROTECTIVE GROUNDING MEANS.

5-12. ADJUSTMENT PROCEDURES**5-13. Power Supply Adjustments**

5-14. Adjust resistor A21R27 (37 kHz frequency) as follows:

- a. Place A21 on extender board. Monitor A21TP2 with an oscilloscope.
- b. Adjust A21R27 (bottom, right side pot) for a $25 \mu\text{s} \pm 1 \mu\text{s}$ period as shown:



- c. Replace A21 in instrument.

5-15. Adjust resistor A21R17, +5V (D) as follows:

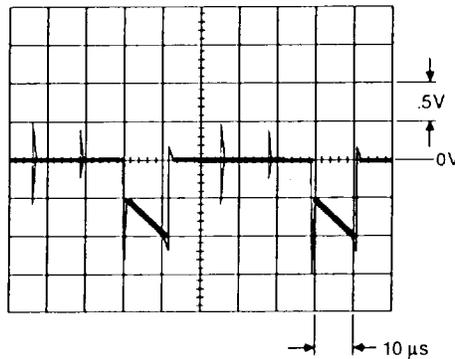
With a 3465A Multimeter in the DC VOLTS FUNCTION and 20V range, measure the dc voltage of the -5.2V supply at XA21 (5, $\bar{5}$). Adjust A21R17 for a -5.20 (-0.1, +0.05)V dc.

WARNING

PRIOR TO MAKING ANY VOLTAGE TESTS ON THE A19 PRIMARY POWER ASSEMBLY, THE VOLTMETER TO BE USED OR THE 5342A MUST BE ISOLATED FROM THE POWER MAINS BY USE OF AN ISOLATION TRANSFORMER. A TRANSFORMER SUCH AS AN ALLIED ELECTRONICS, 705-0048(120V AC) MAY BE USED FOR THIS PURPOSE. CONNECT THE TRANSFORMER BETWEEN THE AC POWER SOURCE AND THE AC POWER INPUT TO THE 5342A.

5-16, Adjust resistor A19R5 (over-current threshold) as follows:

- a. Put A19 on extender board.
- b. Apply power to 5342A via the isolation transformer.
- c. Connect scope probe to A19TPJ and scope probe ground to A19TPG.
- d. Adjust A19R5 for -1 volt amplitude on trailing edge of pulse as shown:



- e. Momentarily short +5V TP on A17 to ground. Observe red LED on A21 turn on and green LED on A20 turn off for approximately 2 seconds.
- f. Remove isolation transformer and replace A19.

5-17. Main Synthesizer Adjustment

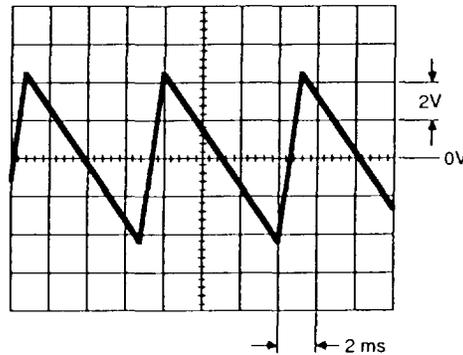
5-18. Adjust resistor A8R22 (Main VCO free-run frequency) as follows:

- a. Put 5342A in 10 Hz—500 MHz range, 50 Ω, Using cable with BNC on one end, clip leads on the other, connect XA5 ($\bar{10}$), the Main OSC signal, to the direct count input of the 5342A and measure the main VCO frequency.
- b. With a clip lead, ground A9TP1.
- c. Adjust A8R22 for a 325 (±2) MHz reading.
- d. Remove ground on A9TP1.

5-19. Offset Synthesizer Adjustments

5-20. Offset Synthesizer adjustments are made on assemblies A4 and A6 as follows:

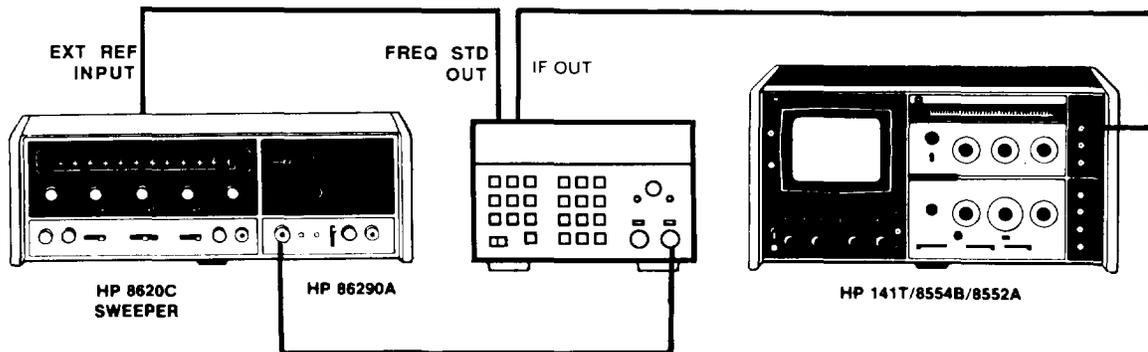
- a. Adjust A4R1 (Offset VCO free-run frequency) as follows:
 - 1. Put 5342A in 10 Hz—500 MHz range, 50 Ω . Using cable with BNC on one end, clip leads on the other, connect XA4 (10), the Offset OSC signal, to the direct count input of the 5342A and measure the Offset VCO frequency.
 - 2. With a clip lead, ground A6TP1.
 - 3. Adjust A4R1 for a 325 (± 2) MHz reading.
 - 4. Remove ground on A6TP1.
- b. Adjust A6R1, A6R2 (search sweep) as follows:
 - 1. Remove the A7 Assembly from the 5342A.
 - 2. Connect scope probe to A6TP1.
 - 3. Adjust A6R1 and A6R2 to obtain an 8V peak-to-peak ($\pm 0.8V$) triangular waveform, centered around 0V, as shown. When adjusted properly, the period will be 7.5 (± 2) ms.



- c. Reinstall A7 Assembly.

5-21. IF Adjustment

- a. Connect the test equipment as shown below.



b. Set the 5342A controls as follows:

Impedance 50 Ω
 Frequency Range 500 MHz to 18GHz
 Sample Rate Fully CCW

c. Set the Spectrum Analyzer controls as follows:

Center Frequency 100MHz
 Frequency Span/Div 20 MHz
 Bandwidth 300kHz
 Sweep Time 2msec
 Input Attenuation 0dB
 Reference Level 0dBm

5-22. A25R28 (preamp gain) adjustment

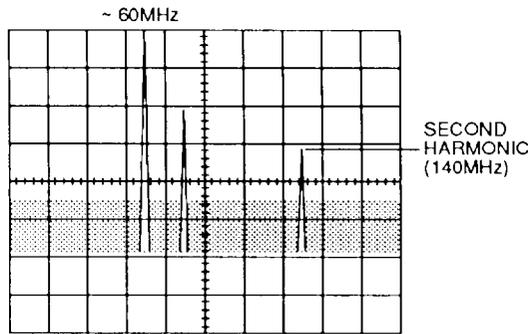
a. Set the 5342A controls as follows:

Press SET
 Press MAN
 Enter 500
 Press ENTER

b. Set the Signal Generator controls as follows:

Frequency 530 MHz
 Amplitude 0dBm

c. Adjust second harmonic (approx. 140MHz) as shown on Spectrum Analyzer display to minimum using A25R28.



5-23. A25C11 (175 MHz rolloff) adjustment

a. Set the 5342A controls as follows:

Press AUTO
 HOLD Fully CW
 press 2 times SET
 Enter 7
 Verify display indicates 350.5 MHz

- b. Set the Signal Generator controls as follows:

Start Frequency 60 MHz
 Stop Frequency 100 MHz
 Frequency Increment 5MHz
 Amplitude -15dBm

- c. Manually sweep the Signal Generator output from 60 MHz to 100 MHz and record the signal amplitude as shown on the Spectrum Analyzer display,
- d. Set the Signal Generator frequency to 175 MHz.
- e. On the 5342A, adjust SAMPLE RATE CCW until the 5342A display indicates approximately 330MHz, Set SAMPLE RATE to HOLD.

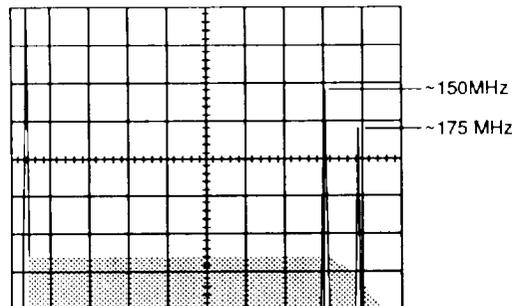
NOTE

Do not adjust A25C11 unless reading is not within specification.

- f. Adjust 175 MHz signal as shown on Spectrum Analyzer display to a level 10dB ±1dB less than the level recorded in step c using A25C11.

CAUTION

It will be necessary to use long nose pliers to adjust A25C11, Exercise care in making the adjustment as not to short out the circuit card to the equipment housing.



- g. On the 5342A, press RESET.

5-24. A11R1 (“Amp gain) adjustment

- a. Place A12 on a 22-pin extender board (HP P/N 05342-60034).
- b. Set sample rate fully ccw.
- c. Enter a center frequency of 500 MHz by keying in SET, MAN, 500, ENTER.
- d. Apply a 530MHz, -15dBm signal to the 5342A.
- e. Probe A12U2 pin 1 with a spectrum analyzer.
- f. Adjust A11R1 to minimize the second harmonic signal (at about 140MHz) seen on the spectrum analyzer.

5-25. A12R2 and A12R2 and A12R12 (gain) adjustments

- a. Apply a 530MHz, -25dBm signal to the 5342A.
- b. Probe A12U2 pin 5 with a spectrum analyzer.
- c. Adjust A12R2 to minimize the second harmonic signal (at about 140MHz) seen on the spectrum analyzer.
- d. Apply a 530MHz, -35dBm signal to the 5342A.
- e. Probe A12U4 pin 8 with a spectrum analyzer.
- f. Adjust A12R12 to minimize the second harmonic signal (at about 140MHz) signal seen on the spectrum analyzer.
- g. Remove extender board from A12 slot and insert A12 board.

5-26. A12R7 (threshold detect) adjustment

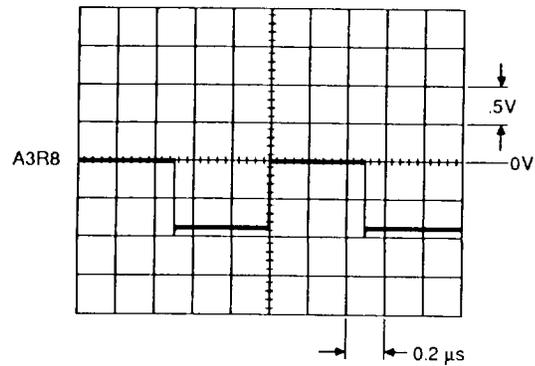
- a. Set 5324A to AUTO.
- b. Pre-set A12R7 maximum cw. Observe that the 5342A is not counting.
- c. Apply a 500MHz, -28dBm signal to the 500MHz-18GHz input of the 5342A.
- d. Adjust A12R7 ccw until the counter correctly reads 500MHz.
- e. Check frequencies up to 1GHz to assure proper count.
- f. Set synthesizer to -20dBm power level and manually sweep from 1 GHz to 18GHz to assure proper count.

5-27. Deleted.

5-28. Direct Count Adjustment

5-29. Adjust resistor A3R8 (Balance) as follows:

- a. Set 5342A to 10 Hz—500 MHz range and 50 Ω .
- b. Apply a 1 MHz sine wave signal at a level of 25 mV rms.
- c. Monitor A3TP1 (output of U5) on scope and adjust A3R8 for a 50% duty cycle.
- d. Decrease input level further and adjust A3R8 for 50% duty cycle. Keep decreasing level and adjusting A3R8 to the point where the counter no longer counts,

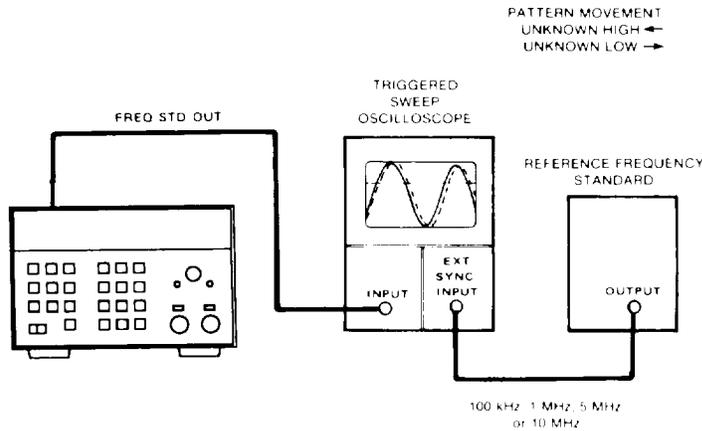
**5-30. OSCILLATOR ADJUSTMENTS**

5-31. Deleted

5-32. Oven Oscillator. Adjust the oscillator as follows:

NOTE

Allow 24-hour warmup for oven before this adjustment.



- Connect reference frequency standard to the external sync input of the oscilloscope.
- Connect rear panel FREQ STD OUT of the 5342A to Channel A of the scope.
- Adjust oscillator frequency for minimum sideways movement of the 10 MHz displayed signal.
- By timing the sideways movement (in CM per second), the approximate offset can be determined based on the oscilloscope sweep speed as shown in the following:

MOVEMENT	SWEEP SPEED			NOTES
	1 $\mu\text{s}/\text{cm}$	0.1 $\mu\text{s}/\text{cm}$	0.01 $\mu\text{s}/\text{cm}$	
1 cm/s	1×10^{-6}	1×10^{-7}	1×10^{-8}	TIME SCOPE TRACE MOVEMENT WITH SECOND HAND OF WATCH OR CLOCK
1 cm/10 s	1×10^{-7}	1×10^{-8}	1×10^{-9}	
1 cm/100 s	1×10^{-8}	1×10^{-9}	1×10^{-10}	

For example, if the trace moves 1 centimetre in 10 seconds and the sweep speed is 0.01 $\mu\text{s}/\text{cm}$, the oscillator signal is within 1×10^{-9} of the reference frequency.

- e. Verify amplitude of 10MHz signal as shown on the Oscilloscope is 1.41 to 1.70Vp-p (0.55Vrms \pm 50mV). If incorrect, adjust as follows:

NOTE

Oscilloscope must be terminated into 50 Ω . Incorrect amplitude will be displayed if other than 50 Ω impedance is used.

1. Remove A24 Assembly from 5342A.

THE A24 OSCILLATOR ASSEMBLY INTERNAL OVEN MASS TEMPERATURE MAY BE AS HIGH AS 85° C (185°F). TO AVOID SERIOUS BURNS DO NOT REMOVE OSCILLATOR CIRCUITS AND/OR OVEN MASS ASSEMBLY FROM THE OUTER HOUSING UNTIL THE OSCILLATOR HAS SUFFICIENTLY COOLED (APPROXIMATELY 1 HOUR WITH BOTTOM COVER AND FOAM INSULATOR REMOVED). THE OUTER HOUSING TEMPERATURE IS NOT A RELIABLE INDICATION OF THE INTERNAL TEMPERATURE.

2. Remove the three screws securing the A24 Assembly bottom cover. Remove the two screws securing P.C. edge connector to the outer can. Remove the top foam insulator to expose the A24 circuits.



DO NOT pull the oscillator circuits out of the outer housing by pulling on the P.C. edge connector or flex circuit!!

3. Once A24 Assembly is cool enough to handle, remove the oscillator circuits by pushing on the tuning capacitor (top of can) with a long, small diameter tool until the oscillator circuits can be removed freely.

NOTE

Under no circumstances should the oven circuit be operated with the oven mass removed from the outer housing. To do so will cause damage to components inside the oven mass.

4. Remove fuse A24A1F1 (Fig. C-14).
5. Using a 15 pin extender board, reinstall A24 Assembly.
6. Remove A18 Assembly,
7. Connect AC Power Cable to 5342A rear panel and set front panel POWER switch to STBY.

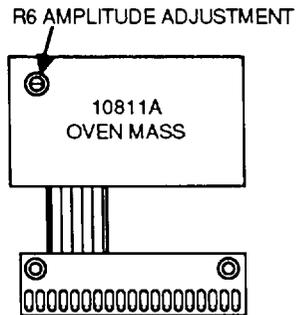
CAUTION

It will be necessary to support A24 during adjustment

8. Connect oscilloscope 50 W 1:1 probe to XA18 pin $\bar{8}$. Adjust A24A1R6 until amplitude as shown on oscilloscope display is from 1.41 to 1.70Vp-p.

NOTE

Oscilloscope must be terminated into 50 Ω . Incorrect amplitude will be displayed if other than 50 Ω impedance is used.



9. Remove power. Reinstall A18 Assembly.

10. Reassemble and reinstall A24 Assembly.

5-33 through 5-42. Deleted

**SECTION VI
REPLACEABLE PARTS**

Deleted

SECTION VII MANUAL CHANGES

Deleted

SECTION VIII SERVICE

8-1. INTRODUCTION

8-2. This section provides service information and symbol descriptions, theory of operation, troubleshooting procedures, and schematic diagrams. The arrangement of content of this section is described in detail below. Refer to the Table of Contents for specific page and paragraph numbers.

- a. **Schematic Diagram Symbols and Reference Designations.** Describes the symbols used on schematic diagrams and reference designators used for parts, subassemblies and assemblies.
- b. **Identification Markings.** Describes the method used by Hewlett-Packard for identifying printed-circuit boards and assemblies.
- c. **Safety Considerations.** Describes the safety considerations applicable during maintenance, adjustments, and repair.
- d. **Signal Names.** Lists signal mnemonics, names, source, destination, and function for 5342A signals.
- e. **Disassembly and Reassembly Procedures.** Describes removal of covers, front frame, assemblies to gain access to parts.
- f. **Factory Selected Components.** Lists procedures for replacement of parts whose values are selected at time of manufacture for optimum performance.
- g. **Service Accessory Kit 10842A.** Describes the use and function of kit (extender boards) used for testing pc boards.
- h. **Logic Symbols.** Description of logic symbols used on schematics.
- i. **Theory of Operation.** Includes block diagram description of overall operation, special function descriptions, and detailed circuit operation explanations.
- j. **Assembly Locations.** Describes and illustrates location of assemblies, adjustments, front and rear panel components by reference designators.
- k. **Troubleshooting Procedures.** Provides troubleshooting techniques, recommended test equipment, and troubleshooting tables arranged to isolate trouble to an assembly and then to the component level.
- l. **Schematic Diagrams.** A diagram for each assembly is included, arranged in order of assembly number. A component locator photo is included adjacent to each diagram. The schematic diagrams contain tables of reference designations, tables of active elements (by part number), voltage measurements and signature analyzer signatures, where applicable.

8-3. SCHEMATIC DIAGRAM SYMBOLS AND REFERENCE DESIGNATORS

8-4. Figure 8-1 shows the symbols used on the schematic diagrams. At the bottom of Figure 8-1, the system for reference designators, assemblies, and subassemblies is shown.

8-5. Reference Designations

8-6. Assemblies such as printed-circuits are assigned numbers in sequence, A1, A2, etc. As shown in Figure 8-1, subassemblies within an assembly are given a subordinate A number. For

example, rectifier subassembly A1 has the complete designator of A25A1. For individual components, the complete designator is determined by adding the assembly number and sub-assembly number if any. For example, CR1 on the rectifier assembly is designated A25A1CRI.

8-7. IDENTIFICATION MARKINGS ON PRINTED-CIRCUIT BOARDS

8-8. HP printed-circuit boards (see *Figure 8-1*) have four identification numbers: an assembly part number, a series number, a revision letter, and a production code.

8-9. The assembly part number has 10 digits (such as 05342-60001) and is the primary identification. All assemblies with the same part number are interchangeable. When a production change is made on an assembly that makes it incompatible with previous assemblies, a change in part number is required. The series number (such as 1720A) is used to document minor electrical changes. As changes are made, the series number is incremented. When replacement boards are ordered, you may receive a replacement with a different series number. If there is a difference between the series number marked on the board and the schematic in this manual, a minor electrical difference exists.

8-10. Revision letters (A, B, etc.) denote changes in printed-circuit layout. For example, if a capacitor type is changed (electrical value may remain the same) and requires different spacing for its leads, the printed-circuit board layout is changed and the revision letter is incremented to the next letter. When a revision letter changes the series number is also usually changed. The production code is the four-digit seven-segment number used for production purposes.

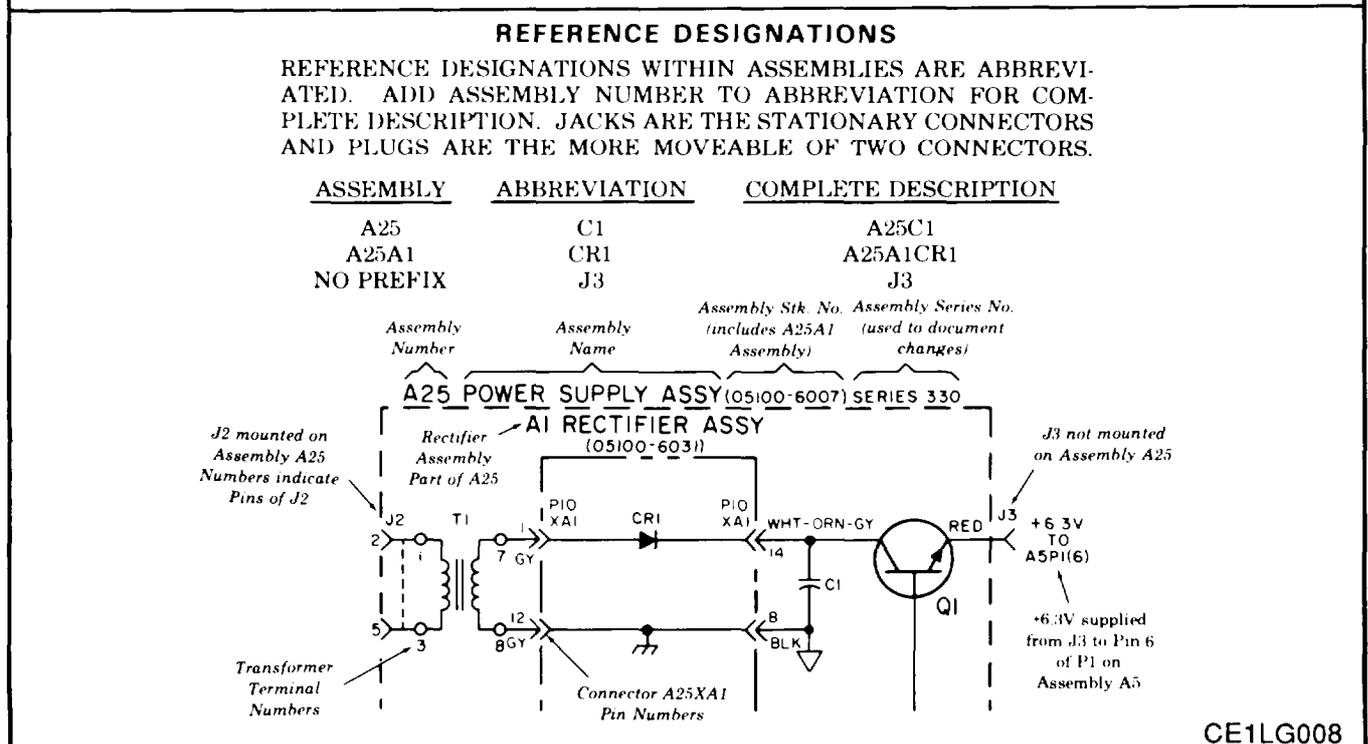
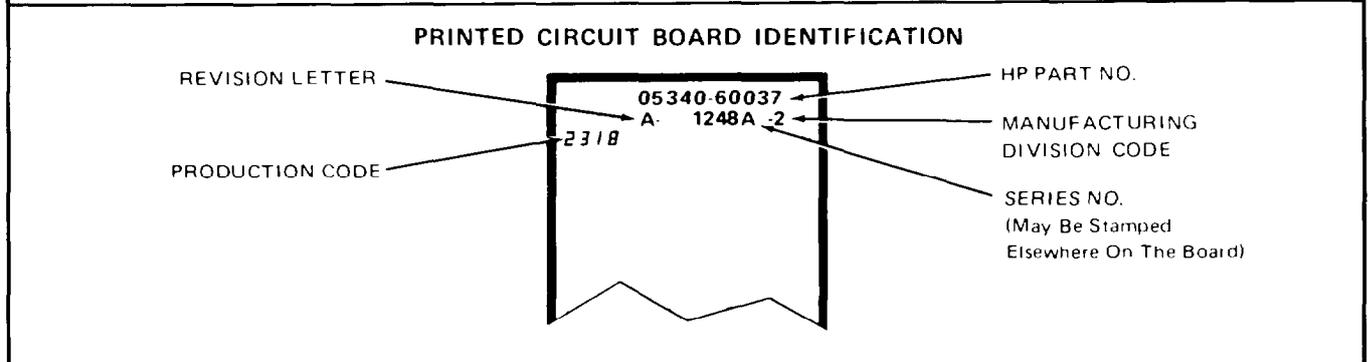
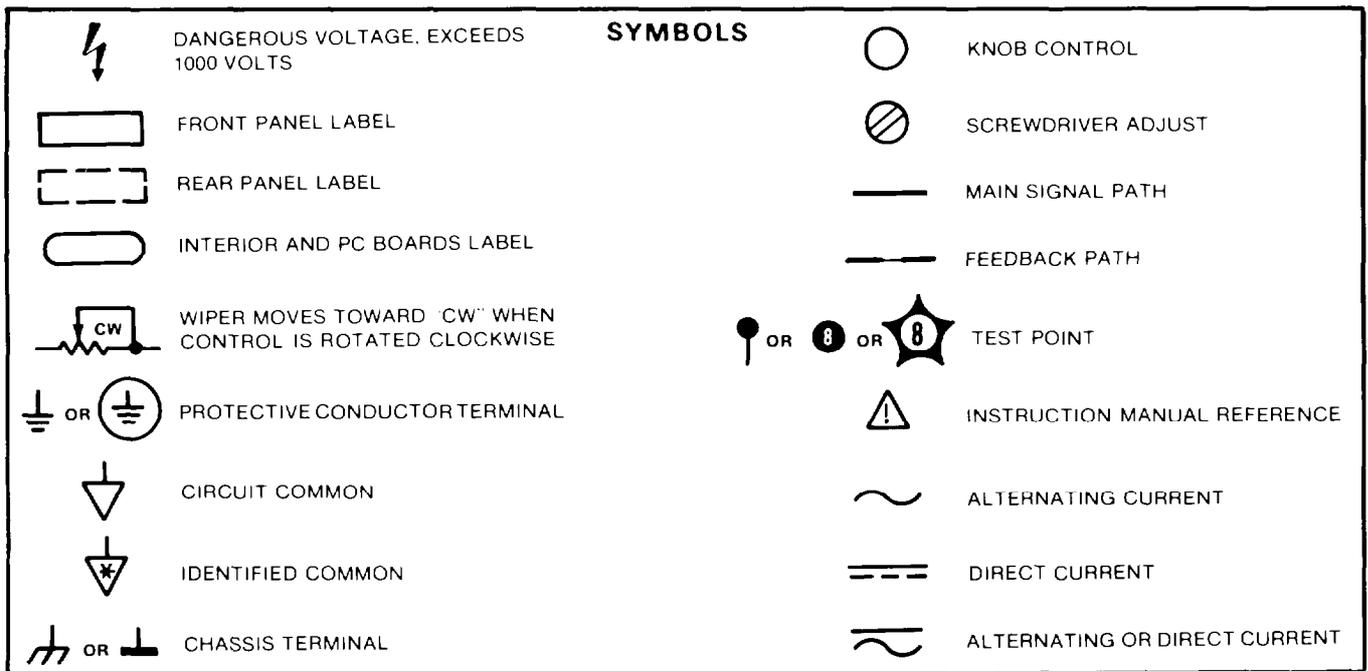


Figure 8-1. Schematic Diagrams Notes

8-11. Assembly Identification

8-12. The assembly number, name, and Hewlett-Packard part number of 5342A assemblies are listed in Table 8-7.

Table 8-1, Assembly Identification

ASSEMBLY	NAME	HP PART NO.
A1 A2	Keyboard Display Display Driver	05342-60041 05342-60002
A3 A4	Direct Count Amplifier Offset VCO	05342-60042 05342-60004
A5 A6 A7 A8 A9	RF Multiplexer Offset Loop Amplifier Mixer/Search Control Main VCO Main Loop Amplifier	05342-60005 05342-60006 05342-60007 05342-60008 05342-60009
A10 A11 A12 A13 A14	Divide-by-N IF Limiter IF Detector Counter Processor	05342-60010 05342-60011 05342-60012 05342-60013 05342-60072
A15	HP-IB	05342-60015
A17 A18	Timing Generator Time Base Buffer	05342-60017 05342-60068
A19 A20 A21 A22 A23	Primary Power Secondary Power Switch Drive Motherboard Power Module	05342-60019 05342-60020 05342-60069 05342-0067 0960-0444
A24 A25 A26 U1	Oscillator Preamplifier Sampler Driver Sampler	10811-60111 05342-60025 05342-60026 5088-7022
A29	HP-IB Interconnection	05342-60029

8-13. SAFETY CONSIDERATIONS

8-14. Although this instrument has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings which must be followed to ensure safe operation and to retain the instrument in safe condition. Service and adjustments should be performed only by service-trained personnel.

WARNING

ANY INTERRUPTION OF THE PROTECTIVE (GROUNDING) CONDUCTOR (INSIDE OR OUTSIDE THE INSTRUMENT) OR DISCONNECTION OF THE PROTECTIVE EARTH TERMINAL IS LIKELY TO MAKE THE INSTRUMENT DANGEROUS. INTENTIONAL INTERRUPTION IS PROHIBITED.

8-15. Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible and, when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

8-16. Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

8-17. Make sure that only fuses with the required rated current and of the specified type (normal blow, time delay, etc.) are used for replacement. The use of repaired fuses and the short-circuiting of fuseholders must be avoided.

WARNING

PRIOR TO MAKING ANY VOLTAGE TESTS ON THE A19 PRIMARY POWER ASSEMBLY, THE VOLTMETER TO BE USED OR THE 5342A MUST BE ISOLATED FROM THE POWER MAINS BY USE OF AN ISOLATION TRANSFORMER. A TRANSFORMER SUCH AS AN ALLIED ELECTRONICS, 705-0048 (120V AC) MAY BE USED FOR THIS PURPOSE. CONNECT THE TRANSFORMER BETWEEN THE AC POWER SOURCE AND THE POWER INPUT TO THE 5342A.

8-18. Safety Symbols

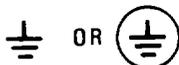
8-19. The following safety symbols are used on equipment and in manuals:



Instruction manual symbol. The product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.



Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts must be so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. A terminal marked with the symbol must be connected to ground in the manner described in the installation (operating) manual, and before operating the equipment.



Frame and chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



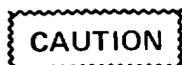
Direct current (power line).



Alternating or direct current (power line).



The WARNING signal denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury.



The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

8-20. SIGNAL NAMES

8-21. Table 8-2 is a list of signal names used in the 5342A. The list is in alphabetical order and includes the mnemonics for cross-reference with the schematic diagram signal names. A description of the function of each signal and the source and destination is included in the table.

Table 8-2. Signal/Names

MNEMONIC	NAME	FROM	TO	FUNCTION
A0	Address 0	XA14A(3)	XA13(1), XA15A(3), XA16A(3), A22W4(5), A22J1(24)	Address Lines
A1	Address 1	XA14A(4)	XA13(2), XA15A(4), XA16A(4), A22W4(6), A22J1(23)	
A2	Address 2	XA14A(5)	XA13(3), XA15A(5), XA16A(5), A22W4(9), A22J1(22)	
A3	Address 3	XA14A(6)	XA13A(4), XA15A(6), XA16A(6), A22W4(10), A22J1(10)	
A4	Address 4	XA14A(7)	XA13(5), XA15A(7), XA16A(7), A22W4(17)	
A5	Address 5	XA14A(8)	XA13(6), XA15A(8), XA16(8), A22W4(18)	
A6	Address 6	XA14A(9)	XA15A(9), XA16A(9), A22W4(19)	
A7	Address 7	XA14A(10)	XA15A(10), XA16A(10), A22W4(20)	
A8	Address 8	XA14A(11)	XA15A(11), XA16A(11), A22W4(33)	
A9	Address 9	XA14A(12)	XA15A(12), XA16A(12), A22W4(34)	
A10	Address 10	XA14A(13)	XA15A(13), XA16A(13), A22W4(35)	
A11	Address 11	XA14A(14)	XA15A(14), XA16A(14), A22W4(36)	
A12	Address 12	XA14A(15)	XA15A(15), XA16A(15), A22W4(37)	
A13	Address 13	XA14A(16)	XA15A(16), XA16A(16), A22W4(38)	
A14	Address 14	XA14A(17)	XA15A(17), XA16A(17), A22W4(39)	
A15	Address 15	XA14A(18)	XA15A(18), XA16A(18), A22W4(40)	
.T1 or (ATT)	Attenuation	A25(AT1)	XA16B(3)	Signal from A25 Preamp current source to the XA16.

Table 8-2. Signal Names (Continued)

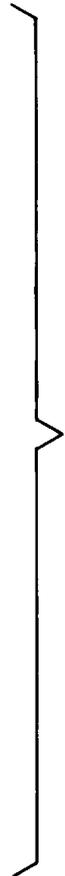
MNEMONIC	NAME	FROM	TO	FUNCTION	
CHECK	Check Output	XA10($\overline{11}$)	XA11&7, $\overline{7}$	75 MHz signal sent from A10 Divide-by-N to A11 IF Limiter when 5342A is in CHECK mode.	
CLOCK (CLK)	Clock	XA17(4)	XA14B(8, $\overline{8}$)	1 MHz TTL clock sent from A17 Timing Generator to A14 Microprocessor clock generator to derive $\theta 1$ and $\theta 2$ from MPU.	
DIRECT A	Direct Count A Output	XA3(2)	XA13($\overline{7}$)	Divide-by-two output of Direct Count Amplifier Assembly to A13 Counter Assembly.	
DIRECT B	Direct Count B Output	XA3($\overline{1}$)	XA13(14)	Divide-by-four output of Direct Count Amplifier Assembly to A13 Counter Assembly.	
DIV N	Divide-by-N	XA8($\overline{5}$)	XA10(8)	Signal from A8 Main VCO to A10 Divide-by-N.	
D0	Data 0	XA14A(3)	XA9($\overline{9}$), XA10(15), XA13(1), XA14A(3), XA15A(3), XA16A(3), XA17(10), A22J1(20), X22W4(11)	 <p style="text-align: center;">Data Lines</p>	
D1	Data 1	XA14A(4)	XA10(16), XA13(2), XA17(11), A22J1(19), A22W4(12)		
D2	Data 2	XA14A(5)	XA10(17), XA13(3), XA15A($\overline{5}$), XA16A(5), XA17(12), A22J1(18), A22W4(13)		
D3	Data 3	XA14(6)	XA10(18), XA13(4), XA15A(6), XA16A(6), XA17(13), A22J1(17), A22W4(14)		
D4	Data 4	XA14A(7)	XA10($\overline{15}$), XA12(15, $\overline{15}$), XA15A(7), XA16A(7), XA17(11), A22J1(5), A22W4(15)		
D5	Data 5	XA14A(8)	XA10($\overline{16}$), XA12(16, $\overline{16}$), XA15A(8), XA16A(8), XA17(10), A22J1(6), A22W4(16)		
D6	Data 6	XA14A(9)	XA10($\overline{17}$), XA12(17, $\overline{17}$), XA15A(9), XA16A(9), XA17(9), A22J1(7), A22W4(23)		
D7	Data 7	XA14A(10)	XA10($\overline{18}$), XA12(18, $\overline{18}$), XA15A(10), XA16A(10), XA17(8), A22J1(8), A22W4(24)		
EXT IN	External Input	J2 (rear panel)	XA18($\overline{10}$)		Signal from an external source via J2 on rear panel to A18 Time Base Buffer Assembly

Table 8-2. Signal Names (Continued)

MNEMONIC	NAME	FROM	TO	FUNCTION
HECL RST (HECLR)	High ECL Reset	XA13(10)	XA3(4)	High signal from A13 Counter Assembly that resets the main gate on A3 Direct Count Amplifier Assembly.
HDSP WRT (HDSP)	High Display Write	XA14B(10)	XA2(3)	High signal from A14 Microprocessor causes data from bus to be written into RAM on A2 Display Driver. When signal goes low, contents of RAM are displayed.
HSRCH EN	High Search Enable	XA7(2)	XA6(8)	High signal from 500 kHz detector on A7 sent to Search Generator on A6 if the offset VCO frequency is not 500 kHz less than the main VCO frequency.
IF	Intermediate Frequency	A25J1	XA11(\overline{T}), via A22W3	A25 Preamplifier output to A11 IF Limiter Assembly.
IF COUNT	Intermediate Frequency to Counter	XA12(8)	XA13(7)	A12 IF Detector output to A13 Counter Assembly
IF LIM	Intermediate Frequency Limiter Output	XA11($\overline{T2}$)	XA12(\overline{T})	A11 IF Limiter output to A12 IF Detector Assembly.
IF OUT	Intermediate Frequency Output	A25J2	J4 (rear panel) via W3	A25 Preamplifier intermediate frequency output to rear panel connector.
ISOLATOR	Optical Isolator	XA19(18, $\overline{T8}$)	XA20(15, $\overline{T5}$), XA21(17, $\overline{T7}$)	Signals excessive current load to the U3 Timer Over-current shutdown circuit.
LCTR RD	Low Counter Read	XA14B(2)	XA13(6)	Signal from A14 Microprocessor to A13 Counter Multiplexer circuit to read contents of A or B counter to the data bus (depending upon the state of the A5 line).
LCTR WRT	Low Counter Write	XA14B(3)	XA13(7)	Signal from A14 Microprocessor to A13 Counter FF circuit that selects either IF or Direct B to be counted.

Table 8-2. Signal Names (Continued)

MNEMONIC	NAME	FROM	TO	FUNCTION
LDIRECT	Low Direct	XA13($\overline{14}$)	XA16B($\overline{7}$)	Signal from A13 Counter that switches A27 LF Amp or U2 HF Amp.
LDIR Gate	Low Direct Gate	XA17($\overline{4}$)	XA3(5)	Low signal from A17 Timing Generator that enables the direct count main gate on A3 Direct Count Amplifier Assembly.
LDVRST	Low Device Reset	XA14B(4)	XA2J1(9)	Temporary low signal from A14 Microprocessor to A2 Display that blanks the display during power up.
LEXT	Low External	S4 (rear panel)	XA18(9)	Low signal from rear panel switch (EXT/INT) in EXT position that selects external oscillator input to A18 Time Base Buffer instead of internal oscillator.
LFM	Low Frequency Modulation	S3 (rear panel)	XA17($\overline{12}$)	Low signal from rear panel switch (CW/FM) in FM position that selects long prs and illuminates FM indicator on display.
LFRRUN (LFRUN)	Low Free Run	XA14B($\overline{1}$)	A14S2 (Ground)	Low signal cause MPU on A14 Microprocessor to continuously increment the addresses on the address bus (for diagnostic purposes).
LHP-IB	Low HP Interface Bus	XA14B($\overline{14}$)	XA15B(6)	Low signal from decoder on A14 Microprocessor to enable reading from and writing to A15 HP-IB.
LIF Gate	Low Intermediate Frequency Gate	XA17($\overline{5}$)	XA13(16)	Low signal from A17 Timing Generator that enables counter A or B on A13 Counter Assembly (depending upon the state of the LO switch signal).
LIRQ	Low Interrupt Request	XA2J1(1)	XA14A(13)	Low signal from A2 Display Driver or HP-IB Option 011 that interrupts A14 Microprocessor.
LKBRD (LKBR)	Low Keyboard	XA14B(9)	XA2(4)	Low signal enables A2 Display Driver to send keyboard information to A14 Microprocessor.
LO FREQ	Local Oscillator Frequency	A4W1	A26J2	A5 Multiplexer Local Oscillator output to A26 Sampler Driver.

Table 8-2. Signal Names (Continued)

MNEMONIC	NAME	FROM	TO	FUNCTION
LO Switch	Local Oscillator Switch	XA17($\overline{11}$)	XA5($\overline{5}$), XA13($\overline{8}$)	Low signal from A17 Timing Generator that switches A5 Multiplexer between Main VCO and Offset VCO synchronously with switching between Counter A and B on A13 Counter Assembly.
LOVL (OL)	Low Overload	A25C29	XA12(14)	Low signal from A25 Pre-amplifier amplitude detector to A12 IF Detector bus driver to indicate input signal level to 5342A exceeds +5 dBm.
LPD READ (LPDRD)	Low Power Detect Read	XA14B($\overline{9}$)	XA12($\overline{13}$)	Low signal from A14 Microprocessor to A12 IF Detector that causes A12 to output data to the bus.
LPD WRT	Low Power Detect Write	XA14B($\overline{10}$)	XA12($\overline{14}$), XA9(9)	Low signal from A14 Microprocessor to A12 IF Detector that causes A12 to detect input signal power level. When high, selects narrow or wide filter on A9 Main Loop Amplifier, depending upon the state of data bit D0.
LPOS SLOPE (LPOS SL)	Low Positive Slope	XA6($\overline{8}$)	XA7($\overline{2}$)	Low signal from A6 Search Generator to A7 Mixer/Search Control prevents loop from locking on upper sideband when offset VCO is 500 kHz greater than main VCO.
LTIM RD (LTMRD)	Low Timing Read	XA14B($\overline{6}$)	XA17(8)	Low signal from A14 Microprocessor that results in data transfer from A17 Timing Generator to A14 via the data bus.
LTIM WRT (LTMWRT)	Low Timing Write	XA14B($\overline{7}$)	XA17(9)	Low signal from A14 Microprocessor that clocks data into the Input Register on A17 Timing Generator.
LSYNHI (LSYH)	Low Synch High	XA14B($\overline{11}$)	XA10($\overline{14}$)	Low to high transition from A14 Microprocessor decoder that loads the high order bits into the N register on the A10 Divide-by-N Assembly.

Table 8-2. Signal Names (Continued)

MNEMONIC	NAME	FROM	TO	FUNCTION
LSYNLO (LSYL)	Low Synch Low	XA14B($\overline{12}$)	XA10(14)	Low to high transition from A14 Microprocessor decoder that loads low order bits into N register.
LXROM	Low External ROM	XA15A(16), XA16A(16)	XA14A(16)	Not used.
MAIN $\Delta\phi 1$	Main Phase Error 1	XA10(1)	XA9(12)	Phase error signals from A10 Divide-by-N assembly to A9 Main Loop Amplifier
MAIN $\Delta\phi 2$	Main Phase Error 2	XA10($\overline{1}$)	XA9($\overline{12}$)	that control the A8 Main Main VCO.
MAIN CTRL	Main Control	XA9(6)	XA8(1)	Control voltage signal from A9 Main Loop Amplifier that controls the frequency of the A8 Main VCO.
MAIN OSC	Main Oscillator	XA8(7)	XA5(10)	A8 Main VCO output to A5 RF Multiplexer Assembly.
MAIN VCO	Main Voltage Controlled Oscillator	XA8(3)	XA7(12)	A8 Main VCO output to A7 Mixer/Search Control Assembly that is mixed with the signal from A4 Offset VCO.
OFFSET $\Delta\phi 1$	Offset Phase 1	XA7(1)	XA6(10)	A7 Mixer/Search Control outputs that are processed by A6 Offset Loop Amplifier
OFFSET $\Delta\phi 2$	Offset Phase 2	XA7($\overline{1}$)	XA6($\overline{10}$)	to develop OFFSET CONTROL signal.
OFS CNTRL	Offset Control	XA6(6)	XA4(5)	A dc control voltage signal from A6 Offset Loop Amplifier to A4 Offset VCO Assembly.
OFS OSC	Offset Oscillator	XA4(10)	XA5(1)	A4 Offset VCO output to A5 RF Multiplexer Assembly.
OFS VCO	Offset Voltage Controlled Oscillator	XA4($\overline{7}$)	XA7(9)	A7 Offset VCO output to A7 Mixer/Search Control Assembly.
500 kHz	500 kilohertz	XA18(3)	XA7($\overline{7}$), XA10(5, $\overline{5}$)	500 kHz signal from A18 Time Base to the phase detector on A7 and to $\div 10$ circuit on A10 Divide-by-N Assembly.
1 MHz	1 Megahertz	XA18(1)	XA12($\overline{10}$), XA17(6)	1 MHz signal from A18 Time Base to A12 IF Detector and to the prs generator on A17 Timing Generator.
10 MHz OUT	10 Megahertz Out	XA18(5)	J3 (rear panel)	10 MHz signal from A18 Time Base to FREQ STD OUT connector on rear panel.

8-22. DISASSEMBLY AND REASSEMBLY

8-23. Before performing any of the following disassembly or reassembly procedures, the following steps must be performed.

- a. Set LINE ON-STBY switch to STBY position.
- b. Remove line power cable from Input Power Module (A23).

8-24. Top Cover Removal

8-25. To remove the top cover proceed as follows:

- a. Place 5342A with top cover facing up.
- b. At top rear of instrument remove pozidrive screw from rear cap retainer and remove retainer.
- c. Slide top cover back until free from frame and lift off.
- d. To gain access to pc assemblies remove screws from top plate and remove plate.

8-26. Bottom Cover Removal

8-27. To remove the bottom cover proceed as follows:

- a. Place 5342A with bottom cover facing up.

CAUTION

In the following step, the two front plastic feet must be removed from the bottom panel to avoid damage to internal wiring.

- b. Remove two front plastic feet from bottom cover. Lift upon back edge of plastic foot and push back on front edge of plastic foot to free foot from bottom cover.
- c. Loosen captive pozidrive screw at rear edge of bottom cover.
- d. Slide bottom cover back until it clears the frame. Reverse the procedure to replace the cover.

8-28. FRONT FRAME REMOVAL

8-29. To remove front frame from main housing of the instrument, proceed as follows:

- a. Remove top and bottom covers as described in preceding paragraphs.
- b. Remove nut from type N connector on front panel.
- c. Remove two screws from front of each side strut attaching front panel frame.
- d. From bottom front of instrument, remove coax cable by pulling off connectors from A1J1 and A1J3. Remove cable strap connector from A2 Display Driver board. Note orientation of connector pins for reference during reassembly.

CAUTION

In the following step, note the cable attached to the power LINE switch and avoid stress on cable connections during removal of front panel frame.

- e. Slowly slide front panel frame off while pressing type N connector rearward through panel.
- f. The front panel frame (containing assemblies A1 and A2) can now be moved freely within limits of the power cable, as shown in Figure 8-2.

8-30. Removal of A1 Display Assembly and A2 Display Drive Assembly from Front Panel Frame

8-31. To remove A1 and A2 assemblies, remove frame as described in above paragraph and proceed as follows:

- a. Remove the A1-A2 assemblies (combined) from front panel frame by removing the nut from the front panel BNC connector and removing the 5 large attaching screws from A2 Display Driver board.
- b. Separate the A1 and A2 assemblies by removing the two nuts attaching plug P1 on the A1 Display assembly. Do not remove the attached screws from A2 Display Driver assembly.
- c. Reassembly procedures are essentially the reverse of the disassembly procedures.

8-32. Replacement of LED's in Front Panel Switches

8-33. To replace a defective LED in a front panel pushbutton switch, remove and separate the A1 and A2 boards as described in the preceding paragraphs, and proceed as follows:

- a. Pull off the switch cap that covers the defective LED.
- b. Use a short length (approximately 2 inches) of heat-shrink tubing that will fit over the replacement LED. Apply heat to the tubing to make a tight fit.
- c. Unsolder the connections to the defective LED on the A1 board. Slide the heat-shrink tubing over the defective LED and withdraw.
- d. Place the replacement LED into the heat-shrink tubing and insert into the switch. Solder the leads to the board.

8-34. Removal of U1 Sampler, A25 Preamplifier, and A26 Sampler Driver

8-35. Remove U1, A25, and A26 as follows:

- a. Remove 5342A bottom panel by loosening screw at rear, remove two front feet and slide panel rearward.
- b. Refer to Figure 8-22 and locate assemblies at bottom front of instrument.
- c. Pull off coax cables from A1J1, A1J3, A25J1 (IF OUT INT), and A25J2 (IF OUT EXT).
- d. Disconnect rigid coax from U1 Sampler by loosening attaching nut.
- e. Remove nut on front panel type N connector and remove rigid cable to allow access.
- f. Remove W2 cable strap connector at A22 motherboard and move cable strap to one side to allow access.
- g. Remove 5 screws attaching A25 mounting bracket (four corner and one middle screw) and withdraw bracket (and attached assemblies) from instrument.
- h. Remove A26 from bracket by removing the 2 small attaching bolts and nuts. Separate A26 from U1 by loosening the interconnecting hex connector from U1. Remove the cover from A26 to gain access to components.
- i. Remove U1 by removing one small bolt and nut. Pull U1 up out of socket.
- j. Assembly procedures are essentially the reverse order of the disassembly.

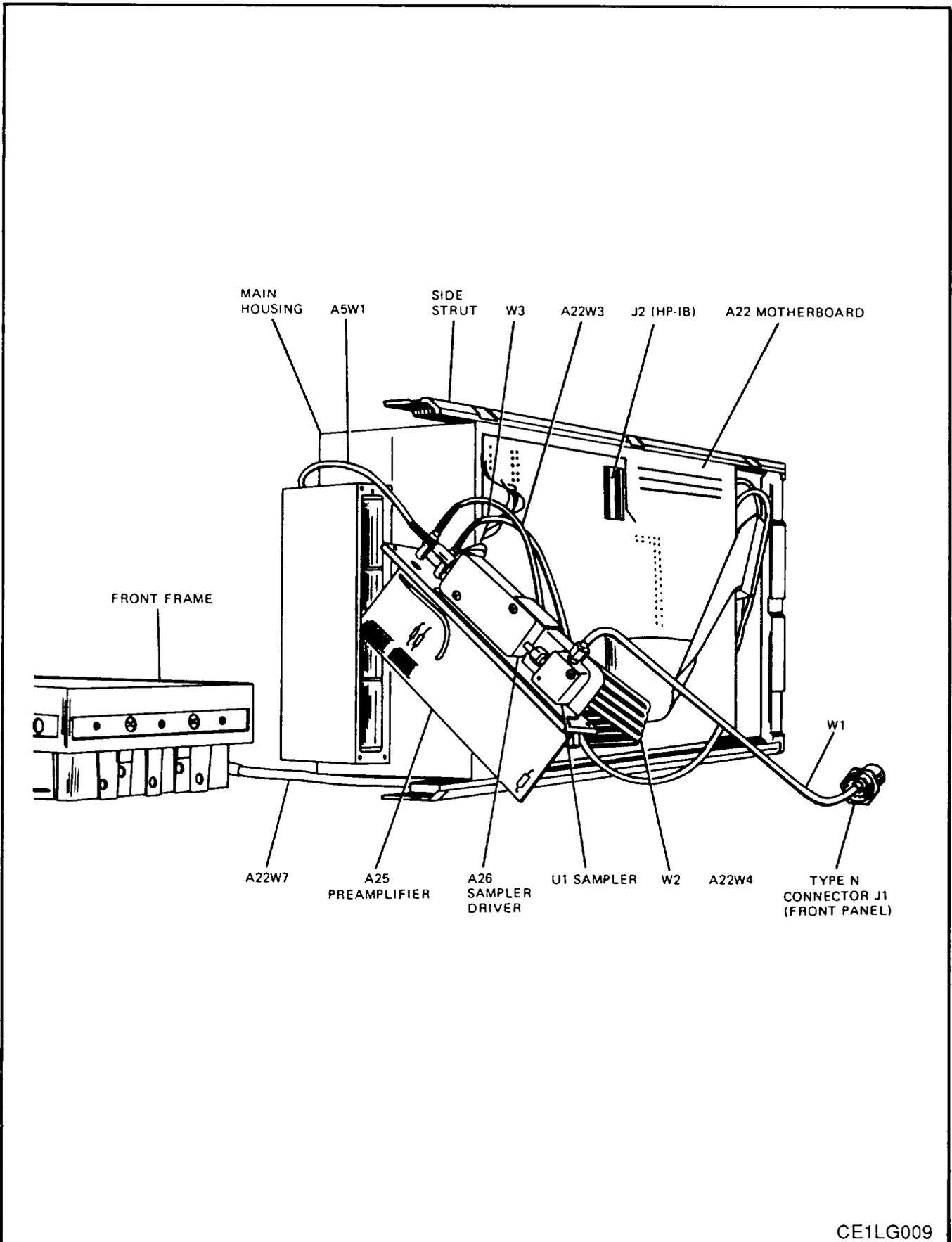


Figure 8-2. Front Frame, A25,A26, and U1 Removal

CE1LG009

8-36. FACTORY SELECTED COMPONENTS

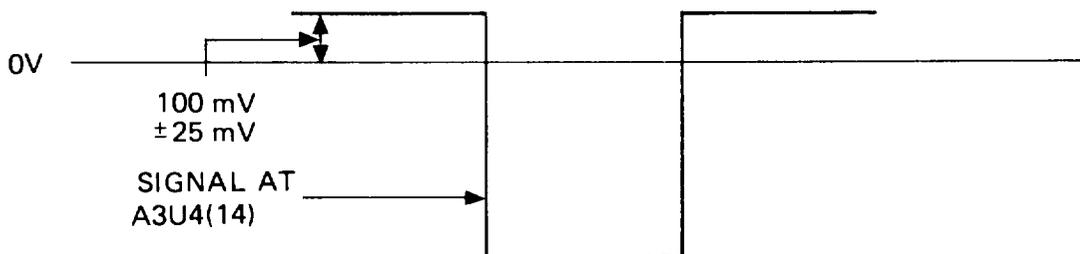
8-37. Some component values are selected at the time of final checkout at the factory. These values are selected to provide optimum compatibility with associated components and are identified on schematics and parts lists by an asterisk (*). The recommended procedure for replacing a factory-selected part is as follows:

- a. Refer to paragraphs 8-38 through 8-45 for test procedures required for selection of critical value parts.
- b. For factory selected components that are not listed in paragraphs 8-38 through 8-45, use the original value.
- c. After replacing parts, perform the test specified for the circuit in the performance and adjustment sections of this manual to verify correct operation.

8-38. Procedure for Selecting Resistor R15 on Direct Count Amplifier A3

8-39. If resistor A3R15 is not properly selected for value (average value 42.2 ohms), the 5342A may exhibit a miscount at the low frequency direct count input for frequencies near 500 MHz. To properly select A3R15, perform the following:

- a. Set the 5342A to the 10 Hz—500 MHz RANGE and select 1 kHz RESOLUTION.
- b. With assembly A3 on an extender board, monitor A3U4(14) with an oscilloscope.
- c. The signal at A3U4(14) must go positive by 100 mV (± 25 mV).



- d. To determine the value of A3R15, first decide how much the actual upper voltage level at A3U4(14) must change in order to fall between +75 mV to +125 mV. For every 5 mV increase required, the value of A3R15 must be increased by 1 ohm and for every 5 mV decrease, the value of A3R15 must be decreased by 1 ohm. For example, if the actual voltage only goes positive by 25 mV, then a 75 mV increase is required. Increase A3R15 by 15 Ω .
- e. Use a 1%, 0.125W resistor for A3R15. The following are HP part numbers for resistors which may be used.

Value	Part No.
61.9 Ω	0757-0276
56.2 Ω	0757-0395
51.1 Ω	0757-0394
46.4 Ω	0698-4037
42.2 Ω	0757-0316
38.3 Ω	0698-3435
34.8 Ω	0698-3434
31.6 Ω	0757-0180
28.7 Ω	0698-3433

8-40. Procedure for Selecting Resistor R16 and Capacitor C10 on Direct Count Amplifier A3

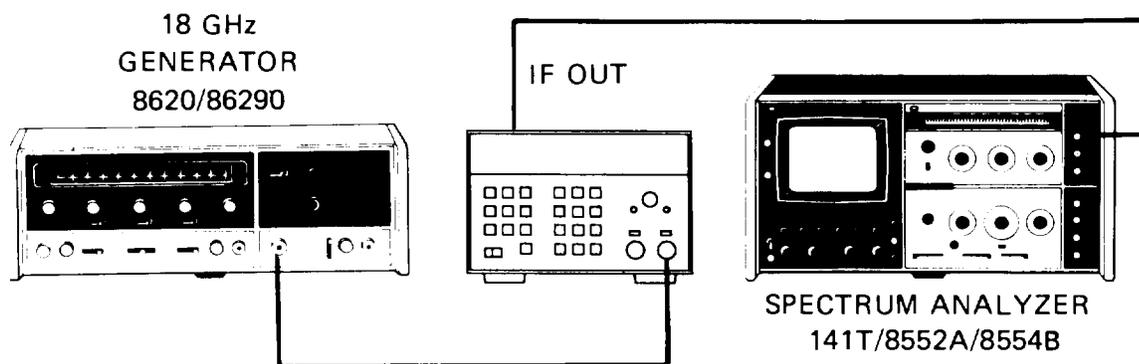
8-41. If resistor A3R16 and capacitor A3C10 are not the proper value, the 5342A will exhibit miscount at low levels for frequencies near 10 Hz at the high impedance direct count input. This miscount is caused by leakage of the 300 MHz synthesizer frequency into the low frequency input. To select A3R16 and A3C10, perform the following:

- a. With the 5342A set to the 10 Hz—500 MHz range, impedance select set to 1 M Ω , 1 Hz resolution, apply a 10 Hz signal at a level of 50 mV rms. If the counter properly counts 10 Hz, leave A3R16 at 51 Ω (0698-3378) and A3C10 at 2.2 pF (0160-3872).
- b. If the counter miscounts change A3R16 to 510 Ω (0698-5176) and change A3C10 to 10 pF (0160-3874).

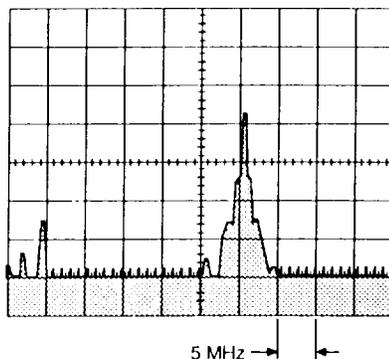
8-42. Procedures for Selecting Resistor R16 on Main Loop Amplifier A9

8-43. Whenever a repair is made in the main synthesizer loop consisting of assemblies A9, A8, and A10, it may be necessary to change the value of resistor A9R16. If A9R16 is not the proper value, the counter will miscount at high frequencies. This miscount will be independent of input signal level. Start with A9R16 equal to 10 M Ω (HP P/N 0683-1565) and test as follows:

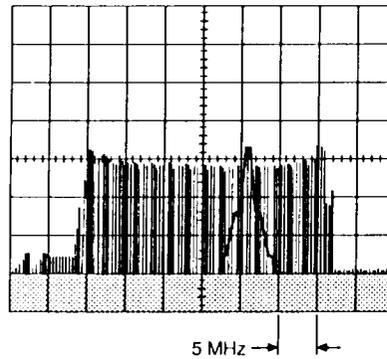
- a. Test setup:



- b. Set the signal generator to 18 GHz and approximately -10dBm. Place the 5342A to AUTO and observe 18 GHz count.
- c. Set 5342A to MANUAL and observe the 5342A rear panel IF OUT on the spectrum analyzer. Set spectrum analyzer SCAN WIDTH to 5 MHz and observe the following:

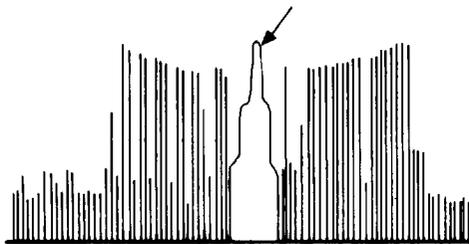


- d. Reduce input signal level until counter no longer counts 18 GHz but displays all zeros. The IF OUT on the spectrum analyzer should appear as:

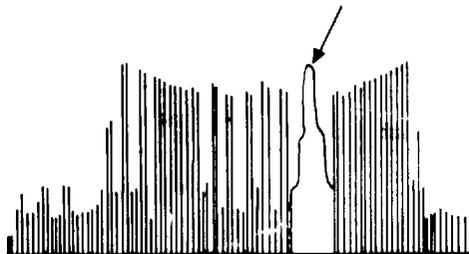


- e. If the spectrum analyzer display remains as in the first photo, or if the IF is centered as shown below, then change A9R16 to 15 M Ω (0683-1565).

IF THIS IS CENTERED, THEN
CHANGE A9R16 to 15 M Ω .



SHOULD BE OFFSET FROM
CENTER (EITHER SIDE)



8-44. Deleted

8-45. Deleted

8-46. SERVICE ACCESSORY KIT 10842A

8-47. The 10842A Service Accessory Kit contains 10 special extender boards (Figure 8-3) designed to aid in troubleshooting the 5342A. The following paragraphs describe equipment supplied, replaceable parts and operation.

8-48. Equipment Supplied

8-49. Table 8-3 lists the boards contained in the 10842A Service Accessory Kit with their general description and usage. The kit is shown in Figure 8-3.

Table 8-3. 10842A Kit Contents

HP PART NO.	QTY.	DESCRIPTION FOR USE
05342-60030	1	10 pin X2 Extender Boards for A4, A5, A6, and A18 assemblies.
05342-60031	1	12 pin X2 Extender Boards for A3, A7, A8, A9, and A11 assemblies.
05342-60032	1	15 pin X2 Extender Boards for the A24 assembly.
05342-60033	2	18 pin X2 Extender Boards for the A17 assembly.
05342-60034	2	22 pin X2 Extender Boards for A10, A12, A13, A20, A21 assemblies.
05342-60035	1	24 pin X2 Extender Boards for the A19 assembly.
05342-60036	1	Double 18 pin X2 Extender Boards for the A14 assembly.
05342-60039	1	Keyed double 18 pin X2 Extender Boards for the A15 HP-IB assembly.

8-50. Replaceable Parts

8-51. The only replaceable parts in the 10842A kit are the two integrated circuits and five switches on the 05342-60036 extender board. Table 8-4 lists the HP part number and description of those parts.

Table 8-4. Replaceable Parts for Extender Board 05342-60036

Ref. DESIG.	HP PART NO.	QTY.	DESCRIPTION	Mfr. CODE	MFR PART NO.
U1	1820-1197	1	IC GATE TTL LS NAND QUAD 2-INPUT	01698	SN74LS00N
U2	1820-1281	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INPUT	01698	SN74LS139N
S1	3101-1856	1	SWITCH-SL-8-1A-NS DIP-SLIDE-ASSY .1A	28480	3101-1856
S2	3101-1856	1	SWITCH-SL-8-1A-NS DIP-SLIDE-ASSY .1A	28480	3101-1856
S3	3101-1856	1	SWITCH-SL 8-1A-NS DIP-SLIDE-ASSY .1A	28480	3101-1856
S4	3101-1213	1	SWITCH-TGL SUBMIN DPST .5A 120VAC PC	28480	3101-1213
S5	3101-1675	1	SWITCH-TGL SUBMIN DPST .5A 120VAC/ DC PC	28480	3101-1675

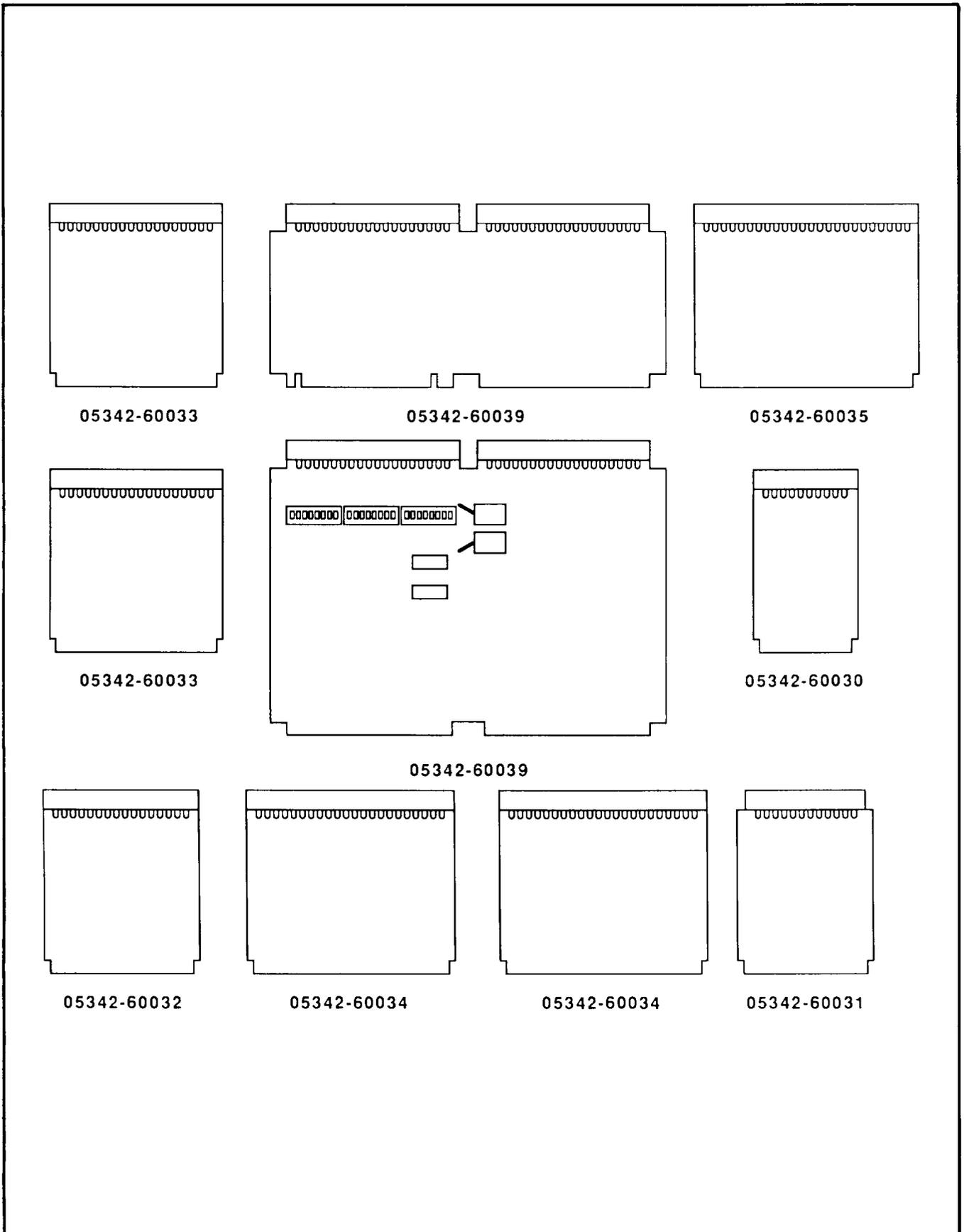


Figure 8-3. 10842A Service Accessory Kit

8-52. Using Extender Board 05342-60036

8-53. The following paragraphs describe the general operation of the extender board (05342-60036). Included is a description of the 3 DIP switches (S1, S2, and S3) the two toggle switches (S4 and S5) and test points R1, R2, and R3. figure 8-4 shows the signals present at R1, R2, and R3, Figure 8-5 is the schematic diagram of the extender board.

8-54. The 05342-60036 extender board is used for troubleshooting the A14 Microprocessor Assembly in the 5342A. This extender board not only allows operation of A14 outside the instrument casing but it also permits:

- a. Isolation of the 16-line address bus and the 8-line data bus from the rest of the instrument.
- b. Generation of START/STOP signals for performing signature analysis on individual ROM's on A14.
- c. Manual control of the microprocessor reset.

8-55. The S1 switch (leftmost switch) opens the data bus. With all switches up, the switches are in the closed position, The S2 and S3 switches open the 16 lines of the address bus.

8-56. Test points R1, R2, and R3 are used in taking signatures of the A14 ROM outputs as described in Table 8-9. U1 and U2 decode address lines to generate signals which bracket the addresses of each specific ROM, The signal at R1 is low only when ROM U1 is enabled. The signal at R2 is low only when ROM U4 is enabled. The signal at R3 is low only when ROM U7 is enabled.

8-57. If the A14 Microprocessor is put into free-run as described in Table 8-9, the signals shown in Figure 8-4 should be observed at test points R1, R2, and R3 on the extender board.

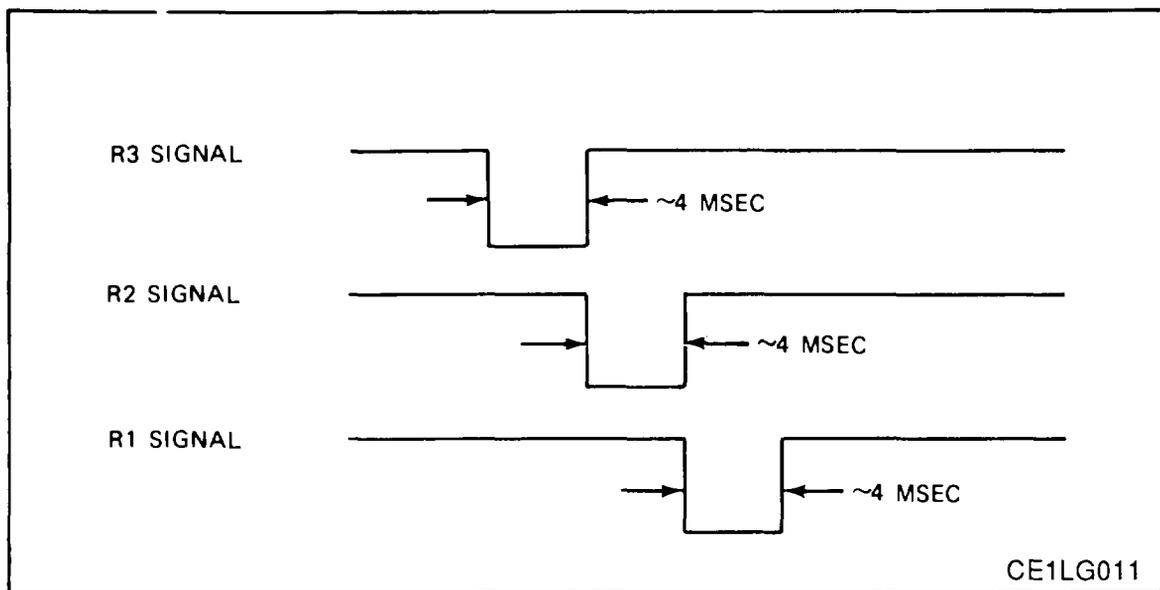


Figure 8-4. Extender Board (05342-60036) Test Points R1, R2, and R3

8-58. LOGIC SYMBOLS

8-59. Logic symbols used in this manual conform to the American National Standard ANSI Y32.14-1973 (IEEE Std. 91-1973). This standard supersedes MIL-STD-806B. In the following paragraphs logic symbols are described. For further descriptions refer to HP Logic Symbology manual, part number 5951-6116.

8-60. Logic Concepts

8-61. The binary numbers 1 and 0 are used in pure logic where 1 represents true, yes, or active and 0 represents false, no, inactive. These terms should not be confused with the physical quantity (e.g., voltage) that may be used to implement the logic, nor should the term "active" be confused with a level that turns a device on or off. A truth table for a relationship in logic shows (implicitly or explicitly) all the combinations of true and false input conditions and the result (output). There are only two basic logic relationships, AND and OR. The following illustrations assume two inputs (A and B), but these can be generalized to apply to more than two inputs.

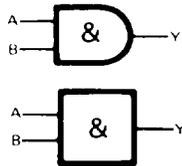
AND Y is true if and only if A is true and B is true (or more generally, if all inputs are true).
 $Y=1$ if and only if $A=1$ and $B=1$
 $Y=A \cdot B$

OR Y is true if and only if A is true or B is true (or more generally, if one or more input(s) is (are) true).
 $Y=1$ if and only if $A=1$ or $B=1$
 $Y=A+B$

TRUTH TABLE

A	B	Y
1	1	1
1	0	0
0	1	0
0	0	0

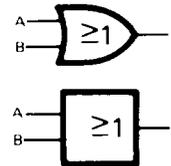
EQUIVALENT SYMBOLS



TRUTH TABLE

A	B	Y
1	1	1
1	0	1
0	1	1
0	0	0

EQUIVALENT SYMBOLS



8-62. Negation

8-63. In logic symbology, the presence of the negation indication symbol \circ provides for the presentation of logic function inputs and outputs in terms independent of their physical values, the \emptyset -state of the input or output being the 1-state of the symbol referred to the symbol description.

EXAMPLE 1



TRUTH TABLE

A	B	Z
1	1	0
1	0	1
0	1	1
0	0	1

EXAMPLE 2



TRUTH TABLE

A	B	Z
1	1	0
1	0	1
0	1	1
0	0	1

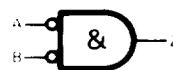
EXAMPLE 3



TRUTH TABLE

A	B	Z
1	1	0
1	0	0
0	1	0
0	0	1

EXAMPLE 4



TRUTH TABLE

A	B	Z
1	1	0
1	0	0
0	1	0
0	0	1

- EXAMPLE 1 says that Z is *not* true if A is true *and* B is true or that Z is true if A *and* B are *not* both true. $\overline{Z} = AB$ or $Z = \overline{AB}$. This is frequently referred to as NAND (for NOT AND).
- EXAMPLE 2 says that Z is true if A is *not* true or if B is *not* true. $Z = \overline{A+B}$. Note that this truth table is identical to that of Example 1. The logic equation is merely a DeMorgan's transformation of the equations in Example 1. The symbols are equivalent.
- EXAMPLE 3 $\overline{Z} = A+B$ or $Z = \overline{A+B}$ and,
- EXAMPLE 4 $Z = \overline{A \cdot B}$, also share common truth table and are equivalent transformations of each other. The NOT OR form (Example 3) is frequently referred to as NOR.

NOTE

In this manual the logic negation symbol is NOT used.

8-64. Logic Implementation and Polarity Indication

8-65. Devices that can perform the basic logic functions, AND and OR, are called gates. Any device that can perform one of these functions can also be used to perform the other if the relationship of the input and output voltage levels to the logic variables 1 and 0 is redefined suitably,

8-66. In describing the operation of electronic logic devices, the symbol H is used to represent a "high level", which is a voltage within the more-positive (less-negative) of the two ranges of voltages used to represent the binary variables, L is used to represent a "low level", which is a voltage within the less-positive (more-negative) range.

8-67. A function table for a device shows (implicitly or explicitly) all the combinations of input conditions and the resulting output conditions.

8-68. In graphic symbols, inputs or outputs that are active when at the high level are shown without polarity indication. The polarity indicator symbol  denotes that the active (one) state of an input or output with respect to the symbol to which it is attached is the low level.

NOTE

The polarity indicator symbol "  " is used in this manual.

- EXAMPLE 5 assume two devices having the following function tables.

DEVICE #1
FUNCTION TABLE

A	B	Y
H	H	H
H	L	L
L	H	L
L	L	L

DEVICE #2
FUNCTION TABLE

A	B	Y
H	H	H
H	L	H
L	H	H
L	L	L

POSITIVE LOGIC by assigning the relationship H=1, L=0 at both input and output, Device #1 can perform the AND function and Device #2 can perform the OR function. Such a consistent assignment is referred to as positive logic. The corresponding logic symbols would be:

DEVICE #1



DEVICE #2



NEGATIVE LOGIC alternatively, by assigning the relationship $H=0, L=1$ at both input and output, Device #1 can perform the OR function and Device #2 can perform the AND function. Such a consistent assignment is referred to as negative logic. The corresponding logic symbols would be:

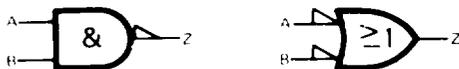


8-69. **MIXED LOGIC.** The use of the polarity indicator symbol (\blacktriangleleft) automatically invokes a mixed-logic convention. That is, positive logic is used at the inputs and outputs that do not have polarity indicators, negative logic is used at the inputs and outputs that have polarity indicators.

**EXAMPLE 6
FUNCTION TABLE**

A	B	Z
H	H	L
H	L	H
L	H	H
L	L	H

This may be shown either of two ways:



Note the equivalence of these symbols to examples 1 and 2 and the fact that the function table is a positive-logic translation ($H=1, L=0$) of the NAND truth table, and also note that the function table is the negative-logic translation ($H=0, L=1$) of the NOR truth table, given in Example 3.

**EXAMPLE 7
FUNCTION TABLE**

A	B	Z
H	H	L
H	L	L
L	H	L
L	L	H

This may be shown either of two ways:



Note the equivalence of these symbols to examples 3 and 4 and the fact that the function table is a positive-logic translation ($H=1, L=0$) of the NOR truth table, and also note that the function table is the negative-logic translation ($H=0, L=1$) of the NAND truth table, given in Example 1.

8-70. It should be noted that one can easily convert from the symbology of positive-logic merely by substituting a polarity indicator (\blacktriangleleft) for each negation indicator (\bullet) while leaving the distinctive shape alone. To convert from the symbology of negative-logic, a polarity indication (\blacktriangleleft) is substituted for each negation indicator (\bullet) and the OR shape is substituted for the AND shape or vice versa.

8-71. It was shown that any device that can perform OR logic can also perform AND logic and vice versa. DeMorgan's transformation is illustrated in Example 1 through 7. The rules of the transformation are:

1. At each input or output having a negation (\bullet) or polarity (\blacktriangleleft) indicator, delete the indicator.
2. At each input or output not having an indicator, add a negation (\bullet) or polarity (\blacktriangleleft) indicator.
3. Substitute the AND symbol D for the OR symbol D or vice versa.

These steps do not alter the assumed convention; positive-logic stays positive, negative-logic stays negative, and mixed-logic stays mixed.

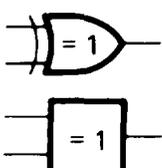
8-72. The choice of symbol may be influenced by these considerations: (1) The operation being performed may best be understood as AND or OR. (2) In a function more complex than a basic gate, the inputs will usually be considered as inherently active high or active low (e.g., the J and K inputs of a J-K flip-flop are active high and active low, respectively). (3) In a chain of logic, understanding and the writing of logic equations are often facilitated if active low or negated outputs feed into active low or negated inputs.

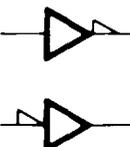
8-73. Other Symbols

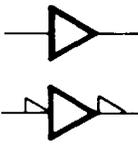
8-74. Additional symbols are required to depict complex logic diagrams, as follows:

- 

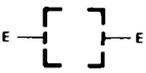
Dynamic input activated by transition from a low level to a high level. The opposite transition has no effect at the output.
- 

Dynamic input activated by transition from a high level to a low level. The opposite transition has no effect at the output.
- 

Exclusive OR function. The output will assume its indicated active level if and only if one and only one of the two inputs assumes its indicated active level.
- 

Inverting function. The output is low if the input is high and it is high if the input is low. The two symbols shown are equivalent.
- 

Noninverting function. The output is high if the input is high and it is low if the input is low. The two symbols shown are equivalent.
- 

OUTPUT DELAY. The output signal is effective when the input signal returns to its opposite state.
- 

EXTENDER. Indicates when a logic function increases (extends) the number of inputs to another logic function.
- 

FLIP-FLOP. A binary sequential element with two stable states: a set (1) state and a reset (0) state. Outputs are shown in the 1 state when the flip-flop is set. In the reset state the outputs will be opposite to the set state.
- 

RESET. A 1 input will reset the flip-flop. A return to 0 will cause no further effect,
- 

SET. A 1 input will set the flip-flop. A return to 0 will cause no further action.
- 

TOGGLE. A 1 input will cause the flip-flop to change state. A return to 0 will cause no further action.



J INPUT. Similar to the S input except if both J and K (see below) are at 1, the flip-flop changes state.



K INPUT. Similar to the R input (see above).



D INPUT (Data). Always dependent on another input (usually C). When the C and D inputs are at 1, the flip-flop will be set. When the C is 1 and the D is 0, the flip-flop will reset.



Address symbol has multiplexing relationship at inputs and demultiplexing relationship at outputs.

8-75. Dependency Notation “C” “G” “V” “F”

8-76. Dependency notation is a way to simplify symbols for complex IC elements by defining the existence of an AND relationship between inputs, or by the AND conditioning of an output by an input without actually showing all the elements and interconnections involved. The following examples use the letter “C” for control and “G” for gate. The dependent input is labeled with a number that is either prefixed (e.g., 1X) or subscripted (e.g., X₁). They both mean the same thing. The letter “V” is used to indicate an OR relationship between inputs or between inputs and outputs with this letter (V). The letter “F” indicates a connect-disconnect relationship. If the “F” (free dependency) inputs or outputs are active (1) the other usual normal conditions apply. If one or more of the “F” inputs are inactive (∅), the related “F” output is disconnected from its normal output condition (it floats).



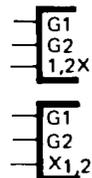
The input that controls or gates other inputs is labeled with a “C” or a “G”, followed by an identifying number. The controlled or gated input or output is labeled with the same number. In this example, “1” is controlled by “G1.”



When the controlled or gated input or output already has a functional label (X is used here), that label will be prefixed or subscripted by the identifying number.



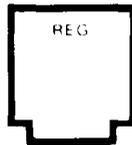
If a particular device has only one gating or control input then the identifying number may be eliminated and the relationship shown with a subscript.



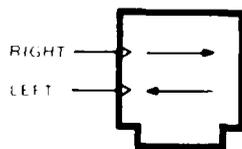
If the input or output is affected by more than one gate or control input, then the identifying numbers of each gate or control input will appear in the prefix or subscript, separated by commas. In this example “X” is controlled by “G1” and “G2.”

8-77. Control Blocks

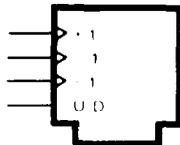
8-78. A class of symbols for complex logic are called control blocks. Control blocks are used to show where common control signals are applied to a group of functionally separate units. Examples of types of control blocks follow.



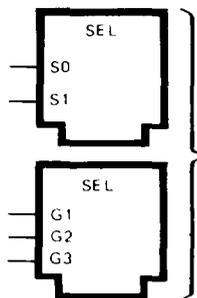
Register control block. This symbol is used with an associated array of flip-flop symbols to provide a point of placement for common function lines, such as a common clear.



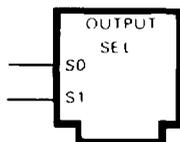
Shift register control block. These symbols are used with any array of flip-flop symbols to form a shift register. An active transition at the inputs causes left or right shifting as indicated.



Counter control block. The symbol is used with an array of flip-flops or other circuits serving as a binary or decade counter. An active transition at the +1 or -1 input causes the counter to increment one count upward or downward, respectively. An active transition at the ± 1 input causes the counter to increment one count upward or downward depending on the input at an up/down control.



Selector control block. These symbols are used with an array of OR symbols to provide a point of placement for selection (S) or gating (G) lines. The selection lines enable the input designated 0, 1, . . . n of each OR function by means of a binary code where S0 is the least-significant digit. If the 1 level of these lines is low, polarity indicators (b) will be used. The gating lines have an AND relation with the respective input of each OR function: G1 with the inputs numbered 1, G2 with the input numbered 2, and so forth. If the enabling levels of these lines is low, polarity indicators (\triangleleft) will be used.



Output selector control block. This symbol is used with a block symbol having multiple outputs to form a decoder. The selection lines enable the output designated 0, 1, . . . n of each block by means of a binary code where S0 is the least-significant digit. If the 1 level of these lines is low, polarity indicators (\triangleleft) will be used.

8-79. Complex Logic Devices

8-80. Logic elements can be recombined to produce very complex devices that can perform more difficult functions. A control block symbol can be used to simplify understanding of many complex devices. Several examples of complex devices are given here. These examples are typical of the symbols used in schematic diagrams in this manual.

Reference Designation
A2U2, A2U7
Part Number
1820-0468
SN7445N

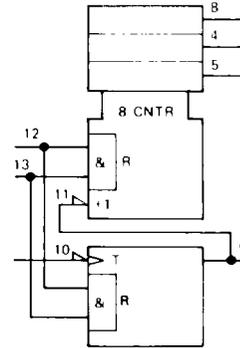
Description
 BCD TO DECIMAL DECODER/DRIVER

The output which is low will correspond to the binary weighted input. The minus signs at the output indicate that the element is capable of supplying LOW's only.

Reference Designation
A2U3
Part Number
1820-1443
SN74LS293N

Description
 4-BIT BINARY COUNTER

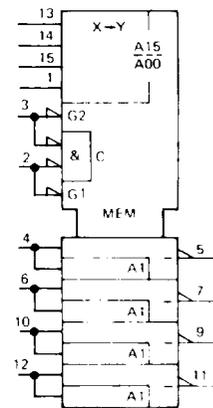
This binary counter has four master-slave flip-flops and gating for which the count cycle length is divide-by-eight. The counter has a gated zero reset. To use the maximum count length, the pin 11 input is connected to the pin 9 output. The input count pulses are applied to the pin 10 input.



Reference Designation
A2U8, A2U11
Part Number
1820-0428
SN7489

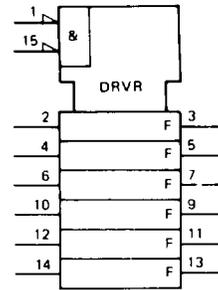
Description
 64-BIT READ/WRITE MEMORY

This memory has an array of 64 flip-flop memory cells in a matrix to provide 16 words of 4 bits each. Information present at the data input (pins 4, 6, 10, 12) is written into memory by holding both the memory enable (pin 2) and write enable (pin 3) LOW while addressing the desired word at the BCD weighted inputs (pins 1, 13, 14, 15). The complement of the information written into memory is readout at the four outputs by holding memory enable (pin 2) LOW, write enable (pin 3) HIGH and selecting the desired address.

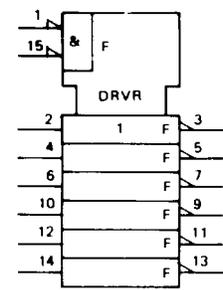


Reference Designation
A2U12, A2U16
 Part Number
1820-1254
DM8095N

Reference Designation
A14U16, A14U18
 Part Number
1820-1368
DM8096N



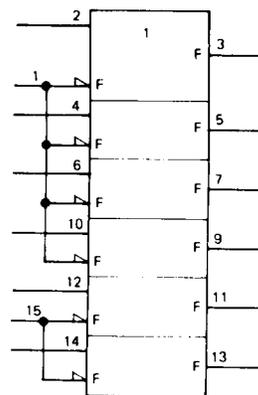
A2U12, A2U16



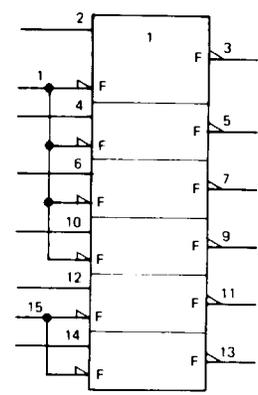
A14U16, A14U18

Reference Designation
A2U6
 Part Number
1820-1049
DM8097N

Reference Designation
A14U8
 Part Number
1820-1255
DM8098N



A2U6

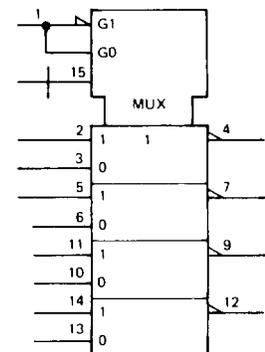


A14U8

Description
 HEX BUFFERS - HEX INVERTERS

The buffers (8095-8097) and inverters (18096-8098) convert standard TTL or DTL outputs to THREE-STATE outputs. The 8095 and 8096 control all six devices from common inputs (pins 1 and 15 LOW). The 8097 and 8098 control four devices from one input (pin 1 LOW) and two devices from another input (pin 15 LOW).

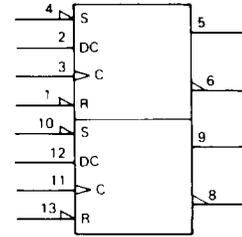
Reference Designation
A2U17
 Part Number
1820-1428
74LS158



Description
 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

This quad two input multiplexer selects one of two word inputs and outputs the data the data when enabled. The level at pin 1 selects the input word. The outputs are LOW when pin 15 is LOW.

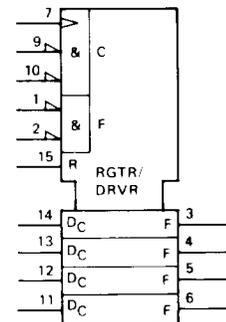
Reference Designation
A2U18, A2U18, A9U1,
A10U4, A12U13, A13U4,
A14U9, A15U3, A15U4,
A15U9, A15U10, A15U14,
A15U19, A15U34, A15U34,
A17U9, A17U15
Part Number
1820-1112
SN74LS74N



Description
DUAL D-TYPE FLIP-FLOP

The dual D-type flip-flop consists of two independent D-type flip-flops. The information present at the data (D_c) input is transferred to the active-high and active-low outputs on a low-to-high transition of the clock (C) input. The data input is then locked out and the outputs do not change again until the next low-to-high transition of the clock input. The set (S) and reset (R) inputs override all other input conditions: when (S) is low, the active-high output is forced high; when (R) is low, the active-high output is forced low. Although normally the active-low output is the complement of the active-high output, simultaneous low inputs at the set and reset will force both the active-low and active-high outputs to go high at the same time on some D-type flip-flops. This condition will exist only for the length of time that both set and reset inputs are held low. The flip-flop will return to some indeterminate state when both the set and reset inputs are returned to the high state.

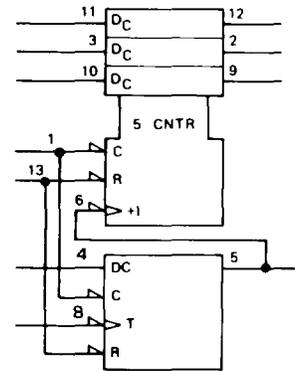
Reference Designation
A1U22
Part Number
1820-0574
DM8551N



Description
4-BIT D-TYPE REGISTERS

When both data-enable inputs (9 and 10) are LOW, data at the D_c inputs is loaded into the flip-flops on the next positive transition of the clock (pin 7). When both output control inputs (pins 1 and 2) are LOW, data is available at the outputs. The outputs are disabled by a HIGH at either output control input. The outputs then represent a high impedance.

Reference Designation
A10U1, A13U13, A13U14
A13U17, A13U18
Part Number
1820-1251
SN74LS196N

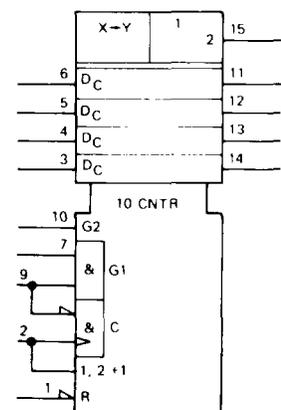


Description
 50/30 MHz PRESETTABLE DECADE COUNTER/LATCH

The Decade Counter consists of a divide-by-two and a divide-by-five counter formed by connecting pin 5 to pin 6 and taking the output from pin 12.

The outputs may be preset to any state by making "C" active low and entering the desired data at the "Dc" inputs. The outputs at pins 5, 9, 2, and 12 will then correspond to the data inputs independent of the state of the count-up clocks at pins 6 and 8. An active high signal at pin 1 then enables the counter by latching the parallel data into the counter. The count-up clock at pin 8 clocks the ÷2 counter and pin 6 clocks the ÷5 counter. When the counter is clocked at pins 8 or 6, the outputs will change on the negative-going edge of the signal. An active low at the "R" (reset) input (pin 13) causes all the outputs to go low independent of the counting state.

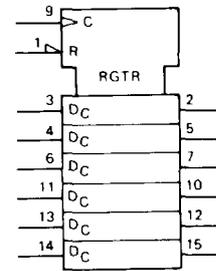
Reference Designation
A10U8, A10U9,
A10U13, A10U14
Part Number
1820-1429
74LS160



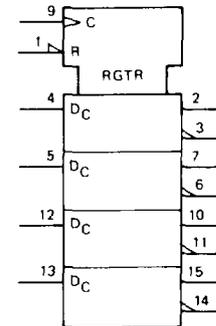
Description
 SYNCHRONOUS DECADE COUNTER

This synchronous presettable decade counter has four master slave flip-flops that are triggered on the positive-going edge of the clock pulse (pin 2). A LOW at the load input (pin 9) disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels at the enable inputs (pins 7 and 10). The clear function (pin 1) is asynchronous and a low level clear input sets all outputs low regardless of the levels of the clock, load or enable inputs. Both count enable inputs (pins 7 and 10) must be HIGH to count and the pin 10 input is fed forward to enable the carry output (pin 15).

Reference Designation
A10U10, A10U15, A10U17
Part Number
1820-1196
SN74LS174N



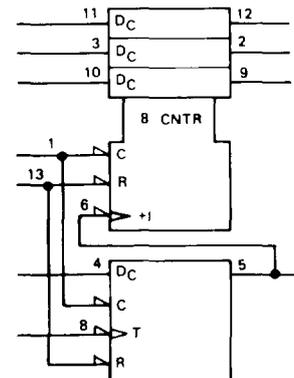
Reference Designation
A10U11, A10U16
Part Number
1820-1195
SN74LS175N



Description
 HEX/QUAD D-TYPE FLIP-FLOPS

Information at the D inputs is transferred to the outputs on the positive-edge of the clock pulse (pin 9). Clock triggering occurs at a particular voltage level. The hex FFs have single outputs, the quad FFs have complementary outputs.

Reference Designation
A12U10, A12U15
Part Number
1820-1193
SN74LS197N



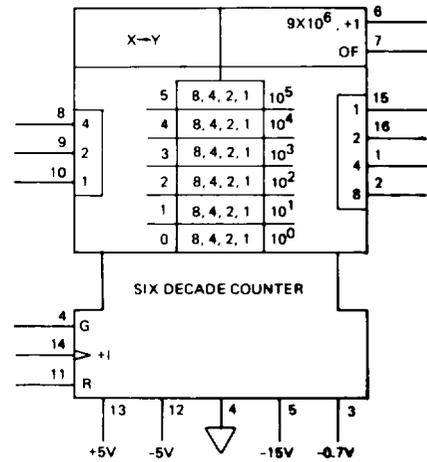
Description
 30 MHz PRESETTABLE BINARY
 COUNTERS/LATCHES

This counter consists of four master-slave flip-flops that form a divide-by-two and a divide-by-eight counter. The outputs may be preset to any state by placing a low on pin 1 and entering the desired data. The outputs will change to agree with the inputs regardless of the state of the clocks. When used as a high-speed 4-bit ripple-through counter, the output of pin 5 must be externally connected to the clock 2 input (pin 6). The input count pulses are applied to the clock 1 input (pin 8). Simultaneous divisions by 2,4,8, and 16 are performed at output pins 12,2,9, and 5, respectively.

When used as a 3-bit ripple-through counter, the input count pulses are applied to the clock 2 input (pin 6). Simultaneous frequency divisions by 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit ripple-through counter.

Reference Designation
A13U1, A13U2
Part Number
1820-0634

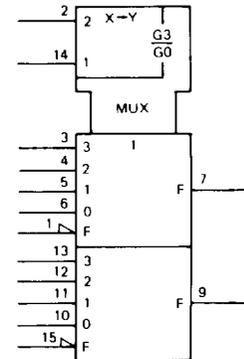
Description
SIX DECADE COUNTER



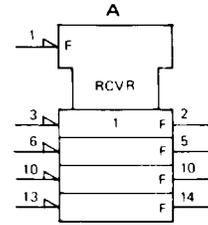
The six decade counter is an MOS, 6 digit, 10 MHz ripple-through counter with buffer storage for each of the 6 decades. The circuit has one set of BCD (positive logic (8421) outputs that may be switched from digit-to-digit by means of a 3-to-6 line decoder. An overflow output (pin 7) and a fifth decade carry output (pin 6] is also available. When the transfer input (pin 4) is held LOW, the decimal count of a selected decade can be transmitted through its own decade storage buffer to the BCD outputs by means of the 3-to-6 line decoder which is controlled by the BCD inputs.

Reference Designation
A13U5, A13U6,
A13U9, A13U10
Part Number
1820-1238
SN74LS253N

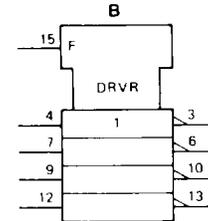
Description
DUAL 4-INPUT MULTIPLEXER



Input states on pins 2 and 14 are decoded according to their weighting modifiers to form AND gates (G0 through G3) in the common control block. The data inputs have numeric modifiers to indicate the specific gate which must be active for that input to be selected. The output on pin 7 will be HIGH IFF the selected input is HIGH and the inhibit input on pin 1 is LOW. Similarly, the output on pin 9 will be HIGH IFF the selected input is HIGH and the inhibit input on pin 15 is LOW. If an inhibit input (pin 1 or 15) is HIGH the corresponding output (pin 7 or 9) will be LOW regardless of the state of the selected input.



Reference Designation
A14U2, A14U3
Part Number
1820-1081
8126

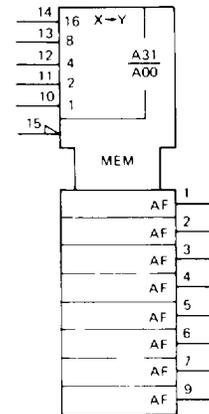


Description
 QUAD BUS DRIVER/RECEIVER

The bus driver/receiver consists of four pairs of inverting logic gates and two buffered common enable inputs (pins 1 and 15). A LOW on the input enable (pin 1) enables the receiver gates. A HIGH on the bus enable (pin 15) input allows input data to be transferred to the output of the driver, and a LOW forces the output to a high impedance state.

Reference Designation
A15U23
Part Number
1816-1154

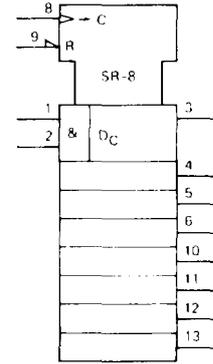
Reference Designation
A15U26
Part Number
1816-1155



Description
 READ ONLY MEMORY (ROM) WITH 32 ADDRESSES

Address selection is determined by the five upper inputs which are decoded into 32 possible addresses (A00 through A31) corresponding to the weighing modifiers at the inputs. Input modifier F (pin 15) gates the outputs. Stored data will be read from the selected memory address if F is active (LOW). The output data (pins 1-7 and 9) are active HIGH.

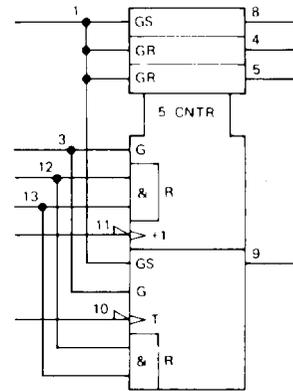
Reference Designation
A17U4, A17U5, A17U7
Part Number
1820-1433
SN74LS164N



Description
8-BIT PARALLEL OUT SERIAL SHIFT REGISTER

This 8-bit shift register has gated serial inputs and an asynchronous clear. A LOW at one or both gated serial inputs (pins 1, 2) inhibits entry of data and resets the first FF to the low level at the next clock pulse (pin 8). A high-level input (pin 1 or 2) enables the other input which will then determine the state of the first FF. Data is serially shifted in and out of the 8-bit register during the positive-going transition of the clock pulse. Clear is independent of the clock and occurs when pin 9 is LOW.

Reference Designation
A17U11
Part Number
1820-1442
SN74LS290N



Description
DECADE COUNTER

The decade counter has four master-slave flip-flops and gating for which the count cycle length is divided by five. This counter has a gated zero reset and a gated set-to-nine input. To use the maximum count length, the pin 11 input is connected to the pin 9 output. The input count pulses are applied to the T input at pin 10. A symmetrical divide-by-ten count can be obtained by connecting the pin 8 output to the pin 10 input and applying the input count to the pin 11 input to obtain a divide-by-ten square wave at the pin 9 output.

8-81. THEORY OF OPERATION

8-82. The following theory of operation is introduced with a description of the unique harmonic heterodyne technique used in the 5342A, Then the overall operation is described with a simplified block diagram, followed by discussions of FM tolerance, automatic amplitude discrimination, and sensitivity. The function and relationships of the major assemblies are described next (to a complete block diagram), followed by a detailed description of the circuits on each assembly with reference to the schematic diagrams.

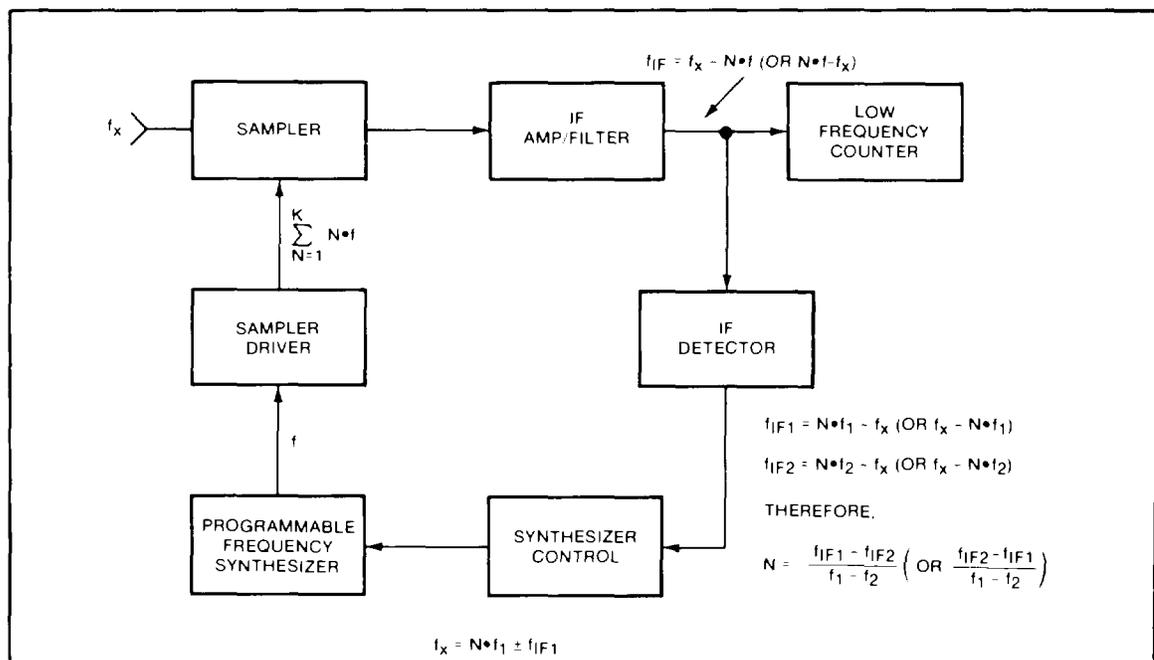
8-83. HARMONIC HETERODYNE TECHNIQUE

8-84. The HP 5342A Frequency Counter uses a harmonic heterodyne down-conversion technique to down convert the microwave input frequency into the range of its internal, low-frequency counter. This technique combines the best performance characteristics of heterodyne converters and transfer oscillators to achieve high sensitivity, high FM tolerance, and automatic amplitude discrimination.

8-85. All microwave counters must down convert the unknown microwave frequency to a low frequency signal which is within the counting range of an internal low frequency counter typically 200 to 500 MHz). Heterodyne converters down convert the unknown signal, f_x , by mixing it with an accurately known local oscillator frequency, f_{LO} , such that the difference frequency, f_{IF} ($f_x - f_{LO}$ if $f_x > f_{LO}$ and $f_{LO} - f_x$ if $f_x < f_{LO}$) is within the counting range of the low frequency counter. The counted frequency, f_{IF} , is then added (or subtracted if $f_x < f_{LO}$) to/from the local oscillator frequency to determine the unknown frequency.

8-86. Like heterodyne converters, transfer oscillators also mix the unknown signal with harmonics of an internally generated signal, f_{VCO} . When one of the harmonics of the VCO signal, $N \cdot f_{VCO}$, mixes with the unknown to produce zero beat, then the VCO frequency is measured by the low frequency counter. After determining which harmonic produced zero beat, the measured VCO frequency is multiplied by N ($f_x = N \cdot f_{VCO}$). One of the major differences between the heterodyne technique and the transfer oscillator technique is the fact that the heterodyne

converter employs a filter to select only one harmonic of the internal oscillator to mix with the unknown whereas the transfer oscillator mixes the unknown simultaneously with all harmonics of the internal frequency.



CE1LG013

Figure 8-6. Harmonic Heterodyne Technique

8-87. Figure 8-6 is a simplified block diagram of the harmonic heterodyne technique. In this technique, all of the harmonics of an internal oscillator (a programmable frequency synthesizer locked to the counter's time base) are simultaneously mixed with the unknown signal by the sampler and sampler driver (samplers are like harmonic mixers except that the conduction angle is much narrower — the sampling diodes in the HP5342A sampler, for example, conduct for only a few picosecond during each period of the sampling signal). The output of the sampler consists of sum and difference frequencies produced by each harmonic of the internal oscillator mixing with the unknown. The programmable frequency synthesizer is incremented in frequency until one of the outputs of the sampler is in the counting range of the low frequency counter. The IF detector detects when the IF is in the range of the low frequency counter and sends a signal which causes the synthesizer control to stop incrementing the frequency of the frequency synthesizer. The IF is then counted by the low frequency counter. The unknown frequency can be determined from the relation: $f_x = N \cdot f_1 \pm f_{IF1}$

where f_x = unknown frequency

N = harmonic of frequency synthesizer which mixed with unknown to produce countable IF

f_1 = programmed frequency of synthesizer

f_{IF1} = IF produced by $N \cdot f_1$ mixing with f_x

8-88. The frequency, f_1 , of the programmable synthesizer is known since it is known where indexing of the synthesizer was stopped. The IF, f_{IF1} , is known since it is counted by the low frequency counter. Still to be determined are the N number and the sign (\pm) of the IF (the sign of f_{IF1} will be (+) if $N \cdot f_1$ is less than f_x ; the sign of f_{IF1} is (—) if $N \cdot f_1$ is greater than f_x).

8-89. To determine N and the sign of f_{IF1} , one more measurement must be taken with the synthesizer offset from its previous value by a known frequency, $f_2 = f_1 - \Delta f$. This produces an IF, f_{IF2} , which is counted by the low frequency counter. N is determined by the following:

$$f_{IF2} = N \cdot f_2 - f_x \text{ (if } Nf_2 > f_x \text{)}$$

$$\text{therefore } N = \frac{f_{IF1} - f_{IF2}}{f_1 - f_2}$$

or, if f_x is greater than Nf_1 :

$$f_{IF1} = f_x - N \cdot f_1 \text{ (if } Nf_1 < f_x \text{)}$$

$$f_{IF2} = f_x - N \cdot f_2 \text{ (if } Nf_2 < f_x \text{)}$$

$$\text{therefore } N = \frac{f_{IF2} - f_{IF1}}{f_1 - f_2}$$

8-90. Referring to Figure 8-7, it is seen that if f_x is greater than $N \cdot f_1$, then f_{IF1} , produced by mixing $N \cdot f_1$ with f_x , will be less than f_{IF2} , produced by mixing $N \cdot f_2$ with f_x , since f_2 is less than f_1 , by Δf . However, if f_x is less than $N \cdot f_1$, then f_{IF1} will be greater than f_{IF2} .

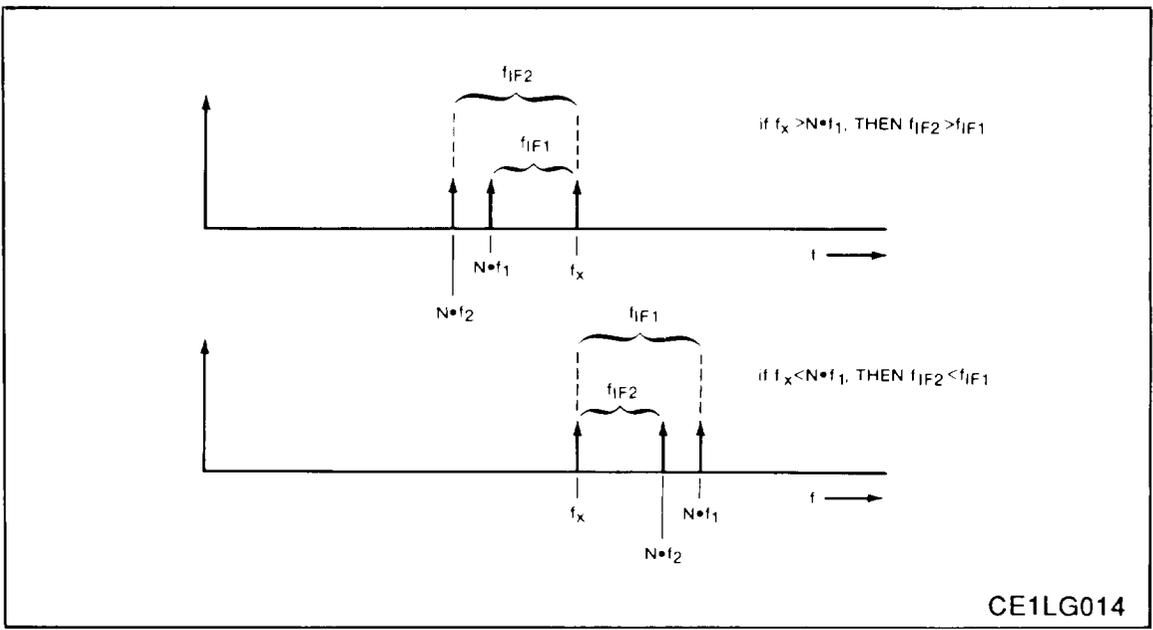


Figure 8-7. Frequency Relationships

8-91. If f_{IF2} is less than f_{IF1} , then N is computed from

$$N = \frac{f_{IF1} - f_{IF2}}{f_1 - f_2}$$

If f_{IF2} is greater than f_{IF1} , then N is computed from

$$N = \frac{f_{IF2} - f_{IF1}}{f_1 - f_2}$$

8-92. The unknown frequency is then computed from the following:

$$f_x = N \cdot f_1 - f_{IF1} \text{ (if } f_{IF2} < f_{IF1} \text{)}$$

$$f_x = N \cdot f_1 + f_{IF1} \text{ (if } f_{IF1} < f_{IF2} \text{)}$$

8-93. Since the frequency of the synthesizer is known to the accuracy of the counter's time base and the IF is measured to the accuracy of the counter's time base, the accuracy of the microwave measurement is limited-only by the time base error and ± 1 count error.

8-94. HP 5342A OVERALL OPERATION

8-95. If all signals into the counter could be guaranteed to have little or no FM, then the counter could operate quite simply as described previously. However, many signals in the microwave region, such as those originating from microwave radios, have significant amounts of frequency modulation. To prevent FM on the signal from causing an incorrect computation of N, the harmonic heterodyne technique is implemented as shown in Figure 8-8 which is a simplified block diagram of the HP 5342A. The differences between figure 8-8 and the block diagram of figure 8-6 are:

- a. Two synthesizers which are offset by precisely 500 kHz.
- b. Two counters.
- c. A multiplexer which multiplexes between the two synthesizer frequencies — when f_1 is driving the sampler driver, the IF₁ produced is measured by counter A and when f_1 drives the sampler driver, the IF₂ produced is measured by counter B.
- d. A pseudorandom sequence generator which controls the multiplexer during N determination.

8-96. The overall operating algorithm for the block diagram of Figure 8-8 is as follows: With the multiplexer having selected the main oscillator output, the main oscillator frequency, f_1 , is swept from 350 MHz to 300 MHz in 100 kHz steps (the offset oscillator frequency, f_2 , is maintained at $f_1 - 500$ kHz by a phase-locked loop) until the IF detector indicates the presence of an IF signal in the range of 50 MHz to 100 MHz. At this point, the synthesizer stops its sweep and the counter starts the harmonic number (N) determination, A pseudorandom sequence (prs) output by the prs

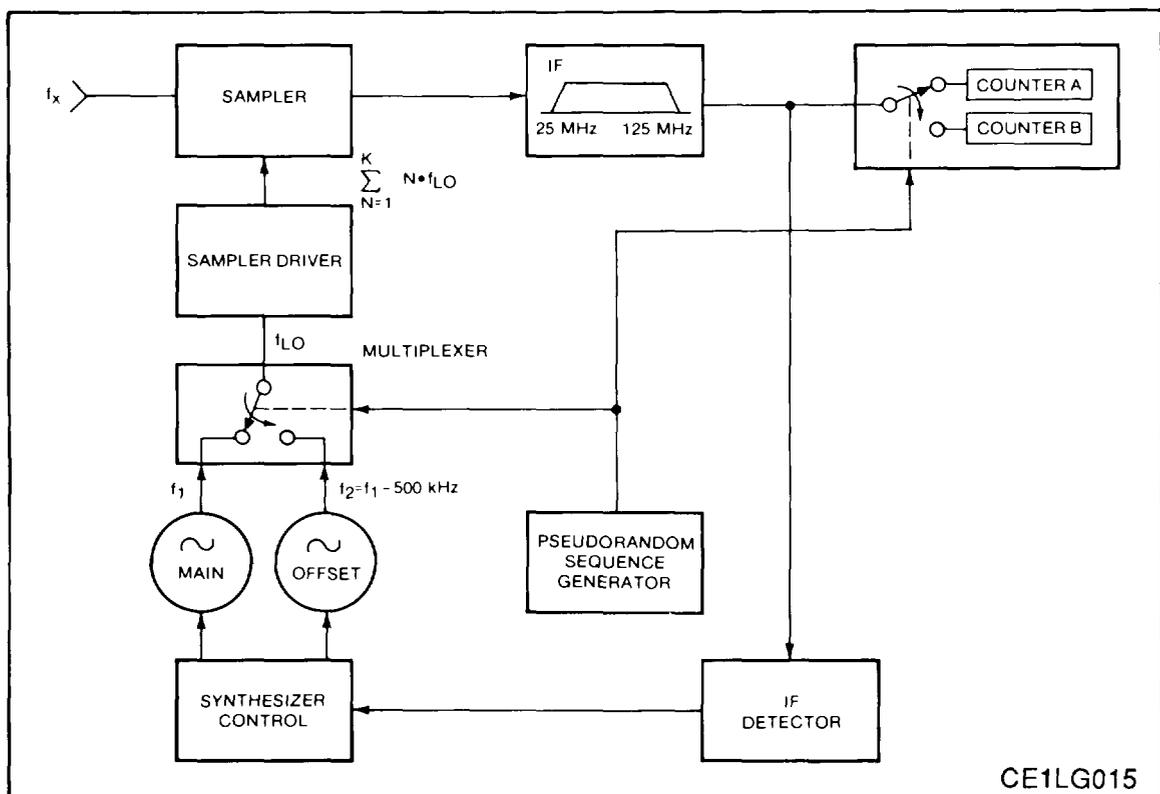


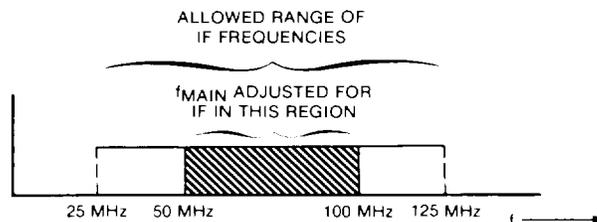
Figure 8-8. HP 5342A Simplified Block Diagram

generator switches between the main oscillator and offset oscillator as well as counter A and B so that counter A accumulates f_{IF1} (produced by $N \cdot f_1$ mixing with f_x) and counter B accumulates f_{IF2} (produced by $N \cdot f_2$ mixing with f_x). The pseudorandom switching prevents coherence between the switching rate of the multiplexer and the modulation rate of the FM from producing an incorrect computation of N . Of course, during the sequence, each counter is enabled for exactly the same total amount of time. The N number and sign of the IF are computed as previously described since counter A accumulates f_{IF1} , and counter B accumulates f_{IF2} . The prs (pseudorandom sequence) is then disabled, the main oscillator is selected, and the frequency of f_{IF1} is measured in counter A to the selected resolution.

8-97. The total measurement time, then, consists of these three components: sweep time, N determination time, and gate time. The period of the sweep is 150 ms which is the worst case time to detect a countable IF. The normal prs for N determination lasts for 360.4 ms (a rear panel switch selects a longer prs for higher FM tolerance). The gate time required depends on the resolution. For 1 Hz resolution, the gate is 1 second. For gate times from 10 Hz to 100 kHz, the gate time is 4 s/Hz so that 1 kHz resolution is achieved in 4ms. 1 MHz resolution takes a 10-microsecond gate time.

8-99. FM TOLERANCE

8-99. The worst case normal mode FM tolerance is 20 MHz p-p and occurs when the period of the modulation is near the period of the pseudorandom sequence which is 360.4 milliseconds. When the FM exceeds 20 MHz p-p, the computation of N maybe in error by ± 1 (round off error), For FM is excess of 20 MHz p-p, a wide range FM mode with a long prs is selectable (via a rear panel switch) which provides a worst case FM tolerance of 50 MHz p-p. In this case, however, the limiting factor is not round off in the computation of N but the allowable range of frequencies in the IF.



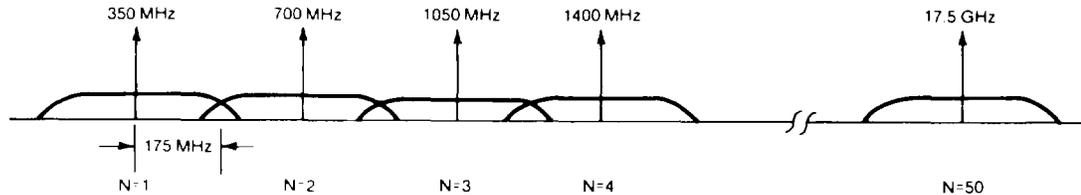
8-100. During the sweep, the frequency of the main oscillator is adjusted until f_{IF1} and f_{IF2} both fall within the range of 50 MHz to 100 MHz. In the worst case, when the IF occurs at 100 MHz or 50 MHz, the signal may deviate by a maximum of 25 MHz before crossing the band-edge of allowable IF frequencies. This gives a worst case FM tolerance of 50 MHz peak-to-peak. For the wide range FM, the period of the long pseudorandom sequence is 2.096 seconds which means that acquisition time is significantly longer for the wide range FM mode.

8-101. AUTOMATIC AMPLITUDE DISCRIMINATION

8-102. The HP 5342A has the ability to automatically discriminate against lower amplitude signals in its range of 0.5—18GHz in favor of the highest amplitude signal in the range. Thus, if there is 20 dB separation (typically better than 10 dB) between the highest amplitude signal and any other signal in the 0.5—18 GHz range, the counter automatically measures the highest amplitude signal.

8-103. Amplitude discrimination is a feature of the HP 5342A because of two design features: the bandwidth of the preamplifier, which is 175 MHz, means that there are no gaps between the power spectrums produced by mixing harmonics of the oscillator with the input; and limiting of

all IF signals produced by inputs greater than the counter's sensitivity means that the IF is at the frequency of the largest amplitude signal in the input spectrum and is frequency modulated by the lower amplitude signals. (This is the well known AM to PM conversion characteristic of limiters. The bandwidth and roll off of the preamp are chosen so that the PM does not introduce errors into the count.)



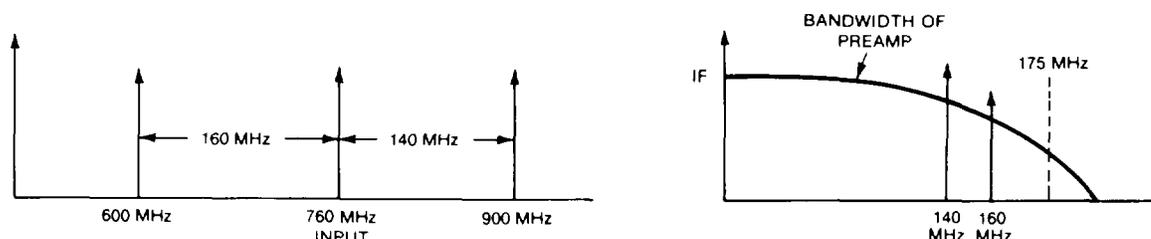
8-104. If there were gaps, then there could be a signal in the 0.5—18 GHz range which would not appear in the down converted IF. Thus, this signal, even if it were the largest, could not be measured.

8-105. SENSITIVITY

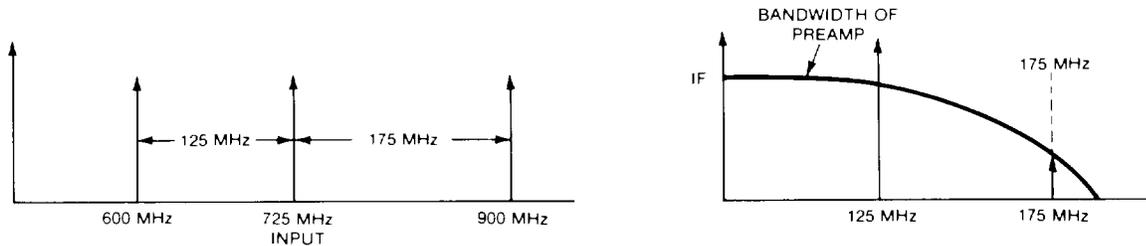
8-106. The limiting factor in determining the sensitivity of the HP 5342A is the effective noise bandwidth of the IF. Since the IF signal to noise ratio must be kept at a value which insures that there are no noise induced errors in counting the IF signal, the noise bandwidth of the IF determines the noise power; and, therefore, sets the minimum input signal level.

8-107. The IF Detector detects two parameters: one output is true if the IF signal is in the range of 50 MHz to 100 MHz and the input power level is greater than approximately -30 dBm; the other output is true if the IF signal is in the range of 25 MHz to 125 MHz and the input power level is greater than approximately -30 dBm. The detector thus insures that the input signal is sufficiently large to produce an IF with an acceptable signal to noise ratio. The 50 to 100 MHz IF output is used when sweeping since, to achieve the specified FM tolerance, the counter must center the IF somewhere in the range of 50 to 100 MHz. The 25 to 125 MHz output is used to ensure that the IF signal does not exceed those limits and that the input does not drop below -30 dBm. Either of these events occurring could cause a wrong computation for N.

8-108. The reason the IF is restricted to a 25 to 125 MHz bandwidth is examined in the following: the actual bandwidth of the IF is 175 MHz (set by the A25 Preamplifier) which is required for automatic amplitude discrimination. However, the counter restricts the countable IF to frequencies less than 125 MHz so as to prevent generating two IF signals — one generated by “N” times the main oscillator frequency and the other generated by “N±1” times the main oscillator frequency. If two IF signals are generated, then incorrect counting may result. By restricting the IF signal to be less than 125 MHz, the upper tone is of a high enough frequency as to be sufficiently attenuated by the 175 MHz bandwidth of the preamplifier so that no errors are introduced. Consider what would happen if IF frequencies to 175 MHz were allowed. Take the example of a 760 MHz input signal. By mixing with the second harmonic of 300 MHz, an IF of 160 MHz is produced. The input also mixes with the third harmonic of 300 MHz to produce another IF signal at 140 MHz. Neither signal is greatly attenuated by the 175 MHz bandwidth of the preamp as shown below and miscounting results because of interference between the two tones.



8-109. By limiting the IF to frequencies less than 125 MHz, the problem described in paragraph 8-108 does not occur. For the case of a 725 MHz input, the second harmonic of 300 MHz produces an IF of 125 MHz (the maximum allowable IF) and the third harmonic produces an IF of 175 MHz. But the IF signal at 175 MHz is attenuated by the 175MHz bandwidth of the preamplifier as shown below so as to prevent errors in counting.



8-110. HP 5342A BLOCK DIAGRAM DESCRIPTION

8-111. Figure 8-9 is a block diagram of the HP5342A showing the major assemblies of the instrument. There are five major sections: The direct count section, the synthesizer section, the IF section, the time base section, and the control section. Each of these are discussed in the following paragraphs.

8-112. Direct Count Section

8-113. The direct count section consists of the A3 Direct Count Amplifier assembly and the A13 Counter assembly. Frequencies less than 500 MHz may be measured directly by the direct count input. The input signal, which is applied to the front panel BNC connector, is amplified and conditioned by the input amplifier on A3. The direct count main gate, also on A3, is enabled for a specific period of time (determined by the resolution selected) by the LDIR GATE signal from A17. During the time that the A3 main gate is enabled, counts pass through the main gate to Counter A on the A13 Counter assembly where they are totalized. At the conclusion of the gate time, the A14 Microprocessor assembly reads the contents of Counter A and sends the result to A1 Display along with the correct annunciators and decimal point. The microprocessor continually reads the status of a hardware flag on A17 which indicates the end of the sample rate delay. At the end of the delay, the measurement process begins again.

8-114. Synthesizer Section

8-115. The synthesizer section consists of a main oscillator and an offset oscillator to provide two output frequencies to AS RF Multiplexer in the range of 300 MHz to 350 MHz which are locked to the counter's 10 MHz time base. The frequency is selected with 100 kHz resolution by the A14 Microprocessor. The main oscillator is formed by the A8 Main VCO assembly, the A9 Main Loop Amplifier assembly, and the A10 Divide-by-N assembly. The microprocessor controls the division factor N in A10 which determines the main oscillator frequency. The offset oscillator consists of the A4 Offset VCO assembly, the A7 Mixer/Search Control assembly, and the A6Offset Loop Amplifier assembly. The offset loop is phase locked at a frequency 500 kHz below the main VCO frequency. Figure 8-70 is a block diagram of the synthesizer section which is described in the following paragraphs.

8-116. Main Loop Operation

8-117. A buffered signal from the A8 Main VCO is fed back to the A10 Divide-by-N assembly. The division factor, N, is programmed by the A14 Control assembly and is chosen by the relation $N = \text{programmed frequency} / 50\text{kHz}$. For example, if the program requests a frequency of 346.7 MHz, then N would be equal to 6934 ($=346.7/0.05$). When the main loop is locked, the output of the divide-by-N circuitry on A10 is 50 kHz. This is compared to a 50 kHz signal which is derived

from the time base and the phase error is sent to the A9 Main Loop Amplifier. The phase error signals, available at XA10(1) and $\overline{1}$, are used by the main loop to drive the VCO frequency to the programmed frequency.

8-118. The A9 Main Loop Amplifier sums and integrates the two phase detector outputs of A10. The error signal is then passed through one of two low pass filters. When the HP 5342A is searching for an input signal in the range of 500 MHz to 18 GHz, the main loop VCO is programmed to step from 350 MHz to 300 MHz in 100 kHz steps in approximately 90 milliseconds. To achieve this fast search rate, a wideband low pass filter of approximately 2 kHz bandwidth is selected. When the counter is actually making a measurement by opening the main gate and counting the IF frequency, a narrow band low pass filter of approximately 100 Hz bandwidth is selected to achieve high spectral purity in the VCO output.

8-119. The error signal at the output of A9 drives the A8 Main VCO to a frequency which minimizes the error signal. Three buffered outputs are provided: one output is fed back to the A10 Divide-by N; another goes to the A5 RF Multiplexer; the third goes to the A7 Mixer/Search Control assembly and is used by the OFFSET LOOP to set the offset VCO to a frequency which is exactly 500 kHz below the Main VCO frequency.

8-120. Offset Loop Operation

8-121. The frequency of the main VCO and the frequency of the offset VCO are fed to a mixer on the A7 Mixer/Search Control assembly. The difference frequency at the output of the mixer is fed to a phase detector and a 500 kHz detector. The 500 kHz detector sends a search enable (HRSC EN) signal to the search generator on the A6 Offset Loop Amplifier if the offset VCO frequency is not 500 kHz less than the main VCO frequency. The search signal on A6 is a ramp waveform which drives the offset VCO to a frequency which is 500 kHz less than the main VCO frequency. When the 500 kHz detector on A7 detects the presence of 500 kHz, the search is stopped. The phase detector on A7 compares the difference frequency out of the mixer with a 500 kHz reference derived from the time base. The phase error signal is sent to A6.

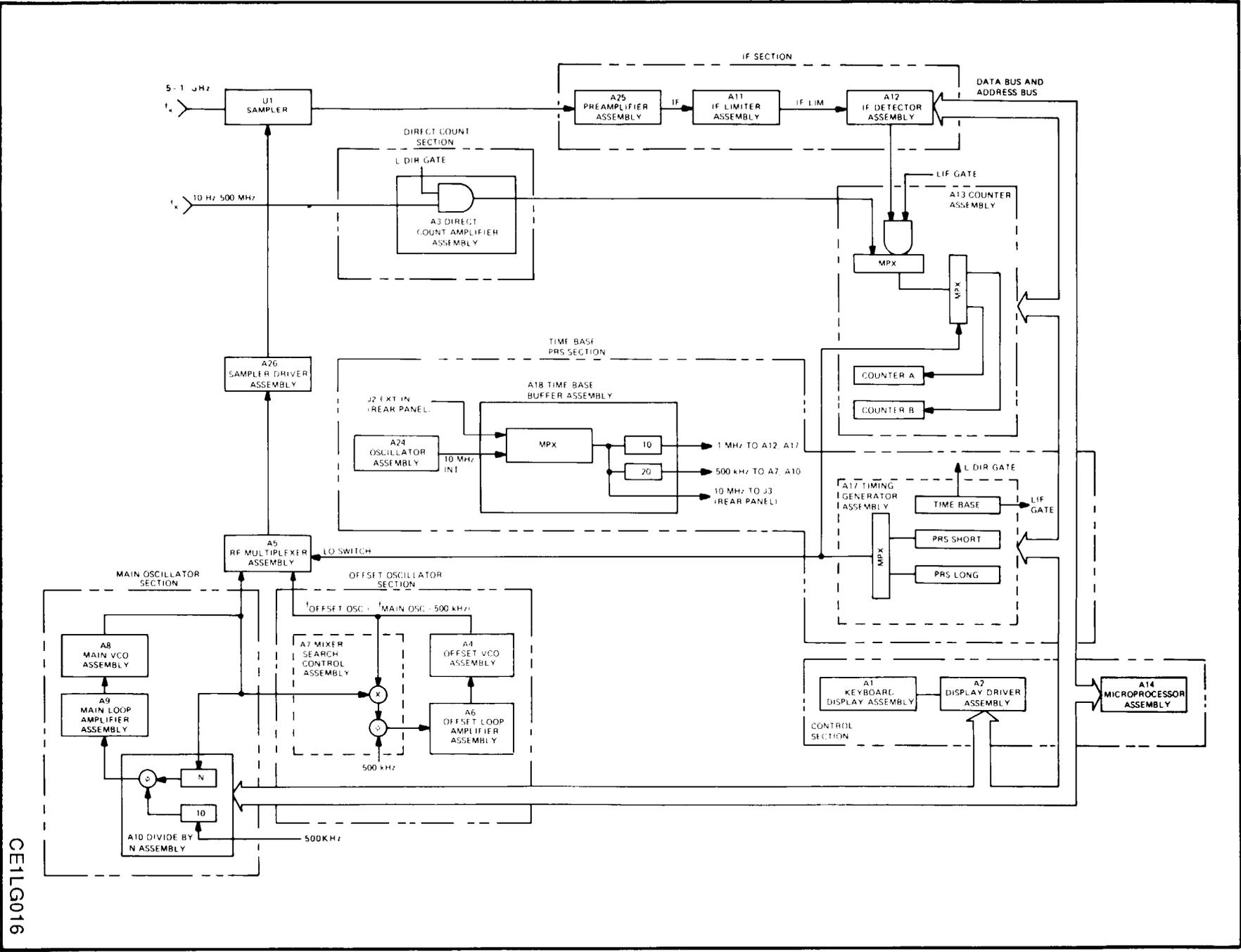
8-122. The A6 Offset Loop Amplifier sums and integrates the two outputs of the phase detector on A7. This error signal keeps the offset VCO on a frequency which is 500 kHz below the main VCO frequency. To get the difference frequency out of the mixer on A7 into the capture range of the phase-locked loop formed by A7, A6, and A4, a search generator on A6 is turned on in the absence of a 500 kHz difference frequency. The generator sweeps the offset VCO over its range until the VCO is 500 kHz less than the main VCO (the LPOS Slope signal generated on A6, prevents the loop from locking on the upper sideband where the offset VCO is 500 kHz greater than the main VCO). At this point the search generator is disabled and the output of the phase detector on A7 keeps the loop locked.

8-123. The offset VCO has two buffered outputs: one goes to the A5 RF Multiplexer and the other is fed back to the A7 Mixer/Search Control assembly.

8-124. IF Section

8-125. The IF section amplifies the output of the U1 sampler and routes this IF to A13 for counting. It also provides digital outputs which indicate that the IF signal is of sufficient amplitude to be counted and that it is in the proper frequency range. The A25 Preamp assembly provides high gain amplification (approximately 42 dB) for the output of the sampler (the sampler has a -48dB conversion efficiency which means that an input signal at a level of 0 dBm will yield an IF at approximately -48 dBm). The All IF Limiter assembly limits the amplitude of the IF signal. The A12 IF Detector assembly detects both the amplitude of the IF as well as the frequency of the IF. During the sweep, the microprocessor monitors the state of the 50 MHz—100 MHz detector output of A12 and stops sweeping when that detector is true. At the conclusion of the N determination the latched 25 MHz—125 MHz detector output is checked. If this detector is true, then the IF signal never varied beyond the 25—125 MHz range nor did it drop too low in amplitude. If the detector is false, then the computation of N may be incorrect and the algorithm specifies that the sweep start at a frequency 100 kHz lower than where it previously stopped sweeping.

Figure 8-9. HP 5342A Block Diagram



CE1LG016

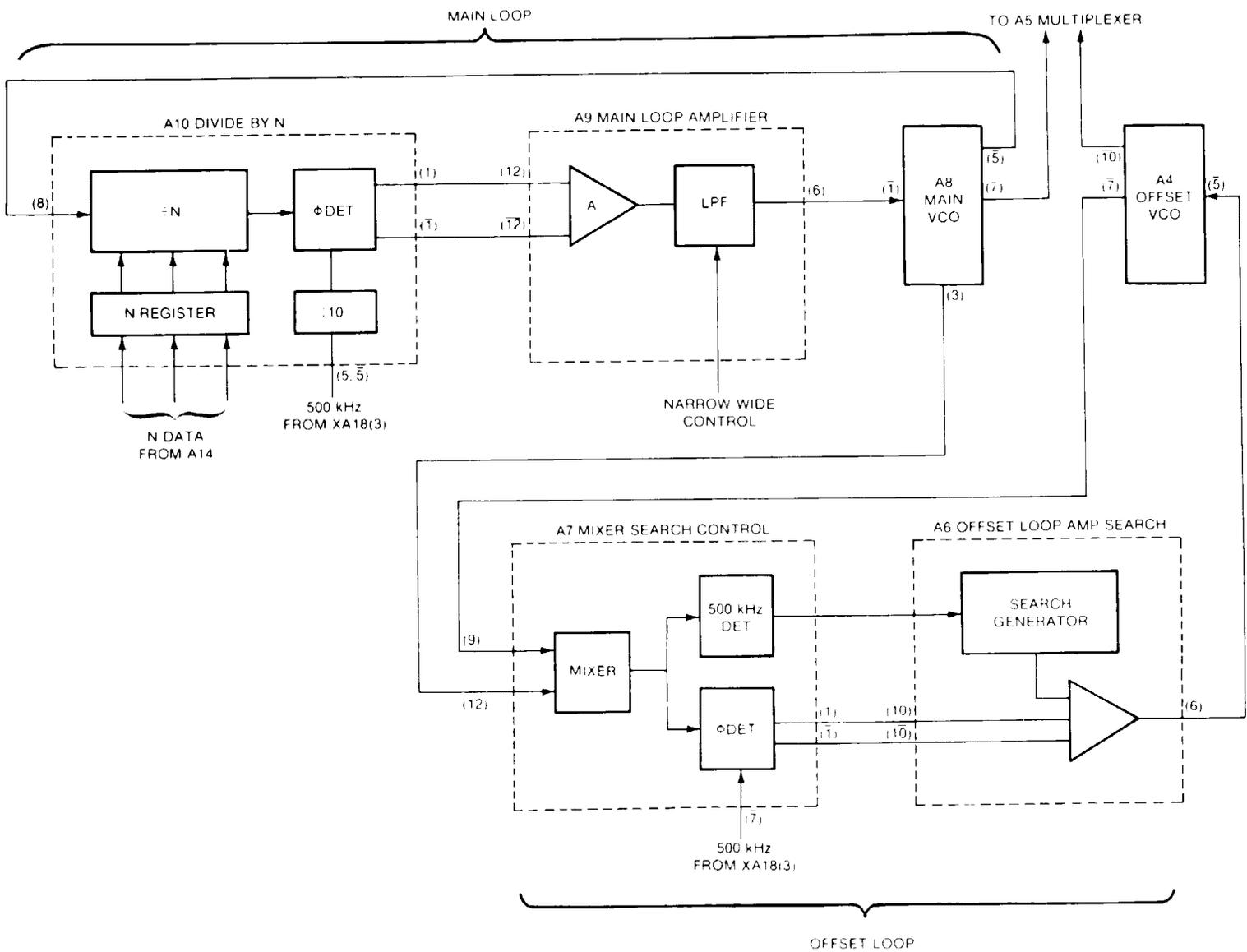


Figure 8-70. Block Diagram of Synthesizer Section

CE11G017

8-126. Time Base/PSR Section

8-127. The time base section consists of the A24 Oscillator assembly which provides a 10 MHz sine wave to the A18 Time Base Buffer assembly. A18 provides TTL compatible 10 MHz, 1 MHz, and 500 kHz outputs to the rest of the counter. The A17 Timing Generator assembly uses the 1 MHz signal to provide gate times from 1 microsecond to 1 second in decade steps as well as generate a pseudorandom sequence during the N determination portion of the algorithm. Based on the position of the rear panel FM switch, the microprocessor selects a short prs (360.4 ms long) for 20 MHz p-p FM tolerance (CW) or a long prs (2.096 seconds long) for 50 MHz p-p FM tolerance (FM).

8-128. Control Section

8-129. The control section is made up of the A14 Microprocessor assembly, the A2 Display Driver assembly, and the A1 Key board/Display assembly. The program stored in ROM on the A14 assembly controls the operating algorithm of the instrument. The A1 assembly is used by the operator to interface with the stored program. Via the A1 keyboard, the operator selects operating modes (AUTO, MANUAL, CHECK], resolution and offsets. The A1 assembly also displays measurement results. The A2 Display Driver assembly controls A1 and provides the interface with the A14 Microprocessor.

8-130. DETAILED THEORY OF OPERATION

8-131. The detailed theory of operation is provided in the following paragraphs in numerical order of the assemblies.

8-132. A1 DISPLAY ASSEMBLY AND A2 DISPLAY DRIVER ASSEMBLY

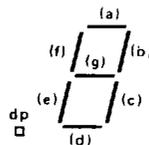
8-133. The A1 Display assembly and A2 Display Driver assembly shown in Figure 8-24 operate together to provide the user interface with the microprocessor. For a description of microprocessor operation, refer to paragraph 8-228. The keyboard on the A1 Display permits the operator to input commands to the microprocessor. The display on the A1 Display is used by the microprocessor to display measurement results, error codes, and other information to the operator. As an example, consider what occurs when the SET key is pressed by the operator. Pressing the key generates an interrupt to the microprocessor. The program stops executing the current program and jumps to a subroutine to find out which device caused the interrupt and why. The subroutine determines that the keyboard generated the interrupt. Circuitry on A2 tells the microprocessor that the SET key was pressed. The program then sends commands to A2 to cause the light in the SET key to blink as well as the code to be displayed, both of which act as prompts to the user. All of this occurs very quickly and is virtually transparent to the user.

8-134. The A2 Display Driver assembly is driven by a 6 kHz clock (scan clock) formed by Schmitt trigger U5E, feedback resistor R7, and capacitor C5. This clock is continuously running and outputs a TTL signal with a positive pulse width of approximately 40 μ s. The output of the scan clock goes through a jumper (which maybe removed to allow testing with a logic pulser to simulate the clock) and drives decade counter U3. The outputs of U3 are decoded by U13C and U6 to reset the U3 outputs to all TTL low after 13 clocks have been counted. These 13 states correspond to the 11 digits and 2 annunciator lines which need to be driven in the display.

8-135. The output of the U3 counter passes through 3-state driver U6. The purpose of U6 is to force invalid states into column scanner U2 and U7 so that on power-up, (when LDVRSST goes low) the display is blank. On reset, the input to U10D goes low and the control to U6(1) goes high, which forces U6 to the high Z state. Pull up resistors R2(C,D,G,F) put state 16 into U7 and state 7 into U2. Since these states are out of the normally operating range of the scanners, all display digits and annunciators are blanked.

8-136. In normal operation, U6(1) is low and the output of the 13 state counter drives BCD-to-decimal decoders U2 and U7. These two devices forma column scanner whose low output turns on, one at a time, A1 driver transistors Q13, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q1, Q2, Q11, Q12 for a period of approximately 166 μ s (1/6kHz). For example, when the 13 state counter reaches 0111 (7), then U7(9) goes low, turning on transistor A1Q4 and applying +5.0V to the LED digit A1DS14. Whatever segment inputs are low will thus be momentarily lighted. The correct code to be input to the LED digit is stored in TTL RAM A2U11 and U8. U8 and U11 each can store sixteen 4-bit words. When the 13 state counter is in state 0111, then the inputs to RAM U11 and U8 are at 0111 and the desired digits code for DS14 is output, through A2U1 and U4, to the selected digit. Limiter resistors R8, R13, R15, R16, R6, R4, R11, and R14 limit the current through the LED segments when the NAND gate output (U4and U1) goes low. When the 13 state counter reaches 1000, then the input to U2 looks like 0000 and U2(1) goes low which applies +5.0 volts to Q1 and lights DS13. When the 13 state counter reaches 1100 (12, 13th state since started at 0), then the input to U2 is 0010 and U2(5) goes low and one or more annunciator lights are turned on according to the code stored in RAM U11, U8.

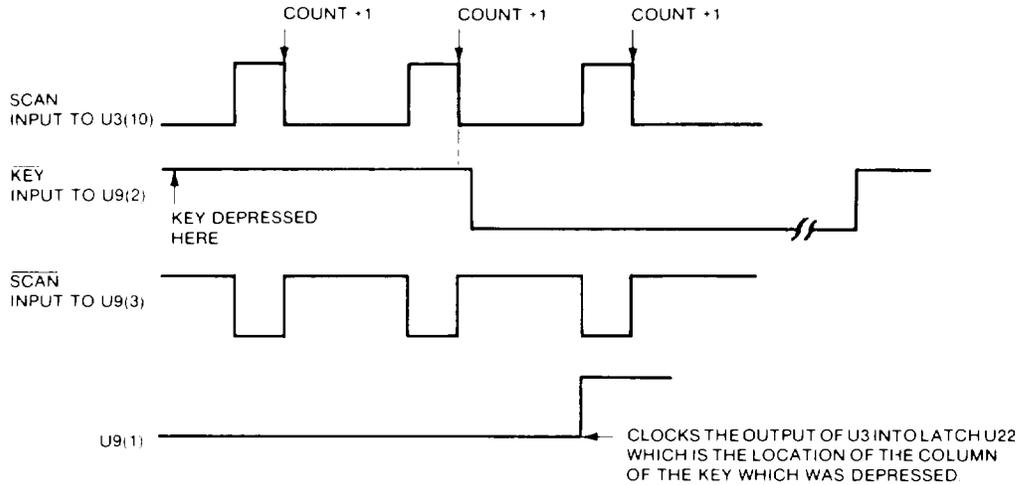
8-137. HDSPWRT comes in at A2J1(3). When this signal is high, data is written into RAM U8, U11 from the microprocessor for display. When HDSPWRT goes low, the output of U13D is low and quad multiplexer U17 selects its "1" inputs. Thus, the output of the 13 state counter increments through 13 locations in RAM and causes the contents of RAM to be displayed. When HDSPWRT is high, U17 selects its "43" inputs, The write enable inputs to U11 and U8 pin 3 are enabled and data appearing on the D0 through D7 data lines is stored at the addresses appearing on the A0 through A3 address lines. Segments are labeled as shown below. D0 lines sends (a) segment information; D1 sends (b), D2 sends (c), D3 sends (d), Segments (a), (b), (c), and (d) are stored in U11. The D4 data lines sends (e) segment information, D5 sends (f), D6 sends (g), D7 sends decimal point. Segments (e), (f), (g), (alp) are stored in U8. For example, if it were desired to display 2 in the DS21 or least significant digit, then segments (a), (b), (g), (e), and (d) must be lighted.



To light these segments the following action occurs. In address location 1111 (the output of U17 is inverted in U11, 1 (=D1) 1 (=D2) 0 (=D3) 1 (=D4) are stored. In address location 1111 in U8, 1 (=D1) 0 (=D2) 1 (=D3) 0 (=D4) are stored. When the 13 state counters puts out 0000, then the output of U11 will be 1101 (5,7,9,11) and the output of U8 will be 1010(5,7,9,11). The column scanner has output U7(1) low and all other outputs high (U2(10) is also low but it is not connected to any digit). Thus +5.0 volts is applied to DS21 and the correct segment inputs to DS21 are grounded to turn on segments (a), (b), (g), (e), and (d) which forms a digit 2. The D0—D3data lines and A0, A1 address lines are also connected from driver U17 to the Option 004 (DAC) circuit on A2 assembly, Figure 8-25.

8-138. Keyboard Operation

8-139. When a key (pushbutton switch) is depressed, it is not immediately recognized but must wait until the column scanner reaches that particular key. However, since the scan rate is 6 kHz, this is much faster than the operator can depress and withdraw his finger. When the column scanner places a low on the line connected to the key which has been depressed, a low pulse is generated on the output of A2U5(6). This pulse is called KEY and when low, indicates that a key has been depressed.



8-140. With $\overline{\text{KEY}}$ low and $\overline{\text{SCAN}}$ low, U9(1) goes high which clocks latch U22 and causes it to store the address 10000 to 11001 of the column of the key which was pushed. Since there are two keys per column, another line is used to indicate top or bottom row. The output of U9(1), which clocks U22, also clocks U19A. U19A(5) will be low if a top row key is pushed and will be high if a bottom row key is pushed. In this manner, the microprocessor determines exactly which key has been depressed.

8-141. Flip-flop U18A is also clocked by the output of U9(1). Its output at U18A(5) will be high anytime that a key is pushed. It is reset to low when the 13 state counter reaches the end of the scan at state 1100. The low signal at U2(5) causes the output of U9(10) to go momentarily low and reset U18A. The End of Scan signal at the output of U9(13) clocks U19B and, if U18A(5) is high, will clock a high into U19B(9). This output is the Key Down signal. Key Down high goes to U22(9, 10) and inhibits other addresses from being latched. U19B(9) is also used as part of the Recall subroutine. To recall a value, the recalled value will be displayed as long as its associated key is depressed. The program examines the output of U19B(9) and if it remains high, continues to display the recalled value. When the key is released, U19B(9) will be reset by End of Scan and the program, upon detecting this, stops displaying the recalled value and displays the original display (e.g., frequency).

8-142. Flip-flop U18B stores the interrupt. U19B(9) going high at the end of the scan clocks a high into U18B(9). This is inverted by U10 and becomes LIRQ which interrupts the microprocessor. The program jumps to a service routine which, upon determining that the keyboard has requested service, issues a low keyboard read command LKBRD. This signal enables three-state latch U22 which puts out its contents onto the bus. LKBRD also enables the three-state buffer U12 which puts out the contents of U19A, U18B, and the position of the front panel RANGE switch. The program determines which key was pressed and acts accordingly. The LKBRD also resets the interrupt flip-flop U18B.

8-143. Processor looks at J1(15) to check if operation is in direct mode (10 Hz—500 MHz) or 500 MHz—18 GHz mode.

8-144. Capacitor C7 is used to differentiate the positive transition of HDSPWRT to produce the write pulse to U8(3) and U11(3).

8-145. A3 DIRECT COUNT AMPLIFIER ASSEMBLY

8-146, The input signal is applied to the BNC connector and switch S23 on the A1 Display assembly as shown in Figure 8-24 (upper left of A1 schematic). Switch S23 routes the signal through either a 1 M Ω path or a 50 Ω path to A3. As shown in Figure 8-26, the Z switch transistors

Q7 and Q6 bias the 1 M Ω input at pin 8 of U7 and the 50 Ω input at pin 7 of U7 to turn balanced amplifier U7 either on or off, depending upon which signal path has been selected by switch S23. The impedance select line biases pin 7 or 8 approximately -2 volts (50 Ω) or -3.3 volts (1 M Ω).

8-147. The 50 Ω signal path consists of 0.1 amp fuse F1 (3.5V rms maximum input), clamping diodes CR8, CR5, and the limiting diode bridge formed by CR3, CR4, CR6, CR7 which limit the output to 1 volt peak-to-peak.

8-148. The 1 M Ω path consists of ac coupling capacitor A1R13, A1C1, A2 compensation network C8, R13, clamping diodes CR1, CR2, source follower Q3, and emitter follower Q1. Field effect transistor Q2 is biased as a current source for Q3.

8-149. Balanced amplifier U7 provides complementary outputs of the input signal increased in amplitude by times 2. These complementary outputs drive differential amplifier U6 which provides amplification of times 10 so that the overall gain from U7 input to U6 output is approximately times 20. A portion of the output of U6 is integrated by U3, C17 to provide a dc voltage proportional to amplitude. This voltage provides AGC to U7 so that the input to Schmitt trigger U5 remains relatively constant. The output of U5 is a 0V to -650 mV signal which is divided-by-2 in U4 and divided-by-2 in U1. The main gate on U4 passes the output of U5 on to the dividers only when it is enabled by the LDIR GATE signal from A17 going low.

8-150. The DIRECT A output passes through EECL to TTL converter formed by Q8, Q9 to A13 where it is ready by the microprocessor. The DIRECT B output passes through EECL to ECL converter U2 to A13 where it is counted by the A counter.

8-151. HECL RSET high clears U4, U1 before LDIR GATE opens the main gate for counting.

8-152. A4 OFFSET VCO

8-153. The A4 OFFSET VCO (Figure 8-27) is essentially identical to the A8 MAIN VCO assembly described in paragraph 8-172, with the exception that A4 has one less buffer amplifier. The OFS OSC amplitude at XA4($\overline{10}$) should be approximately 600mV rms and OFS OSC at XA4 ($\overline{7}$) should be approximately 300 mV rms. Measure with a high impedance RF millivoltmeter. such as the HP 411A.

8-154. A5 RF MULTIPLEXER ASSEMBLY

8-155. The A5 RF Multiplexer assembly shown in Figure 8-28, receives two input signals: MAIN OSC from the A8 Main VCO assembly at XA5 ($\overline{10}$) and OFFSET OSC from the A4 Offset VCO assembly at XA5($\overline{1}$). Upon command by the LO SWITCH signal from the A17 Timing Generator assembly, MAIN OSC (if LO SWITCH is TTL high) or OFFSET OSC (if LO SWITCH is TTL low) is gated to the output of A5 and becomes the LO FREQ signal which drives the A26 Sampler Driver.

8-156. The oscillator signals enter A5 at a level of approximately +4 dBm at XA ($\overline{1}$) for the OFFSET OSC and XA5($\overline{10}$) for the MAIN OSC. After passing through 6dB matching pads formed by R8, R7, R6, and R22, R21, R20, both signals are amplified by differential amplifiers; U1 amplifies OFFSET OSC and U4 amplifies MAIN OSC. The amplified outputs pass through ac coupling capacitors C6 and C20, respectively, and then are either blocked or passed by diode switches. The offset channel switch is composed of CR3, CR1, CR2, and the main channel switch is composed of CR5, CR6, CR4. With the LO SWITCH signal TTL high, the base of Q3 increases to approximately 3.8 volts which decreases the current through the Q3 emitter. Since the differential amplifier formed by Q2, Q3 is driven by constant current source Q1, the current through the Q2 emitter increases since the total current must remain constant. This causes the voltage dropped across R27 to decrease (because the current decreased) so that the collector of Q3 is at -0.8 volts. Since the voltage dropped across R18 increases, the collector of Q2 goes to +0.8 volts. The -0.8 volts at the Q3 collector is passed through the decoupling network L1, L2, C2 which prevents the 300-350

MHz signal in one channel from passing through the switching network over to the other channel. A -0.8 volt at the cathode of CR1 causes CR1 to be forward biased and CR2, CR3 to be reversed biased, thereby blocking the OFFSET OSC signal. The +0.8 volt at the cathode of CR6 reverse-biases CR6 and forward-biases CR5 and CR4, thus permitting the MAIN OSC signal to pass in to the differential amplifier U2. With LO SWITCH TTL low, the current through Q3 increases and the operation is reversed.

8-157. The output of the U2 differential pair drives common emitter amplifier U3 which uses one-half of a differential transistor pair. The output, at a level of approximately +15 dBm, is ac coupled through C25 and sent to the A26 Sampler Driver.

8-158. A6 OFFSET LOOP AMP/SEARCH GENERATOR ASSEMBLY

8-159. The A6 Offset Loop Amplifier/Search Generator assembly (Figure 8-29) consists of:

- a. A filter and amplifier which condition the phase error signal from A7 for locking the offset loop.
- b. A search signal generator which drives the offset VCO such that the difference frequency between the offset VCO and the main VCO is within the capture range of the offset phase-locked loop. A signal, called LPOS Slope, is generated on A6 which prevents the loop from locking up when the offset VCO is 500 kHz above the main VCO; this insures that the offset VCO is always 500 kHz below the main VCO.

8-160. The search generator consists of transistor Q4, Schmitt trigger NAND gates U1A, U1B, U1D, diodes CR3, CR4, and the integrator formed by operational amplifier U2 and integrating capacitor C10. This integrator is also used by the error signals from A7 and is part of the compensation for the phase-locked loop.

8-161. Variable resistors R1 (SWEEP CENTER FREQ) and R2 (SWEEP RANGE) are adjusted to provide a triangular waveform at test point TP1 of -4 to +4 volts which corresponds to a VCO search frequency range of approximately 380 MHz to 270 MHz.

8-162. With HSRCH EN low, both diodes CR3 and CR4 are reversed-biased and the search generator is effectively isolated from the integrator U2. With HSRCH EN low, the loop is maintained in a locked condition by the phase error signals at XA6(10) and XA6($\overline{10}$). These signals are summed and integrated by U2 and then filtered by the low pass filter formed by R21, C12, and R20. The error signal drives the offset VCO to maintain a constant 500 kHz offset.

8-163. Two voltage regulators convert the +15 and -15 volt inputs to +12 and -12 volts, respectively. The +12 volt regulator consists of transistor Q2, diode CR1, resistors R4, R6, and capacitors C1 and C3. The -12 volt regulator consists of transistor Q3, diode CR2, resistors R8 and R11, and capacitors C8 and C6.

8-164. When the 500kHz detector on A7 detects that there is not a 500kHz difference frequency present, the HSRCHEN at XA6(8) goes TTL high and enables U1A and U1B. Since U1D(13) is tied to +5V, it is already enabled. The threshold voltages for U1D(12) are 0.8 volts and 1.6 volts which means that a logic condition is not recognized until the input to U1D(12) moves from below 0.8 volts up through 1.6 volts. A logic 0 condition does not occur until the signal moves from above 1.6 volts down through 0.8 volts. Assuming a 0.8 volt level at U1D(12) to start with, the operation is as follows: U1D(11) is high, which drives U1B(6) low and U1A(3) high. With U1A(3) high, Q4 is turned off and CR4 is reversed-biased since the voltage at U2 inputs is at +1.5 volts. Since U1B(6) is low, CR3 is forward-biased and sinks current from the integrating capacitor C10. This causes the voltage at the output of operational amplifier U2(6) to increase linearly until the voltage at U1A(2) crosses above 1.6 volts. With the output of U1A(3) high, the LPOS Slope signal is high and prevents the loop from locking up on an offset VCO signal which is 500 kHz higher than the main VCO. This is so because with LPOS Slope high, the offset VCO is changing from its high fre-

quencies to lower frequencies. A 500 kHz difference frequency resulting from this sweep would be on the upper sideband. With LPOS Slope low, the offset VCO is changing from low frequencies to higher frequencies. A 500 kHz difference resulting from this sweep only occurs if the offset VCO frequency is 500 kHz less than the main VCO frequency.

8-165. When the sweep ramp present at U1D(12) crosses above the upper threshold of 1.6 volts, the output of U1D(11) goes low, U1B(6) goes high and U1A(3) goes low. This causes Q4 to conduct which forward-biases CR4. Since U1B(6) is high, CR3 is reversed-biased. Current is now supplied through CR4 to the integrating capacitor C10. This causes the output of U2(6) to decrease linearly. Since U1A(3) is low, LPOS Slope is TTL low and the loop is allowed to lock once a 500 kHz difference frequency is detected on A7. When lock is achieved, HSRCH EN goes TTL low which causes U1B(6) and U1A(3) to both go TTL high, thereby reverse-biasing both CR4 and CR3. The voltage at the output of U2(6) is therefore maintained at that level which achieved lock. The timing diagram for this operation is shown in Figure 8-77.

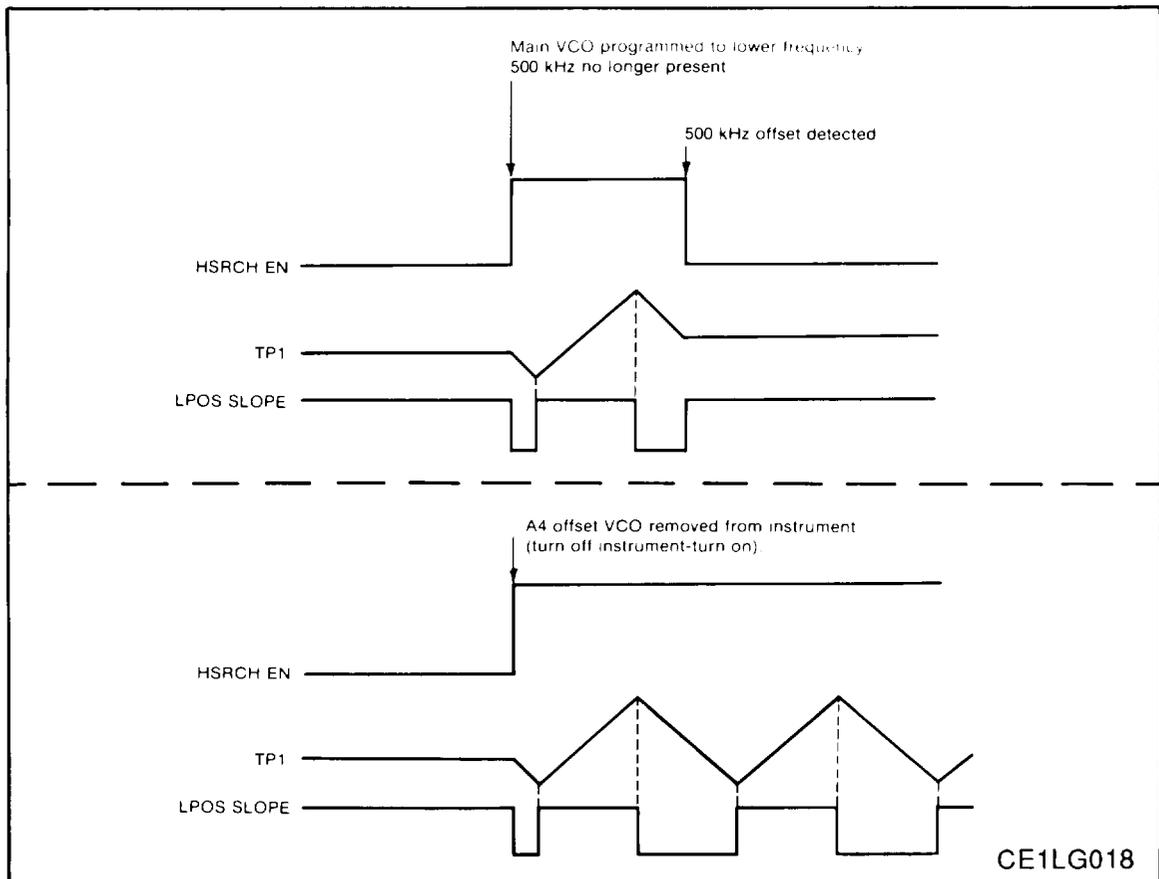


Figure 8-77, Timing Diagram of A6 Search Generator Operation

8-166. A7 MIXER/SEARCH CONTROL ASSEMBLY

8-167. The output of the main loop VCO, which comes in at XA7(12), Figure 8-30, is amplified by differential pair U4 to a level of approximately +5 dBm and is half-wave rectified by transistor Q6 whose base-emitter junction is used as the rectifying diode. The output of the offset VCO, which comes in at XA7(9), is amplified by U3 to a level of approximately 0dBm and is applied to the base of Q1. Since Q1 is being alternately turned on and off by the Main VCO signal appearing at the Q1 emitter, the output appearing across R15 contains the sum and difference frequencies $f_{MAIN} \pm f_{OFFSET}$ (if $f_{MAIN} > f_{OFFSET}$) or $f_{OFFSET} \pm f_{MAIN}$ (if $f_{OFFSET} > f_{MAIN}$). Since Q2 is a low frequency

transistor, the sum frequency is attenuated and only the difference frequency is amplified. At test point TP1, the difference frequency at an amplitude of 0 to 5V is available.

8-168. To insure that the offset phase-locked loop locks up only when a 500 kHz difference frequency is produced by the Main VCO being 500 kHz greater (not less) than the offset VCO frequency, three control signals are produced which control the search enable flip-flop u2. When the HSRCH EN output at XA7(2) is TTL high, the triangle search waveform on A6 is enabled. HSRCH EN goes low when the U2(3,4,5) inputs are all low. This occurs when the following conditions are met:

- a. The output of the 500 kHz detector is low.
- b. The U1(2) equal frequency output is low.
- c. The LPOS Slope signal from A6 is low.

8-169. The 500 kHz detector consists of the low-pass filter formed by resistors R5, R6, and capacitor C16, a full-wave rectifier formed by diodes CR1, CR2, and capacitor C22, and emitter follower Q3. For signal less than approximately 1 MHz, the full-wave rectifier produces a level at the base of transistor Q4 sufficient to turn Q4 on. This develops a voltage across resistor R3 which turns transistor Q5 on. The collector of Q5 then drops from a TTL high to a TTL low,

8-170. U1 is a phase detector which produces fixed amplitude variable duty cycle pulse trains at its two outputs. The duty cycle of the pulse train is proportional to the phase difference between the signals at its inputs. The $OFFSET\Delta\phi_1$ and $OFFSET\Delta\phi_2$ outputs are summed, integrated, and amplified by A6 to provide a dc control voltage to the A4 OFFSET VCO. When the frequency at U1(1) is less than or equal to the 500 kHz reference frequency at U1(3), U1(2) goes TTL low. ATTL low at U2(4) is necessary but not sufficient to disable the search waveform on A6.

8-171. The third input to the NOR gate on U2 is the LPOS Slope signal from A6. This signal is TTL low when the search signal from A6 is sweeping the A4 VCO from low frequencies to high frequencies. Consequently, if a 500 kHz difference frequency is obtained and LPOS Slope is low, then the offset VCO must be 500 kHz less than the main VCO.

8-172. A8 MAIN VCO ASSEMBLY

8-173. The synthesizer uses two voltage controlled oscillators which are essentially identical in operation (A8 and A4). The oscillator circuit shown in Figure 8-37 consists of transistor Q1, feedback capacitor C7, and varactor diodes CR1 and CR2. Resistors R14 and R13 provide dc bias for Q1. Capacitor C11 resonates with the inductance of ferrite bead E1 to provide a low impedance path to ground for frequencies in the range of the VCO, thus eliminating parasitic oscillations. Transistor Q1, which is operating a common base mode for the VCO frequency range, has a portion of the output signal at its emitter fed back to its collector via capacitor C7. This positive feedback sets up oscillations at a frequency equal to the parallel resonant frequency of the tank circuit formed by varactor diodes CR1 and CR2 and the inductance of a metal trace on the A8 board. By changing the MAIN VCO CONTROL voltage at A8(1), the capacitance of the varactors change which changes the resonant frequency of the tank circuit and hence the frequency of oscillation. The modulation sensitivity of the VCO is approximately -12.5 MHz/volt. For a MAIN VCO CONTROL voltage at A8(1) of +2 volts, the VCO frequency should be approximately 300 MHz while a control voltage of -2volts results in an output frequency of approximately 350 MHz.

8-174. A voltage regulator, consisting of 11-volt Zener diode CR3, transistor Q2, resistors R21, R22, R23, and capacitor C1, is used to provide low noise dc power to the oscillator circuit since any noise on the power supply of the oscillator will degrade the oscillator's spectral purity. Potentiometer R22 is used to adjust the output voltage of the voltage regulator circuit so that the free-run frequency of the VCO (i.e., the frequency with 0 volts at the MAIN VCO CONTROL A8(1) input) is 325 MHz \pm 2 MHz. The nominal voltage which achieves this free-run frequency is 8.5 volts and is measured at the junction of C20 and CR2. Inductor L8, capacitors C23 and C16, and resistor R19 provide further filtering for the dc power to the VCO.

8-175. The output of the VCO is sent to three buffer amplifier U1, U2, and U3. Capacitor C4 is a dc blocking capacitor. The differential transistor pairs contained in U1, U2, and U3 provide +6dB, +8dB, and +6dB gain, respectively. The gain is determined by the dc current flowing through the emitters of the transistors. This current is set by the networks connected to pin 3 of the IC. Decoupling networks L7 and C15, L1 and C3, L4 and C8, L11, C22, C24, C25, C26 isolate the -5.2 volt power from the RF signal. Decoupling networks L5 and C10, L2 and C5, L9 and C14, and L12, C18, C27, C28, C29 isolate the +5 volt power from the RF signal. The output of each buffer amplifier, after removal of the dc component by dc blocking capacitor C17, C6, or C12, is transmitted to other parts of the instrument over a 50 Ω microstrip transmission line. The ground plane of the microstrip board is connected to the ground plane of the motherboard. The output at XA8(5) and XA8(3) should be approximately 250 mV rms while the output of XA8(7) should be approximately 500 mV rms.

8-176. A9 MAIN LOOP AMPLIFIER ASSEMBLY

8-177. The two variable duty cycle pulse outputs from the phase detector on A10, Main $\Delta\phi 1$ and Main $\Delta\phi 2$, are summed and integrated by U2 on the A9 Main Loop Amplifier assembly, shown in Figure 8-32. Bidirectional switch U3(B, C, and D) controlled by D flip-flop U1B, selects the compensation for the phase-locked loop by selecting one of two feedback paths around operational amplifier U2 and by selecting one of two low pass filters in the output. When the HP 5342A is searching for an input signal, the wideband filter is selected. When the HP 5342A is making an actual measurement, the narrowband filter is selected.

8-178. When the least significant bit of the data bus from A14(D0), is a logic 1 and the LPD Write address is decoded on A14 so that LPD Write goes high, then U1(8) goes low which selects the wideband filter consisting of inductors L1, L2, capacitors C2, C12, C16, C11, and C1, With U1(8) low and U1(9) high, transistor Q3 is turned on and provides +5.6 volts to control pins U3(6) to turn on the switch; transistor Q2 is turned off, thus providing a -5.6 volt level to control pins U3(5) and U3(12) to turn off the switch.

8-179. When D0 is a logic 0 and LPD Write goes high, U1(9) goes low and U1(8) goes high. This selects the narrowband filter consisting of L3, C8, C9, and C10 and also selects the R15 feedback resistor connected to U2. With U1(9) low, Q2 is turned on so that +5.6 volts is applied to control pins U3(5) and U3(12) to turn on the switch. With U1(8) high, Q3 is off and -5.6 volts is applied to control U3(6) to turn off the switch.

8-180. The voltage regulator consisting of transistor Q4, diode CR4, resistors R10, R11, and capacitor C17 converts +15 volts to +5.6 volts and the voltage regulator consisting of transistor Q1, diode CR1, resistors R1, R3, and capacitor C3 converts -15 volts to -5.6 volts.

8-181. A10 DIVIDE-BY-N ASSEMBLY

8-182. The A10 Divide-by-N assembly is essentially a programmable frequency divider and phase detector. As shown in Figure 8-33 the output of the A8 Main VCO enters at DIV N XA10(8), and is initially divided by two by the ECL D flip-flop U6. The divider chain formed by U12, U9, U13, U14, and U8 divides the output of U6(4) by N. The division factor N is programmed from the A14 Microprocessor assembly via the data bus lines. The output of the divider chain goes from U8 through U3B to the U2 phase comparator where it is compared to a 50 kHz reference frequency. The phase error outputs of the U2 phase comparator, MAIN $\Delta\phi 1$ and MAIN $\Delta\phi 2$, are conditioned by the A9 Main Loop Amplifier and cause the A8 MAIN VCO to go to that frequency which, when divided by N in the divider chain on A10, produces a 50 kHz output.

8-183. Registers U10, U15, and U7A provide storage for the BCD encoded N data sent from A14 and registers U16, U11, and U17 provided buffer storage for the N data. Decade divider U1 outputs a 50 kHz reference frequency to U2 against which the N divided VCO frequency is compared.

8-184. The N divider chain formed by U12, U9, U13, U14, and U8 is programmed by the A14 Microprocessor assembly with a 4-digit positive-true BCD encoded number which is the 9's complement of the desired main VCO frequency. The main VCO frequency may be programmed with 100 kHz resolution. To program the main VCO to a frequency of 342.6 MHz, for example, the program would want N to be 6573 (9's complement of 3426). The actual overall division factor is

$$\frac{342.6}{0.050} = 6852$$

8-185. Since the data bus is only 8-bits wide, the 4-bit BCD encoded N number is divided into two 2-bit bytes. The two more significant bits form the upper byte and the two lower significant bits form the lower byte. The upper byte is first loaded into U17 when LSYH, decoded on A14, goes high. Since the range of VCO is 270 to 380 MHz, the most significant digit of the N number will be either a 6 or 7 (9's complement of 3 and 2, respectively). In BCD, this means that only the least significant bit of the BCD encoded most significant digit of the N number need be sent. If the most significant digit of N is 6, then the D4 input will be a low. If MSD of N is 7, then D4 will be high. U7A stores the D4 bit and presents it to U8 which represents the most significant digit of the N number.

8-186 The lower byte is loaded into U16 and U11 when LSYL, decoded on A14, goes high. The data, which has been temporarily stored in U16, U11, and U17, is next transferred to U10, U15, and U7A by the operation of U4A and U4B. When LSYL goes high, a high is clocked into U4A(S) and is presented to U4B(12). The next positive transition at U4B(11) causes U4B(8) to go low, which clears U4A(5). The following positive transition at U4B(11) then clocks U4B(8) high. The low to high transition of U4B(8) loads the data into U10, U15, and U7A. figure 8-72 shows the timing of this operation.

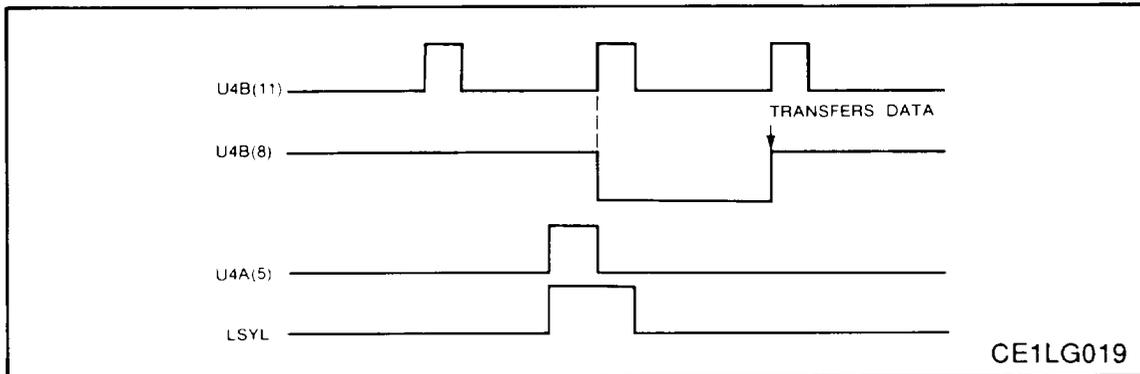
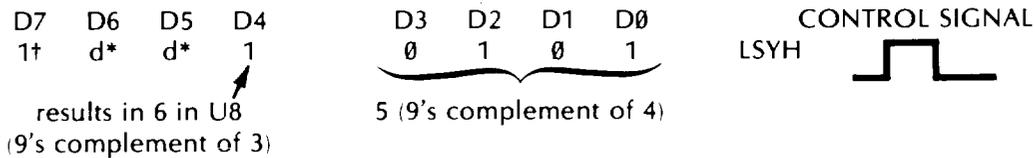


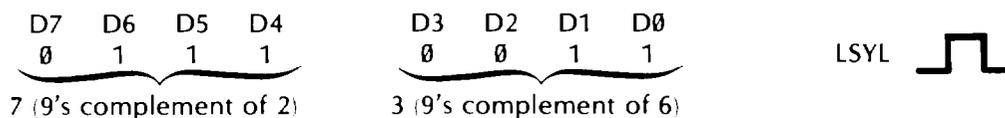
Figure 8-72. Data Transfer Timing in A10 Circuit

8-187. For example, if the program wants to set the main VCO to 342.6 MHz, the following data would be sent:



*don't care digits
†not check if 1 (check if = 0)

This would be followed by:



8-188. The most significant bit in the upper byte is used to indicate the CHECK condition. If U17(12) is low, the D flip-flop US is enabled and the output of U6 is again divided by two. In CHECK mode, the main VCO is programmed to 300 MHz. The CHECK signal at XA10(11) is 300 MHz divided by four so that the 5342 A displays 75 MHz in CHECK, In CHECK, the following outputs should be present:

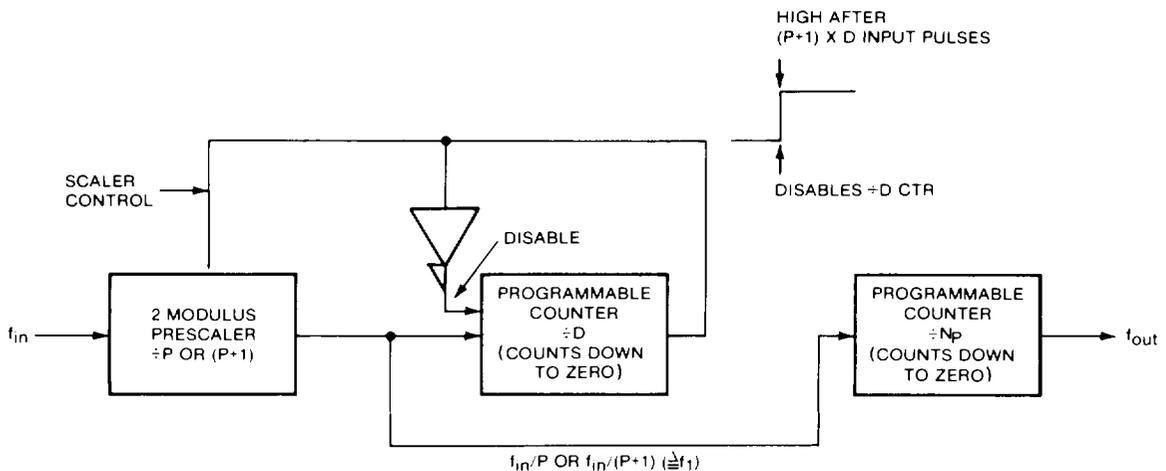
U16(15)	1	LSB	} Least significant BCD digit (9's complement of 0)
U16(10)	0		
U16(2)	0		
U16(7)	1	MSB	
U11(7)	1	LSB	} Digit 2 (9's complement of 0)
U11(2)	0		
U11(15)	0		
U11(10)	1	MSB	
U17(2)	1	LSB	} Digit 3 (9's complement of 0)
U17(5)	0		
U17(7)	0		
U17(10)	1	MSB	
U17(15)	0	—	Most significant digit
U17(12)	0	—	CHECK

8-189. Before the divider chain formed by U12, U9, U13, U14, and U8 can be explained, the two following divide-by-N techniques must be discussed:

- a. Two modulus prescaler technique.
- b. A counter (divider) chain utilizing 9's complement.

8-190. Two Modulus Prescaler Technique

8-191. The two modulus prescaler technique is illustrated below.



8-192. At first, the scaler control line is set to a low level so that the two modulus prescaler can operate as a $\div (P+1)$ prescaler. Therefore, it generates a pulse every $P+1$ input pulses. After $(P+1) \times D$ input pulses occur, the second counter ($\div D$) reaches zero since it was preprogrammed to D at first, When the content of the second counter ($\div D$) gets to zero, it generates a pulse which changes the level of the scaler control line high and disables the $\div D$ counter (itself) at the same time. So, actually, the output of $\div D$ is not a pulse but a level change, Therefore, after this change occurs, the $\div D$ counter stops counting and keeps the new state which lets the two modulus prescaler operate as a $\div P$ prescaler.

8-193. When the level change occurs, the content of the ÷Np counter (which was preprogrammed to Np) is Np-D since D pulses have passed by so far. So, the ÷Np counter will reach zero after receiving (Np-D)•P input pulses (fin). As soon as the ÷Np counter gets to zero, it generates a pulse at fout terminal.

8-194. Therefore, the total input pulses (fin) necessary to get one output pulse is:

$$(P+1) \cdot D + p \cdot (Np-D) \tag{1}$$

8-195. For example, if we choose 10 as P and 100A + 10B + C as Np, equation (1) becomes as follows:

$$\begin{aligned} & 11D + 10(100A + 10B + C) - D \\ & = 1000A + 100B + 10C + D \end{aligned} \tag{2}$$

NOTE

The output is also used as a loading pulse to initiate the next dividing cycle.

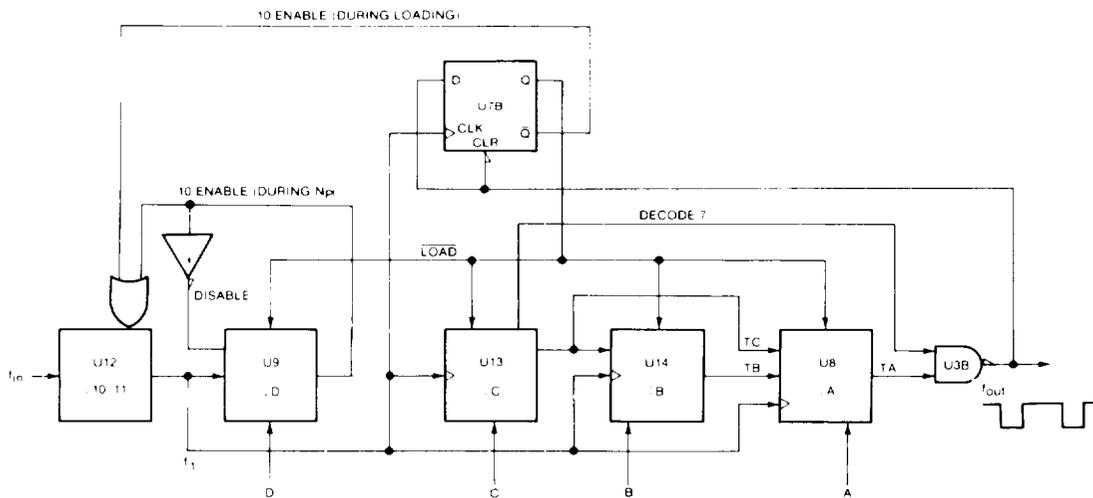
8-196. Now, we have a complete programmable divider chain which can be programmed to any dividing ratio expressed by equation (2). The only limitation on this technique is as follows:

$$Np \geq D \tag{3}$$

8-197. This limitation doesn't matter for our application because $Np \geq 299 \geq 9 \geq D$.

8-198. Counter (Divider) Chain Utilizing 9's Complement

8-199. A counter chain utilizing 9's complement numbers is illustrated below. In the explanation above, we used down counters to achieve ÷D and ÷Np. In the actual circuit, however, up counters (74LS160) are used for that purpose. The up counter generates a positive pulse when used for that purpose. The up counter generates a positive pulse when it reaches a state 9. Therefore, a divide-by-D can be realized if it is preprogrammed to 9-D at first. Then, it generates a pulse after getting D input pulses. One comment to note is that after generating an output pulse (after getting D pulses), it will operate as a divide-by-10 divider unless it is present (loaded to D again).



- Remarks:
1. TA, TB, and TC are outputs of ÷A, ÷B, and ÷C.
 2. TC for ÷A is look forward connection.
 3. ÷B and ÷C operate as divide-by-10 after their first dividing cycle.
 4. A, B, C, and D are numbers to be loaded.
 5. U9 is preset to 9 in check. Output is high so it is always disabled and always ÷10.

8-200. A two-pulse period of f_1 is used to load the divider chain since one pulse period is not long enough to load the divider chain. The load pulse is provided by U7B. As soon as the f_{out} pulse (negative pulse) appears, LOAD goes low because of CLR input and stays low when the next f_1 pulse comes in because of the low input to D input. LOAD goes high when the second f_1 comes in because of a high input to D input. As long as LOAD is low, the counter chain is inhibited and the state of each divider agrees with the number to be loaded. Since we use a two-pulse period for loading, we have to decode 997 (999-2) for the $\div N_p$ chain to get a correct dividing ratio as a whole. The BCD output of U13 is decoded to detect 7 for this purpose. The output of U8 which corresponds to 99X (X = don't care) is AND'ed with the decoded 7 to get the f_{out} pulse. Since a NAND gate is used, the output pulse is a negative pulse.

8-201. When CHECK mode is selected, the MPU writes to the A10 Divide-by-N assembly to enable D flip-flop US and to select a 300 MHz main oscillator frequency. With LSYNHI going low, bit D7 low at u17(13) is clocked into cause U17(12) to go low, thus enabling U5($\div 2$). When CHECK is not selected, U17(12) is high so that US is disabled and the CHECK output at XA10(11) is inhibited.

8-202. A11 IF LIMITER ASSEMBLY

8-203. The A11 IF Limiter assembly, shown in Figure 8-34, provides an additional 14 dB gain to the IF signal over a bandwidth of 0.1 to 175 MHz. For high amplitude signals, the output of A11 is amplitude limited. The 14 dB amplification is provided by differential pair u2. Potentiometer R1, "AMP", is used to maximize the gain through U2 by balancing the currents through the differential pair. The 75 MHz CHECK signal from A10 enters the IF circuitry at XA117, $\overline{7}$. . CHECK should not be selected when a signal at the type N input connector is present.

8-204. Deleted

8-205. As shown in Figure 8-34, detecting diode CR1 and capacitor C2 detect the negative half-cycle of the IF signal. This dc level is sent to voltage comparator U1 which compares the detected level with a reference level set by the "DET" potentiometer, R14. For input signals greater than approximately -15 dBm, the detected IF appearing at U1(3) will be more negative than the reference voltage at U1(2) and the output at U1(7) will be TTL high. When the input level to the counter drops below about -15 dBm, U1(7) will go TTL low which means that LPWR RST is low, Resistor R4 on U1 provides hysteresis of about 1 dB in IF signal amplitude so that the output of U1 does not go high again until the IF amplitude increases by 1 dB over the level where it caused LPWR RST to go low.

8-206. A12 IF DETECTOR ASSEMBLY

8-207. The A12 IF Detector assembly shown in Figure 8-35, further amplitude limits the IF signal by amplifying it an additional 28 dB before sending it to the A13 Counter assembly to be counted. A level-detecting diode detects if the input signal level is of sufficient amplitude to be counted. A digital filter provides two outputs which indicate: 1) the IF is in the range of 48 MHz to 102 MHz, and 2) the IF is in the range of 22 MHz to 128 MHz. The program reads these filter outputs and stops the sweep when the IF is in the range of 48 MHz to 102 MHz. The 22 MHz to 128 MHz output is latched and is reset if the input power to counter drops below a preset level or if the IF leaves the range of 22 MHz to 128 MHz. This output is examined at the conclusion of the N determi-

nation routine to insure that the count during the prs was not invalidated by a power drop-out or excessive FM deviation.

8-208. The IF signal enters differential pair U2 and is amplified by approximately 14 dB. The output at U2(5) passes through a 125 MHz low pass filter formed by C5, L1, C10, L2, C7, and is detected by CR1 and C1. The voltage across C1 is presented to the inverting input of voltage comparator U1, which, due to the positive feedback provided by resistor R9, exhibits approximately 5 mV hysteresis. The OFFSET potentiometer R7 is adjusted so that the output of U1(7) goes low when the input signal to the counter drops below -32 dBm (for a 1 GHz input).

8-209. The other IF output of U2,U2(8), is ac coupled through C11 to differential pair U4 where it is amplified by another 14dB. Potentiometer R12,(B2) is used to equalize (balance) the currents through the two emitters of the transistor pair. This is done by adjusting R5 for maximum gain through the stage. Potentiometer R2, (B1) is adjusted in a similar manner. U4 has two outputs: U4(5) and U4(8). The output at U4(5), IF COUNT, appears at XA12 (8) and is sent to the A13 counter to be counted. The output at U4(8) is ac coupled by capacitor C16 to a digital filter,

8-210. The digital filter consists of U6, U5, U10, U8, U9, U11, U14, and U15. The filter counts the IF signal for a period of 4 microseconds and, based on the number of counts totalized during the 4 microseconds, sets two qualifiers which indicate if the IF is within the necessary frequency range. The counters are reset every 8 microseconds and the counting of the IF begins again. This process of counting the IF for 4 microseconds, setting the qualifiers, and resetting the counters after 8 microseconds occurs continuously.

8-211. The IF signal output is prescaled by 4 in U3A ($\div 2$) and U3B ($\div 2$). The ECL output of U3(15) is translated to TTL levels by transistor Q1. This signal is then counted for 4 microseconds. The NOR gate U6 is enabled for a period of 4 microseconds by U6(2) going low for 4 microseconds. This 4-microsecond gate is generated by divider U15 which divides a 1 MHz input by 8. The input is from the A18 Time Base Buffer. During the 4-microseconds gate time, the count is totalized by binary counters U5 and U10 . The contents of the counters are decoded by U8, U9 suchthat if the IF frequency is in the range of 48 MHz to 102 MHz (the U5 and U10 counters count 48 to 102 counts during the 4-microsecond gate), U6(13) [TP5] will be high. If the IF is in the range of 22 MHz to 128 MHz, U6(10) [TP6] will be high. Dual flip-flop U13 is loaded with this qualifier information every 8 microseconds by a clock signal from U11(12) [TP4]. After a 1-microsecond delay, the U5, U10 counters are reset by a low level from U14(6). Figure 8-73 shows the timing for the filter.

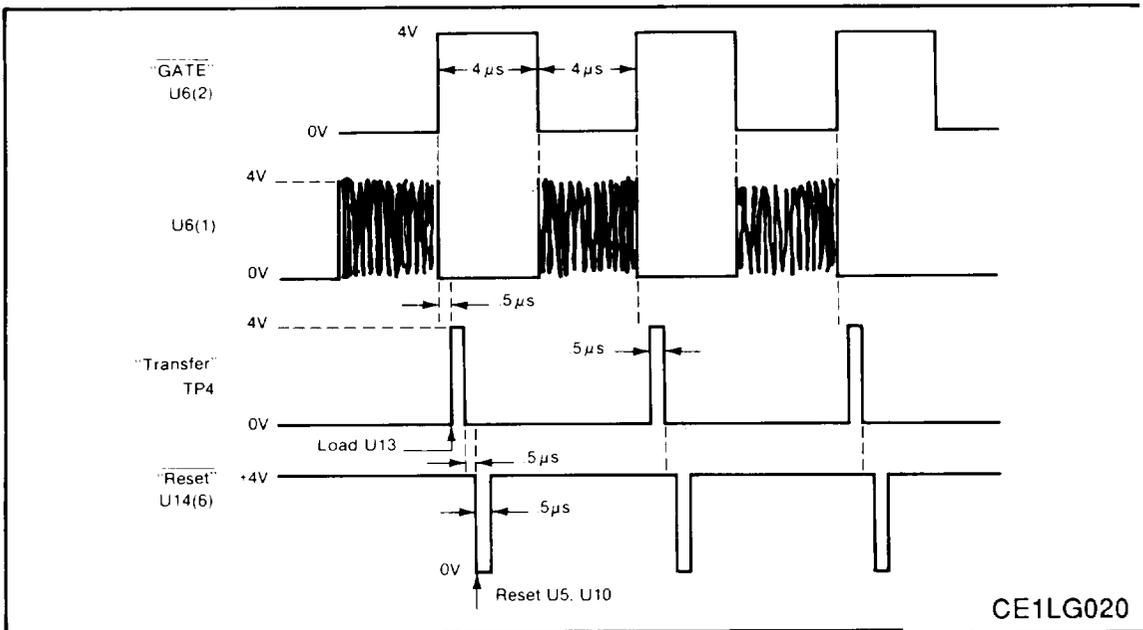


Figure 8-13. Filter Timing on A12 IF Detector

8-212. When the instrument is sweeping, the A14 Microprocessor issues LPDREAD which enables the three-state buffer/driver U12, and data from A12 is placed onto the data bus. The 48—102 MHz detector output (D6) is examined and when D6 is low (TP8 high), the microprocessor stops sweeping the main oscillator. After the sweep has stopped, the microprocessor issues LPDWRT which sets the U7(11) output of the latch formed by U7C and U7D to the low state, U7(11) [TP10] goes low when LPDWRT goes low since U13(5) is high (since U6(13) is high, then U6(10) must also be high).

8-213. The program then begins the N determination. At the conclusion of the N determination, the microprocessor sends LPDREAD and examines the latched 22—128 MHz detector D7. If the input power has dropped below -32 dBm or if the IF has exceeded the range of 22 MHz to 128 MHz, then U13(5) will have been low at some time and the U7(11) output of latch U7C, U7D will have been reset to a high. If the D7 bit read by the microprocessor is low, then the N determination is considered invalid and the sweep routine is recentered at a point 100 kHz lower in frequency than when it previously stopped searching.

8-214. Deleted

8-215. A13 COUNTER ASSEMBLY

8-216. The IF Count signal enters the A13 Counter Assembly shown in Figure 8-36 at XA13(17) and is capacitively coupled via C10 into the main gate of the counter, U11C. U11 is a high-speed ECL AND gate. When U11(9) and U11(10) are both low (-0.8V = high; -1.5V = low), the gate is enabled and the IF Count signal is passed through the gate to be counted. Flip-flop U4B selects either the IF Count signal at XA13(17) or the Direct B signal from the direct count amplifier at XA13(14) to be counted. If in direct count mode, the microprocessor sets the D1 bit to logic 0 and writes to the counter so that LCTRWRT (low counter write) will clock a logic 0 into U4(9). When operating in the 500 MHz—18 GHz range, D1 will be logic 1 and the U4(9) output will be a logic 1. This enables U11B and disables U11C.

8-217. There are two operating modes, one during and one after acquisition. During acquisition the A5 multiplexer is switched between the two LO'S. In synchronism with the A5 multiplexer switching, the IF signal on the A13 Counter assembly is switched between counter A (U17, U13, and U1) and counter B (U18, U14, and U2). Thus, counter A accumulates counts only during the time that the main VCO is producing the IF and counter B accumulates counts only during the time that the offset VCO is producing the IF. After acquisition, the pseudorandom switching between VCO'S stops and the multiplexer selects the main VCO. The IF is then measured by counter A with a gate time determined by the desired resolution.

8-218. The LO Switch signal comes in at XA13(8) and, after passing through TTL to ECL converters, drives U12A and U12B to switch the IF between counter A and counter B. When LO Switch is high, counter A is selected and LO Switch is low, counter B is selected.

8-219. The 8-decade channel A counter consists of decade counter U17 (the least significant decade), decade counter U13, and 6-decade counter U1. The 8-decade channel B counter consists of decade counter U18 (least significant decade), decade counter U14, and 6-decade counter U2.

8-220. To output the contents of the 8 decades to the microprocessor, each counter has outputs which pass through multiplexer. The counter A multiplexer consists of 4-line-to-1-line data selectors U5A, U5B, U9A, U9B. The counter B multiplexer consists of U6A, U6B, U10A, and U10B. If the LCTRRD (low counter read) signal goes low and if A5 = logic 1, then the A counter multiplexer is enabled (otherwise the three-state outputs are in the high Z state) and the contents of

the A counters are output on the data lines to the microprocessor. With LCTRRD low and the A5 = logic 0, then B counter multiplexer is enabled and its contents are output on the data lines.

8-221. After passing through main gate U11, the signal is switched to either the A counter or the B counter by gates associated with ÷2 flip-flop U12A and U12B. If the A counter is selected, the IF signal is divided by 2 by U12B and divided by 2 again by U16B. The output of U16B(14) passes through ECL to TTL level converter U15. The outputs of these first two binaries are connected to the "0" data inputs of the multiplexer and are read first by the microprocessor.

8-222. For example, the output of the first binary in the A counter chain U12B(14) is connected, via an ECL to TTL converter, to U9A(6). Consequently, the state of the A counter's two least significant binaries is read by the microprocessor by sending LCTRRD low, A5 = logic 1, and A3 = A4 = logic 1 (the inverter U7 causes the "Ø" data inputs of the multiplexer to be connected to the multiplexer outputs). The outputs of the first decade counter following the binaries are read in a similar fashion. These outputs are connected to the "1" data input of the multiplexer. For example, to read the first decade of the A counter, LCTRRD goes low with A5 = logic 1, A3 is set to logic Ø and A4 is set to logic 1 (because of the inversion, the "1" data inputs to the multiplexers are selected). To read the last six decades, the "3" data inputs of the multiplexer are selected by setting A3 = A4 = logic Ø. The AØ, A1, and A2 address lines used to address the decades in U2 (if A5 = logic Ø) or U1 (A5 = logic 1). To address the least significant decade in U1, for example, the logic state of the address lines would be:

LCTRRD	A5	A4	A3	A2	A1	AØ
Ø	1	Ø	Ø	1	1	1

8-223. The Direct A input at XA137 $\bar{1}$ is the output of the first high-speed binary located on the A3 Direct Count Amplifier. The Direct B input is the output of the second high-speed binary on A3 and it drives the A counter when making direct count measurements. The state of the first and second binaries on A3 are connected to the "0" data inputs of U5A and U5B on A13 and are read first for direct count measurement. The state of the ÷4 output from A3, which causes the output of A13U11C(4), passes through an ECL to TTL converter formed by Q2 and Q3 before going to U5B(10). Therefore, in direct count, the signal is divided by 4 on A3 and then divided by 4 in U12A, U16A on A17, before passing to the decade counters U17, U13, and U1.

8-224. After counting, the decades are reset by writing to A13 counter board with D0 = logic 0. This causes U4(5) to go low to reset U18, U17, and U13. U4(6) goes high to reset U2 and U1 as well as U12 and U16.

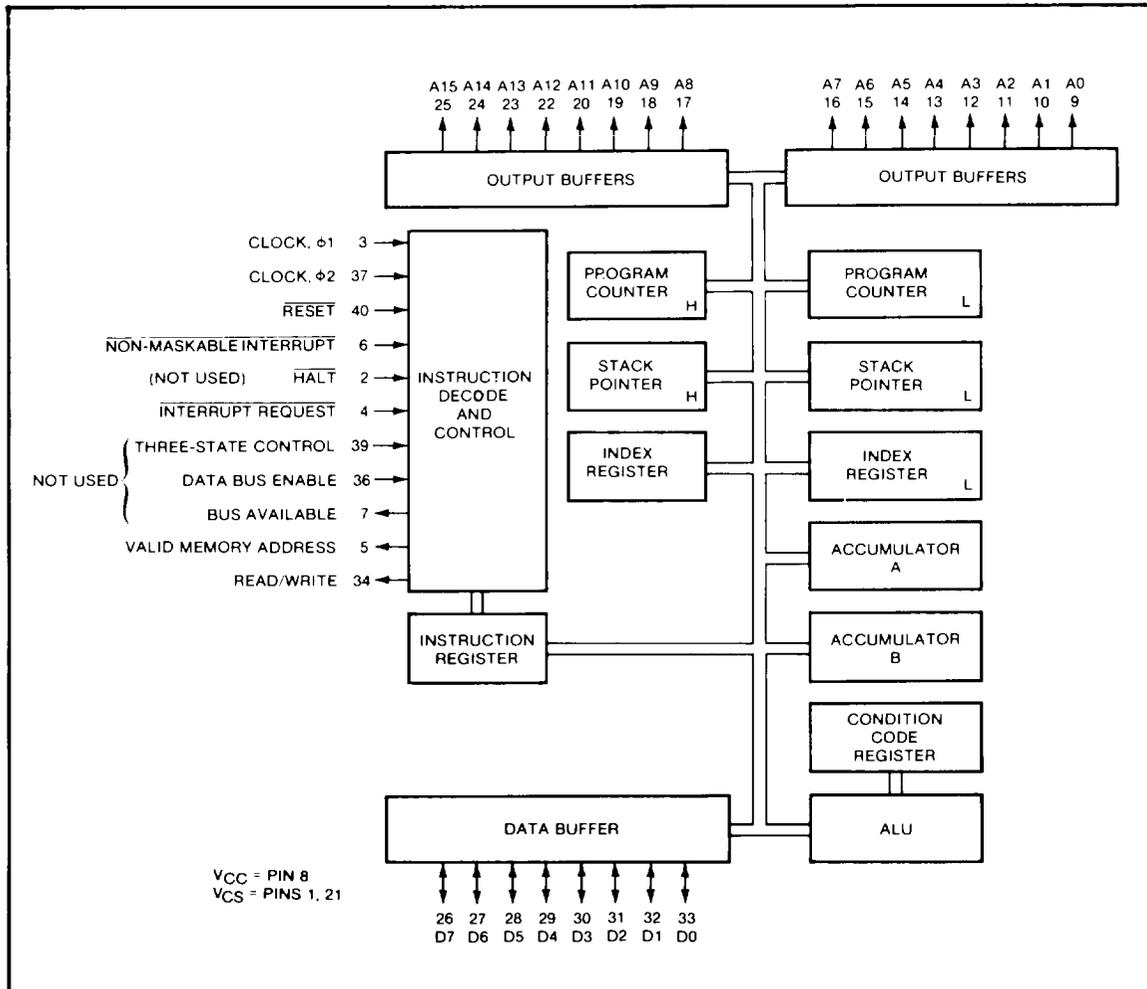
8-225. A14 MICROPROCESSOR ASSEMBLY

8-226, The A14 Microprocessor (MPU) assembly shown in Figure 8-37 contains in ROM the operating algorithm of the instrument. This assembly controls the measurement cycle, performs numerical computations for frequency measurements, and interfaces with many of the other assemblies.

8-227. The A14 MPU assembly uses the Motorola 6800 MPU (U21). The application in the HP 5342A is described in the following paragraphs.

8-228. Microprocessor Operation

8-229. The HP 5342A uses U21 for control and computation purposes. An expanded block diagram of U21 is shown in Figure 8-74. The 16-bit address bus allows the MPU to address up to 64K memory locations. The data bus is 8 bits wide and is bidirectional. Data on the bus is read into the internal MPU registers when the Read/Write control line is low. All operations are synchronized to a two-phase nonoverlapping 1 MHz clock, 1ϕ and $\phi.2$. Each instruction requires at least two-clock cycles for execution. The HP 5342A utilizes the following additional 6800 control lines:

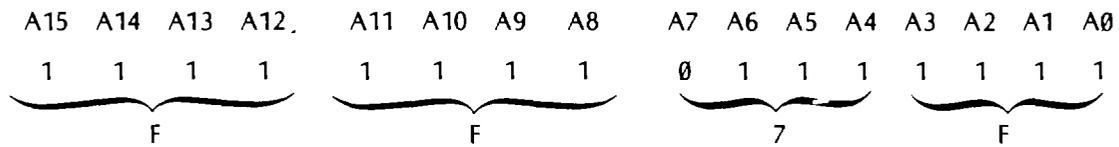


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figure 8-14. A14U21 Expanded Block Diagram

- a. **RESET** — This input is used to reset and start the MPU from a power-down condition, resulting from a power failure or an initial start-up of the processor. If a positive edge is detected on the input, this will signal the MPU to begin the reset sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFE, FFFF) locations in memory will be used to load the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by IRQ.
- b. **NONMASKABLE INTERRUPT (NMI)** — A low-going edge on this input request that a nonmask-interrupt sequence be generated within the processor. As with the INTERRUPT REQUEST signal, the processor will complete the current instruction that is being executed before it recognizes the NMI signal. The interrupt mask-bit in the Condition Code Register has no effect on NMI. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations causes the MPU to branch to a nonmaskable interrupt routine in memory. NMI has a high impedance pullup internal resistor, however, a 3 K Ω external resistor to Vcc should be used for wire-OR and optimum control in interrupts. Inputs IRQ NMI are hardware interrupt lines that are sampled during $\phi 2$ and will start the interrupt routine on $\phi 1$ following the completion of an instruction.

After going through the inverting line drivers U16, U18, and U8, the address lines become:



8-233. To address a location in RAM, all the enable inputs must be true. Consequently, U12 (11) must be low, U12 (12) must be low, U12 (14) must be low, U12(10) must be high, U12(13) must be high, and U12(15) must be low. The seven address inputs then select one of 128 locations in the RAM, For the case of 0080 sent out by the MPU, it is seen that U12 (11) goes low when the inputs to U22D are both high (VMA high indicating that the address data on the address bus has settled and is valid data and 02 high); U12(12) is low since the inputs to U9B (inverted A15, A14, A13) are all high; U12(14) is low since the inputs to U9C (inverted A12, A11, A10) are all high; U12(10) is high since the inputs to U5D are both high (inverted A9 and LFRERUN); U12(13) is high since inverted A8 is high; U12(15) is low since inverted A7 is low. Thus, due to the inversion, 0080 on the address bus from the MPU accesses location 00FF in RAM. In a similar fashion, memory assignments are made to ROM U1 (7800 to 7FFF), ROM U4 (7000 to 77FF), and ROM U7 (6800 to 6FFF).

8-234. The address lines are decoded by device decoding circuitry on A14. In some instances, further decoding occurs at a particular device (for example, on the A13 Counter assembly). The MPU treats an external device just like a memory location. To pass information between the registers of the MPU and the registers of an external device (such as the count registers on the A13 Counter assembly), the program writes or reads data from (or to) the location associated with the device. Address decoding circuitry decodes the address output from the MPU and generates a strobe which enables the register on the device. For example, to read data from the AI keyboard, LKBRD goes low which enables the three-state bus driver A1U12 to drive the data bus and send keyboard information back to the MPU. The address location assigned to reading the keyboard is 0010. When 0010 is output by the MPU, address decoding causes U20(7) to go low. Since only one device can drive the data bus at a time, all other device code outputs are high (so that the device buffers on these devices are in the high Z state). To see how 0010 causes U20(7) to go low, consider that the inverted address lines at the output of inverter buffers U16, U18, U8 will be:



Since A0, A1, and A2 are all high, these inputs to U20 will cause 7 to be decoded and U20 (7) to go low provided that the control inputs U20(4) and U20(5) are both low. U20(5) goes low when the inputs to U22D are both high (VMA high and 02 high). U20(4) is low when U17 decodes the address output by the MPU and the address in the range of 0010 to 0017. U17(11) is low when U17(14) is high and U17(13) is low, provided that the control input U17(15) is low. Since inverted A3 is high and inverted A4 is low, the U17(11) output will be low provided that U17(15) is low. U17(15) is low provided that U13A(2) and U13A(1) are both low. U13A(1) is low since inverted A5 is high, Inverted A15, A14, A13, A12, A11, A10 all high is decoded by U9A, U9B, and U13C. A9 is also high. Thus U14 is enabled. Since inverted A8, A7, A6 are all high, the decoded 7 output U14(7) goes low. In summary, U14(7) goes low only when inverted A15, A14, A13, A12, A11, A10, A9, A8, A7, A6 are all high. Inverted A5 high, A4 low, A3 high is decoded by U17B. Inverted A2, A1, and A0 all high is decoded by U20.

8-235. The eight bidirectional data bus lines coming out of U21 pass through an eight-section switch, S1, which allows each line in the data bus to be opened for troubleshooting purposes. Resistor pack R6, with individual pull-up resistors connected to the data lines, together with two lines connected to ground via CR2 and CR3 (these lines connected to ground only when LFRERUN is ground by switch S2), cause a CLB (clear accumulator B) instruction to be presented to the MPU when the switch S1 is opened and LFRERUN is grounded. This causes the MPU to continuously increment the addresses on the address bus from the least significant address (0000) to the most significant address (FFFF) for diagnostic purposes when using the 5004A Signature

Analyzer. LFRERUN grounded forces the Clear B instruction and also causes U15E(10) to go low which disables RAM U12. With S1 opened, feedback is broken between the ROM outputs and the MPU inputs which is a necessary condition for taking signatures with the HP 5004A Signature Analyzer. If LXROM (Low External ROM) is grounded, the ROM's U1, U4, and U7 will be disabled by U6A(1) going low and the address lines can now be used to drive external memory residing in the upper 32K of the memory map.

8-236. The power up reset circuitry formed by Schmitt trigger U11A, U11B, and inverter U15F provides a low reset pulse to the MPU reset input U21(40) and a LDVRST output to the A2 Display Driver to blank the display during power-up. The length of the low reset is determined by the time constant of resistors R5, R3, and capacitor C5 (400 milliseconds).

8-237. Deleted

8-238. The eight data lines, after passing through switch S1, pass through bidirectional inverting line drivers U3, U2. When data is being written out to the external devices (or to RAM), U21(34) goes low which causes U12(16) to go low and U3(15), U2(15) to go high (and U3(1), U2(1) low) thereby enabling the drivers which write to external devices. When data is being read from external devices (or RAM), U21(34) goes high which causes U12(6) to go high and U3(1), U2(1) to go low (and U3(15), U2(15) high). This enables the drivers in U2, U3, which read data from external devices.

8-239. The memory assignments are summarized in Figure 8-75. Ordinarily, when power on, the MPU executes the instructions in FFFF and FFFE. Since the A14 MPU assembly has the A15 address line configured as "don't care", the MPU in the HP5342A executes 7FFF and 7FFE after the power on reset.

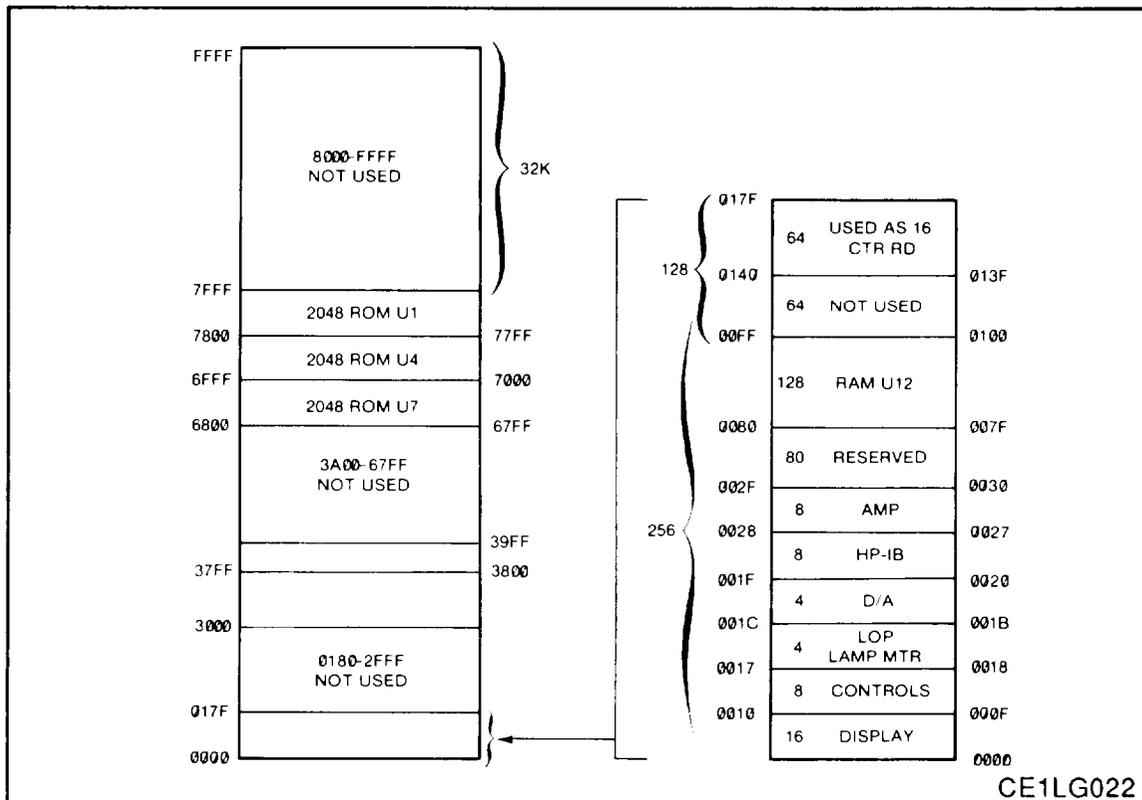


Figure 8-15. Memory Arrangement

8-240. A15 HP-IB ASSEMBLY

8-241. The A15 HP-IB assembly is described in paragraph 8-346.

8-242. Deleted

8-243. Deleted

8-244. A17 TIMING GENERATOR ASSEMBLY

8-245. The A17 Timing Generator shown in Figure 8-41 has the following functions: during acquisition, it generates the pseudorandom sequence used to switch the A5 Multiplexer and the A13 counters for N determination; after acquisition, it generates gate times for the measurement of the IF on A13; between measurements, its sample rate circuitry determines when to begin a new measurement.

8-246. The DO through D5 data lines from the microprocessor data bus transmit data from the microprocessor to the hex D-type register U19 when the LTIM WRT signal (decoded on A14) goes low. LTIM WRT returning high clocks the data into the register. The data lines also transmit data back to the microprocessor from hex three-state driver U18 which drives the data bus when LTIMRD (decoded on A14) goes low.

8-247. Pseudorandom Sequence Generation

8-248. During acquisition, after a countable signal has been detected and the sweep stopped, the N number must be computed. By measuring the IF₁ frequency which occurs when the Nth harmonic of the main VCO mixes with the unknown frequency and then measuring the IF₂ that occurs when the Nth harmonic of the offset VCO mixes with the unknown, the harmonic number N can be determined. N equals $(IF_1 - IF_2) / 500$ kHz where 500 kHz is the precise frequency difference between the main VCO and the offset VCO. To speed the process of determining N, two counters (on A13) are used, counter A and counter B. To prevent coherence between FM on the unknown signal and the switching rate between counters from causing an incorrect computation of N, the switching between counter A and B (which is synchronous with the switching in AS between the main VCO and the offset VCO) is done in a pseudorandom fashion. Two different sequence lengths are possible: 1) the normal or short pseudorandom sequence (prs) which lasts for a total time of 360.4 milliseconds (counter A and counter B are open for 163.83 ms each — there's -32.8 ms of "dead" time). This short prs gives a worst case FM tolerance of 20 MHz peak-to-peak; or 2) the long prs, which is selected by a rear panel switch, lasts for a total time of 2,096 seconds (counter A and counter B are open for 524 ms each in addition to 1.048 seconds of "dead" time). This long prs gives FM tolerance of 50 MHz peak-to-peak.

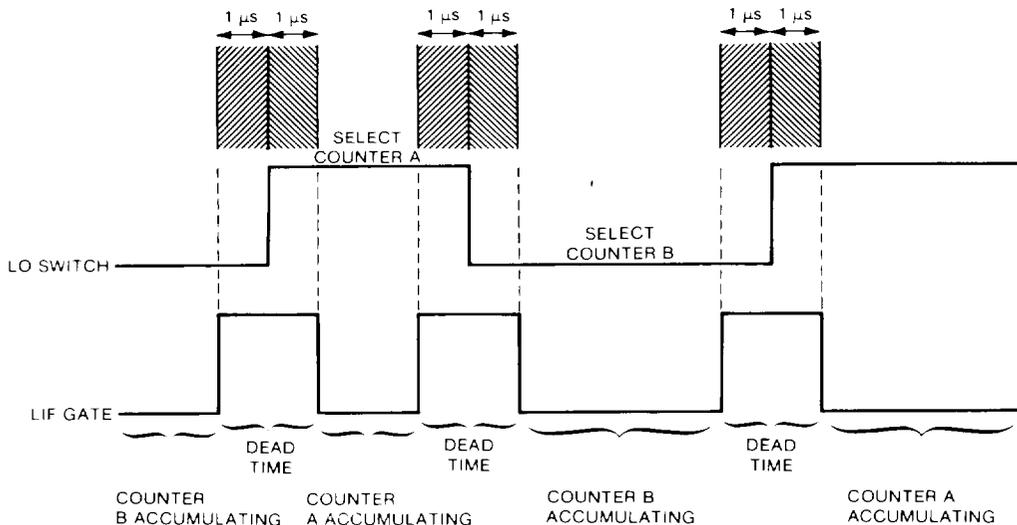
8-249. To begin the pseudorandom sequence, the microprocessor writes to A17 and sets U19(15) high (prs enable), U19(12) low (gate time disable), U19(7) high (for 1 MHz prs clock), and U19(5) high for the long prs or sets U19(2) high for the normal prs. For the short prs, a 100 kHz prs clock is used and U19(7) is low. Decade divider U11 divides down the 1 MHz input to 100 kHz which appears at U10(8). For the long prs, a 1 MHz prs clock is used and U19(7) is high. Since U11(1,3) are both high, the counter is preset to 9 so that U11(9,8) are both high which enables U10. Thus the 1 MHz input appears at U10(8) and becomes the prs clock.

8-250. The prs generator consists of shift registers U7, U4, U5, 4-bit counters U2, U1, and logic gates U6, U3. When U19(15) (prs enable) goes high, the output of U14(11) goes high which releases the reset signal from all the components of the prs generator and starts the sequence. To generate the sequence, data is shifted through the shift register formed by U5, U4, and U7. Feedback taps exclusively "OR" two of the shift register outputs to generate the next input. This feedback generates the prs. For the short prs, U3B(4) is high and U6A is used to perform the exclusive "OR" function (the output of U7(6) is not used for the short prs). For the long prs, U3A(1) is high and U6B performs the exclusive "OR". The data is then fed back to the input of the shift register at U5(1, 2) via inverter U3C.

8-251. The short prs is 15 bits long and stops after 14 consecutive highs in the sequence are detected. The long prs is 20 bits long and stops after 19 consecutive highs in the sequence are detected. The detection of the number of consecutive highs in the sequence is performed by pre-settable counters U2 and U1. For the short prs, "1" is preset into U2(least significant counter) and "15" is preset into U1 (most significant counter) by a low level on U2(9) and U1(9). When a high appears in the sequence, the U2 counter is incremented by the prs clock at U2(2). When a low appears in the sequence, U2 and U1 are reset to the initial preset conditions and counting up begins again. After 14 consecutive highs in the prs, U2 has counted to "15" and the carry output U2(15) has enabled U1 so that the 14th clock causes the carry output U1(15) to go high. This causes U8A(3) to go low which resets the latch formed by U14A and U14B so that U14D(11) goes low to reset U7, U4, U5, U2, and U1.

8-252. For the long prs, operation is similar: this time "12" is preset in U2 and "14" is preset into U1 so that after 19 consecutive 1's in the prs, the carry out of U1 sets U14A(3) low so that U14D(11) is low and clears the prs generator.

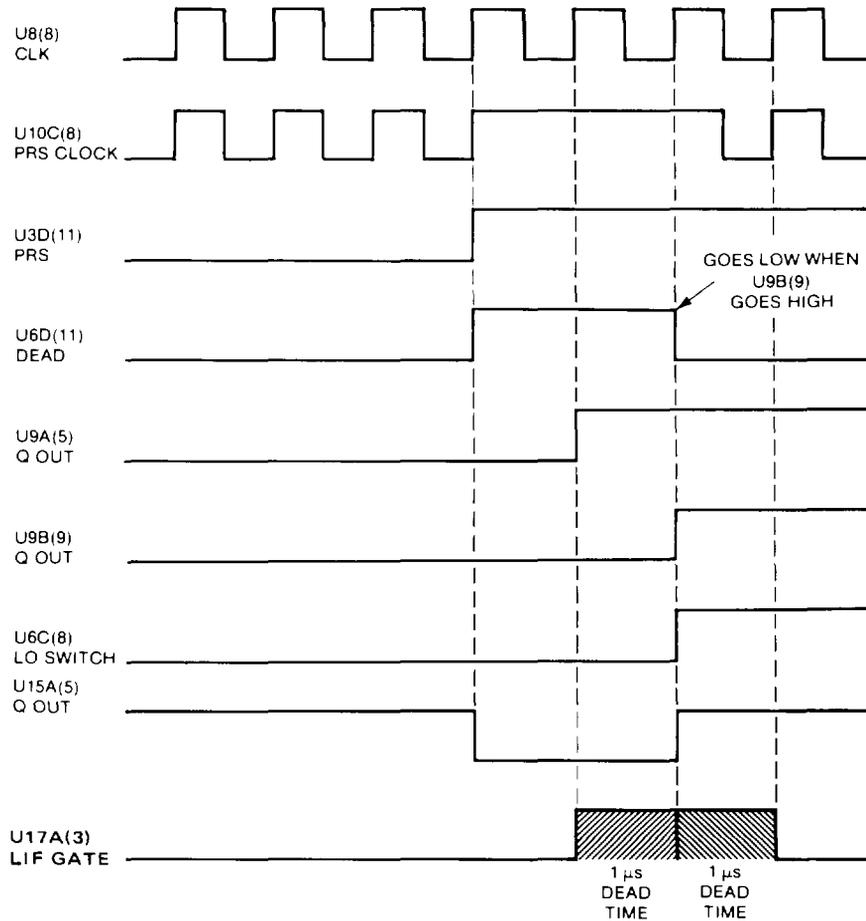
8-253. To allow sufficient settling time for the multiplexer on A5 after switching, 2 microseconds of dead time are added to each transition in the sequence which means that the transitions of the LIF GATE signal (which enables counter A or counter B on A13) are delayed with respect to the LO Switch signal which switches the A5 multiplexer and switches between counter A and counter B on A13 as shown below:



8-254. The dead time in the LIF GATE signal is generated by D flip-flops U9A, U9B, exclusive "OR" U6D, and D flip-flop U15A. The dead time is generated when U6D(11) goes high for two periods of the 1 MHz clock. With U6D(11), high, U10B is disabled and the prs clock at U10C(8) remains high. The reset input to U15A(1) is low during the prs generation so that U15A(5) is low. When the preset input U15A(4) goes low also, the output goes high for the time that the preset

signal is high (both Q and \bar{Q} outputs go high when preset and clear inputs are both low). When U6D(11) goes high to disable the prs clock for 1 μ s, U15A(5) goes low for 2 μ s. The low is presented to U17A(7) and on the next clock at U17A(6), the low at U17A(7) is clocked into the output so that LIF GATE goes low to enable counting on A13.

8-255. The following timing diagram for the long prs generation (prs clock = 1 MHz) will help clarify the operation:



8-256. When the prs is over, U14D(11) goes low. When the A17 board is read by the microprocessor, LTIM RD goes low and three-state drivers U18 are enabled. If the prs is over, U18(5) is low and the program detects this, causing the next program segment to be executed.

8-257. Gate Time Generation

8-258. Gate times for measuring the IF signal after acquisition and N determination are generated by time base generator U16, D flip-flops U15 and U17. To generate gate times from 10 μ s to 1-second, the microprocessor writes to A17 to set U19(21) (gate time enable) high, U19(10) (sets LO SWITCH to high which selects counter A and the main loop VCO) high, U19(15) low (prs disabled), and a 3-bit resolution code on U19(7, 5, 2) which selects the division factor of the decade dividers in U16.

8-259. For gate time generation, divider U11 divides the 1 MHz clock input to 100 kHz. Since U14(8) is high, the 100 kHz passes through gate U12D to U16(3). The 100 kHz signal at U16(3) will be divided by a factor of 10^3 to 10^5 , depending upon the resolution code at U16(14,13,12) and will appear at the output U16(1):

U16(14)	U16(13)	U16(12)	U16(1)
1	0	1	1 Hz
0	0	1	10 Hz
0	1	1	100 Hz
0	1	0	1 kHz
1	0	0	10 kHz
0	0	0	100 kHz

8-260. Since U15B(8) is high, the low to high transition at U15(3) clocks a high into U15A(5). U15A(6) low then presets U15B(8) low so that after one period of the divided U16 output, a low is clocked into U15A(5). After passing through a TTL to ECL level shifter, the gate signal is clocked into the high-speed ECL D flip-flop U17A and U17B. U17A and U17B act as the main gate flip-flop for the counter. U17A is used for measurements in the 0.5—18 GHz range and U17B for direct measurements below 500 MHz.

8-261. U15A(6) goes low when the gate time has expired and this is sent to three-state driver U18A(2). When LTIM RD goes low, U18A(3) low indicates to the microprocessor that the gate time is over and that the program may advance to the next operation.

8-262. Sample Rate Generation

8-263. The sample rate rundown is initiated by writing a low into U19(2) followed by writing a high into U19(2). During the time that U19(2) is low, C16 is charged toward +5 volts through the saturated transistor Q2. The voltage at the base of Q1 is sufficient to turn on Q1, which generates a TTL high at U18C(6). With U19(2) high, the charge on C16 is discharged through R16 and the 1 M Ω SAMPLE RATE pot R9 on A2 until the voltage at the base of Q1 turns off the transistor, thus producing a TTL low at U18C(6). The microprocessor reads this data and upon detecting the low, advances to the beginning of the measurement algorithm. For infinite sample rate the SAMPLE RATE pot is adjusted to 1 M Ω position so that the leakage through R16 and the SAMPLE RATE pot is less than the charging current flowing through R19.

8-264. U18E, U18F, and U20 are not currently used but are reserved for future use.

8-265. The LFM signal at XA17 ($\overline{12}$) will be low if the rear panel FM switch is on. This will cause bit D3 to be low when the MPU reads the timing generator and tells the program to set the FM light on the front panel as well as select the long prs.

8-266. A18 TIME BASE BUFFER ASSEMBLY

8-267. The A18 Time Base Buffer assembly shown in Figure 8-42, provides logic to select a 10 MHz signal from either the internal 10 MHz standard (A24) or from a 10 MHz external standard applied to the 5342A rear panel. A rear panel switch generates an LEXT signal which, when TTL low, disables gate U5C (and hence the internal 10 MHz) and enables gate U5A which allows the external standard to pass through gate U5B. The output of U5B also drives emitter follower Q1 to provide the 10 MHz reference signal for the FREQ STD OUT on the rear panel.

8-268. The 10 MHz output of U5B is divided by 10 in U3 to provide a 1 MHz output to A12 IF Detector and to the prs generator on A17 Timing Generator, Dividers U2 and U1 divide-by-20 to provide a 500 kHz output to the phase detector on A7 Mixer/Search Control assembly and to the divide-by-10 circuit on A10 Divide-by-N assembly.

8-268a. To allow the 10 MHz reference signal to be present at the FREQ STD OUT whenever the 5342A is connected to line voltage, +8 volts generated on the A21 Switch Drive assembly, is applied to the input of U6, a +5 volt regulator. The +8 volts from A21 is present at all times provided the 5342A is connected to the line voltage. The position of the STBY/ON switch does not affect this supply.

8-269. A19, A20, A21 POWER SUPPLY

8-270. The power supply used in the 5342A is a high efficiency switching regulator which is made up of the A19 Primary Power Assembly, the A20 Secondary Power Assembly, and the A21 Switch Drive Assembly. The ac line voltage is directly rectified on A19. Consequently, A19 is isolated from the rest of the instrument and care must be exercised when voltage measurements are made on A19. A19 measurements should be made by supplying power to the 5342A via an isolation transformer.

8-271. SIMPLIFIED BLOCK DIAGRAM. Figure 8-16 is a simplified block diagram of the 5342A power supply. As shown in the diagram, the supply consists of six major elements: an input rectifier-filter, a pair of push-pull switching transistors (A19Q1, Q2), an RF transformer (A20T1), output rectifiers and associated linear voltage regulators, a pulse width control feedback network, and current limiting circuitry.

8-272. VOLTAGE REGULATION LOOP. Regulation is accomplished primarily by switching transistors Q1 and Q2 under control of a feedback network consisting of the A21U4 20 kHz oscillator/pulse width modulator, and the switch drive transformers on A19. The schematic diagram is shown in Figure 8-43. If the 5V (D) output (digital supply) voltage attempts to decrease, the +5V sense signal drops which causes an error signal (difference between +5V sense and +5V reference set by A21R17) to drive a pulse width modulator (part of U4) and increase the pulse width of the 20 kHz outputs of A21U4. Conversely, for an increase in the voltage of +5V (D), the pulse width of the A21U4 outputs decrease. The net result of controlling the pulse width of the 20 kHz output is to control the duty cycle of the output waveforms of Q1, Q2, and hence the duty cycle of the rectangular waveform delivered to the LC filter in the +5V (D) output. The LC filter averages this rectangular waveform to produce a dc output level which is proportional to the duty cycle of the input waveform.

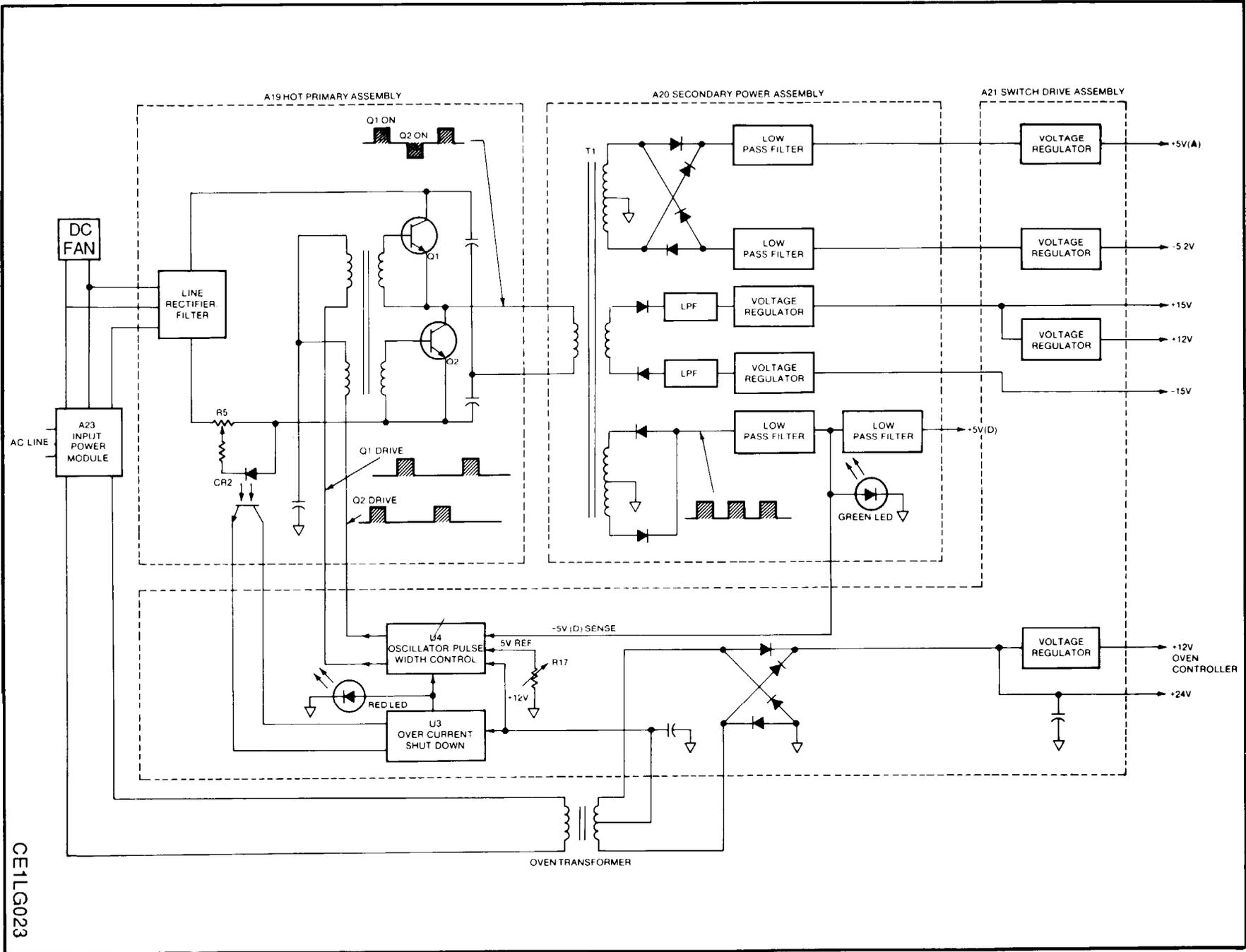
8-273. The feedback provided by the +5V (D) sense signal establishes a controlled input to the primary of A20T1. Other taps on the secondary of A20T1 are rectified, filtered, and delivered to individual linear voltage regulators to provide +5V (A) output (analog supply), -5.2V, +15V, -15V, and +12V.

8-274. The oven transformer output is rectified and filtered to provide power to the control circuits U3, U4 on A21 and oven power when the Option 001 oven oscillator is installed. These oven transformer voltages are available whenever the 5342A is plugged into the line voltage, regardless of the position of front panel power switch.

8-275. CURRENT LIMITING. Total current load is sensed by resistor A19R5 and a signal is sent, via optical isolator CR2, to the A21U3 Timer which acts as an overcurrent shutdown circuit. When excessive current is drawn, the output of U3 turns off the 20 kHz oscillator on U4 for approximately 2 seconds.

8-276. For output voltages other than the +5V (D) output, excessive current may or may not cause A21U4 to turn off since the current limiting circuitry built into the individual linear regulator may shutdown the output before the U3 Timer has time to shutdown the 20 kHz oscillator in U4.

Figure 8-16. A19, A20, and A21 Power Supply Block Diagram



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8-277. When the hold-off output of U3 is TTL high, the 20 kHz oscillator on U4 is disabled. This high level causes a red LED to light which indicates overcurrent shutdown. When this occurs, the green LED on A20 turns off, indicating the absence of +5V (D).

8-277a. The following circuits are driven from the unregulated +27 volts derived from oven transformer T4, CR2, and filter capacitor C15. This +27 volts is available anytime the 5342A is connected to the line voltage. Thus the following circuits are always operating. This is to power the assemblies that provide the FREQ STD OUT signal.

- The +12V regulator, Q7, is driven from the unregulated +27 volts. This is to provide +12 volts for the A24 Oscillator Amplifier circuits.
- A +8 volt supply is generated by components Q14, R34, and CR6 from the unregulated +27 volts, This is to supply the AI 8 Time Base Buffer assembly.
- A +24 volt regulator circuit consisting of Q16, Q17, Q18, CR7, and associated components is derived from the unregulated +27 volts. This is to supply the A24 Oscillator Oven circuits.

8-278. A22 MOTHERBOARD

8-279. The A22 Motherboard contains the XA (Assembly No.) connectors for the plug-in printed circuit assemblies (cards) and provides interconnections between the cards. The motherboard also contains terminals and connectors for interconnection of assemblies to the front and rear panels.

8-280. A23 POWER MODULE

8-281. The A23 Power Module is mounted on the rear panel of the 5342A and contains a connector for a power cable, a fuse and a pc card. The pc card can be inserted in any one of four positions to select 100-,120-,200-, or 240-volt ac operation. The schematic diagram of the power module is shown in Figure 8-43.

8-282. A24 OSCILLATOR ASSEMBLY

8-283. The A24 board contains an oven-controlled crystal oscillator that results in higher accuracy and longer time periods between calibration. Refer to the specifications listed in Table 1-1. Complete repair information consisting of adjustment, principles of operation, and troubleshooting procedures are provided in Appendix C of this manual.

8-284. A25 PREAMPLIFIER

8-285. The A25 Preamplifier Assembly shown in Figure 8-45, combines the two outputs from the sampling diodes in the U1 Sampler and provides approximately 42 dB gain for the sampler output. This gain remains approximately flat out to 125 MHz and rolls off by 8 to 10 dB at 175 MHz. This roll-off for frequencies above 125 MHz prevents interference between the difference frequency produced by the desired Nth harmonic of the VCO mixing with the unknown and the difference frequency produced by the (N±1) harmonic of the VCO mixing with the unknown. Refer to paragraph 8-105 for a detailed description of sensitivity.

8-286. A level detecting diode (CR1) detects RF level and is used to indicate overload to the microprocessor.

8-287. The two sampler outputs are combined in C5 and C9 at the input and are passed to the first stage of amplification. High frequency transistor Q22 and its associated circuitry provide approximately 10 dB gain. Resistors R6 and R7 provide negative feedback to stabilize Q2's operating point. Emitter resistors R14 and R13 are low inductance strip resistors and also provide negative feedback for gain stabilization. The amplified output of Q2 is coupled through dc blocking capacitor C7 to a similar stage of amplification built around Q1. The output of this second stage is approximately 24 dB greater than the input from the sampler and is coupled through C8 to a 3 dB pad, consisting of R9, R17, and R16, which provides a well defined driving impedance for all subsequent filter and amplifier stages. The signal then passes through an elliptic function filter consisting of L3, L4, L6, C10, L5, L7, and C11. This filter reduces the 500 MHz bandwidth of the first two stages to something less than 175 MHz. Variable capacitor C11 is adjusted to provide the required roll-off at 175 MHz. Differential pair U1 provides approximately 14 dB gain.

8-288. The output of U1 passes through a 200 MHz low-pass filter whose major purpose is to filter out the fundamental sampling frequencies of the main oscillator and offset oscillator which appear in the output of the sampler. Differential pair U2 provides another 14 dB gain and the output is coupled through capacitor C26 to the A11 IF Limiter Assembly.

8-289. Diode CR1 rectifies the output of the 175 MHz elliptic filter and provides an output which is proportional to the amplitude of the RF input signal. This level is fed to voltage comparator U3, which, due to the positive feedback provided by R33, has hysteresis and operates like a Schmitt trigger. When the dc level from the detecting diode CR1 rises above the level at U3(2), set by "OFST" potentiometer R31, the output of U3 goes TTL high which causes U4(3) to go low. This output, called LOVL, is sent to the A12 IF Detector where it is buffered and read by the microprocessor. If LOVL is low, then the microprocessor sends dashes to the counter display. Potentiometer R31 is adjusted so that LOVL goes low when the RF into the counter exceeds about +5 dBm. When U4A(3) goes low due to the RF input level exceeding +5 dBm, the RS latch formed by U4B and U4D is set so that U4B(6) is TTL high. This causes U4C(8) to go low which turns off transistor Q4. With Q4 turned off, the voltage at the base of Q5 goes to +15 volts and Q5 is turned off. The current source formed by Q6, R41, R39, CR5, and R40 is always on.

8-290. A26 SAMPLER DRIVER ASSEMBLY

8-291. The A26 Sampler Driver shown in Figure 8-46 converts the LO FREQ sine wave signal into a negative spike waveform at the same frequency as the LO FREQ signal input. The spike goes from +0.7V dc to about -8V dc with a slew rate of approximately 8 picoseconds/volt. This fast transition is used to turn on the sampling diodes in the sampler for a few picosecond and is necessary in order to produce useable harmonics of the VCO frequency up beyond 18 GHz.

8-292. The input frequency, in the range of 300 to 350 MHz, is applied to a common collector amplifier formed by one-half of transistor pair U1 (ac coupling for the LO FREQ signal is provided on the A5 RF Multiplexer). The output is taken off the emitter of the 1st transistor, through R5, and is applied to the common emitter formed by the other half of U1. Matching network R1, L1, C3, L3, L2, C1 is used to match the output impedance of U1 to the step recovery diode CR1.

8-293. AGC is provided by coupling part of the U1 output through CR5 to detecting diode CR2. The detected dc voltage which appears across C10 is used to cause transistor Q1 to conduct more or less current, thereby changing the gain through the first transistor in U1. The gain is changed in such a fashion as to cause the A26 output at the SMA connector A26J1 to have little change in amplitude for variations in input signal amplitude. The output is sent to U1 Sampler.

8-294 through 8-345. Deleted.

Figures 8-17 and 8-18. Deleted

8-346. HEWLETT-PACKARD INTERFACE BUS (HP-IB)

8-347. Introduction

8-348. The A15 HP-IB Assembly serves as an interface between the microprocessor on A14 and the device controlling the lines of the HP interface bus as shown in Figure 8-38. The A15 HP-IB consists of seven interface registers (which are used by the microprocessor for interpreting commands and data, sending status, sending data, interpreting interrupts, etc.), two command decoding ROM's, source handshake circuitry, and acceptor handshake circuitry.

8-349. Interface Registers

8-350. There are seven interface registers on A15 which are used by the A14 microprocessor to communicate with the device controlling the HP interface bus. A register is selected by the microprocessor when the microprocessor sends that particular register's address. This address is decoded by 1-of-8 decoder U11. Decoder U11 is enabled by the LHPIB signal (decoded from address lines on A14) and the phase 2 clock, $\phi 2$, also from A14. A particular register is selected by decoding the two-least-significant address lines of the microprocessor, LA0 and LA1, in addition to the read/write line, LR/HW also from A14. The following table shows which register is selected for each combination of the three inputs to U11, provided U11 is enabled by LHPIB and $\phi 2$.

U11(3) (LR/HW)	U11(2) (LA1)	U11(1) (LA0)	U11 OUTPUT GOES LOW	ENABLES REGISTER
0	0	0	U11(15)	U30 STATE IN
0	0	1	U11(14)	U15 COMMAND IN
0	1	0	U11(13)	U18 INTERRUPT IN
0	1	1	U11(12)	U27 DATA IN
1	0	0	U11(11)	— —
1	0	1	U11(10)	U16 CONTROL OUT
1	1	0	U11(9)	U24 STATUS OUT
1	1	1	U11(8)	U21 DATA OUT

8-351. State in buffer U30 is read by the microprocessor when the microprocessor wants to determine the state of the interface. Listen flip-flop U20B, talk flip-flop U20A, serial poll mode flip-flop U29B, remote flip-flop U29A, and service request flip-flop U9A are all buffered by U30. Buffer U30 is enabled by U11(15) going low.

8-352. Command In register U15 is read by the microprocessor whenever an addressed command is sent by the controller.

8-353. Interrupt In buffer U18 is read by the microprocessor in response to an interrupt. The output of the interrupt buffer indicates why the A15 assembly generated the interrupt (LIRQ low).

8-354. Data In register U27 stores programming codes which have been sent over the HP-IB by the controller. Data In register U27 is clocked by decoding ROM U23(5) which sets Data flip-flop U19A. After one byte of ASCII program data has been clocked into U27, an interrupt is generated by A15 and the microprocessor reads the U18 Interrupt In buffer to find out why the interrupt was generated. Since U18(2) is high, the microprocessor knows that program data is ready to be read from U27. The microprocessor then reads U27. If the byte completes a code (for example, the "5" of the code "SR5"), the microprocessor executes the code and then continues executing the operating program. If the byte does not complete a code, the microprocessor waits until the completed code has been sent.

8-355. Control Out register U16 is used by the microprocessor to control the HP-IB board. For example, in response to a front panel reset, the microprocessor returns A15 to local control by setting U16(10) low then high, which resets the remote flip-flop U29B. On power up, U16(2) is set low then high which resets Serial Poll FF U29B, Talk FF U20A, and Listen FF U20B. When measurement data is sent to the HP-IB, the microprocessor sets U16(12) low which sets the EOI control line of the HP-IB low after the final byte of the data message is sent (i.e., after CR, LF).

8-356. Status Out register U24 is used by the microprocessor to send a status byte when the serial poll mode is ordered by the system controller. The microprocessor sends octal 120 (01010000) to indicate that it has pulled on SRQ (bit 7) and that a measurement has been completed (bit 5).

8-357. Data Out register U21 is used by the microprocessor to output measurement data, one byte at a time, to the HP-IB. U21 is clocked by the Address Decoder U11 and is enabled by Serial Poll FF U29B being set low (not serial poll mode).

8-358. Command Decoding ROM's

8-359. Decoding ROM's U23 and U26 decode bytes sent over the data lines of the HP-IB. The acceptor handshake operates when LATN is low (address information is being sent) or when the Listen flip-flop has been set. Decoding ROM U23 is enabled only during the acceptor handshake cycle. The outputs of the ROM's generate interrupts, set or reset various control flags, and are read by the microprocessor via Command in register U15.

8-360. During the acceptor handshake, U1C(8) goes low for one period of the $\phi 2$ clock just prior to the HDAC signal going high, thus enabling U23 (U26 is always enabled). The byte on the data lines of the HP-IB appears at the inputs to U23 and U26. The ROM outputs change accordingly.

8-361. If the Unlisten command is given, U26(1) goes low and U23(2) goes high to clock Unlisten FF U20B, causing it to be reset. If a talk address other than the 5342A's talk address is sent, U23(1) goes high to clock into the U20A Talk FF the output of Address Comparator U33. Since the 5342A's talk address was not sent, U33(14) is low and the U20A Talk FF is set low. If the 5342A's listen address is sent, U23(2) goes high to clock a high from U33(14) into Listen flip-flop U20B.

8-362. Now that the 5342A is addressed to listen, consider what occurs when program data is sent. When program data appears at the inputs to ROM's U23 and U26, output U23(5) goes low to set the Data flip-flop, U19A. When U23(5) returns high, Data In register U27 is clocked and the data byte is stored in U27. At the same time that U23(5) goes low, U23(6) goes low which resets Interrupt flip-flop U14A and causes LIRQ (the output of U17B) to go low and interrupt the microprocessor. The microprocessor reads Interrupt In buffer U18 (which clears interrupt FF

U14A), determines that program data is in U27, and reads U27. When U27 is read (U27(1) goes low), the U19A Data flip-flop is reset in preparation for the next byte.

8-363. Consider what occurs when an addressed command or universal command is sent by the controller. If a command is sent, U23(4) goes low which sets Command flip-flop U14B. When U23(4) returns high, it clocks into Command In register U15 the decoded outputs from U26 as follows:

Command	U26(4)	U26(5)	U26(6)	U20(9)	
LLO (Local lockout)	0	0	0	1	Universal
DCL (device clear)	1	0	0	1	Commands
GTL (go to local)	0	0	1	0	
SDC (selected device clear)	1	0	1	0	Addressed
GET (group execute trigger)	0	1	1	0	Commands

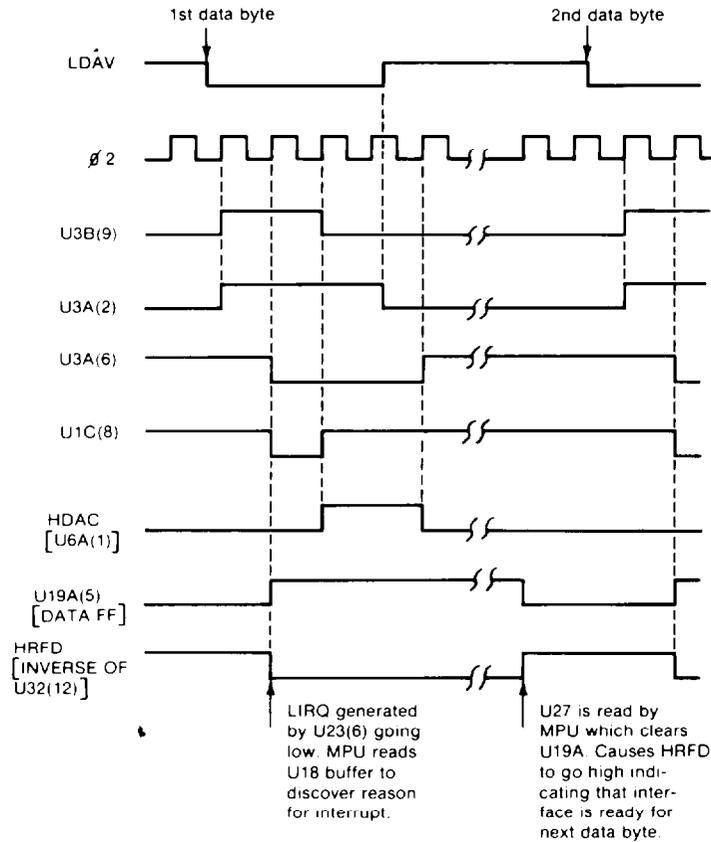
8-364. At the same time that U23(4) goes low, U23(6) goes low. This sets Interrupt flip-flop U14A and causes LIRQ to go low, which interrupts the microprocessor. The microprocessor reads Interrupt In buffer U18, determines that a command code is in U15, and reads U15, The microprocessor determines which command was sent according to the table and acts accordingly.

8-365. When the serial poll enable signal is sent, U26(2) goes high and U23(3) goes high to clock Serial poll flip-flop U29B to the high state. When the serial poll disable signal is sent, U26(3) goes low and U23(3) goes high to clock U29B to the low state.

8-366. Acceptor Handshake

8-367. The acceptor handshake is enabled by U1B(4) low (LATN control line of bus is low, indicating address information is being sent) or U1B(5) low (the 5342A has been addressed to listen). When the talking device puts data on the HP-IB data bus and pulls LDAH low indicating data valid, the acceptor handshake causes HDAC to go high (indicating that the data has been read into U27). After the data in U27 has been read by the microprocessor, the acceptor handshake causes HRFD to go high, indicating that U27 has been read by the MPU and that the MPU is ready to receive the next data byte.

8-368. A timing diagram of a typical acceptor handshake is shown below. The talker places a data byte on the eight data lines and, after allowing for settling, pulls LDAH low to indicate to the listener (5342A in this case) that there is valid data on the data bus. The first positive transition of the ϕ_2 clock after LDAH goes low, clocks a high into flip-flop U3B(9). This causes the input to U3A(2) to go high. On the next clock, U3A(5) goes high and U3A(6) goes low. U3A(5) high and U3B(9) high cause U1C(8) to go low which enables ROM U23. When ROM U23 is enabled, Data flip-flop U19A(5) is set high which causes U32(12) to go high (HRFD goes low) and also clocks the data into U27. Simultaneously, LIRQ goes low to interrupt the microprocessor. The next ϕ_2 clock causes U3B(9) to return low, thus disabling U23. Since U3B(9) is low and U3A(6) is low, HDAC goes high, indicating to the talking device that the data has been accepted (read into U27) and maybe removed from the data lines. The talker then removes the data from the bus and takes LDAH high to indicate that there is not valid data on the bus. U3A(2) goes low when LDAH goes high. On the next positive transition of ϕ_2 , the low at the input to U3A is clocked into the output, causing U3A(5) to go low and U3A(6) to go high. This causes HDAC to return low. After the microprocessor reads the Interrupt In register U18 and determines that data is stored in U27, the U27 Data In register is read by the MPU. This causes the U19A data flag to be reset and also causes HRFD to go high, indicating that the Data In register has been read and is ready for another data byte. The handshake process then repeats as described.

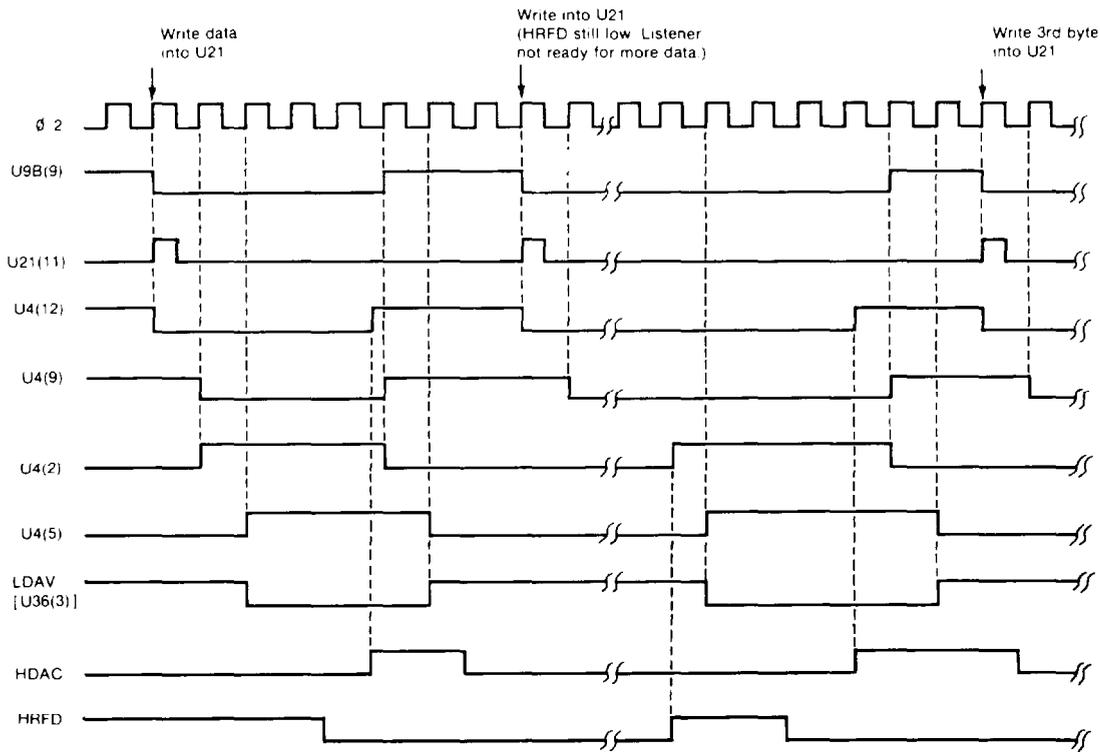


8-369. Source Handshake

8-370. The source handshake controls the LDÁV control line of the HP-IB in response to the state of the HDAC and HRFD control lines which are controlled by the acceptor handshake circuitry in the listening device. When the 5342A operating program finishes a measurement, the microprocessor reads State In buffer U30 to see if the counter has been addressed to talk. if the counter has been addressed to talk, the microprocessor reads Interrupt In buffer U18 to determine the state of Data Out flip-flop U9B. If U9B(9) is high, then the previous data byte has been accepted by the listener and a new data byte maybe written into Data Out register U21. When a data byte is written into U21, U9B(9) is reset low and the source handshake logic sets LDÁV low, two ø2 periods later. When the listener sets HDAC high, U9B(9) goes high on the next positive transition of the ø2 clock. Since the listener has accepted the data, a new data byte is written into U21. However, LDÁV will not go low again until the listener sets HRFD high to indicate that it is ready for more data. Data Out register U21 is always enabled if the Serial Poll FF U29 is set low. The output data bus drivers, U22, U25, U31, and the source handshake circuits however, are only enabled in talk mode and LATN set high.

8-371. A timing diagram of a typical source handshake is shown below. Since U9B(9) is high, the microprocessor clocks data into U21. This clock also resets U9B(9) low. U9B(9) going low causes the input to flip-flop U4B to go low, and U4B'S output goes low on the next ø2 clock positive transition. Since U4(9) is low and HRFD is high, the input to flip-flop U4A(2) goes high and the U4(5) output goes high on the next clock. When U4(5) goes high, LDÁV at U36(3) goes low. Sometimes later the listener set HDAC high to indicate that the data has been accepted. HDAC going high causes the U4(12) flip-flop input to go high and the U4(9) output goes high on the next clock pulse. Since U4(9) is high and U4(5) is high, U12(6) goes high and sets the Data Ready flip-flop U9(9) to high. When U9B(9) goes high, U4(2) input goes low and causes the U4(5) flip-flop output to go low on the next clock. This causes LDÁV to return high. After LDÁV goes high, the listener reset HDAC low in preparation for the next handshake cycle. Since

U9B(9) is high, the microprocessor writes the second data byte into U21. U21(11) going high resets U9B(9) to a low which sets the U4B(9) flip-flop output low. However, the source handshake logic can not indicate the presence of the second data byte (by pulling LDAV low) until the listener sets HRFD high. When HRFD finally does go high, the output of flip-flop U4(5) goes high on the first clock after HRFD goes high. U4(5) going high sets LDAV low. When the listener senses LDAV low, it sets HRFD low and the process continues as previously described.



8-372. ASSEMBLY LOCATIONS

8-373. Figures 8-79, 8-20, 8-27 and 8-22 shows the front (A1 Display Assembly) rear, top and bottom views, respectively, of the 5342A. The front and rear views show reference designators of the front and rear panel controls, connectors, and indicators. The top view shows assembly locations and adjustments.

8-374. TROUBLESHOOTING TO THE ASSEMBLY LEVEL

8-375. Troubleshooting Technique

8-376. In the troubleshooting procedure outlined in Table 8-5, the 5342A is exercised through a series of operating modes which are arranged in an increasing order of complexity. As can be seen in Table 8-6, an increasing number of assemblies is exercised as the operating modes progress from the first mode (power-up diagnostic) to the last mode (AUTO/1 GHz). By noting the first mode in the sequence that fails, it is possible to isolate the defective assembly to a specific group of assemblies by noting those assemblies common to the current (failed) test and all previous tests (which passed). These common assemblies can be eliminated as being the source of the failure and only those assemblies which are not common to previous operating modes are examined. Table 8-7 is a list of the noncommon assemblies for each of the operating modes and it is the basis for the troubleshooting procedure presented in Table 8-5.

8-377. Tables 8-9 through 8-27 are individual troubleshooting procedures for various assemblies and assembly groups and are referenced in the overall troubleshooting of Table 8-5. By using the diagnostic modes of the 5342A, explained in Table 8-8, and the test equipment listed in Table 1-4, the troubleshooting procedure outlined in Table 8-5 and Tables 8-9 through 8-27 allows isolation of a failed assembly. By reading the detailed theory of operation of the assembly and referencing the dc voltages and 5004A signatures provided on the individual schematics, it should be possible to find the failed components.

8-378. Figure 8-23 is a detailed description block diagram of the 5342A and is valuable in troubleshooting. Figure 8-9 shows the relationship of the assemblies listed in Table 8-6.

8-379. RECOMMENDED TEST EQUIPMENT

8-380. Test equipment recommended for troubleshooting, adjustments, operational verification, and full performance testing is listed in Table 1-4. Equipment other than that listed may be used if it meets the required characteristics.

Table 8-5. Overall Troubleshooting

1. **POWER UP DIAGNOSTIC** — Apply power to the 5342A and press front panel power switch to ON. The power-up diagnostic routine progressively lights all LED segments in the 5342A display, from left to right. Finally, the following should be displayed briefly:

If the 5342A powered up properly, go to step 2. If not:

- a. If E's fill the display, then RAM A14U12 failed the check sum routine exercised on power up. A14U12 may be faulty if none of the address lines A0—A15 or data lines D0—D7 are stuck low or high. Check address lines and data lines on A14 for stuck nodes (use current tracer such as 547A to find faulty device). Stuck data lines may be caused by stuck ROM outputs (U1, U4, U7) or stuck buffer inputs (U2, U3). If 1 is displayed, then ROM A14U7 failed the check sum routine exercised on power up. Since the RAM proved good (E's were not displayed), the data lines and address lines be OK. Replace A14U7.
 - 1) If 2 is displayed, then ROM A14U4 failed the check sum routine exercised on power up. Replace A14U4.
 - 2) If 3 is displayed, then ROM A14U1 failed the check sum routine exercised on power up. Replace A14U1.
 - 3) Deleted
 - 4) Deleted
- b. Check for the clock on A14. If the clock is not present, check A24, A18, A17U8.
- c. Go to Table 8-9 for A14 testing.
- d. Go to Table 8-10 for power supply troubleshooting.
- e. Go to Table 8-11 for A1, A2 testing.

Table 8-5. Overall Troubleshooting (Continued)

- TABLE 8-5
OVERALL**
2. **DIAGNOSTIC MODE 8** — Put the 5342A in diagnostic mode 8 (see *Table 8-8* for a description of diagnostic modes and how to set them). Perform the keyboard check, paragraph 3-43. If the 5342A operates properly, go to step 3. If not:
 - a. Go to *Table 8-11* for A1, A2 testing. If the 5342A passed the power-up diagnostic test but failed the diagnostic mode 8 test, then likely problems on A1, A2 are failed A1 keyboard or failed A2 keyboard decoding circuitry such as A2U22, U12, U18, U19, etc.
 - b. Go to *Table 8-9* for A14 testing. The difference between this test and the previous test is that the LKBRD device select is sent by A14.
 3. **DIRECT COUNT MODE** — Apply the 10 MHz FREQ STD OUT from the rear panel of the 5342A to the direct count input (front panel BNC). Place the impedance select switch in 50 Ω position and place the range switch in the 10 Hz—500 MHz position. If the counter counts 10 MHz \pm 1 count for all resolution settings, go to step 4. If not:
 - a. Check the A3 Direct Count Amplifier (*Table 8-12*).
 - b. Check the A14 Microprocessor as described in *Table 8-9*. A difference between this test and previous tests is that LCTRRD, LCTRWRT, TMRD, LTMWRT device select codes are used.
 - c. Check the A13 counter (*Table 8-13*). Only the A counter is used in this mode.
 - d. Check the A17 timing generator (*Table 8-14*). Only the gate time generation circuitry is used in this mode.
 4. **CHECK MODE** — Place the 5342A in CHECK (place range switch in 500 MHz—18GHz position) and verify that the counter displays 75 MHz \pm 1 count for all resolution settings. If the counter operates properly, go to step 5. If not:
 - a. Go to *Table 8-9* for A14 Microprocessor testing. A difference between this test and previous tests is that LSYNHI, LSYNLO, LPDREAD, LPDWRT device select codes are used.
 - b. Check that the 500 kHz output of A18, available at XA18(3), is present.
 - c. Go to *Table 8-15* for A8, A9, A10 Main Loop Synthesizer troubleshooting.
 - d. Go to *Table 8-16* for IF troubleshooting. Since the check signal enters the IF chain at A11(7,7) the A25 Preamp and the U1 Sampler can be eliminated as possible failed modules.
 5. **AUTO/50 MHz MODE** — Place the 5342A in AUTO mode, with the range switch in the 500 MHz—18 GHz position and apply a 50 MHz signal at -10 dBm to the high frequency input. Verify that the counter counts 50 MHz \pm 1 count for all resolution settings. If the 5342A operates properly, go to step 6. If not:
 - a. Place the 5342A in diagnostic mode 0. If the counter displays SP or SP2 only (instead of SP23 followed by Hd), then the failure is likely in the U1 Sampler or A25 Preamp since A11 and A12 are used in the CHECK mode. Go to IF troubleshooting in *Table 8-16*.
 - b. If the counter (still in diagnostic mode 0) displays SP23 but does not display Hd, suspect A17 PRS generation circuitry. Go to *Table 8-74* for A17 Troubleshooting.
 - c. If the counter displays an incorrect answer, go to diagnostic mode 4 to verify that the IF measured is 50 MHz. If it is not, check the A counter on A13 (*Table 8-13*). Also go to diagnostic mode 1 to check the N number computed, If N is not 0, check the B counter on A13 (*Table 8-13*).

Table 8-5. Overall Troubleshooting (Continued)

6. AUTO/1 GHz MODE — Place the 5342A in AUTO mode, with the range switch in the 500 MHz—18 GHz position and apply a 1 GHz signal at -25 dBm to the high frequency input. Verify that the counter counts 1 GHz ± 1 count for all resolution settings.
 - a. Place the 5342A in diagnostic mode 0. If the counter displays SP (instead of SP23 followed by Hal), then the failure is likely to be in the A26 Sampler Driver since the other components in the IF were exercised in step 5. Go to Table 8-18 for A26 Sampler Driver troubleshooting.
 - b. Check U1 Sampler per Table 8-16, step b.
7. Deleted
8. HP-IB MODE — Perform the HP-IB Performance Verification as outlined in paragraphs 4-19 through 4-26 of the manual. If the 5342A fails the performance verification program, refer to Table 8-21, HP-IB Troubleshooting.

Table 8-6. Assemblies Tested by Test Mode

ASSEMBLIES	POWER-UP DIAG.	TEST MODES							TROUBLE - SHOOTING TABLE NO.
		SET 8 DIAG.	DIRECT COUNT	CHECK	AUTO 50 MHz	AUTO 1 GHz	AMPL	HP-IB	
A1 Keyboard Display	✓ (1)	✓	✓	✓	✓	✓	✓		Table 8-11
A2 Display Driver	✓ (2)	✓	✓	✓	✓	✓	✓		Table 8-11
A3 Direct Count Amp			✓				✓		Table 8-12
A4 Offset VCO						✓	✓		Table 8-17
A5 RF Multiplexer						✓	✓		Table 8-19
A6 Offset Loop Amp						✓	✓		Table 8-17
A7 Mixer/Search Control						✓	✓		Table 8-17
A8 Main VCO				✓		✓	✓	✓	Table 8-15
A9 Main Loop Amp				✓		✓	✓	✓	Table 8-15
A10 Divide-by-N				✓		✓	✓	✓	Table 8-15
A11 IF Limiter				✓	✓	✓	✓	✓	Table 8-16
A12 IF Detector				✓	✓	✓	✓	✓	Table 8-16
A13 Counter			✓ (7)	✓ (7)	✓	✓		✓ (7)	Table 8-13
A14 Processor	✓ (3)	✓ (6)	✓ (8)	✓	✓	✓		✓	Table 8-9
A15 HP-IB								✓	Table 8-21
A17 Time Base Generator	✓ (4)	✓ (4)	✓ (9)	✓ (9)	✓	✓	✓	✓ (9)	Table 8-14
A18 Time Base Buffer	✓ (5)	✓ (5)	✓ (5)	✓	✓	✓	✓	✓	Table 8-5
A19 Primary Power	✓	✓	✓	✓	✓	✓	✓	✓	Table 8-10
A20 Secondary Power	✓	✓	✓	✓	✓	✓	✓	✓	Table 8-10
A21 Switch Drive	✓	✓	✓	✓	✓	✓	✓	✓	Table 8-10
A24 Oscillator	✓	✓	✓	✓	✓	✓	✓	✓	Table 8-5 Appendix C
A25 Preamplifier					✓	✓	✓		Table 8-16
A26 Sampler Driver						✓	✓		Table 8-16
U1 Sampler					✓ (10)	✓	✓		Table 8-16

- NOTES:
- (1) Keyboard not exercised
 - (2) Keyboard decoding circuitry such as A2U22,U12,U18,U19 not exercised.
 - (3) HDSPWRT select code is only device select code exercised
 - (4) A17U8 only is exercised, send 1 MHZ clock to A14
 - (5) 1 MHZ output only is used
 - (6) HDSPWRT, LKBRD select codes are only device select codes exercised.
 - (7) B counter not exercised
 - (8) LPDREAD, LPDWRT, LYSYNHI, LYSYNLO device select codes not exercised.
 - (9) PRS generation circuitry not exercised
 - (10) Tests only that atm least one of the two diodes is not open.

Table 8-7. Probable Failed Assemblies by Test Mode

POWER-UP DIAG.	TEST MODES				
	SET 8 DIAG.	DIRECT COUNT	CHECK	AUTO 50 MHz	AUTO 1 GHz
A1	A1(1)	A3	A8	A17(9)	A4
A2	A2(2)	A13(4)	A9	A25	A5
A14	A14(3)	A14(5)	A10	U1	A6
A17		A17(6)	A11	A13(10)	A7
A18			A12		A26
A19			A14(7)		U1
A20			A18(8)		
A21					
A24					

**TABLES 8-6 & 8-7
ASSEMBLIES**

NOTES:

- (1) A1 Keyboard
- (2) A2 keyboard decoding circuitry such as A2U22,U12,U18,U19
- (3) A14 LKBRD device select code
- (4) A counter
- (5) A14 LCTRRD, LCTRVRT, LTIMRD, LTIMWRT device select codes
- (6) A17 gate time generation
- (7) A14 LYSYNHI,LISYNLO, LPDREAD, LPDWRT device select codes
- (8) A18 500 kHz output.
- (9) A17 prs generation.
- (10) A13 B counter exercised

Table 8-8. Diagnostic Modes of the 5342A

To go to a diagnostic mode, press front panel set key twice (SET, SET) and then the number corresponding to the desired mode. For example, pressing SET SET 8 goes into diagnostic mode 8, the keyboard check. To leave a diagnostic mode, press RESET . The following describes the available diagnostic modes:

**TABLE 8-8
DIAGNOSTIC MODES**

DIAGNOSTIC MODE	FUNCTION
0	Displays mnemonics SP 23 followed by Hd. SP indicates that the VCO'S are sweeping. 2 indicates that the unlatched power detector is set, indicating an IF of sufficient amplitude and an IF in the range of 50—100 MHz. 3 indicates that there is a proper IF for both the Main VCO and OFFSET VCO. 3 is displayed after the VCO'S have stopped sweeping. Hd indicates harmonic determination has been complete. It is displayed at the end of the prs.
1	Counter displays Main OSC in MHz to 100 kHz, sign of IF (+ for subtract and - for add) and the harmonic number N. For example: <div style="text-align: center;"> <p>IF is added</p> <p>VCO = 344.2 MHz N = 10.99 (rounded to 11)</p> <p style="text-align: center;">344.2 - 099</p> <p style="text-align: center;">MHz kHz Hz</p> </div> <p>This is displayed at the end of the harmonic determination. (The (-) sign of the IF indicates that the Nth harmonic of the VCO is less than the unknown so that the IF must be added; the (+) sign of the IF indicates that the Nth harmonic of the VCO is greater than the unknown so that the IF must be subtracted.)</p>
2	Counter continuously displays the contents of the A counter during harmonic determination.
3	Counter continuously displays the contents of the B counter during the harmonic determination.
4	Counter continuously displays the measured IF frequency. Resolution determined by resolution selected before going to diagnostic mode 4.
5	Deleted
6	Deleted
7	is not switching Sweeps Main VCO from 350 MHz to 300 MHz in 100 kHz steps. Time between updates in VCO frequency determined by SAMPLE RATE setting. To stay at a particular frequency, put SAMPLE RATE to HOLD. (Remove input signal to counter, place counter in 500 MHz—18 GHz range and AUTO mode.)
8	Keyboard check. Refer to paragraph 3-43 for complete list of what should be displayed when each key is pressed.

To return to normal operation, press RESET

Table 8-9. A14 Microprocessor Troubleshooting

- Place the A14 Microprocessor Assembly on the extender board, P/N 05342-60036 which is shown below. Place the 5004A START and STOP probes on the B(4) test pin of the A14 extender board. (Or, place on AP clip on U8 of A14 and place the START probe and the STOP probe of a 5004A Signature Analyzer on A14U8(2), which is the most significant address line out of the U21 microprocessor (A15).) Place the CLOCK probe of the 5004A on the VMA ϕ_2 test point located in the upper righthand corner of A14. Place the GROUND probe of the 5004A on the ground test point of A14.

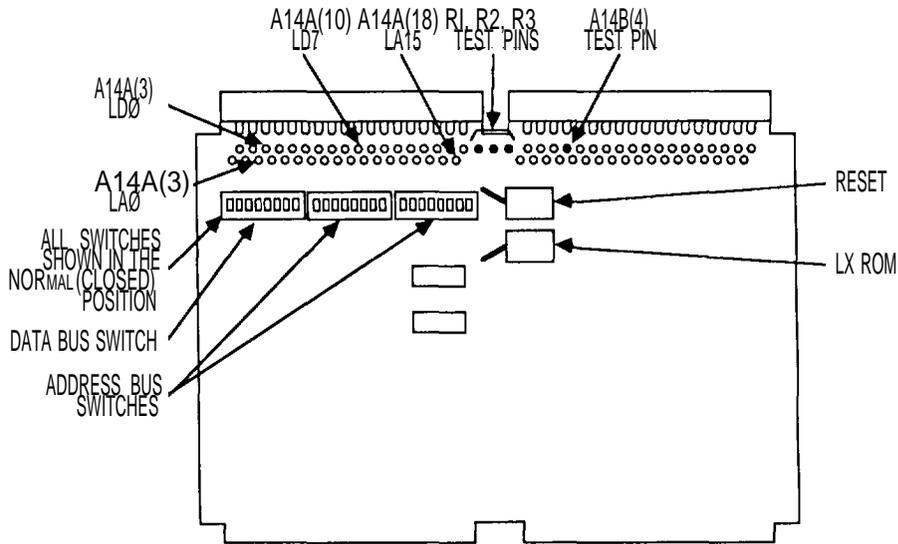


TABLE 8-9
A14

- Set the 5004A for positive slope on START, STOP, and CLOCK (all pushbuttons of the 5004A should be out). Apply power to the 5342A.
- Place the 5342A in free-run mode by moving A14 switch S2A to the up position and all S1 switches down (opens up data bus lines back into MPU U21). Ensure that the LX ROM switch on the A14 extender board is in the up position. Press the RESET switch on the A14 extender board.

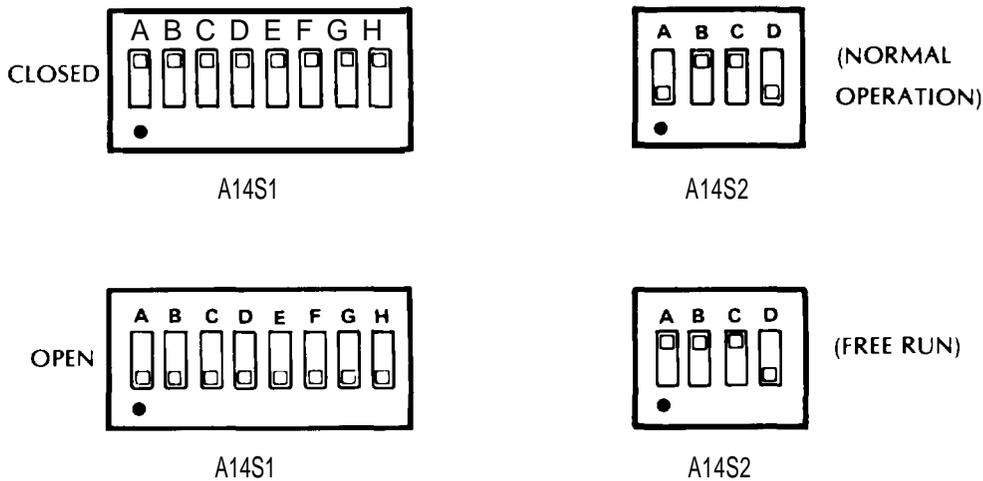
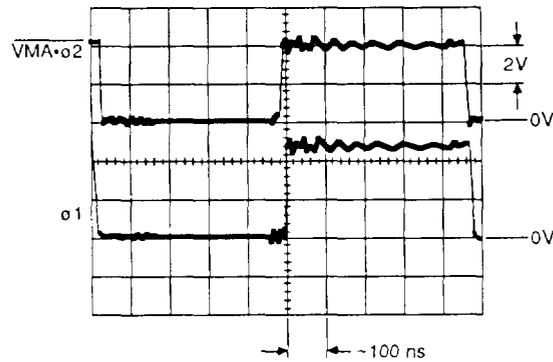


Table 8-9. A14 Microprocessor Troubleshooting (Continued)

4. Place the 5004A data probe on +5V and verify that the characteristic "I's" signature displayed on the 5004A is 0003. If 0003 is not displayed, then the U21 microprocessor is not free-running. If 0003 is displayed when the 5004A data probe is placed on +5V, go to step 5.
 - a. Check the clock inputs to the microprocessor by looking at the $\phi 1$ (phase 1) clock test point on A14 and the VMA $\phi 2$ test point. These signals should be as in the following oscilloscope photos.
 If these signals are not present, troubleshoot the clock generation circuitry U19, U22, U24, etc., on A14.
 - b. If these signals are present, check diodes CR2, CR3, and switches A14S1 and S2. If these parts are good, then the U21 MPU is suspect.
 - c. With switches S1 and S2 set for freerun, check for correct inputs, as listed below:
 RESET U21(40) - High, NMI U21(6) - High, HALT U21(2) - High,
 IRQ U21(4) - High, 3-State U21(39) - Low control



*Time base of scope out of CAL in order to get one complete period in photo.

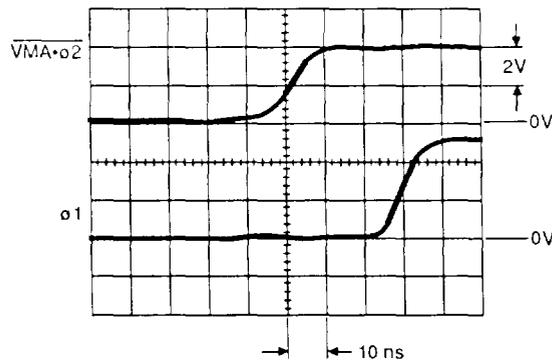
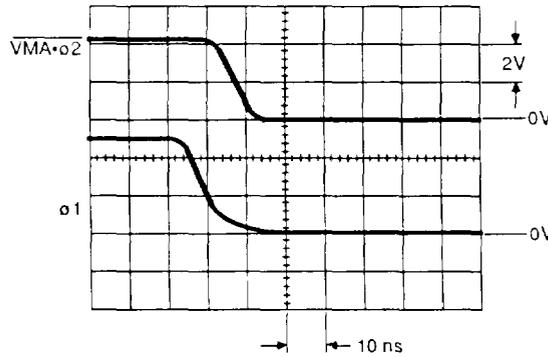


TABLE 8-9
A14

Table 8-9. A14 Microprocessor Troubleshooting (Continued)

5. Place the 5004A data probe on the following address signal points (available on the A14extender board) and check that the proper free-run signatures are obtained:

XA14A(3) . . . UUF	XA14A(11) . . . 7792
XA14A(4) . . . FFFU	XA14A(12) . . . 6322
XA14A(5) . . . 8487	XA14A(13) . . . 37C6
XA14A(6) . . . P760	XA14A(14) . . . 6U2C
XA14A(7) . . . 1U5H	XA14A(15) . . . 4FC9
XA14A(8) . . . 0355	XA14A(16) . . . 486C
XA14A(9) . . . U75A	XA14A(17) . . . 9UP2
XA14A(10) . . . 6F99	XA14A(18) . . . 0001

If these signatures are obtained, go to step 6.

- Check the signatures on the MPU side of buffer/drivers U16, U18, U8. These signatures are adjacent to the A14 schematic. Correct or incorrect signatures should isolate the problem to either U21 or one or more of the buffer/drivers U16, U18, U8.
 - A signature may be incorrect because that particular address line is being held low or high by another assembly which is connected to the address bus. To check this possibility, isolate the A14 address bus from the other assemblies by setting the address bus switches on the A14 extender board all open (low).
6. Place the 5004A data probe on the following device select codes and check that the proper free-run signatures are obtained:

<u>DEVICE SELECT CODE</u>	<u>LOCATION</u>	<u>SIGNATURE</u>
HDSPWRT	U22(8)	U05H
LKBRD	U20(7)	FF48
LTIMRD	U20(9)	7311
LTIMWRT	U20(10)	9FF7
LCTRWRT	U20(11)	A732
LPDRD	U20(12)	A9FU
LPDWRT	U20(13)	6A70
LSYNHI	U20(14)	1A9U
LSYNLO	U20(15)	46A4
LCTRRD	U14(13)	94F1
LHPIB	U17(7)	CC1A
LAMPMTR	U17(6)	1P2A

If these signatures are correct, go to step 7.

- If the signatures are not correct, check the inputs to the IC's with the incorrect signatures. If the inputs are not correct, troubleshoot backwards along the signal flow, from output to input, until a device is found where the input exhibits a correct signature but the output is incorrect. Change that IC.
- If the inputs to U20, U22, U17 have good signatures, then either the IC is bad or the output line is being held high or low by some other assembly connected to that signal. To check this possibility, A14 must be isolated from the rest of the instrument. Perform as follows:
 - Remove A14 assembly and place it near lefthand side of instrument.
 - Connect a clip lead from the +5V test pin on A17 to the +5V test pin on A14.
 - Connect a clip lead from the ground test pin on A17 to the ground test pin on A14.
 - Connect an AP clip to A14U22. Connect a clip lead from test pin TP1 on A17 (1 MHz clock signal) to A14U22(4). The A14 assembly can now be exercised.
 - Connect an AP clip to A14U8. Place the 5004A START and STOP inputs on A14U8(2).

Table 8-9. A 14 Microprocessor Troubleshooting (Continued)

With the 5004A set up and connected as in steps 7d and 7e, take the following signatures;

Signal Name	Location	Signatures (for ROM Combinations listed)		
		A14U1 (P/N 1818-0329) A14U1 (P/N 1818-0330) A14U7 (P/N 1818-0331)	A14U1 (1818-0698) A14U4 (1818-0697) A14U7 (1818-0331)	A14U1 (1818-0698) A14U4 (1818-0697) A14U7 (1818-0706)
D0	U3(9)	1FPC	9141	68A7
D1	U3(12)	2945	6UF0	04F6
D2	U3(4)	127F	CF72	H774
D3	U3(7)	7779	H37F	H37F
D4	U2(12)	5779	3269	3269
D5	U2(9)	163C	5HPU	5HPU
D6	U2(7)	87CH	0653	UUC5
D7	U2(4)	P227	P81H	831C

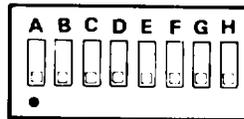
- i. If these signatures are good, suspect buffers U2 and U3. If any of these signatures are bad, then perform the following to isolate the problem to a particular ROM.

U7 ROM Test:

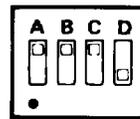
START and STOP of 5004A to R3 test point on A14 extender board
 CLOCK of 5004A to VMA ● Ø2 test point on A14
 START to (-) slope (↘)
 STOP to (+) slope (↗)
 CLOCK to (+) slope (↗)
 GND of data probe to ground

A14S1 and A14S2 switches remain unchanged:

+5V — 826P



A14S1



A14S2

Signal Name	Location	Signatures (for ROM Combinations listed)		
		A14U1 (P/N 1818-0329) A14U1 (P/N 1818-0330) A14U7 (P/N 1818-0331)	A14U1 (1818-0698) A14U4 (1818-0697) A14U7 (1818-0331)	A14U1 (1818-0698) A14U4 (1818-0697) A14U7 (1818-0706)
D0	U7(23)	F3PC	F3PC	HP87
D1	U7(22)	CA11	CA11	CA12
D2	U7(21)	52H7	52H7	52H4
D3	U7(20)	3UP5	3UP5	3UP5
D4	U7(19)	U9H1	U9H1	U9H1
D5	U7(18)	359F	359F	359F
D6	U7(17)	OFUC	OFUC	1197
D7	U7(16)	3PCF	3PCF	3PCU

U4 ROM test — change the START and STOP of the 5004A to the R2 test point on the A14 extender board. All other settings remain unchanged.

+5v — 826P

Table 8-9. A14 Microprocessor Troubleshooting (Continued)

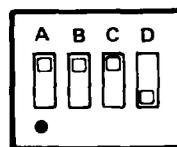
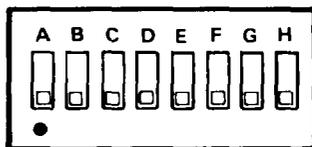
U1 ROM test — change the START and STOP of the 5004A to the R1 test point on the A14 extender board. All other settings remain unchanged:

+5V — 826P

Signal Name	Location	Signatures (for ROM Combinations listed)		
		A14U1 (P/N 1818-0329) A14U4 (P/N 1818-0330) A14U7 (P/N 1818-0331,	A14U1 (1818-0698) A14U4 (1818-0697) A14U7 (1818-0331)	A14U1 (1818-0698) A14U4 (1818-0697) A14U7 (1818-0706)
D0	U4(23)	FAA3	4P63	4P63
D1	U4(22)	9697	6HPH	6HPH
D2	U4(21)	UHU3	UHU3	UHU3
D3	U4(20)	A6A8	2268	2268
D4	U4(19)	196H	5U0A	5U0A
D5	U4(18)	24F6	7UHU	7UHU
D6	U4(17)	A956	1748	1748
D7	U4(16)	92F1	2FHF	2FHF

Signal Name	Location	Signatures (for ROM Combinations listed)		
		A14U1 (P/N 1818-0329) A14U4 (P/N 1818-0330) A14U7 (P/N 1818-0331)	A14U1 (1818-0698) A14U4 (1818-0697) A14U7 (1818-0331)	A14U1 (1818-0698) A14U4 (1818-0697) A14U7 (1818-0706)
D0	U1(23)	6000	AAPC	AAPC
D1	U1(22)	6P3H	A4H6	A4H6
D2	U1(21)	HP60	706P	706P
D3	U1(20)	P686	05F2	05F2
D4	U1(19)	65P0	86A4	86A4
D5	U1(18)	A520	A520	A520
D6	U1(17)	P903	P903	P903
D7	U1(16)	H4UC	H4UC	H4UC

8. To check the read buffers, place A14 in free-run:



- a. Set the LX ROM switch on the A14 extender board to the down position to disable ROM's U1, U4, U7. Ground U19(2) to halt the microprocessor.
- b. With a logic pulser, pulse the read buffer inputs U2(3,6,10,13), U3(3,6,10,13) and verify no output pulse on U2(2,5,11,14) U3(2,5,11,14) outputs with a logic probe. Verify that the read buffer outputs U2(2,5,11,14) U3(2,5,11,14) all indicate an intermediate or high Z state (dim lamp). Place an AP clip on U3 and ground U3(1) to enable the read buffer. Now pulse the U2, U3 inputs with the logic pulser and verify with the logic probe that the U2, U3 outputs pulse.

NOTE

Return A14 switch settings to normal operation (see step 3).

9. It is possible for the MPU (U21) to freerun and still not operate properly. If trouble persists, replace U21.

Table 8-10, A19, A20, A21 Power Supply Troubleshooting

CAUTION

It is extremely dangerous to troubleshoot the A19 assembly of the power supply if an isolation transformer is not used. A19 is connected directly to the power main. Use an isolation transformer such as Allied Electronics P/N 705-0048 (for 120V ac) to isolate the instrument from the power main. The measurements in this troubleshooting procedure may be made only if an isolation transformer is used.

1. Connect 5342A power cord to isolation transformer.
2. The first step in power supply troubleshooting is to check the state of the green LED on A20 and the red LED on A21. If the green LED is on and the red LED is off, then the +5V(D) supply is working properly. If the red LED is on and the green LED is off, then one or more of the voltage outputs of A20, A21 may be drawing excessive current. Even if the green LED is on, one of the regulated outputs of A21 may be shut down due to excessive current. Check the following voltage levels:

TABLE 8-10
A19, A20, A21

SUPPLY	LOCATION	VALUE
-5.2V	XA15B(3)	-5.2(-0.1, +0.05)V*
+5V(D)	XA15B(4)	+5 (±0.1)V
+15V	XA15B(2)	+15 (±0.5)V
-15V	XA15B(1)	-15 (±0.5)V
+5V(A)	XA5(7)	+5 (±0.1)V
+12V oven	XA21(14)	+12 (±0.5)V
+12V	XA21(16, 16)	+12 (±0.5)V

*If this voltage is not correct, adjust A21R17 before making other voltage measurements.

NOTE

If one or more of the voltage outputs is at ground, then a probable cause is that one of the assemblies in the instrument connected to that voltage output has a short to ground. Remove assemblies connected to that voltage output, one at a time, until the short is removed. After removing an assembly, replace it in the instrument if that assembly is not the problem. This must be done because the power supply loses regulation if not run at approximately 75% of full load. The following table shows which assemblies are connected to the various supply voltages:

SUPPLY	FROM	TO
+5V(D)	XA20(18, 18)	A1, A2, A12, A13, A14, A15, A16, A17, A19
-5.2V	XA21(5, 5)	A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A15, A17, A25, A26
+15V	XA21(14)	A4, A6, A7, A8, A9, A10, A11, A12, A13, A15, A17, A25
-15V	XA21(13)	A6, A7, A9, A10, A11, A12, A13, A15, A17, A25
+5V(A)	XA21(1, 1)	A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A18, A25, A26
+12V oven	XA21(14)	A24(8, 8)
+12V	XA21(16, 16)	A24(3)
+24V	XA21(11, 11)	A24(8, 8)

CAUTION

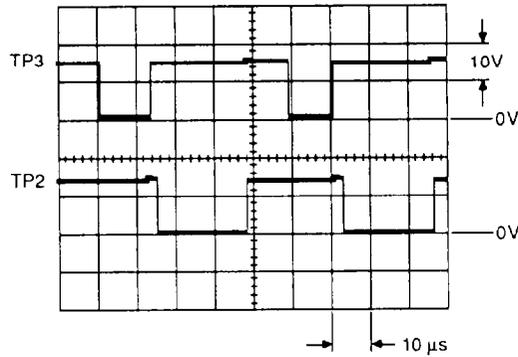
The waveforms in the following paragraph require using an isolation transformer as described in the CAUTION preceding step 1.

Table 8-10, A19, A20, A21 Power Supply Troubleshooting (Continued)

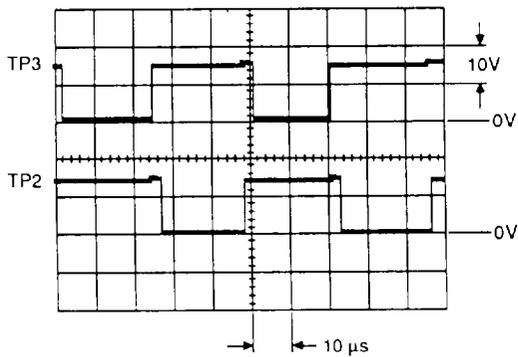
3. A21 Troubleshooting

- a. Pull A19 and A20 from the instrument and put A21 on an extender board. Plug the 5342A to the line but leave the ON/STBY switch in STBY. Measure the voltage at test lead TLS (labeled TLS 13.5V), which is the positive side of A21C20, and verify that this voltage is approximately 13.5 volts. If not, suspect rectifier A21CR2 or oven transformer T4.
- b. With the 5342A still in STBY, monitor test points TP2 and TP3 on A21 with an oscilloscope. Short TPJ and TPG (lower right corner TP on A21) together. Observe the following waveforms:

TABLE 8-10
A19, A20, A21



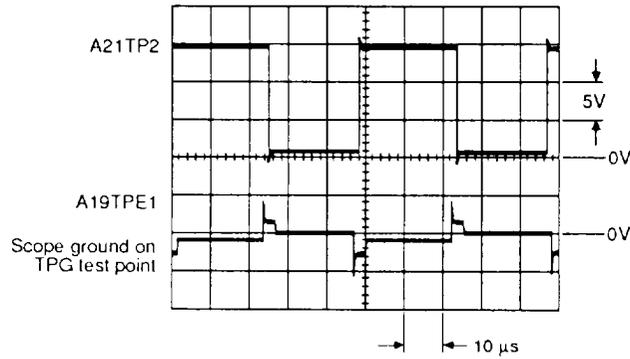
Now remove the short from TPJ to TPG and observe:



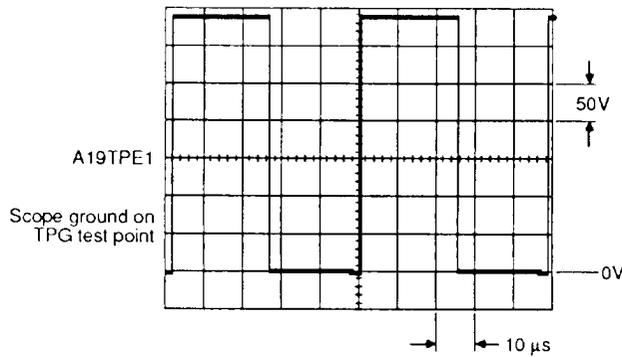
- c. Connect a clip lead to A21TP4 and momentarily ground the other end to the chassis. Observe red LED turn on for approximately 1–2 seconds and waveforms at TP2, TP3 go to a constant +13 volts for same duration. If not, suspect A21U3.

Table 8-10. A19, A20, A21 Power Supply Troubleshooting (Continued)

- With A21 still on extender board (remove short from TPJ to TPG), insert A19 on an extender board into the instrument (A20 is still out of the instrument). Leave the 5342A line switch in STBY. The waveform at A19TP4 indicates that A19 transformers T1 and T2 are operating properly.



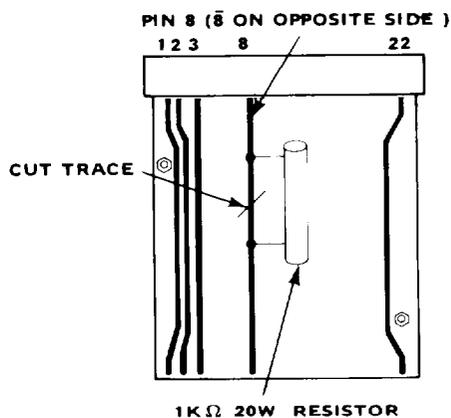
Now switch front panel line switch to ON and observe:



If the above waveform is not present, check the collector of A19Q1 for 300V (with respect to the test point TPG). If 300V dc is not present, suspect input rectifier A19CR1 and associated circuitry. If 300V dc is present, suspect open transistors Q1 and Q2.

Table 8-10. A19, A20, A21 Power Supply Troubleshooting (Continued)

5. Fabricate the following special test extender board shown below. This board is useful because, by placing a 1 K Ω load in series with the A20T1 transformer, the current drawn from transistors A19Q1, Q2 is limited. If A19Q1, Q2 have failed because of excessive current (due to a failure in the A21 overcurrent protection circuitry), then replacing A19Q1, Q2 and using the 1 K Ω load allows the power supply to be checked out without danger of blowing A19Q1, Q2 again.
 - a. Take a 22-pin extender board (such as HP P/N 05342-60034) and cut the traces on pin 8 and $\bar{8}$ as shown below.
 - b. Solder a 1 K Ω , 20W resistor (HP P/N 0819-0006) above and below the cut as shown:



- c. Insert A20 in the above extender board into the instrument. Insert A21 (on standard HP P/N 05342-60034 extender board) into the instrument. Short A21TPJ to TPG (low right test point). Insert A19 on extender into instrument. Monitor A19TP4 with the scope probe ground on A19 TPG test point (emitter of Q2). If an isolation transformer is not used, do NOT make this measurement.

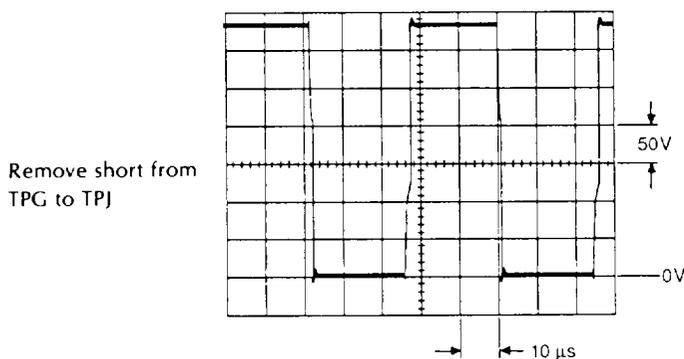
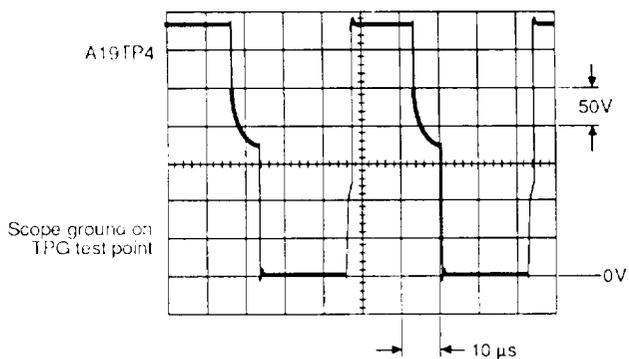
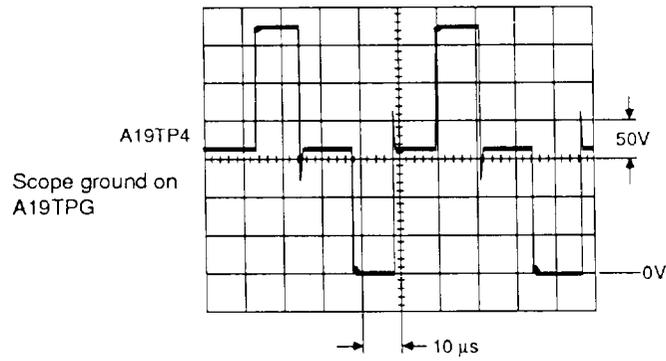


Table 8-10. A19, A20, A21 Power Supply Troubleshooting (continued)

- d. Remove special extender board and remove the short between A21TPJ and TPG. Insert A20 into XA20.



Green LED on A20 should be lit.

- e. Now monitor A19TP5 and observe (adjust A19R1 for -1V on trailing edge):

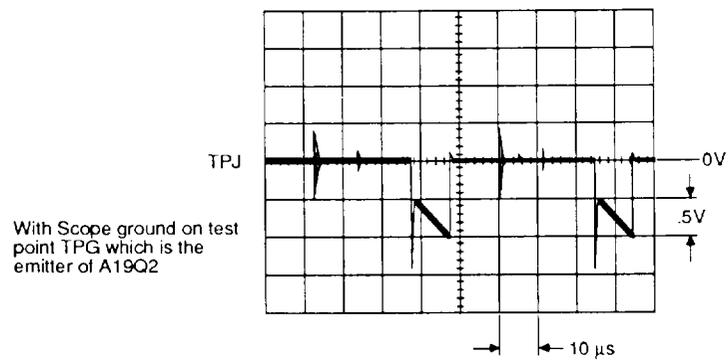
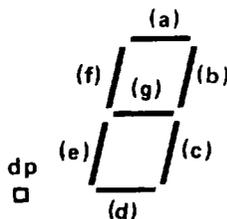


Table 8-11. A1, A2 Keyboard/Display Troubleshooting

1. First verify that HDSPWRT at XA14B(10) pulses high when power is applied to the 5342A by using a logic probe such as the 545A. If not, troubleshoot A14 to obtain an HDSPWRT signal.
2. If HDSPWRT is present on the power up and pulses consistently thereafter but the display/keyboard still does not operate properly, remove the A1, A2 and front panel assembly as follows:
 - a. Remove front panel sample rate knob with allen wrench.
 - b. Remove BNC connector nut and type N connector nut.
 - c. Pull off the two coax cables connected to A1J3 and A1J1.
 - d. Remove the two chassis screws from each side strut holding the front panel to the strut.
 - e. Pull off front panel assembly carefully.
 - f. Remove 5 screws holding A1, A2 to front panel.
 - g. Pull out A1, A2 which are sandwiched together by a center press-on connector.
 - h. Make sure ribbon cable remains connected to A2.
3. Remove A14 from the 5342A chassis. With a clip lead, ground the following pins and observe the display for the following lighted LED segments:
 - a. A2U1(3) all (b) segments and dBm light should light
 A2U1(6) all decimal points and blue key should light
 A2U1(8) all (d) segments, REM light, and MAN key should light
 A2U1(11) all (c) segments, GATE light, and OFS MHz key should light
 - b. A2U4(3) all (g) segments and RECALL key should light
 A2U4(6) all (a) segments and FM light and AMPL key should light
 A2U4(8) all (e) segments and AUTO key should light
 A2U4(11) all (f) segments, SET key and OFS dB key should light



- c. If all segments light as specified, then the LED's A1DS11 through DS21 and the associated transistor drivers on A1 are operating properly. In addition, the scan clock comprised of A2U5, U3, U13, U6, and the column scanners A2U2, U7 are operating properly.
- d. If only one segment in the display lights, troubleshoot the scan clock and column scanners on A2.

TABLE 8-11
A1, A2

Table 8-11. A1, A2, Keyboard/Display Troubleshooting (Continued)

- 4. If the 5342A does not perform the power up diagnostic but A1, A2 properly perform the test described in step 3, the probable cause of the failure is A2U11, U8 (TTL RAM memory), A2U16 (data bus buffer), A2U5, U13 (write enable generation), or U17 (multiplexer).
- 5. If the 5342A performs the power-up diagnostic but does not perform the diagnostic mode 8 keyboard check, the probable cause of the problem is the key decoding circuitry on A2 consisting of U13A, U5C, U18, U19, and U12. To test this circuitry, perform the following tests with A14 still removed from instrument:

- a. Monitor U10(8) with a logic probe and verify that each time a key is depressed, U10(8) goes low. To cause U10(8) to return to high, ground U22(1) momentarily. This verifies that pushing a key generates an interrupt request (LIRQ) and that reading the keyboard (LKBRD) clears the interrupt request.
- b. Place AP clip on U22 and monitor the outputs of latch U22 by grounding U22(1) and verify that when a key is pressed, the latch stores the following data:

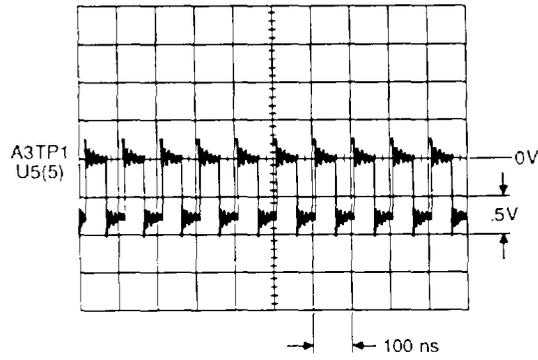
KEY	U22(3)	(4)	(5)	(6)
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
•	0	1	0	1
ENTER	1	1	0	1

- c. Monitor U12(2) and verify that when any of the leftmost grouping of keys (AUTO, MAN, RESET, etc.) is pressed, U12(2) is high and that when any of the rightmost grouping of keys (0, 1, 2, etc.) is pressed, U12(2) is low. This verifies that the top/bottom row decoder U19A is operating properly.
- d. If the A2 assembly passes all the above, then the most probable cause of the problem is the A2U12 bus driver. Another possible cause is that the A14U2 MPU does not respond to the LIRQ signal.

TABLE 8-11
A1, A2

Table 8-12. A3 Direct Count Amplifier Troubleshooting

To check that the direct count amplifier is working, connect the 10 MHz FREQ STD rear panel output to the direct count input (front panel BNC). Place the range switch in the 10 Hz—500 MHz range and the impedance select to 50Ω. Monitor TP1 of A3 for the following waveform (TP1 is the output of Schmitt Trigger U5).



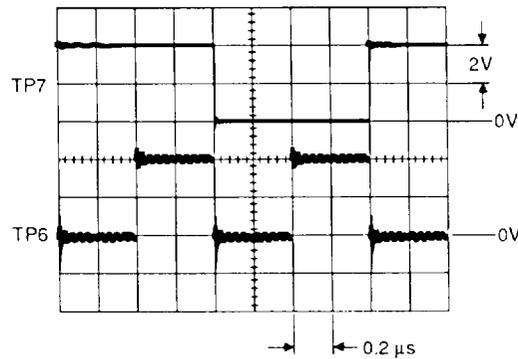
NOTE

Check that the output of A3, DIRECT B available at XA3(1), is divided by four and that DIRECT A available at XA3(2) is divided by two.

Table 8-12
A3

Table 8-13. A13 Counter Troubleshooting

1. Apply approximately 50 MHz signal at -10 dBm to the high frequency input of the 5342A. Put the counter in diagnostic mode 2 (press SET, SET, 2) to read the contents of the A counter. The A counter should read approximately 8,200,000. Put the 5342A in diagnostic mode 3 to read the B counter. It should be the **same** reading as A, ± 1 count (provided the stability of the 50 MHz source is that good). If this is true, then A13 is good. If it is not true, A13 may be at fault (as well as A17 for the prs generation and gate time generation).
2. Check the inputs to the A counter as follows: Apply 10 MHz FREQ STD OUT on rear panel to the direct count input (fron panel BNC) with 50 Ω position selected. Check the following A counter test points (since 10 MHz is divided by four on A3, TP6 which divides A3 output by 2, should have a period of $8 \times 100 \text{ ns} = 800 \text{ ns}$ and TP7, which divides A3 output by four should have a period of $16 \times 100 \text{ ns} = 1.6 \mu\text{s}$):



**TABLE 8-13
A13**

3. Check the inputs to the B counter as follows: Apply a 50 MHz, -10 dBm signal to the high frequency input and select the 500 MHz—18 GHz range. Put the 5342A in AUTO and push RESET to cause the counter to go to the prs generation, thus enabling the B counter. Place the rear panel FM switch to the FM position so that the B counter is enabled for 2.1 seconds.

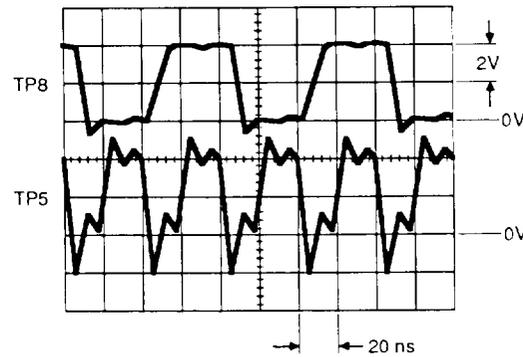
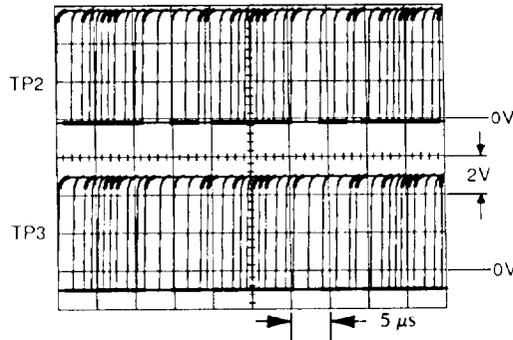
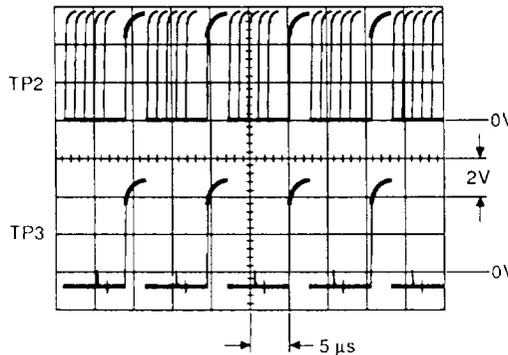


Table 8-13. A13 Counter Troubleshooting (Continued)

4. Test the outputs of U1 and U2 for activity by applying a 50 MHz, -10 dBm signal to the high frequency input. Place the counter in AUTO, 500 MHz—18 GHz range, and diagnostic mode 2 so that the prs is continually generated. Monitor TP2 and TP3 with an oscilloscope. If the signals appears much different than the waveform shown below, one or more of the U3 buffers have probably failed. Use a logic pulser and logic probe to check out the U3, U7 buffers. An HP 1607A Logic State Analyzer may be used to check out the actual data going back to the microprocessor as shown in step 5.



When the counter is not in diagnostic mode 2 but is just measuring the 50 MHz signal, the waveform below shows activity at the A counter (counting the IF) but none at the B counter.



5. 1607A check out of A13
- Put A13 on extender board and put AP clips on A13U3, U5, U8, and U10. Connect the following 1607 data bit lines as follows:

1607 Data Inputs	A13 Connections	Description
Data bit 0	U3(8)	A0 line
1	U3(10)	A1 line
2	U3(12)	A2 line
3	U5(14)	A3 line
4	U5(2)	A4 line
5	U8(1)	A5 line
•GND	U3(7)	GND
6	U8(12)	LCTR RD
7	U5(7)	D0
8	U5(9)	D1
9	U10(7)	D2
10	U10(9)	D3
11	NOT USED	
•GND	U5(8)	GND
CLOCK	VMA • ϕ_2 TP on A14	
•GND	U10(8)	

- Set 1607A to repetitive, Table A, word trigger, delay off and start display. Put bits 15-7 in the OFF (don't care) position. Place the 5342A in CHECK mode and 1 MHz resolution. Select each of the following trigger words (EXAMPLES 1, 2, and 3) and verify the proper 1607A display in the don't card bits of the trigger word.

TABLE 8-13
A13

Example 1: CHECK Mode — 1 MHz Resolution

COMMENTS	OFF DATA BITS SHOULD BE:				TRIGGER WORD (DATA BITS)						
	10	9	8	7	6	5	4	3	2	1	0
*These two bits ignored in CHECK since they represent state of dividers on A3. This reads out least significant counts. In this case we're reading state of divider U12B (bit 9) and divider U16B (bit 10). Count equals 3 in this case.	1	1	*	*	0	1	0	0	0	0	0
Bit 7 = U17(5) output Bit 8 = U17(9) output Bit 9 = U17(2) Bit 10 = U17(12) Count = 8 in this case.	1	0	0	0	0	1	0	1	0	0	0
Bit 7 = U13(5) output Bit 8 = U13(9) output Bit 9 = U13(2) output Bit 10 = U13(12) Count = 1 in this case.	0	0	0	1	0	1	1	0	0	0	0
Bit 7 = U1(15) 10 ⁰ decade Bit 8 = U1(16) 10 ⁰ decade Bit 9 = U1(1) 10 ⁰ decade Bit 10 = U1(2) 10 ⁰ decade Count = 0	0	0	0	0	0	1	1	1	0	0	0
Bit 7 = U1(15) 10 ¹ decade Bit 8 = U1(16) 10 ¹ decade Bit 9 = U1(1) 10 ¹ decade Bit 10 = U1(2) Count = 0	0	0	0	0	0	1	1	1	0	0	1
Bit 7 = U1(15) 10 ² decade Bit 8 = U1(16) 10 ² decade Bit 9 = U1(1) 10 ² decade Bit 10 = U1(2) 10 ² decade Count = 0	0	0	0	0	0	1	1	1	0	1	0
Bit 7 = U1(15) 10 ³ decade Bit 8 = U1(16) 10 ³ decade Bit 9 = U1(1) 10 ³ decade Bit 10 = U1(2) 10 ³ decade Count = 0	0	0	0	0	0	1	1	1	0	1	1
Bit 7 = U1(15) 10 ⁴ decade Bit 8 = U1(16) 10 ⁴ decade Bit 9 = U1(1) 10 ⁴ decade Bit 10 = U1(2) 10 ⁴ decade Count = 0	0	0	0	0	0	1	1	1	1	0	0
Bit 7 = U1(15) 10 ⁵ decade Bit 8 = U1(16) 10 ⁵ decade Bit 9 = U1(1) 10 ⁵ decade Bit 10 = U1(2) 10 ⁵ decade Count = 0	0	0	0	0	0	1	1	1	1	0	1

Total Count = 3+4(8+10) = 75 counts
(Count display 75 MHz)

Multiply all the counts after the 1st by 4 since the input to the decade counters has essentially been prescaled by 4.

Example 2: CHECK Mode — 100 Hz Resolution

COMMENTS	OFF DATA BITS SHOULD BE:				TRIGGER WORD (DATA BITS)						
	10	9	8	7	6	5	4	3	2	1	0
Count = 0	0	0	*	*	0	1	0	0	0	0	0
Count = 0	0	0	0	0	0	1	0	1	0	0	0
Count = 0	0	0	0	0	0	1	1	0	0	0	0
Count = 5	0	1	0	1	0	1	1	1	0	0	0
Count = 7	0	1	1	1	0	1	1	1	0	0	1
Count = 8	1	0	0	0	0	1	1	1	0	1	0
Count = 1	0	0	0	1	0	1	1	1	0	1	1
Count = 0	0	0	0	0	0	1	1	1	1	0	0
Count = 0	0	0	0	0	0	1	1	1	1	0	1

Total Count = 4(187500) + 0 = 750,000 = Display of 75.0000 MHz

Example 3: Apply 10 MHz from EXT FREQ STD OUT to 10 Hz—500 MHz input and select the direct count range with 1 Hz resolution

COMMENTS	OFF DATA BITS SHOULD BE:				TRIGGER WORD (DATA BITS)						
	10	9	8	7	6	5	4	3	2	1	0
Count = 0	0	0	0	0	0	1	0	0	0	0	0
Count = 0	0	0	0	0	0	1	0	1	0	0	0
Count = 0	0	0	0	0	0	1	1	0	0	0	0
Count = 0	0	0	0	0	0	1	1	1	0	0	0
Count = 5	0	1	0	1	0	1	1	1	0	0	1
Count = 2	0	0	1	0	0	1	1	1	0	1	0
Count = 6	0	1	1	0	0	1	1	1	0	1	1
Count = 0	0	0	0	0	0	1	1	1	1	0	0
Count = 0	0	0	0	0	0	1	1	1	1	0	1

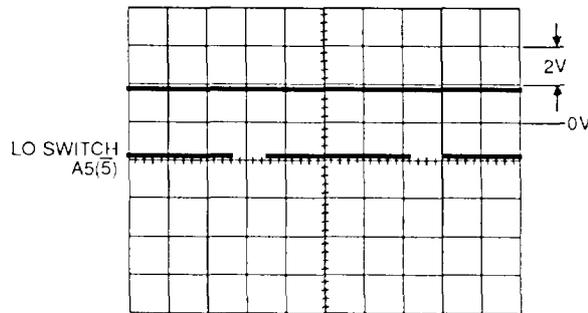
In the direct count mode, because of the divide-by-4 on A3, the output of the decade dividers must be multiplied by 16 instead of 4. So total count is 16 (625,000) + 0 = 10,000,000 and is displayed as 10.000000 MHz.

To check the B counter, the same set-up may be used but Bit 5 in the Trigger word must be a zero. Put the counter in diagnostic mode 3 with a 50 MHz, -10 dBm signal applied to the high frequency input. Observe that a reading of around 8,200,000 is output for 1 Hz resolution.

Table 8-14. A17 Timing Generator Troubleshooting

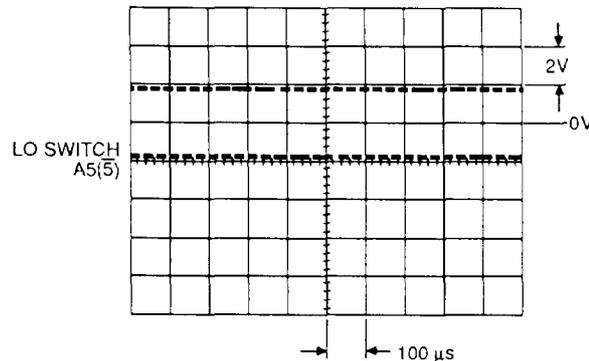
1. The A17 Timing Generator has a number of outputs:
 - a. LO SWITCH at XA17(1) which switches the A5 multiplexer and A13 counters in a pseudorandom sequence after acquisition.
 - b. LDIR GATE at XA17(4) which gates the main gate on A3 for direct count measurements.
 - c. LIF GATE at XA17(5) which gates counter A on A13 for measuring the IF.
 - d. CLOCK at XA17(4) which drives A14.
 - e. When A17 is read by the microprocessor, the D4 line is examined to see if the gate time is over. The D1 line indicates the end of the prs. The D2 line indicates the end of the sample rate run down.

2. LO SWITCH verification. To verify that the LO SWITCH signal is operating properly, the 5342A must be able to acquire so that the counter can be forced into its harmonic determination routine. This means that A25, U1, A11, A12 must be working properly. To check LO SWITCH, apply a 50 MHz signal, -10 dBm, to the high frequency connector and put the 5342A in the 500 MHz—18 GHz range. The LO SWITCH signal at XA5(5) should appear:



The time during which the signal switches between high and low levels in a pseudorandom fashion should be 360 ms. The time where the signal is high and not switching is controlled by the front panel sample rate control and resolution of counter. If the rear panel switch is placed in the FM position, then the time during which the signal is switching should extend to 2.1 seconds (actually 2.096).

A sample of what the sequence looks like is shown below where the sweep speed of the scope has been increased to 100 μs:

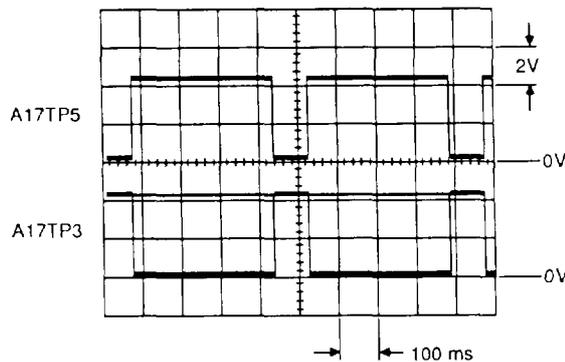
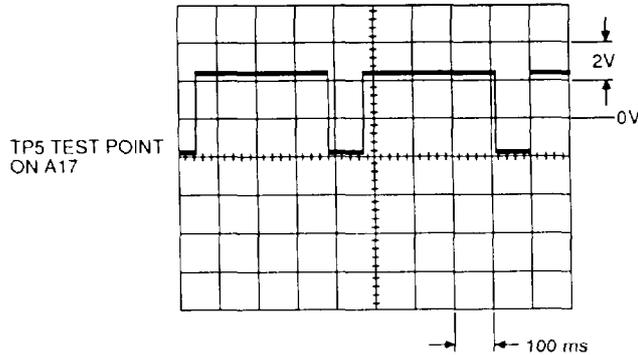


If LO SWITCH is stuck low, then the 5342A will not acquire even if all the IF circuitry is working properly. This is due to the fact that during acquisition, a 1 μs measurement is made on the IF and this requires that LO SWITCH go high to select the A counter on A13. This measurement is made to insure that the IF is in the proper frequency range. The above troubleshooting procedure will not work in this case since diagnostic mode 3 can not be entered. This condition would be evidenced by the counter displaying SP2 in diagnostic mode 0.

**TABLE 8-14
A17**

Table 8-14. A17 Timing Generator Troubleshooting (Continued)

IF LO SWITCH is not present, check the TP5 test point on A17 to see if the prs generator is working. Put the counter in diagnostic mode 2 for continual prs generation. TP5 is high during the prs and should remain high for 360 ms (normal or CW mode on rear panel) or for 2.096 seconds (FM mode).



**TABLE 8-14
A17**

3. Troubleshooting the A17 prs generator.

To troubleshoot the prs generator on A17 (consisting of A17U7, U4, U5, U2, U1, and various gates), pull the A18 time base buffer board from the instrument to disable the 1 MHz clock into A17. Put A17 on an extender board, connect logic probe and logic pulser power leads to A17 +5V and ground, and perform as follows:

a. U7, U4, U5 SHIFT REGISTER CHECK

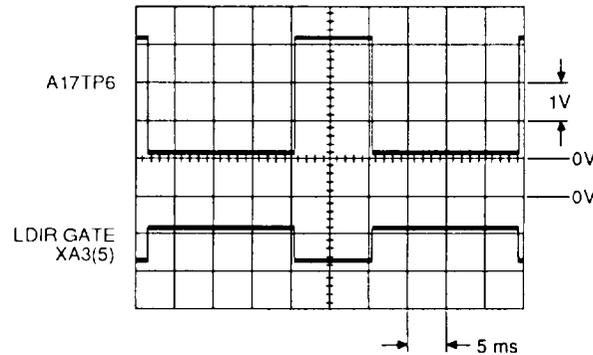
- 1) Put AP clip on U3 and connect clip lead from U3(9) to ground. Verify that U5(1) is high. Clear U7, U4, U5 by applying 1 pulse with logic pulser to TP5 test point. Monitor U5(9) with logic probe to see that the clear input pulses low (if clear input powers up low, then apply a pulse to U19(9) then to U14(2) to cause the clear input to go high).
- 2) Apply logic pulser to TP4 test point and monitor the shift register outputs.
 - After 1 pulse at TP4, U5(3) should go from low to high.
 - Apply 2 more pulses at TP4, U5(5) should go from low to high.
 - Apply 12 more pulses at TP4, U4(12) should go from low to high.
 - Apply 5 more pulses at TP4, U7(6) should go from low to high.

b. U2, U1 Counters Check

- 1) Connect AP clip to U3. Connect clip lead from U3(1) to ground.
- 2) Verify that U1(1) is high. If not, pulse U19(9), then U14(2) with logic pulser. Verify that U2(3) is high and U2(5) is low. If not, pulse U19(9).
- 3) Connect another clip lead from U3(5) to ground. Verify that U1(9) is low. Move clip lead from U3(5) to U3(6) so that U3(6) is grounded. Verify that U1(9) is high. This loads data into U1 and U2 counters.
- 4) Monitor U1(15) with logic probe and pulse TP4 test point with pulser 14 times. ON 14th clock, U1(15) should pulse high.

Table 8-14. A17 Timing Generator Troubleshooting (Continued)

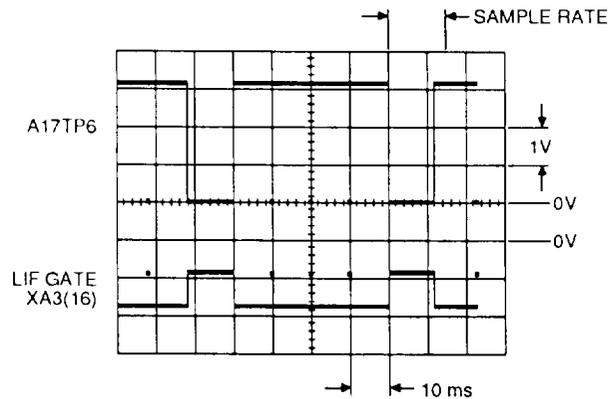
4. A17 LDIR GATE and LIF GATE troubleshooting.
- a. Set the 5342A to 10 Hz—500 MHz range, sample rate full ccw, no input signal, and 100 Hz resolution. With an oscilloscope, monitor LDIR GATE at XA3(5) and TP6 on A17 as shown below:



- b. As the resolution is changed, the width of the gate signal (TP6 high) should vary as follows:

Resolution	Width
1 MHz	1 μ s
100 kHz	10 μ s
10 kHz	100 μ s
1 kHz	1 ms
100 Hz	10 ms
10 Hz	100 ms
1 Hz	1 sec

- c. Change the range of the 5342A to the 500 MHz—18 GHz range and place the counter in MAN mode and observe:



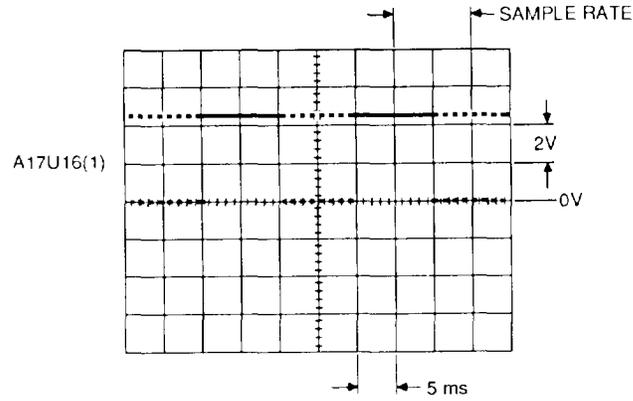
- d. As the resolution is change, the width of the gate signal should vary as follows:

Resolution	Width
1 MHz	10 μ s
100 kHz	Four 10 μ s width pulses, 100 μ s between each
10 kHz	Four 100 μ s width pulses, 100 μ s between each
1 kHz	Four 1 ms width pulses, 100 μ s between each
100 Hz	Four 10 ms width pulses, 100 μ s between each
10 Hz	Four 100 ms width pulses, 100 μ s between each
1 Hz	1 sec

For resolutions from 100 kHz to 10 Hz, each gate time consists of four gate signals separated by 100 μ s dead time.

Table 8-14. A17 Timing Generator Troubleshooting (Continued)

5. IF LDIR GATE or LIF GATE signals are not present, place A17 on an extender board and monitor A17U16(1), the output of the A16 time base generator. Place the 5342A in 10 Hz—500 MHz range, sample rate full ccw, and 1 kHz resolution and observe:



Only the first period of the U16(11) output is used to generate the LDIR GATE signal as shown below:

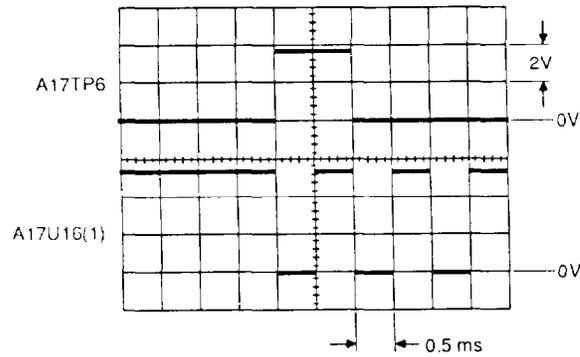
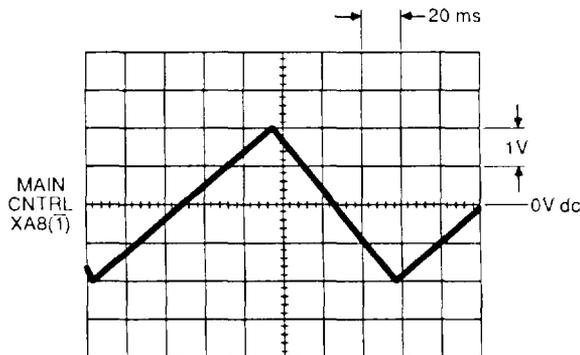


Table 8-15. A8, A9, A10 Main Loop Synthesizer Troubleshooting

1. To test if the A9 Main Loop Amplifier and A10 Divide-by-N are operating properly, put the 5342A in AUTO and select the 500 MHz—18 GHz range. Disconnect any input signal. In diagnostic mode zero (press SET, SET, O), the counter should display SP, indicating that it is sweeping the synthesizers. The MAIN CNTRL signal, measured at XA8(1), should look like:



The sweep up time is approximately 90 ms while the sweep down time is 60 ms. If this signal is present, then A9, A10, and part of A8 as well as the ROM program on A14, are operating properly.

2. To test if the A8 Main VCO is operating properly, put the 5342A in Manual Mode, 500 MHz—18GHz range, and set the MANUAL center frequency to the value in the following table. Connect a coax cable, with BNC connector on one end and alligator clips on the other, from XA5(10) to the 50 OHMS CHANNEL A input of a 5345A Electronic Counter. The 5345A counter will measure the MAIN OSC signal at XA5(10). Verify the 5345A measurement indicates the correct MAIN OSC frequency for each of the MANUAL center frequencies selected.

**TABLE 8-15
A8, A9, A10**

MAN CENTER FREQ	MAIN OSC FREQ
500 MHz	300.0 MHz
550 MHz	312.5 MHz
600 MHz	337.5 MHz
650 MHz	350.0 MHz

Also test the output level of the A8 outputs. Using an RF Millivoltmeter with a high Z probe, the following A8 output levels should be measured (± 100 mV):

XA8(7)	MAIN OSC	500 mV rms
XA8(3)	MAIN VCO	250 mV rms
XA8(5)	DIV N	250 mV rms

These levels are essentially independent of frequency.

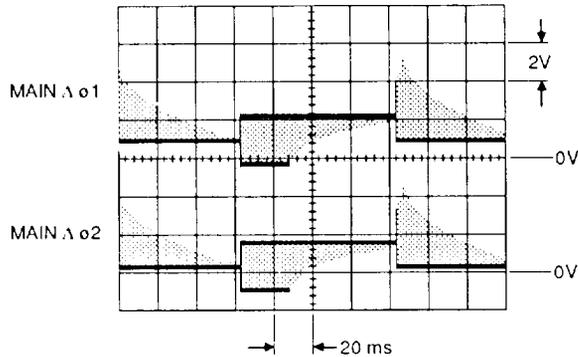
If steps 1 and 2 pass the test, then the Main Loop Synthesizer is working properly. If not, proceed to step 3.

3. A8 FREE RUN FREQUENCY CHECK. Connect XA5(10), the MAIN OSC signal, to the direct count input (front panel BNC), of the 5342A. Use a coax cable, BNC on one end and alligator clips on the other. With a jumper, short MAIN CNTRL, A9TP1, to ground. The 5342A should read approximately 325 MHz (± 2 MHz). If not, adjust A8R22. If no signal is present, repair A8. (Test all of the A8 outputs for a signal.)

Table 8-75. A8, A9, A10 Main Loop Synthesizer Troubleshooting (Continued)

4. Troubleshooting A9 and A10.

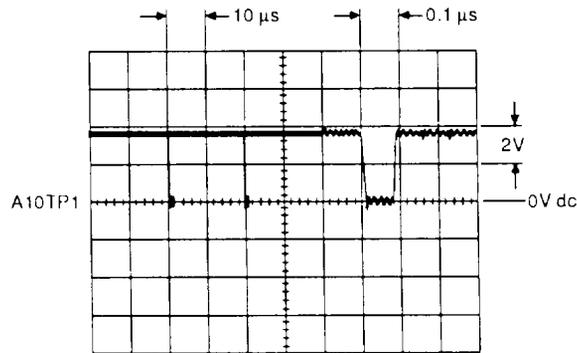
Put A10 on an extender board and put an AP clip on A10U2. Connect scopes probes to U2(5) which is MAIN $\Delta\phi_1$ and U2(10) which is MAIN $\Delta\phi_2$. Ground TP1 on A9 with a clip lead. This causes the A8 VCO to go to its free run frequency of 325 MHz. Put the 5342A in AUTO, 500 MHz—18 GHz range, and no input. This causes the 5342A to sweep the synthesizers. Verify that the U2 phase detector outputs appear as follows:



If these signals are not present, then either the divide-by-N or the phase detector on A10 is faulty. If this signal is present but there is no MAIN CNTRL sweep signal at XA8(1) as in step 1, then A9 is faulty.

5. The following test determines if the divide-by-N is faulty:

With the Main Synthesizer loop working properly, the signal at A10TP1 is a 50 kHz signal as shown:



MIXED SCOPE DISPLAY

TABLE 8-15
A8, A9, A10

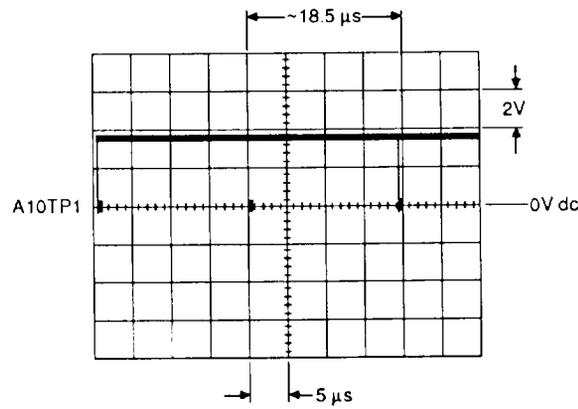
Table 8-15. A8, A9, A10 Main Loop Synthesizer Troubleshooting (Continued)

Ground A9TP1 so that A8 will go to its free run frequency of 325 MHz. Put the 5342A in MANUAL mode and set the following center frequencies. Monitor A10TP1 and check the period of this signal. It should vary per the table below since the 325 MHz free run frequency is divided by the programmed N.

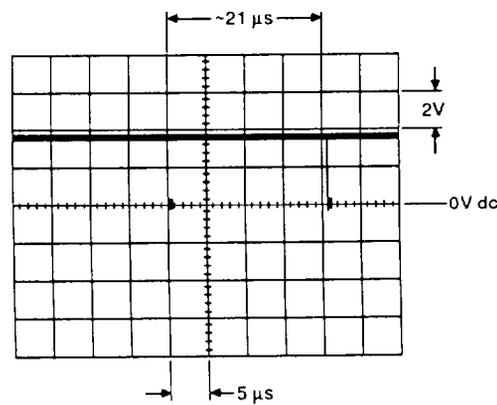
(frequency A8 would go to if A9TP1 not grounded)

MAN CNTRL FREQ	DESIRED VCO FREQ	DIVISION FACTOR N	A10TP1 PERIOD (if free run = 325.0 MHz)
500 MHz	300.0 MHz	6000	18.46 μ s
550 MHz	312.5 MHz	6250	19.23 μ s
600 MHz	337.5 MHz	6750	20.77 μ s
650 MHz	350.0 MHz	7000	21.54 μ s

For example:



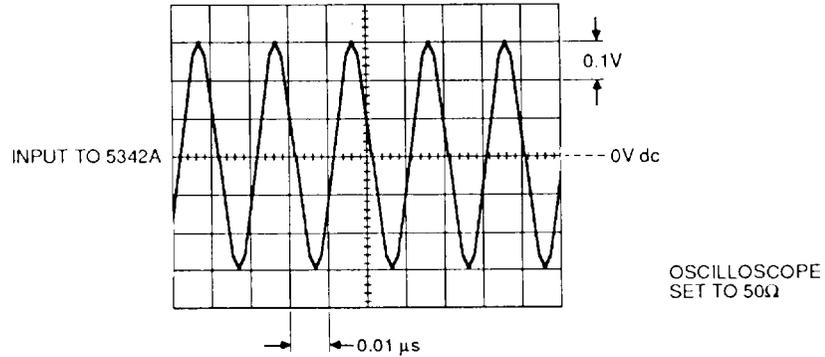
if the MAN CNTRL FREQ is changed to 600 MHz, then the period of A10TP1 changes:



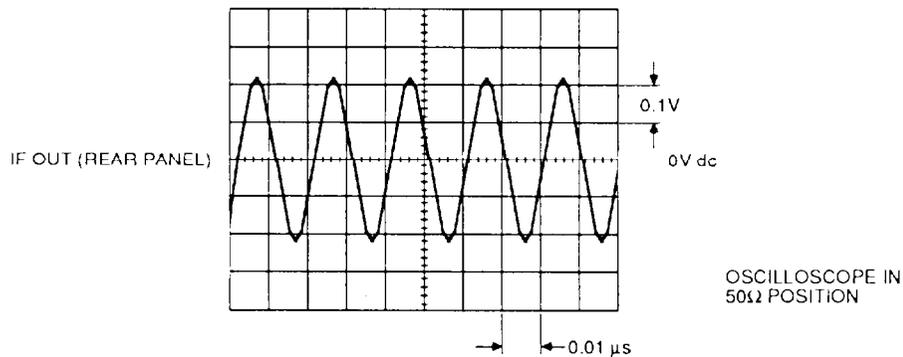
If this doesn't occur, then the divide-by-N circuitry on A10 is faulty.

Table 8-76, A11, A12, A25, U1IF Troubleshooting

1. Set up signal generator at 50 MHz to deliver 0.6V p-p into 50 Ω as measured on an oscilloscope with 100 MHz bandwidth.



2. Apply the 50 MHz signal generator output to the 500 MHz—18 GHz input of the 5342A. Place the 5342A in AUTO and the range switch in the 500 MHz—18 GHz position. The IF OUT on the rear panel of the 5342A should appear as follows:



If this output is as shown above, go to step 3.

- a. If this output is not present, then either the U1 Sampler or the A25 Preamplifier has failed. Check the A25 Preamplifier by checking the dc voltages on the active components as given on the apron of the A25 schematic.

TABLE 8-16
A11, A12, A25

Table 8-16. A11, A12, A25, U1 IF Troubleshooting (Continued)

- b. The U1 Sampler may be checked for continuity (does not guarantee proper operation across the frequency range, however) in the following manner:
- 1) Remove U1 sampler. (Refer to Table 8-18).
 - 2) Measure the following resistance values on an ohmmeter set to the 1 K Ω resistance range (1 mA constant current). Different values are obtained if the current is different than 1 mA.

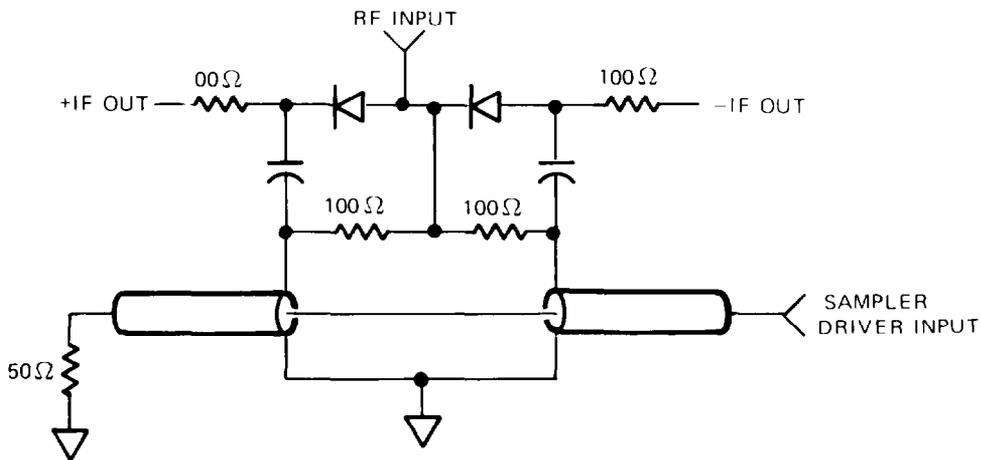
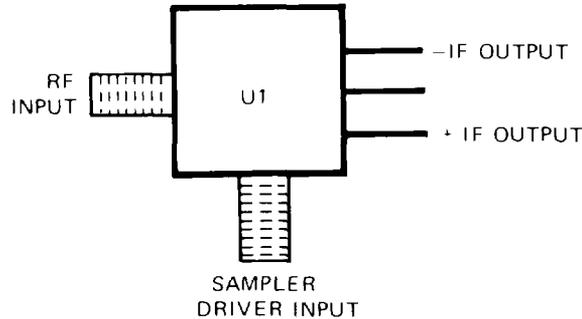
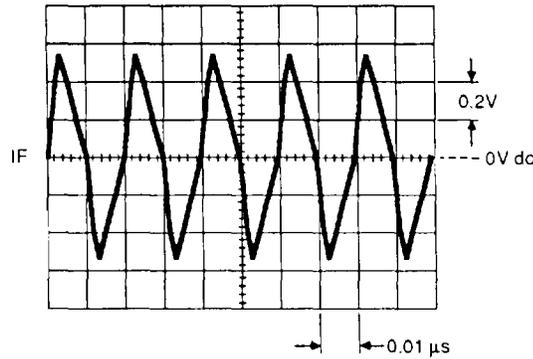


TABLE 8-16
A11, A12, A25

- Measure from the RF Input to + IF OUT, both forward and reverse bias. Ohmmeter should read $\approx 570\Omega$ forward bias, ∞ for reverse bias.
- Measure from the RF Input to - IF OUT, both forward and reverse bias. Ohmmeter should read $\approx 570\Omega$ forward bias, ∞ for reverse bias.
- Measure from the RF Input to ground. Ohmmeter should read $50 \pm 5 \Omega$
- Measure from sampler driver input to ground. Ohmmeter should read $50 \pm 5 \Omega$.

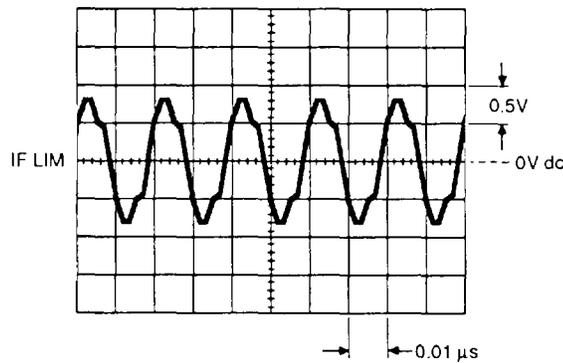
Table 8-16. A11, A12, A25, U1 IF Troubleshooting (Continued)

3. Check the IF signal at XA11(1) using a 10 MΩ/10 pF oscilloscope probe. Signal should appear as follows:



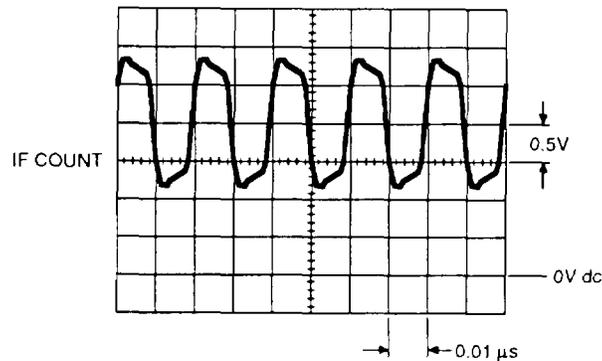
If this signal is not present, suspect A25.

4. Check the IF LIM signal at XA11(12) with 10 M Ω / pF oscilloscope probe. Signal should appear as shown:



If this signal is not present, suspect A11.

5. Check the IF COUNT signal at XA12(8) with 10 MΩ/10pF scope probe. Signal should appear as shown:



If this signal is not present, suspect amplifiers U2 and/or U4 on A12.

TABLE 8-16
A11, A12, A25

Table 8-76. A11, A12, A25, U1 IF Troubleshooting (Continued)

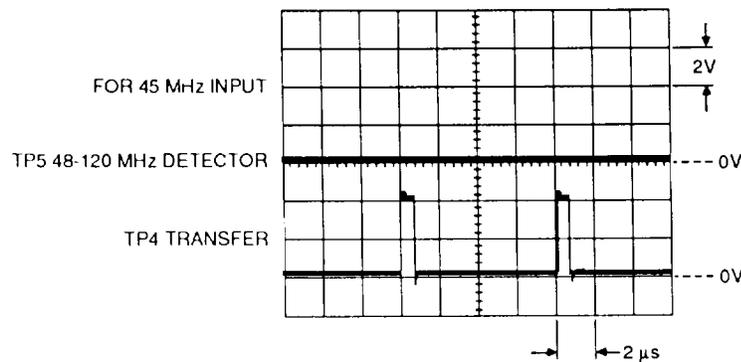
6. Testing A12 IF Detectors

Put the A121F detector on an extender board. Monitor TP8 (48—102 MHz detector) and TP9 (22—128 MHz detector) with a logic probe. Put the 5342A in AUTO and the 500MHz—18 GHz range. Apply a 20 MHz 0 dBm signal to the high frequency input. Note that both TP8 and TP9 are low. Increase the input frequency to 22 MHz and notice that the logic probe indicates a high at TP9 (near the limits of the detectors, the logic probe will blink high). Increase the input frequency to 48 MHz and check that TP8 goes high. As the frequency is increased to 102 MHz, both TP8 and TP9 should be high. As the frequency is increased beyond 102 MHz, TP8 should go low and TP9 should remain high until 128 MHz is reached, at which TP9 also goes low. If these test points are correct the detectors operate properly. If the detectors do not operate, go to step 7.

If the detectors operate as above but if the counter is in AUTO with a 50 MHz signal applied to its high frequency input and if, after placing the counter in diagnostic mode O, the counter displays SP or SP2 only, the most probable cause is that the U12 output gates which drive the data bus are bad or else LPDRD is not being sent by the MPU. Use a logic pulser to pulse LPDRD and check the bus driver outputs with a logic probe. Also use a pulser to pulse LPDWRT to see if that sets the U7 latch to the low state (monitor TP10).

7. Troubleshooting 48-102 MHz Detector on A12. With a dual trace oscilloscope, monitor TP5 (48—102 MHz detector) and TP4 (transfer signal) on A12 under the following conditions. Check that the correct display is obtained. (Put A12 on extender board 05342-60034) .

- a. Apply a 45 MHz signal at 0.6V p-p to the 500 MHz—18 GHz input of the 5342A.



- b. Increase the frequency to 48 MHz. The following display should be observed:

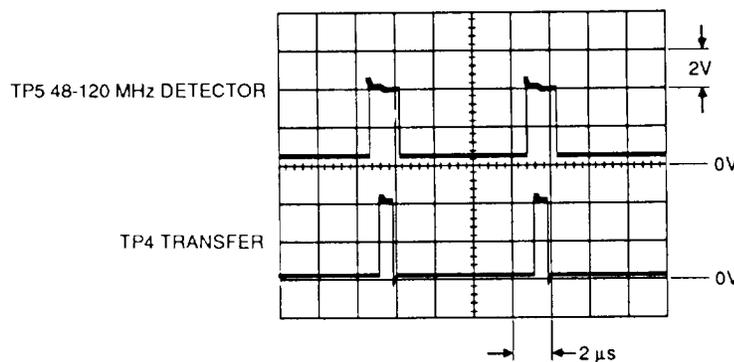
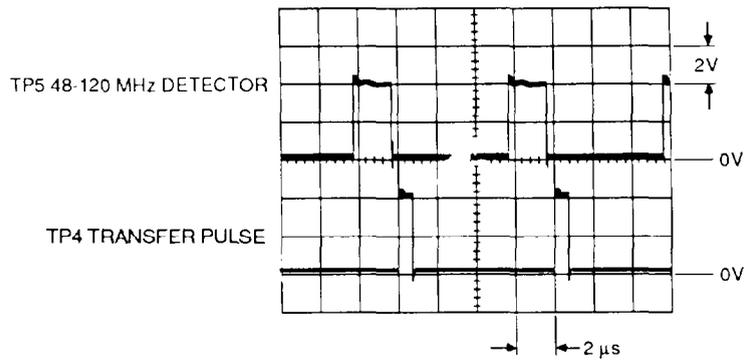


Table 8-76. A11, A12, A25, U1 IF Troubleshooting (Continued)

- c. Increase the frequency from 48 to 102 MHz. Over the entire frequency range, the transfer pulse (TP4) should occur inside the detector pulse (TP5). The transfer pulse clocks the state of the detectors into U13 on A12.
- d. Increase the frequency beyond 102 MHz to obtain the following display:



Transfer pulse occurs outside the detector pulse so that a low is transferred into U13.

- e. Similar waveforms occur for the 22—128 MHz detector with different frequency limits.
- f. Using the 5004A Signature Analyzer, troubleshoot the frequency detectors on A12.

Put A12 on an extender board and an AP clip on A12U15. Place the START probe and STOP probe of the 5004A Signature Analyzer on U15(12) which is the Q_0 output. Place the CLOCK probe of the 5004A on U15(8) which is the 1 MHz input to A12. Place the GROUND probe on U15(7).

Place the CLOCK, START, and STOP switches on the 5004A to positive slope (buttons out).

Connect the 10 MHz FREQ STD output on the rear panel of the 5342A to the high frequency input of the 5342A.

Table 8-16, A11, A12, A25, U1 IF Troubleshooting (Continued)

place the data probe on +5v to see if characteristic 1's signature of UP73 is obtained. If not, replace U15. CHECK the signature at U6(3) to see if the 10 MHz signal is entering the digital filter properly. This signature should be 55H1. Check U6 signatures and work back along the incorrect signature signal path.

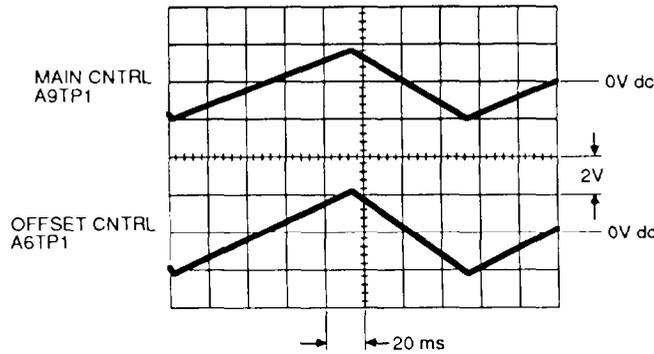
U6(1) A1C9	U5(1) UP73	U8(1) 0000	U9(1)0000
U6(2) 0U16	U5(2) 6097	U8(2) 0000	U9(2) 1F2C
U6(3) 55H1	U5(3) NA	U8(3) HPO1	U9(3) 0000
U6(4) P258	U5(4) NA	U8(4) P258	U9(4) 6097
U6(5) 1F2C	U5(5) 9HP0	U8(5) 0000	U9(5) 2F60
U6(6) 0000	U5(6) 9HP0	U8(6) UP73	U9(6) UP73
U6(7) 0000	U5(7) 0000	U8(7) 0000	U9(7) 0000
U6(8) 0000	U5(8) A1C9	U8(8) 0000	U9(8) 0000
U6(9) UP73	U5(9) 2F60	U8(9) UP73	U9(9) UP73
U6(10) 0000	U5(10) NA	U8(10) 0000	U9(10) UP73
U6(11) 0000	U5(11) NA	U8(11) 0000	U9(11) 0000
U6(12) UP73	U5(12) 1F2C	U8(12) UP73	U9(12) 0000
U6(13) 0000	U5(1) UP73*	U8(13) 0000	U9(13) UP73
U6(14) UP73	U5(14) UP73	U8(14) UP73	U9(14) UP73

U10(1) UP73	U11(1) UP73	U7(1) 6097	U14(1) 0U16
U10(2) 0000	U11(2) 0000	U7(2) 2F60	U14(2) 55H1
U10(3) NA	U11(3) 0000	U7(3) HP01	U14(3) UP73
U10(4) NA	U11(4) UP73		U14(4) FH3F
U10(5) 0000	U11(5) 0000		U14(5) 0000*
U10(6) 0000	U11(6) UP73		U14(6) UP73*
U10(7) 0000	U11(7) 0000		U14(7) 0000
U10(8) 1F2C	U11(8) ACA2		U14(8) UP73*
U10(9) 0000	U11(9) 55H1		U14(9) 0000*
U10(10) NA	U11(10) FH3F		U14(10) FH3F
U10(11) NA	U11(11) 334U		U14(11) NA
U10(12) 0000	U11(12) 0000*		U14(12) ACA2
U10(13) UP73*	U11(13) UP73*		U14(13) 0U16
U10(14) UP73	U11(14) UP73		U14(14) UP73

* probe blinks

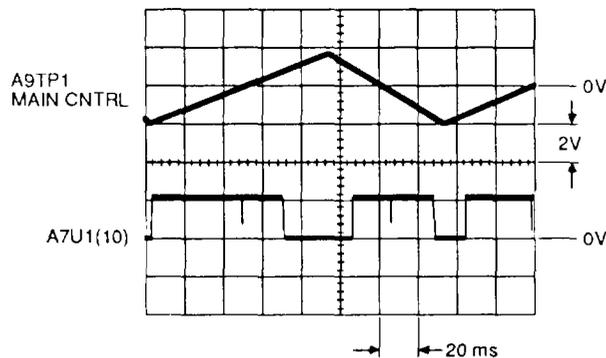
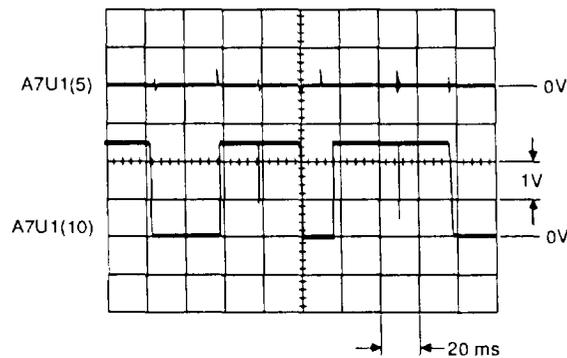
Table 8-17. A4, A6, A7 Offset Loop Synthesizer Troubleshooting

1. To test if the Offset Loop Synthesizer is working, put the 5342A in AUTO, 500 MHz—18 GHz range, and no input signal. Monitor the OFFSET CNTRL signal at A6TP1 and the MAIN CNTRL signal at A9TP1:



Also measure the A4 output signal levels with an RF millivoltmeter with a high impedance probe. XA4(10) should be around 600 mV rms and XA4(7) around 300 mV rms. Both levels are ± 100 mV and essentially independent of frequency.

2. To determine if A4 has failed, use a clip lead to ground A6TP1. This forces the A4 VCO to its free run frequency of 325 MHz ± 2 MHz. Connect XA4(10), the OFFSET OSC signal, to the direct count input of the 5342A using a coax cable with BNC connector on one end and alligator clips on the other. Adjust A4R1 for the proper frequency if necessary. Check that the level is approximately 600 mV rms.
3. If A4 is good, then either A6 or A7 has failed. Pull the A6 OFFSET LOOP AMP from the instrument, put A7 on an extender board and monitor A7U1(5) and A7U1(10), the phase detector outputs, with an oscilloscope. Put the 5342A in AUTO, 500 MHz—18 GHz range, and no signal input. Ground XA4(5), the OFFSET CNTRL signal, with a clip lead to cause A4 to go to 325 MHz. It may be necessary to push MAN, then AUTO, in order to get the characteristic display of all zeros and start the instrument sweeping. The display should be as follows:

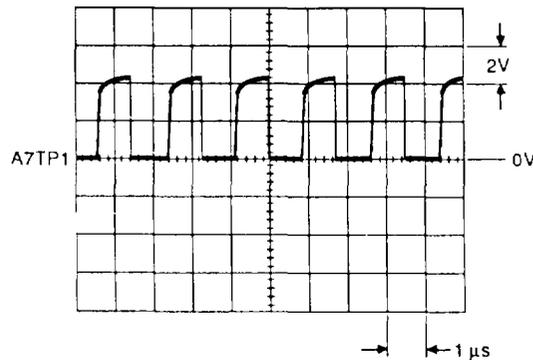


If these signals are present, then A7 is OK.

TABLE 8-17
A4, A6, A7

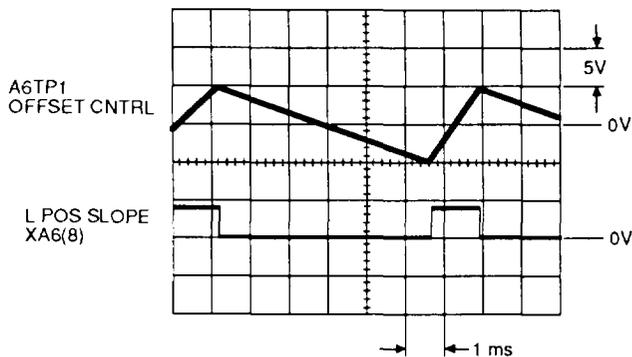
Table 8-17. A4, A6, A7 Offset Loop Synthesizer Troubleshooting (Continued)

4. If these signals are not present, then the mixer portion of A7 should be checked. With A6 out of the instrument, ground XA4(5) so that the A4VCO goes to 325 MHz. Put the 5342A in manual mode and program the MAN center frequency (to check that the VCO frequency is that desired, put the 5342A in diagnostic mode 1 so that the main VCO frequency is displayed). For example, program the MAN center frequency to 576 MHz: the diagnostic mode 1 displays 325.5 MHz as the main VCO frequency. Monitor A7TP1, the output of the mixer and check for the presence of the difference frequency between the main VCO programmed frequency and the free run frequency of A4.



With A6 removed, HSRCH EN, XA7(2) should be TTL high.

5. To check A6, install A6 and remove A7 from the instrument. Remove the short to ground on XA4(5). The search generator on A6 should begin searching and driving the OFFSET CNTRL signal in a search ramp. LPOS SLOPE should go low to indicate when the frequency of the VCO is being swept from higher to lower values.



**TABLE 8-17
A4, A6, A7**

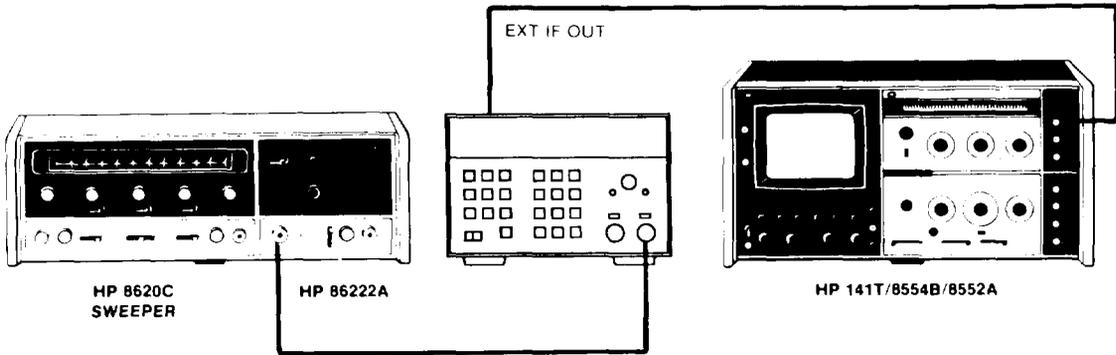
Table 8-78. A26 Sampler Driver Troubleshooting

1. Remove the U1 Sampler and A26 Sampler Driver as follows:
 - a. Remove bottom panel by loosening screw at rear, remove two front feet and slide panel rearward.
 - b. Locate assemblies at bottom front of instrument.
 - c. Pull off coax cables from A1J1, A1J3, A25J1 (IF OUT INT) and A25J2 (IF OUT EXT).
 - d. Disconnect rigid coax from U1 Sampler by loosening attaching nut.
 - e. Remove nut on front panel type N connector and remove rigid cable to allow access.
 - f. Remove cable strap connector at A22 motherboard and move cable strap to one side to allow access.
 - g. Remove 5 screws (four corner and one middle screw) attaching A25 Preamplifier mounting bracket and withdraw bracket (and attached assemblies) from instrument.
 - h. Remove A26 from bracket by removing the two small attaching bolts and nuts. Separate A26 from U1 by loosening the interconnecting hex connector from U1.
2. Set 53424 to CHECK mode and measure the sampler driver output with a power meter. The output should be greater than +16 dBm (if the output of A5, which is driving A26, is at a level of approximately +15 dBm).
3. If the A26 output level is good, then A26U1 and associated circuitry are probably functioning properly. However, a good level does not indicate that the step recovery diode CR1 is working. CR1 could be open. To check the diode with an ohmmeter, connect the positive lead of the ohmmeter (such as the HP 3465A in OHMS function) to the center conductor of the A26 Sampler Driver output and the common leads to the A26 case. Place the ohmmeter in the 2K range (1 mA current source) and measure a forward resistance of approximately 800 ohms. Measure a reverse resistance of infinity.
4. To replace CRI, simply unscrew the plastic holder and remove CRI with tweezers. Reverse the process for assembly.

**TABLE 8-18
A26**

Table 8-79. A5 RF Multiplexer Troubleshooting

Set up the test equipment as shown:



Set the 8620C to 1.2 GHz at approximately -20 dBm. Place the 5342A in AUTO, 500 MHz—18 GHz range, and in diagnostic mode 2 (press SET, SET, 2) so that the counter continuously displays the A counter contents as it remains in the harmonic determination routine. The trace on the spectrum analyzer should show two IF's, indicating that the AS Multiplexer is switching between the main synthesizer and the offset synthesizer.

The wideband filter on A9 is switched in as can be determined by the wider noise skirts about the signal.

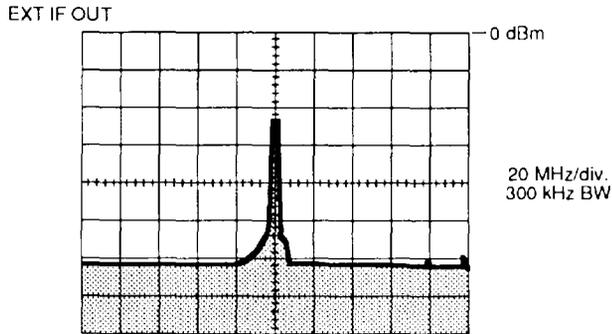


TABLE 8-19
A5

1.2 GHz @ -20 dBm input to CNTR

If the scale is expanded to 1 MHz/div., it is seen that the separation between the IF's is 2 MHz (=4 x 500 kHz) where 4 is the N number. Go to diagnostic mode 1 to verify N=4.

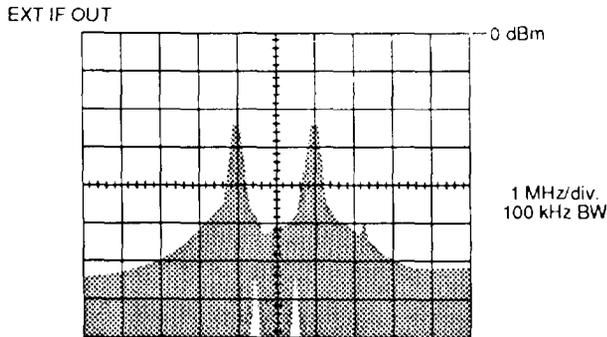


Table 8-79. A5 RF Multiplexer Troubleshooting (Continued)

Put counter in diagnostic mode 4 which continuously measures the IF. The narrow band filter on A9 is switched in and noise skirt about IF reduced:

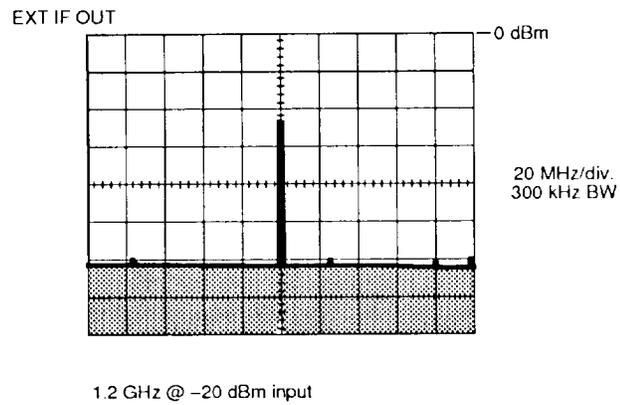


Table 8-20. Deleted

TABLE 8-19
A5

Table 8-21. HP-IB Troubleshooting

1. Acceptor Handshake Troubleshooting

a. Setup:

5342A

HP-IB CABLE

59401A
BUS SYSTEM
ANALYZER

Set 5342A rear panel address switch to:

59401 A settings:

MEMORY OFF

COMP OFF

TALK Mode

HALT

ATN = 1, SRQ= 0, EO1 = 0

REN true (REN light on)

DIO switches to 5342A listen address:

8	7	6	5	4	3	2	1
0	0	1	0	0	0	0	1

b. Remove the A14 Microprocessor assembly from the 5342A. Perform the actions listed in Table 8-27A to verify the acceptor handshake. Use a 546A Logic Pulser to apply a clock pulse to a particular circuit node. Use a 545A Logic Probe to check the state of circuit nodes.

Table 8-21A. Acceptor Handshake (HP-IB)

STEP	ACTION	59401A*			U6(13)	U3(9)	U6(10)	U6(4)	U3(5)	U6(1)	U32(6)	COMMENTS
		DAV light	NRFD Light	NDAC Light								
0	Apply power to 5342A	OFF	ON	ON	Low	High	Low	Low	High	Low	High	Since the 5342A's listen address is on the data lines, U33(14) should be high. If not, check inputs. U33(4,5,6,7,9,10,11,12) should all be TTL high. U33(3,13) should be TTL low.
1	Clock U3(11) once	OFF	OFF	ON	Low	Low	High	Low	Low	Low	Low	U20(10) and U29(6) should go high. U23(2) should go high. U(8) should go high. Interrupt flag U10(5) should go high
2	Press EXECUTE on 59401A	ON	OFF	ON	High	Low	High	Low	Low	Low	Low	
3	Clock U3(11) once	ON	OFF	ON	High	High	Low	High	Low	Low	Low	
4	Clock U3(11) once	ON	ON	ON	Low	High	Low	High	High	Low	High	
5	Clock U3(11)	OFF	ON	OFF	Low	Low	Low	Low	High	High	High	
6	Go to Step 1 and Handshake sequence Repeats											

NOTES:

*DAV "ON" means that LDAH at A15U31(6) is TTL Low.

NRFD "ON" means that HRFD at A15U22(14) is TTL Low.

NDAC "ON" means that HDAC at A15U25(14) is TTL Low.

Table 8-21. HP-IB Troubleshooting (Continued)

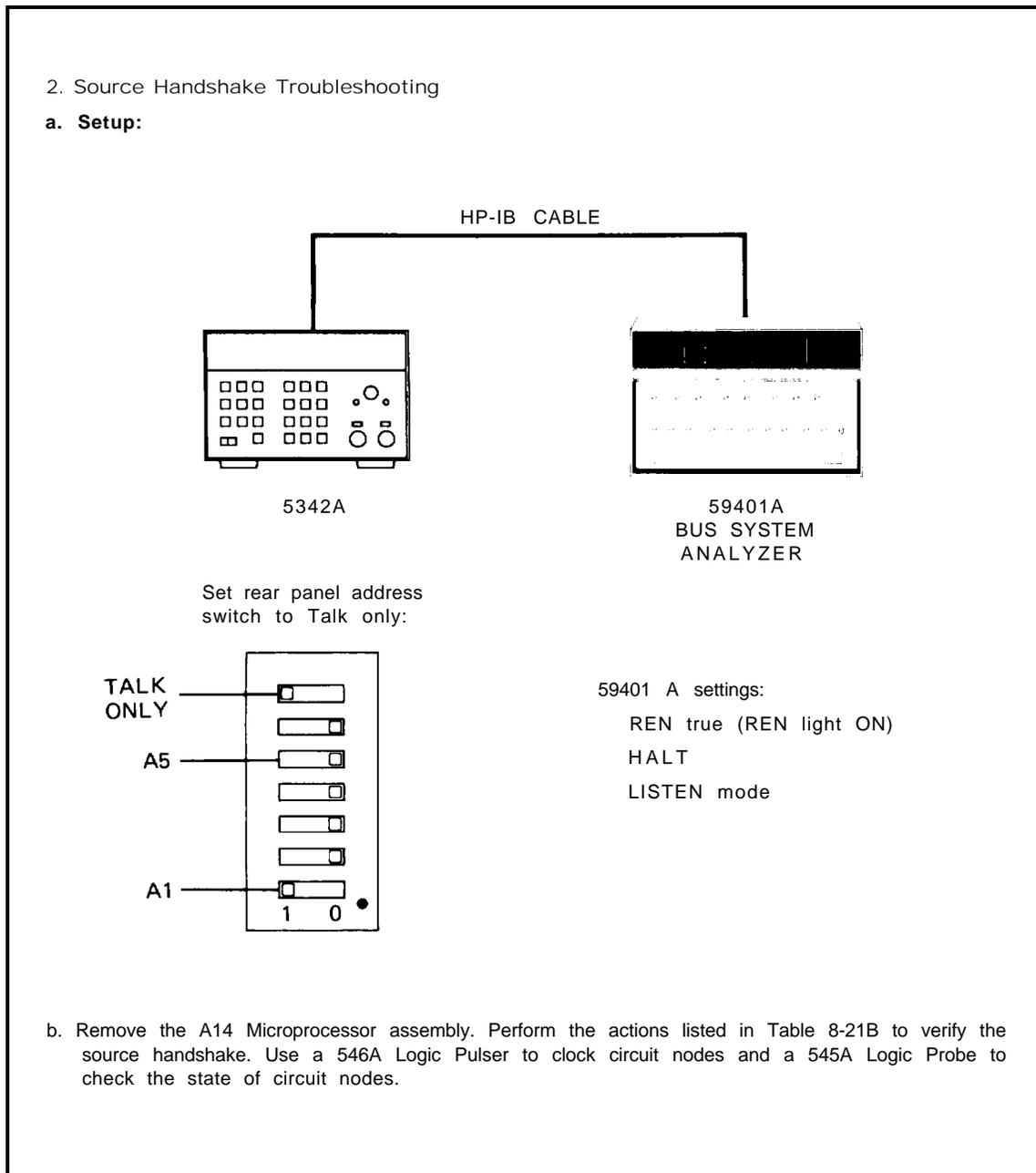


Table 8-21B, Source Handshake (HP-16)

STEP	ACTION	59401A			U5(4)	U9(9)	U2(4)	U2(13)	U4(9)	U5(13)	U4(5)	U36(3)
		DAV Light	NRFD Light	NDAC Light								
0	Apply power to 5342A	OFF	OFF	ON	High	High	Low	Low	High	Low	Low	High
1	Clock U9111 once	OFF	OFF	ON	High	Low	High	Low	High	Low	Low	High
2	Clock U4(11) once	OFF	OFF	ON	High	Low	High	High	Low	Low	Low	High
3	Clock U4(11) once	ON	OFF	ON	High	Low	Low	High	Low	Low	High	Low
4	Press EXECUTE on 59401A	ON	ON	OFF	High	Low	Low	Low	LOW	Low	High	Low
5	Clock U4(1) once	OFF	OFF	ON	Low	High	Low	Low	High	Low	High	High
6	Clock U4(1) once	OFF	OFF	ON	High	High	Low	Low	High	Low	Low	High
7	Go to Step 1 and the Handshake Sequence Repeats											

Table 8-21. HP-IB Troubleshooting (Continued)

3. U23, U26 ROM Troubleshooting

a. Setup:

HP-IB CABLE

5342A

59401A
BUS SYSTEM
ANALYZER

Set rear panel address switch to:

TALK ONLY

A5

A1

1 0

59401 A settings:
MEMORY OFF
COMP OFF
TALK Mode
HALT
SRQ = 0, EOI = 0
REN True

b. Remove the A14 Microprocessor assembly from the 5342A. Place A15 HP-IB assembly on an extender. Place an AP clip on U1 and ground U1(8). Set ATN and the DIO switches on the 59401A as listed in Table 8-21C and check with a 545A Logic Probe for the correct outputs.

Table 8-21 C. U23, U26 ROM Table (HP-IB)

COMMENTS	**59401A SETTINGS								*U23 PINS							*U26 PINS																
	A	T	N	8	7	6	5	4	3	2	1	1	2	3	4	5	6	7	1	2	3	4	5	6	7	9						
Listen Address	1	0	0	1	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0		
Talk Address	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
Data (M)	1	0	0	1	0	0	1	1	0	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1		
Go to Local	1	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	1	1	1	1	1	1	1	0	1	0	1	0	1		
Serial Poll Enable	1	0	0	0	1	1	0	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0		
Serial Poll Disable	1	0	0	0	1	1	0	0	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0		
Group Execute Trigger	1	0	0	0	0	1	0	0	0	0	0	1	1	0	0	1	0	1	1	1	1	1	1	1	1	0	1	0	0	1	0	
Local Lock-Out	1	0	0	0	1	0	0	0	0	1	1	1	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Device Clear	1	0	0	0	1	0	1	0	0	1	1	1	0	0	1	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	0	
Selected Device Clear	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	1	0	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0
Unlisten	1	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Untalk	1	0	1	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTES:

*Ground U1(8) to enable ROM U23

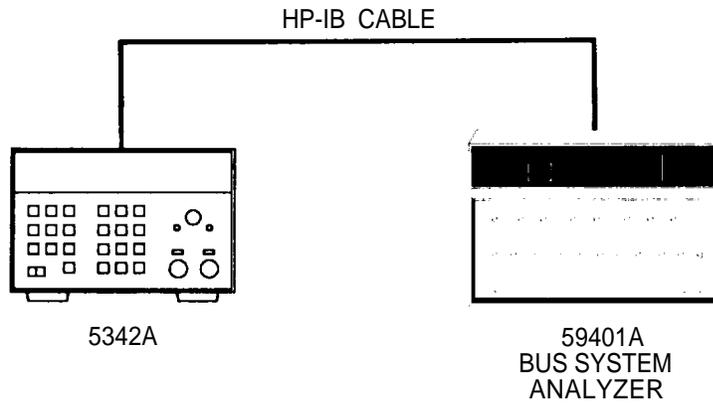
*1 = TTL High for U23, U26

** (1 = TTL Low for 59401A outputs, e.g., if DIO7 set to 1, then LDIO7 at A15U31(10) is TTL Low)

Table 8-21. HP-IB Troubleshooting (Continued)

4. Troubleshooting Registers U27, U24, U21, U16, U18, U30, U15

a. Setup:



b. Remove A14 Microprocessor assembly from the 5342A and place the A15 HP-IB assembly on extender boards.

c. Place an AP clip on U11 and connect a clip lead from U11(12) to ground. This enables the U27 Data In register.

d. U27 CHECK:

Set the 59401A to TALK, HALT, and the 8 DIO switches to 0 (all switches down). Check the inputs to U27(3, 4, 7, 8, 13, 14, 17, 18) for all TTL high. If these inputs are not all TTL high, troubleshoot the input data buffers U22, U25, U31. With the 546A Logic Pulser, pulse U27(11). Check the outputs of U27(2, 5, 6, 9, 12, 15, 16, 19) for all TTL high. Change the DIO switches of the 59401A to all 1 (all switches up). Pulse U27(11) once. Check the U27 outputs for all TTL low.

e. U21 CHECK:

If U27 is working, it is possible to control the state of the microprocessor data bus and thereby check out U21, U24, and U16. To check out U21, ground U12(5) with another clip lead (U12(12) is still grounded). This enables U21. With the 59401A DIO switches all set to 1 (all switches up), clock U27(11) with the Logic Pulser. Now clock U21(11). Check the outputs of U21(2, 5, 6, 9, 12, 15, 16, 19) for all TTL low. Now change all the 59401A DIO switches to 0 (all switches down). Clock U27(11) with the Logic Pulser. Verify that the U21 outputs are still TTL low. Now clock U21(11). Verify that the U21 outputs are all high.

f. U24 CHECK:

Change the clip lead on U12 from pin 5 to pin 13 so that U12(13) is grounded. Check that U21(1) is TTL high. If U21(1) remains low after the clip lead is removed, the serial poll FF U29 must be set high. To do this, ground U29(14) and clock U29(12). Verify that U29(10) is TTL high. U12(13) grounded enables U24. U27 should still be enabled by the ground on U11(12). With the 59401A

DIO switches all set to 0 (switches down), clock U27(11) and clock U24(11). Verify that the outputs of U24(2, 5, 6, 9, 12, 15, 16, 19) are all TTL high. Change the 59401A DIO switches to 1 (all switches up). Clock U27(11) with the Logic Pulser. Verify that all the U24 outputs are still TTL high. Now clock U24(11) and verify that the U24 outputs are all TTL low.

g. U16 CHECK:

Remove the clip lead from U12(13). U27 should still be enabled by the ground on U11(12). With the DIO switches of the 59401A all set to 1 (all switches up), clock U27(11) with the 546A Logic Pulser. Next clock U16(9) and verify that the outputs of U16(2, 5, 7, 10, 12, 15) are all TTL low. Change the DIO switches on the 59401A to 0 (all switches down) and clock U27(11). Verify that U16 outputs remain TTL low. Now clock U16(9) and verify that the U16 outputs are all TTL high.

Table 8-21. HP-IB Troubleshooting (Continued)

h. U18 CHECK:

Change the clip lead on U11 from pin 12 to pin 13 so that U11(13) is now grounded. This action will disable the U27 Data In register and will enable the U18 Interrupt Out register. Clock each of the inputs to U18(2, 4, 6, 10, 12) with a 546A Logic Pulser, and simultaneously check the corresponding output, U18(3,5, 7,9, 11)with the 545A Logic Probe. Remove the ground from U11(13) and verify that clocking an input has no effect upon an output (all the outputs should be in the high Z state).

i. U30 CHECK:

Change the ground to U11(15) with the clip lead, This enables the State In register U30. Clock each of the inputs to U30(2,6, 10,12, 14) and simultaneously check the corresponding outputs of U30(3, 7, 9, 11, 13). Remove the ground from U11(15) and verify that clocking an input has no effect upon an output.

j U15 CHECK:

Change the ground to U11(14) which enables the Command In register U15. Set the DIO switches and ATN to the following:

```
A T N   8 7 6 5 4 3 2 1
1   0 0 1 0 0 0 0 0   (5342A rear panel HP-IB address switches set to 00001)
```

This should cause the U26 ROM outputs to present a TTL low to U15(12, 13,14). Verify this with a logic probe. U15(11) will be TTL high since the A15 assembly powers up with the U20 Listen FF reset.

Clock U15171 with the Logic Pulser and verify that U15(3, 4, 5) are TTL low and U15(6) is TTL high.

Set the DIO switches to the following:

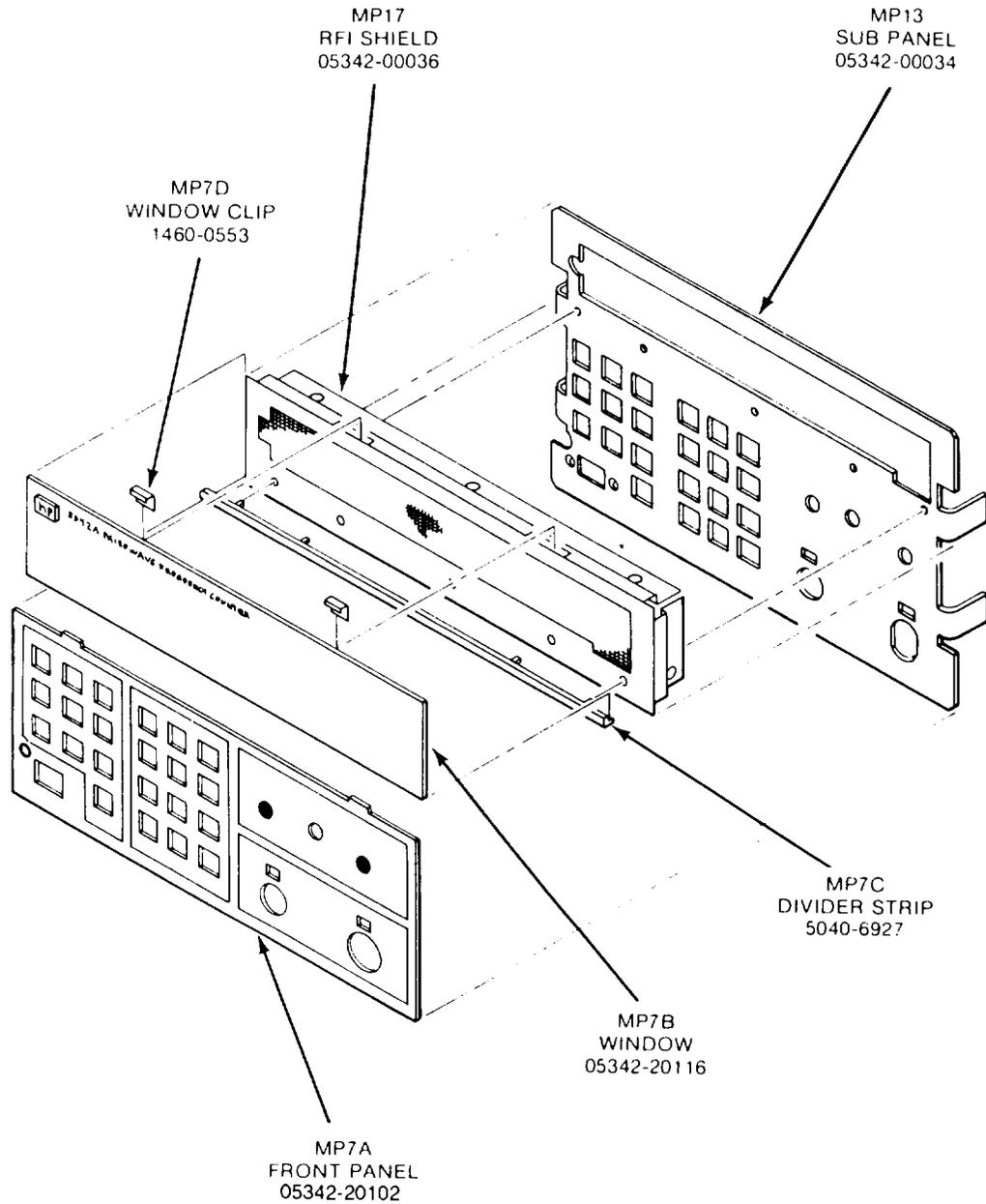
```
A T N   8 7 6 5 4 3 2 1
1   0 0 1 0 0 0 0 1
```

Clock U20(12) to set the U20 Listen FF. This causes U15(11) to go TTL low.

Now set the DIO switches to the following:

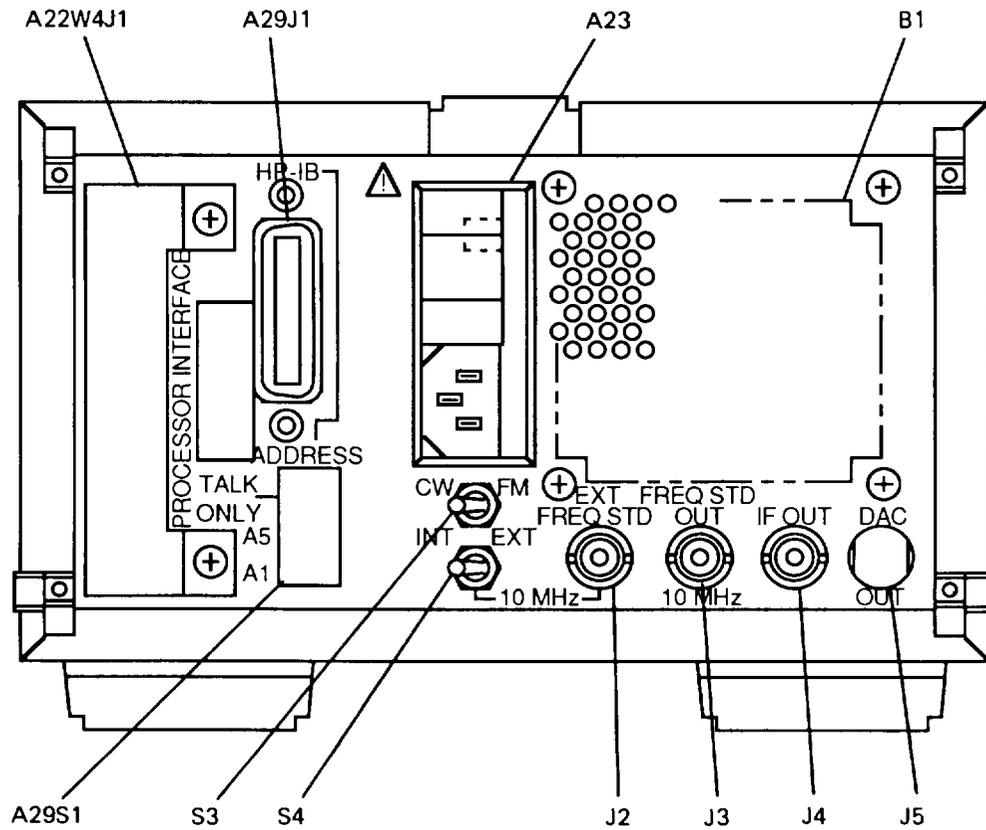
```
A T N   8 7 6 5 4 3 2 1
1   0 0 0 1 0 0 0 1
```

This causes the U26 ROM outputs to present a TTL high to U15(12, 13, 14). Verify this with the logic probe. U15(11) should be TTL low. Clock U15(7) and verify that U15(3,4,5) are TTL high and U15(6) is TTL low.



CE1LG024

Figure 8-19. Front Panel Assembly



CE1LG025

Figure 8-20. 5342A Rear View

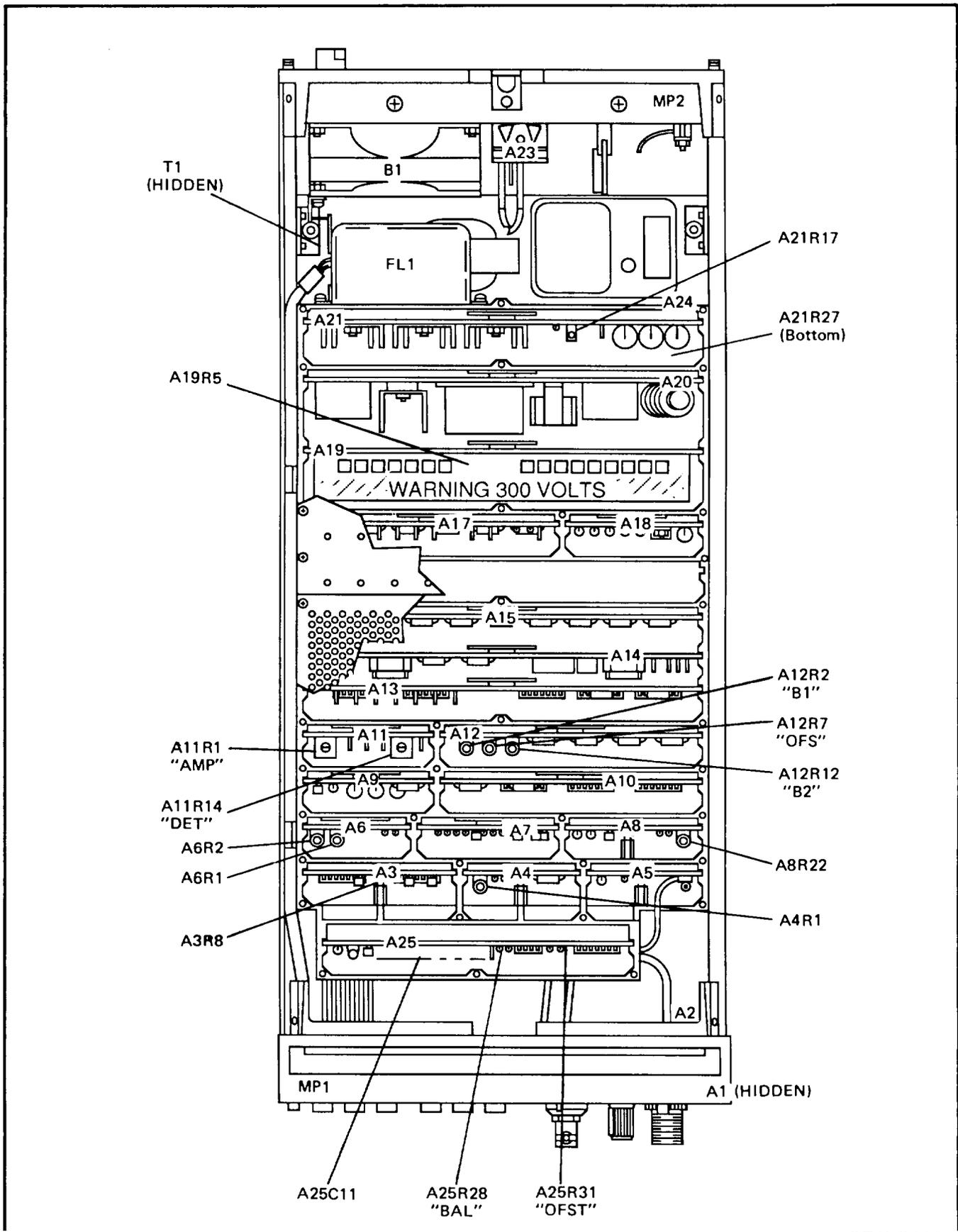
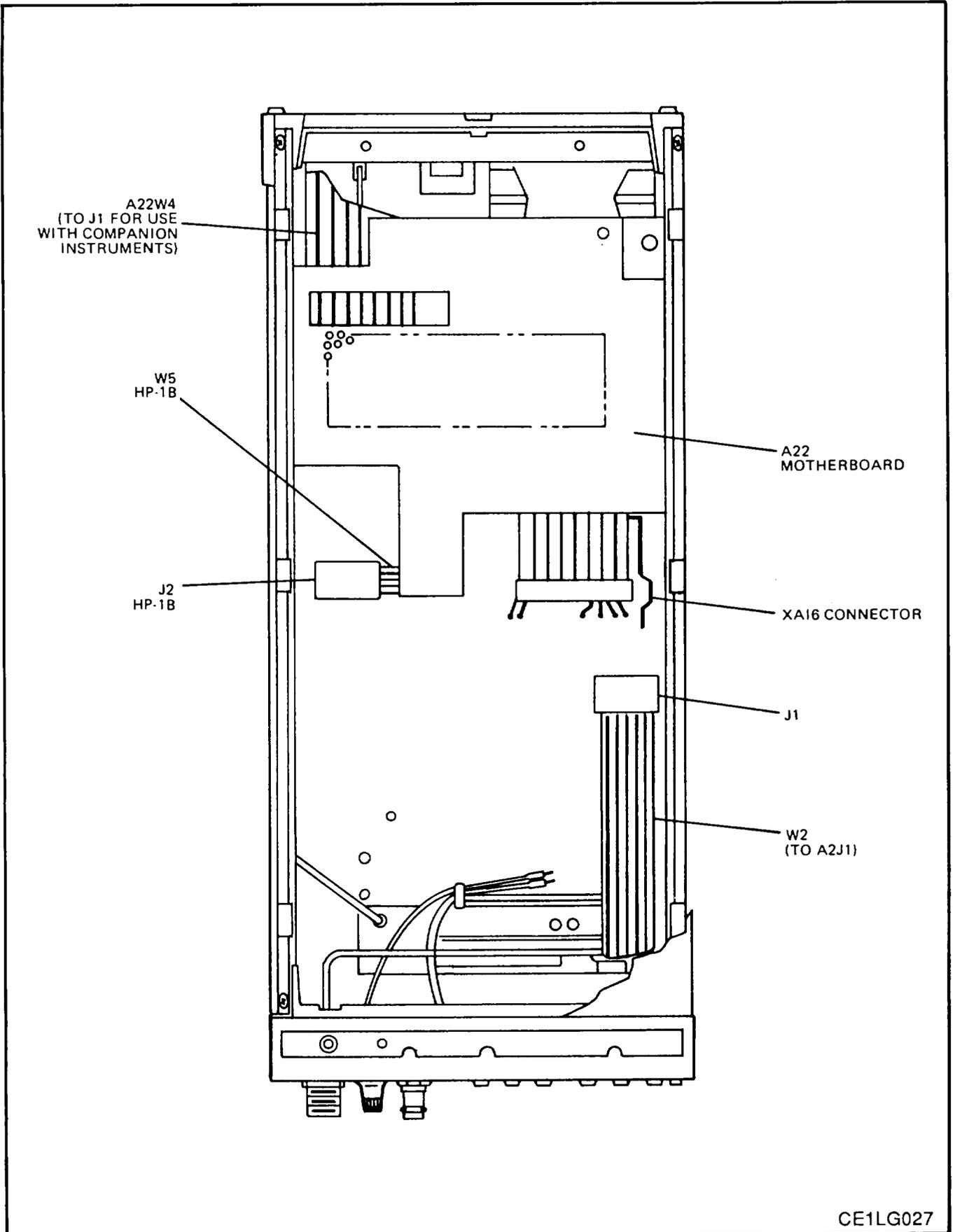


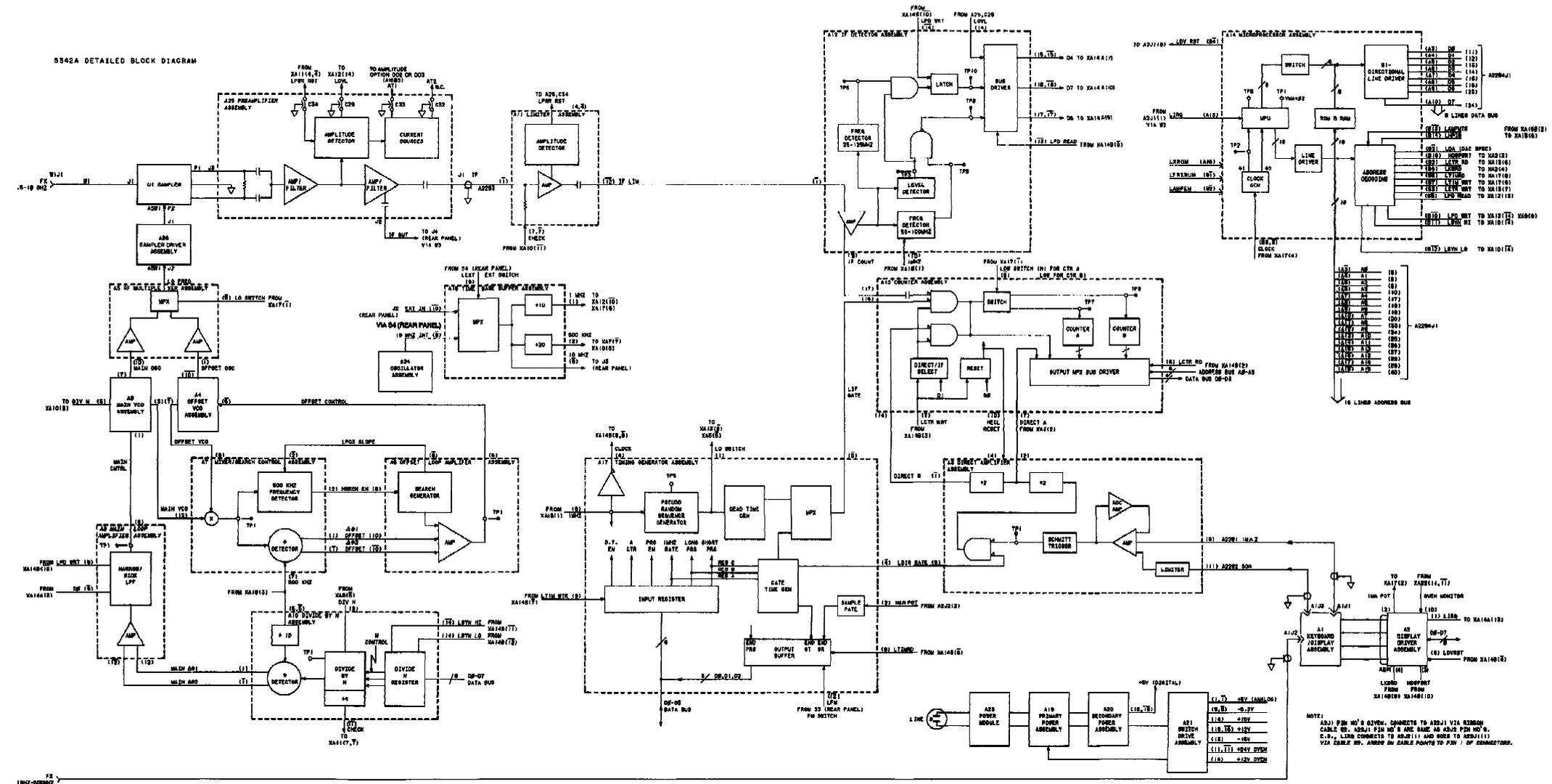
Figure 8-21. 5342A Top View (Assembly Locations and Adjustments)

CE1LG026



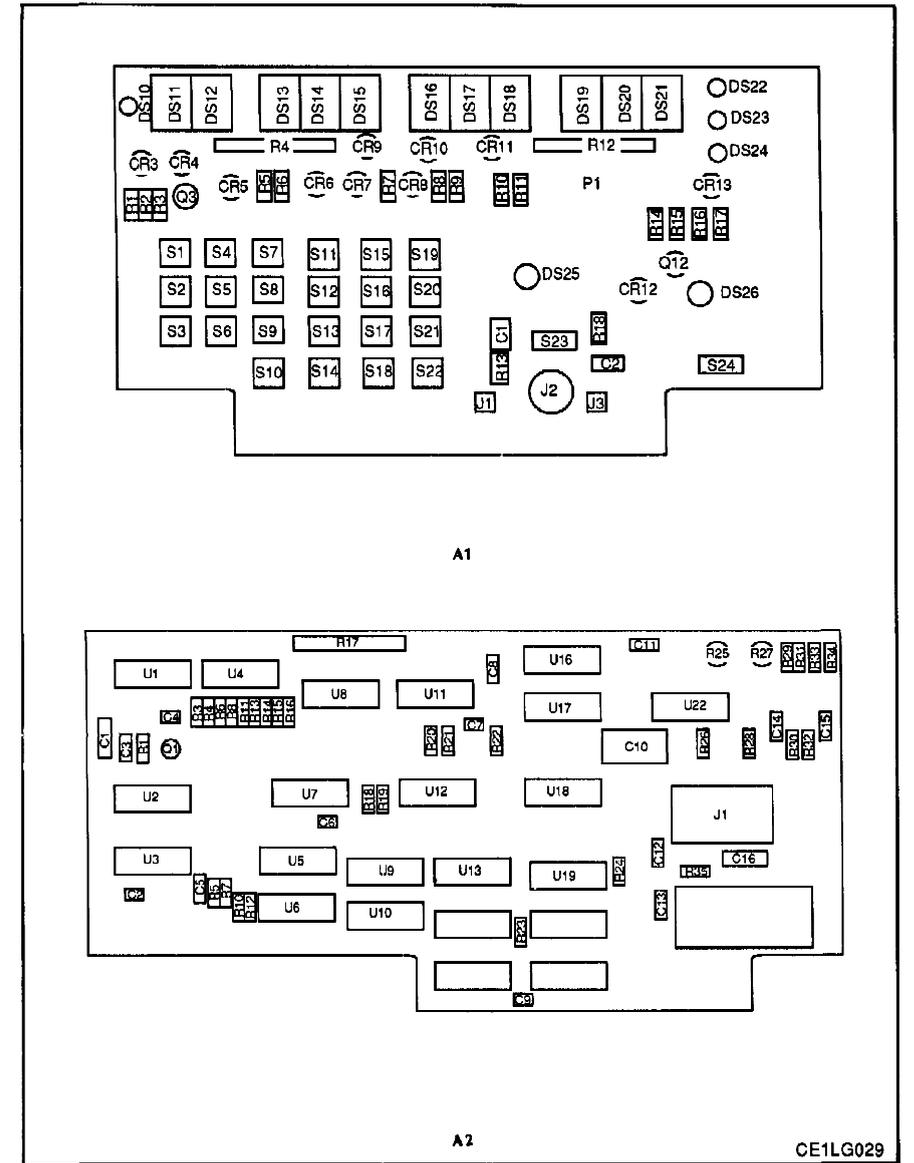
CE1LG027

Figure 8-22. 5342A Bottom View, Options Installed



CE1LG026

FO Figure 8-23. 5342A Detailed Block Diagram



Part of Figure 8-24. A1 Display Assembly and A2 Display Drive Assembly

REFERENCE DESIGNATIONS

A1	A2
C1, C2	C1-C20
DS1-DS26	Q1
J1-J3	R1-R33
Q1-Q18	TP1
R1-R18	U1-U22
S1-S24	
TP1-TP2	

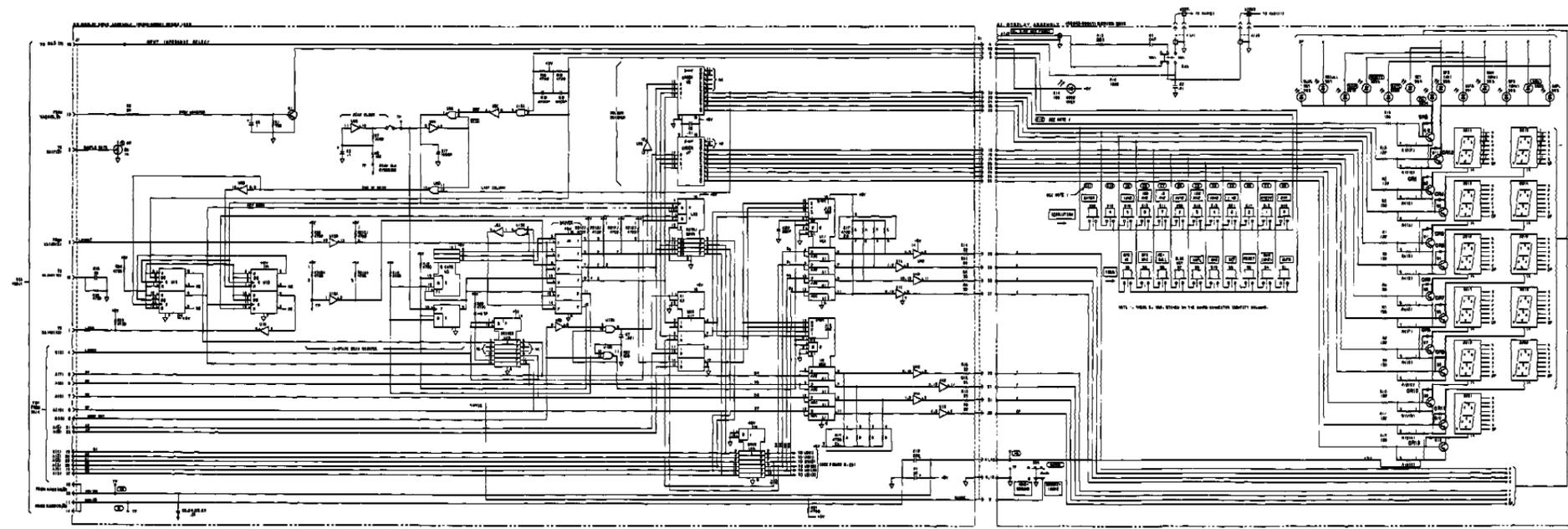
Deleted: DS9

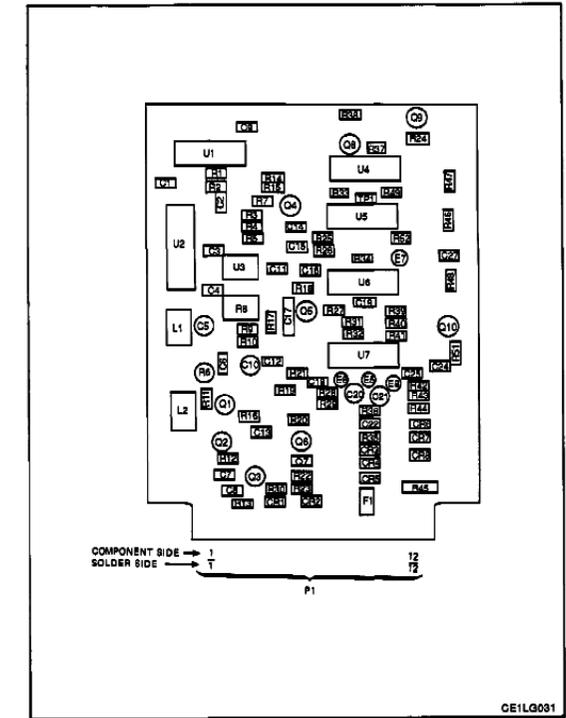
Deleted:
C12, C14, C9
R23, R25, R34
U14, U15,
U20, U21

TABLE OF ACTIVE ELEMENTS

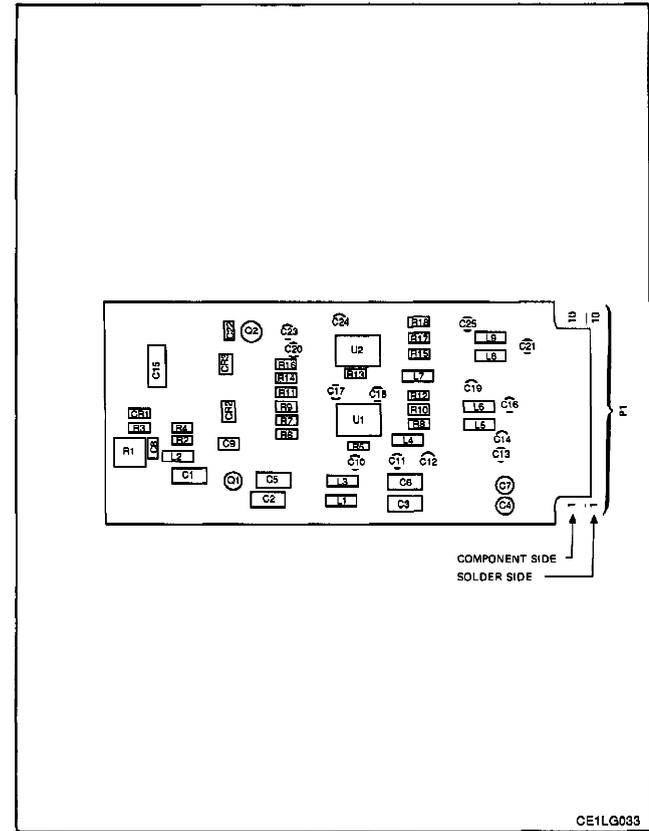
REFERENCE DESIGNATION	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
A1Q1, Q2, Q3, Q11, Q13	1883-0218	MP66662
A1Q2, Q12	1883-0018	
A2		
U1, U4	1820-0839	SN7437N
U2, U7	1820-0466	SN7448N
U3	1820-1443	SN74LS263N
U5	1820-1416	SN74LS14N
U6	1820-1049	DM8097N
U8, U11	1820-1028	SN7159N
U9	1820-1144	9L302PC
U10	1820-1200	SN74LS05N
U12, U16	1820-1254	DM8095N
U13	1820-1426	74LS125
U17	1820-1428	SN74LS158N
U18, U19	1820-1112	SN74LS74N
U22	1820-1885	DM74LS173N

Deleted: U14, U15, U20, U21

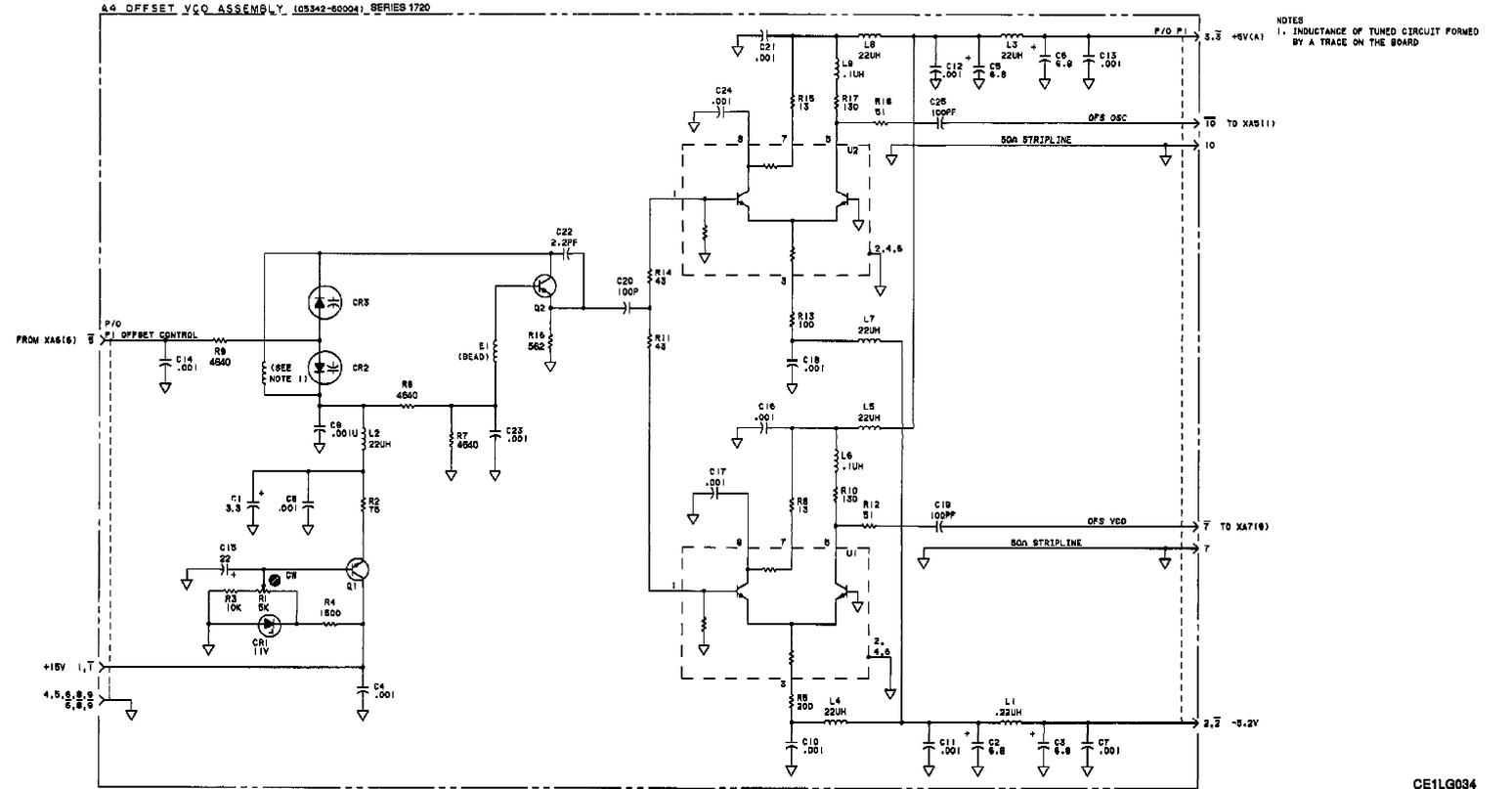
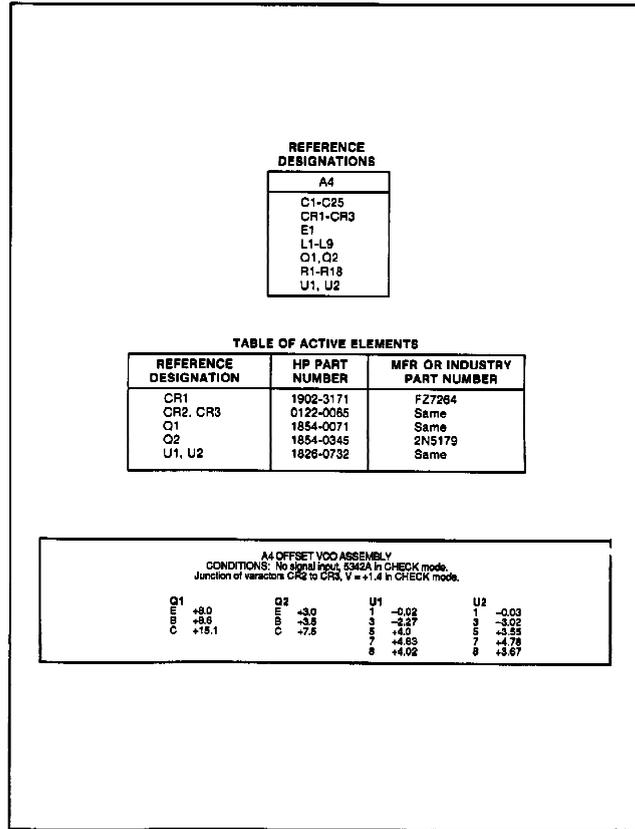




Part of Figure 8-26. A3 Direct Count Amplifier Assembly

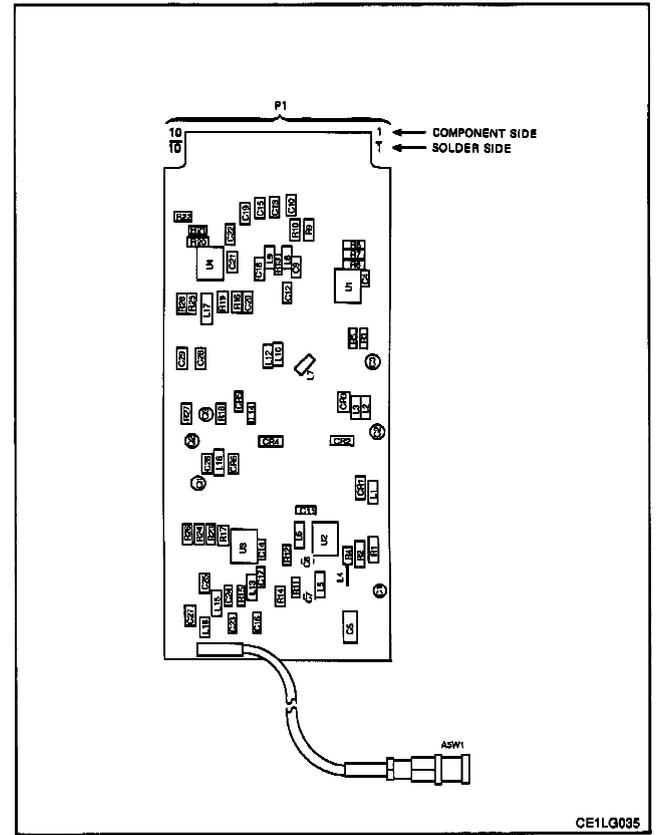


Part of Figure 8-27. A4 Offset VCO Assembly

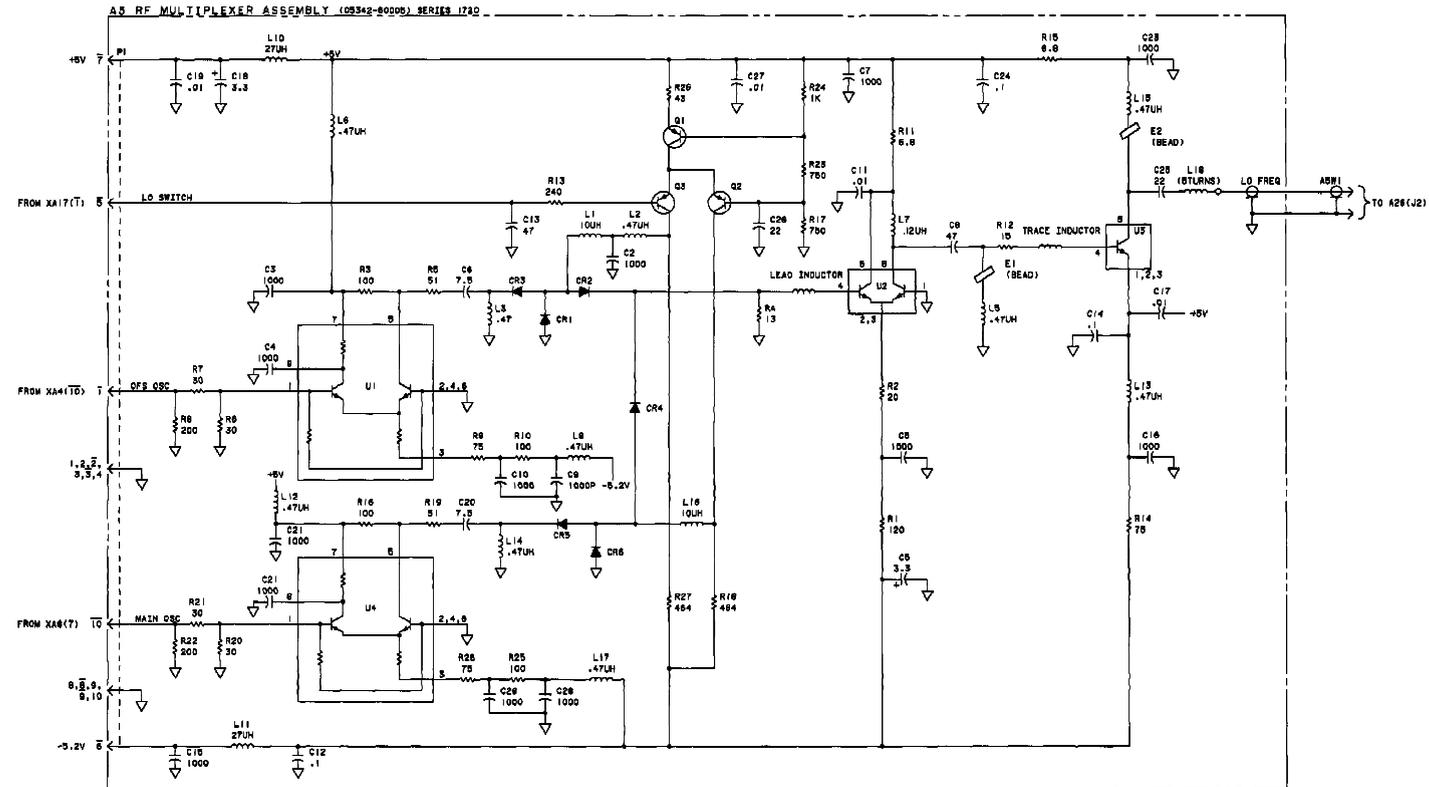
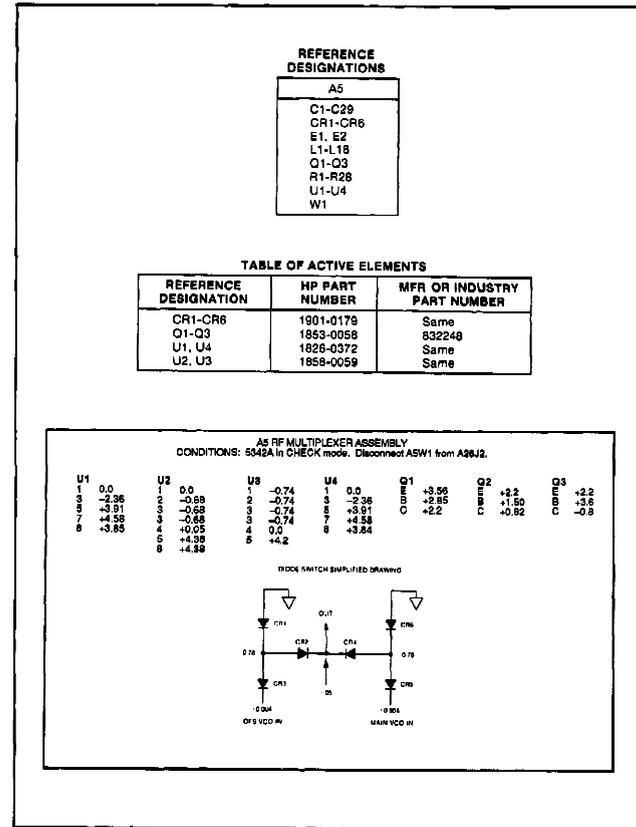


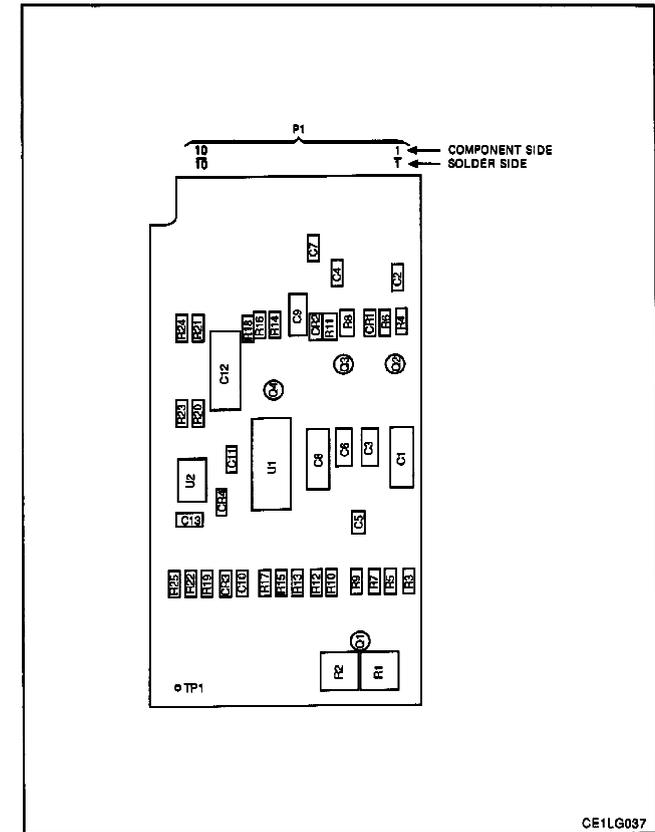
CE1LG034

FO Figure 8-27. A4 Offset VCO Assembly



Part of Figure 8-28. A5 RF Multiplexer Assembly





Part of Figure 8-29. A6 Offset Loop Amp/Search Generator Assembly

REFERENCE DESIGNATIONS

A6
C1-C13
CR1-CR4
Q1-Q4
R1-R25
U1, U2

TABLE OF ACTIVE ELEMENTS

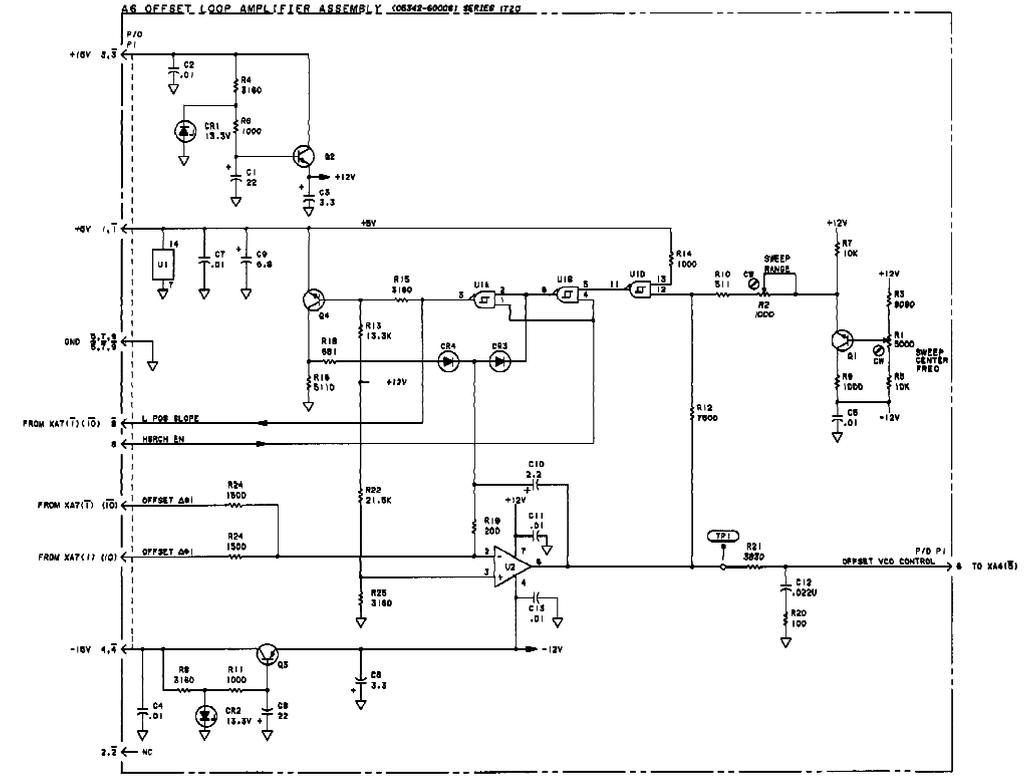
REFERENCE DESIGNATION	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
CR1, CR2	1902-3193	F27272
CR3, CR4	1901-0040	Same
Q1, Q3, Q4	1853-0020	Same
Q2	1854-0071	Same
U1	1820-1425	SN74LS132N
U2	1820-0493	LM307N

A6 OFFSET LOOP AMPLIFIER ASSEMBLY
 CONDITIONS: No signal input, S342A in CHECK mode.

Q1	Q2	Q3	Q4	U2	NOTE
1.3	12.4	-12.1	+5.05	2	Junction of CR2, CR3: +1.55V
+0.7	+13.0	-12.8	+5.3	3	
-11.0	+15.1	-14.7	0.0	4	
				5	
				6	
				7	
				7	

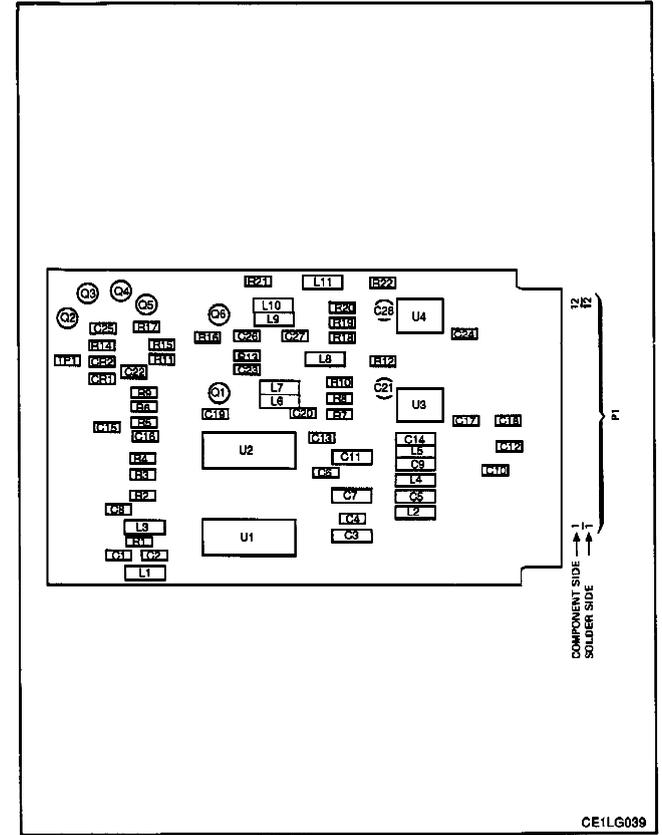
CONDITIONS: A7 Assembly removed; S342A in CHECK mode.

Q4	U2	NOTE
6	2	Junction of CR4, CR3: +1.54
+4.42	3	
+4.37	3	
	6	
	6	
	7	
	7	

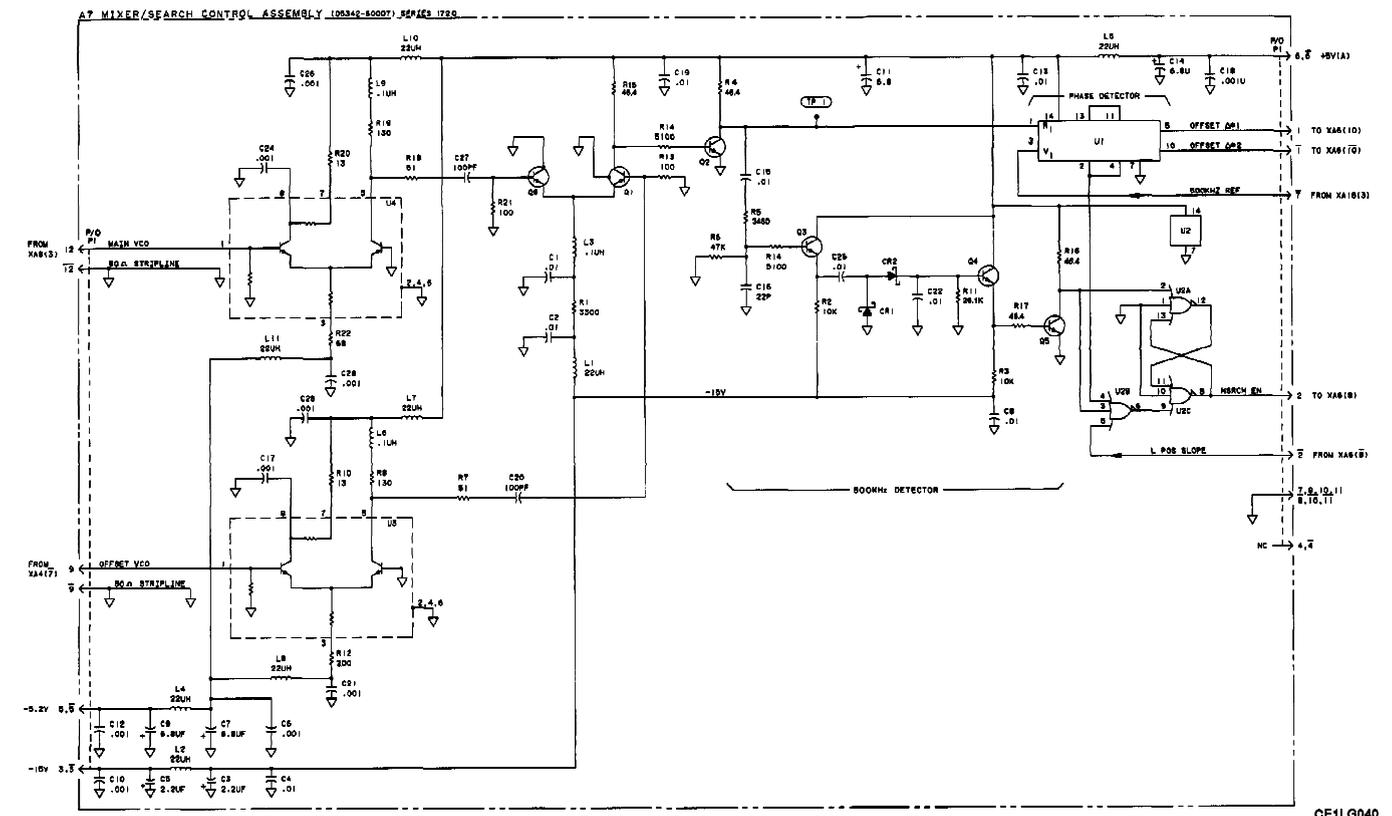
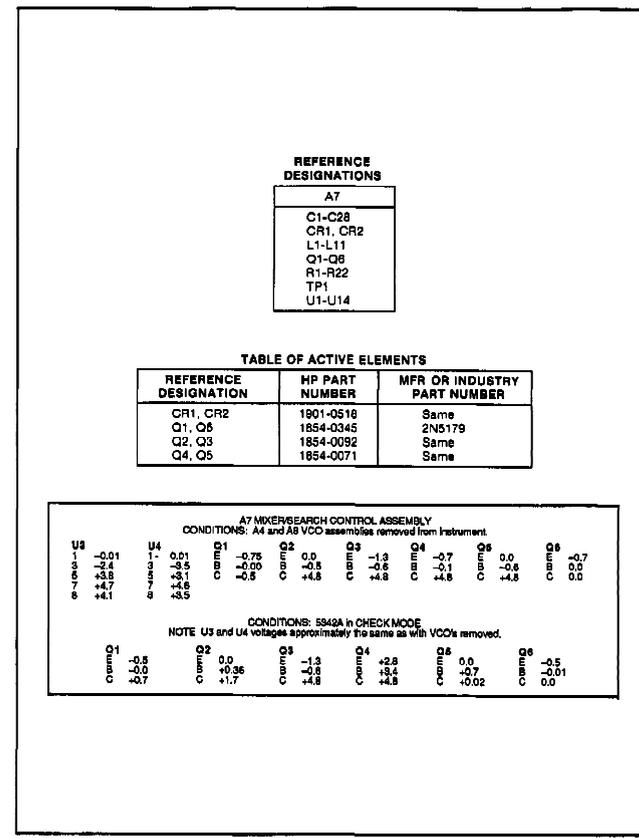


CE1LG038

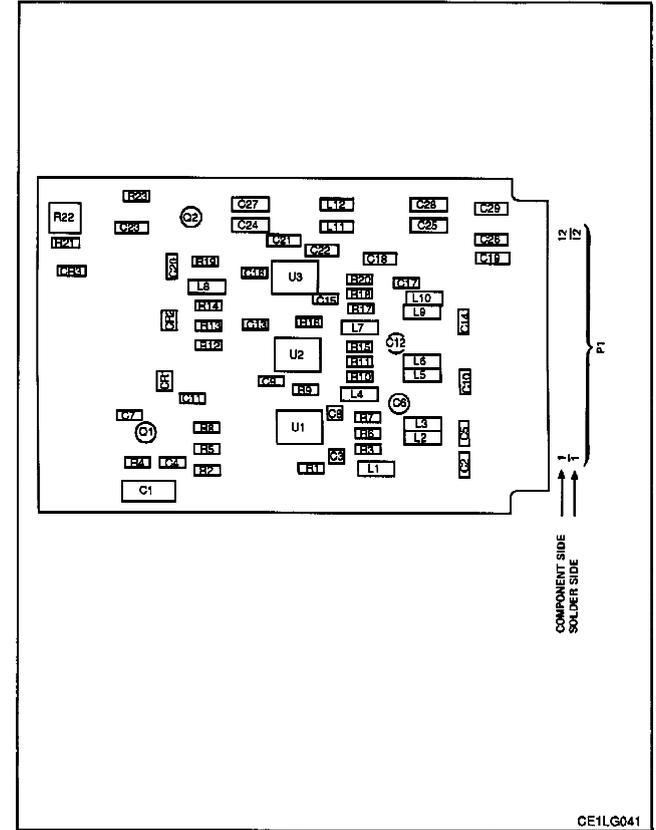
FO Figure 8-29. A6 Offset Loop Amp/Search Generator Assembly



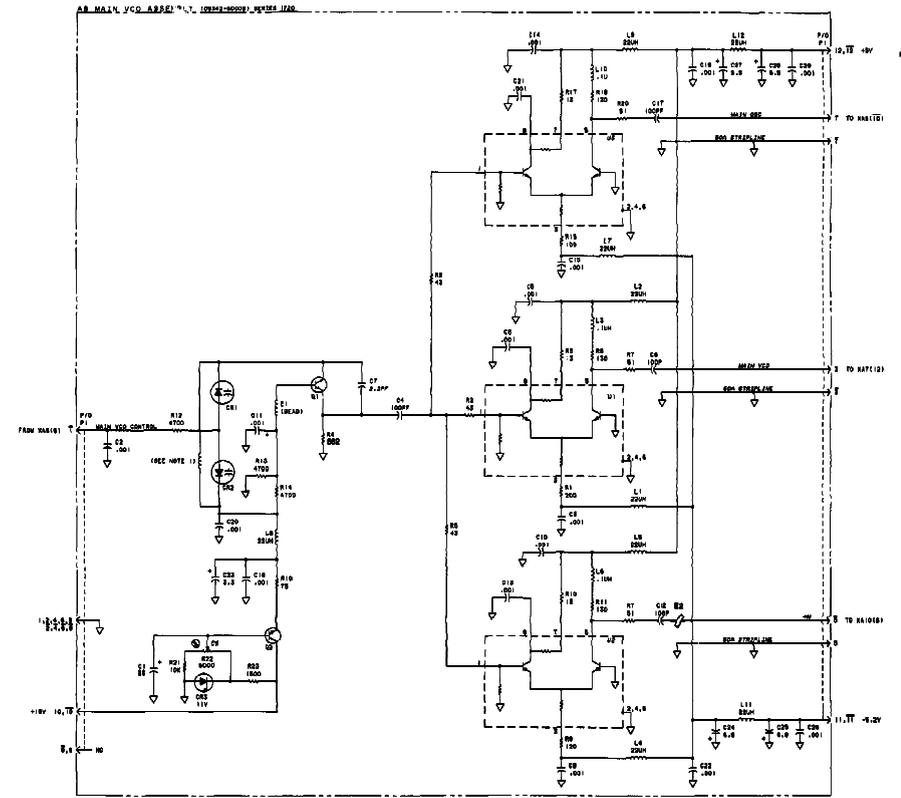
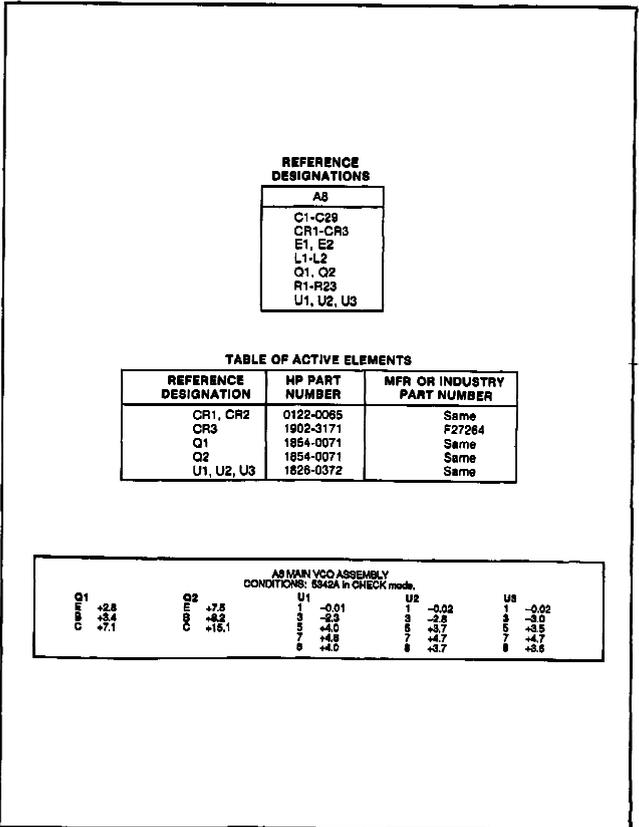
Part of Figure 8-30. A7 Mixer/Search Control Assembly



CE1LG040
 FO Figure 8-30. A7 Mixer/Search Control Assembly
 FP 8-143

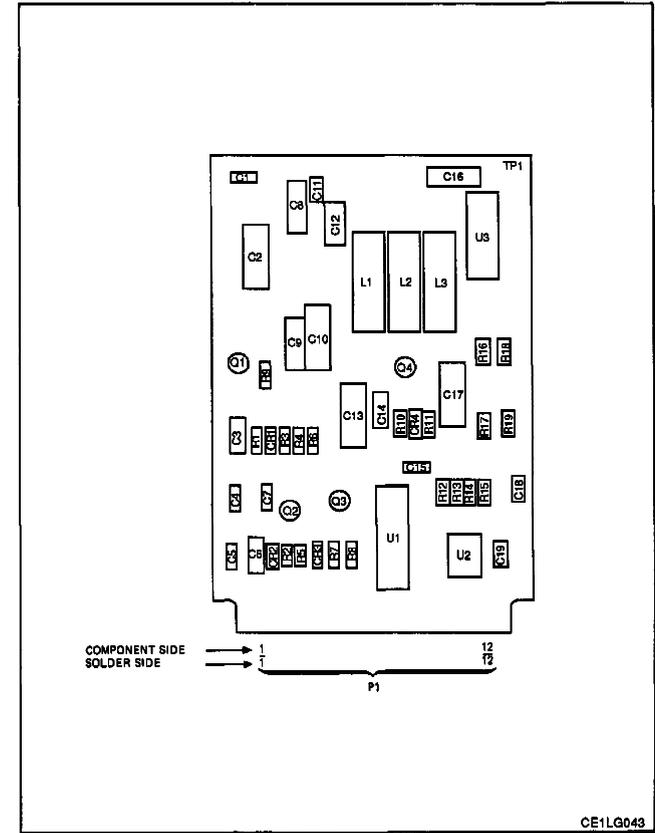


Part of Figure 8-31. AB Main VCO Assembly

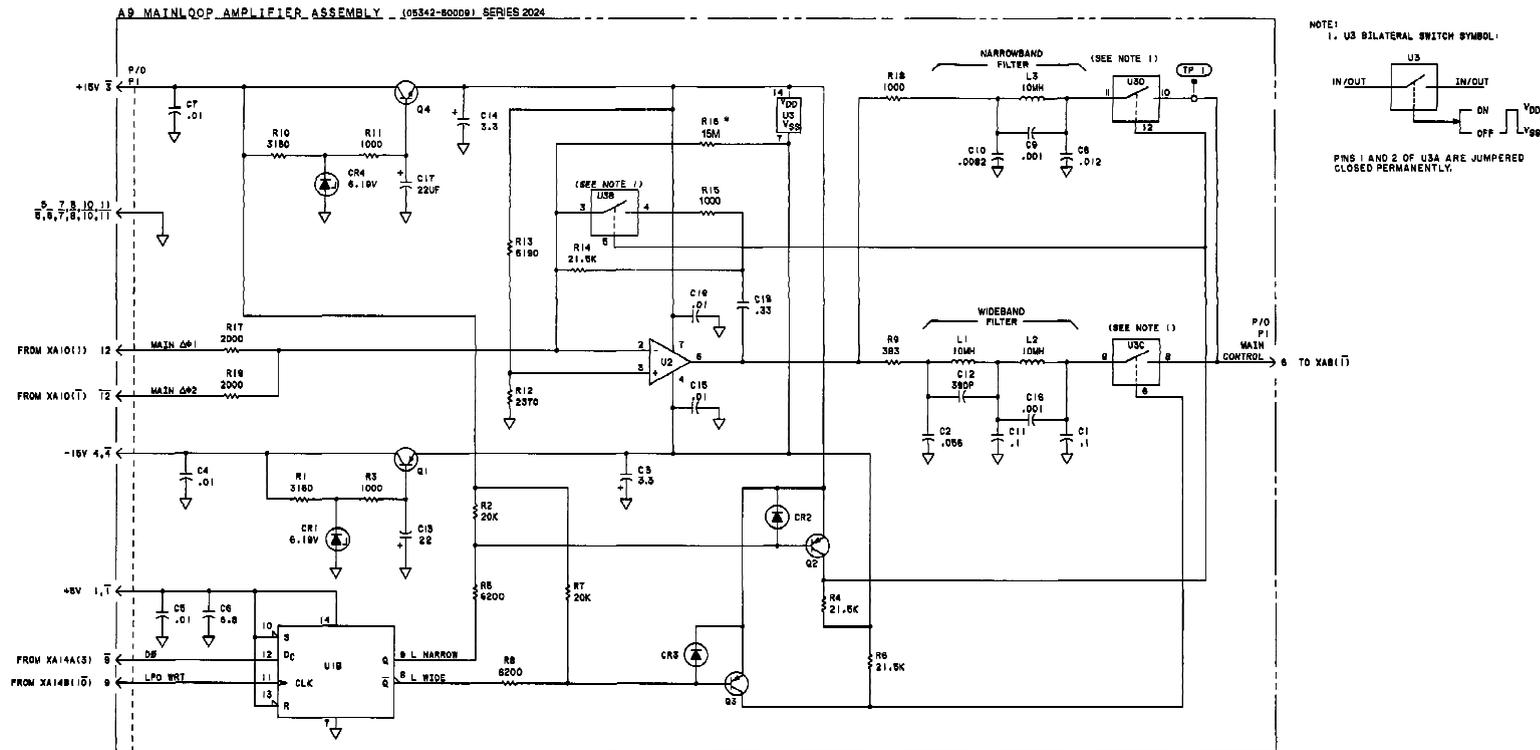
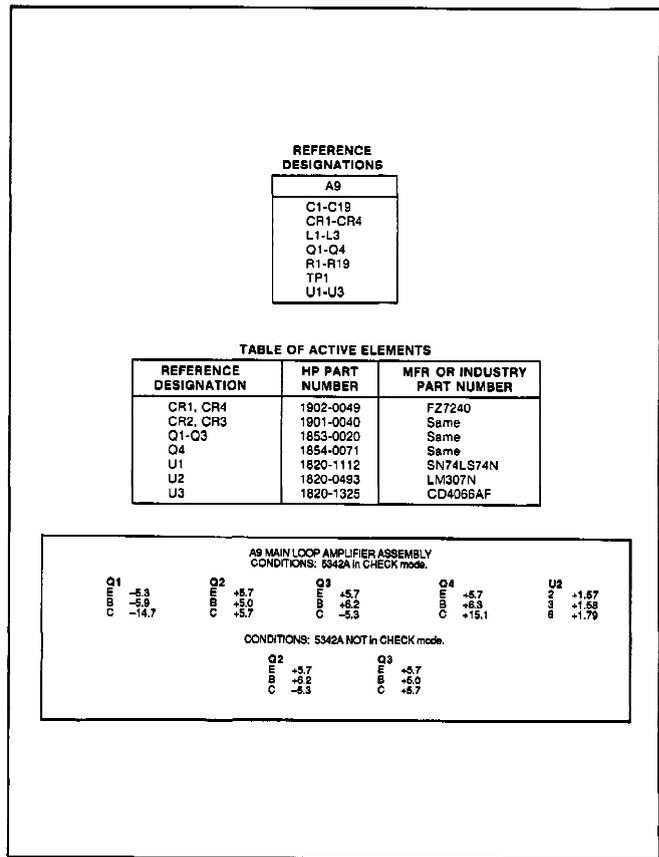


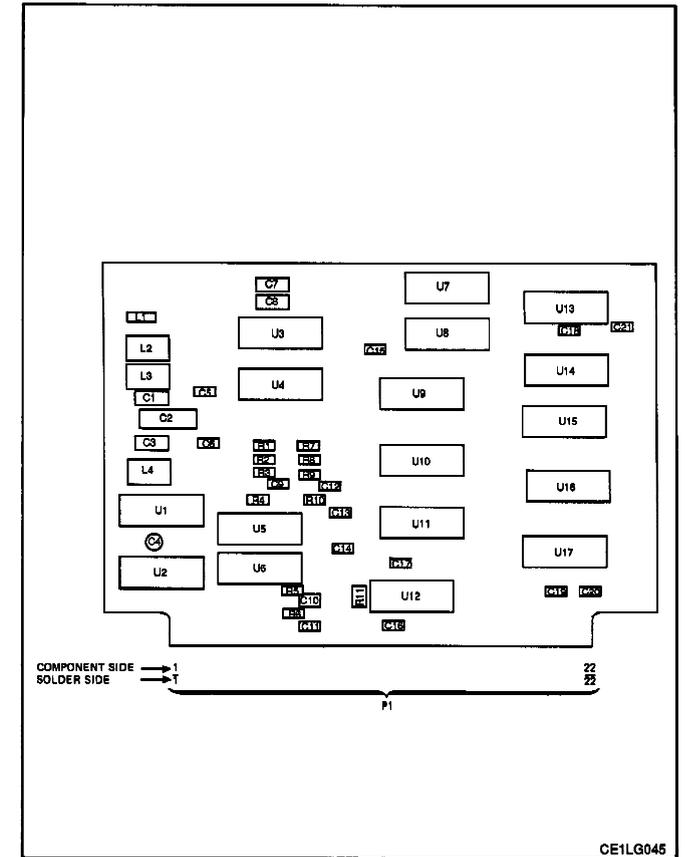
CE1LG042

FO Figure 8-31. A8 Main VCO Assembly



Part of Figure 8-32. A9 Main Loop Amplifier Assembly





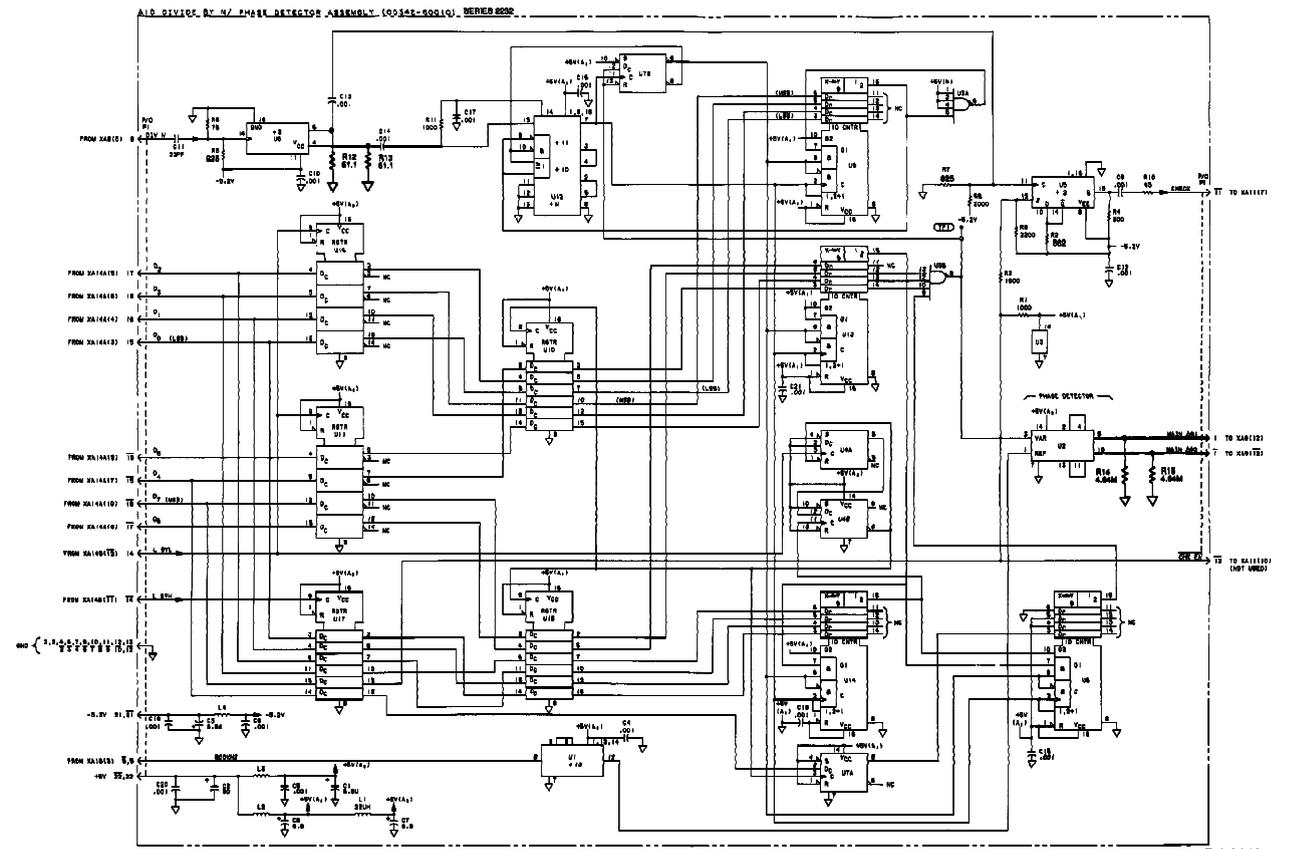
Part of Figure 8-33. A10 Divide-by-N Assembly

REFERENCE DESIGNATIONS

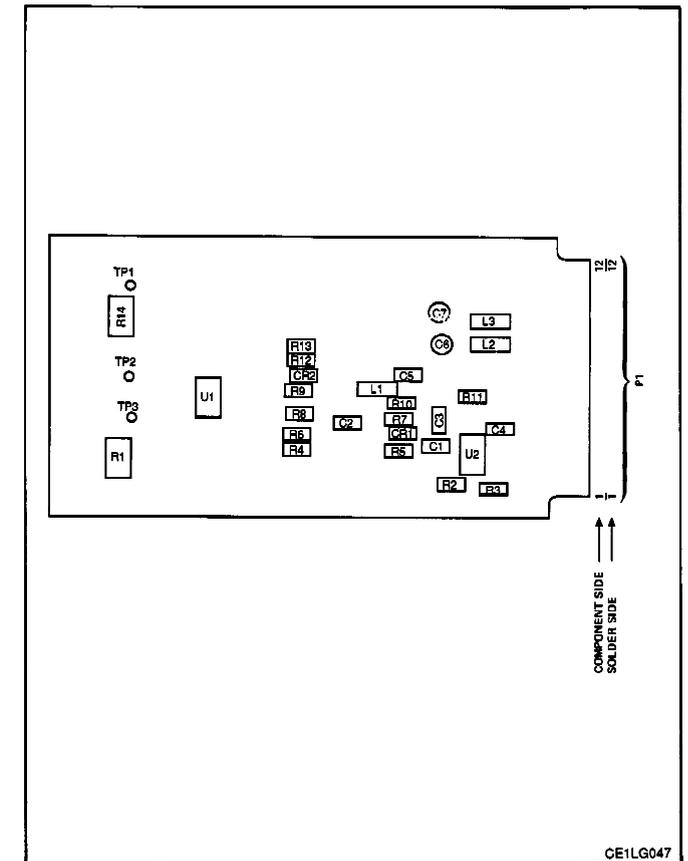
A10
C1-C21
L1-L4
R1-R15
TP1
U1-U17

TABLE OF ACTIVE ELEMENTS

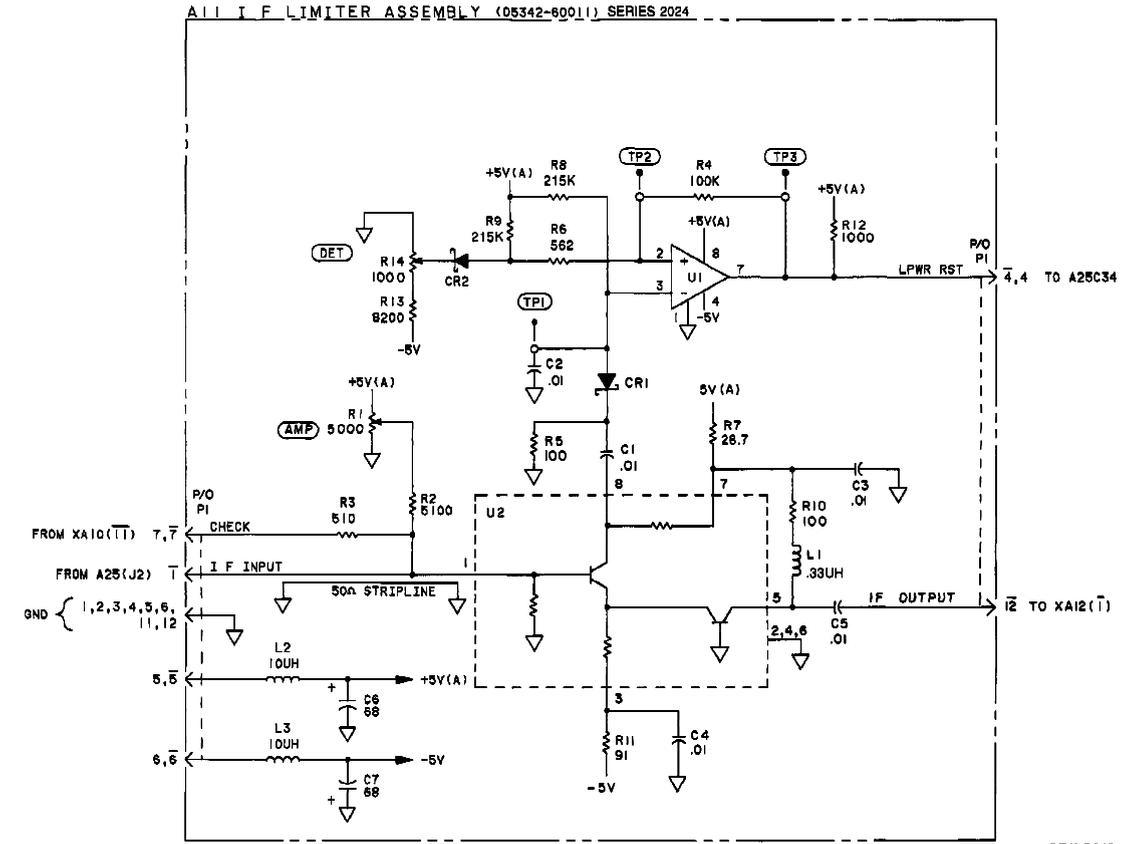
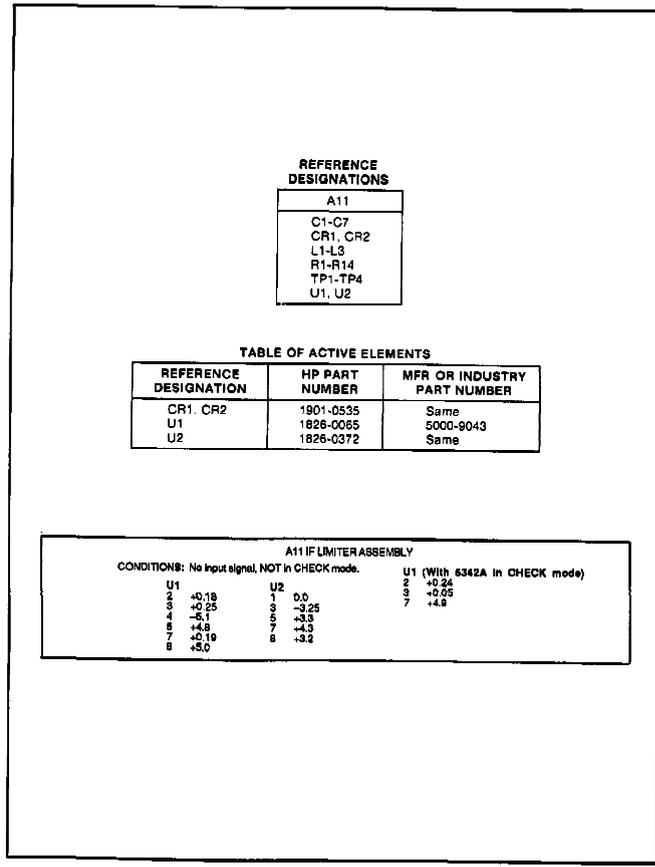
REFERENCE DESIGNATION	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
U1	1820-1251	SN74LS196N
U2	1820-0630	MC4044P
U3	1820-0069	7420PC
U4	1820-1112	SN74LS74N
U5	1820-1225	MC10231P
U6	1820-2000	Same
U7	1820-0693	74S74PC
U8, U9, U13, U14	1820-1429	AM74LS160N
U10, U15, U17	1820-1198	AM74LS174N
U11, U16	1820-1195	AM74LS175N
U12	1820-1888	MC12013L



CE1G046
 FO Figure 8-33. A10 Divide-by-N Assembly
 FP 8-149

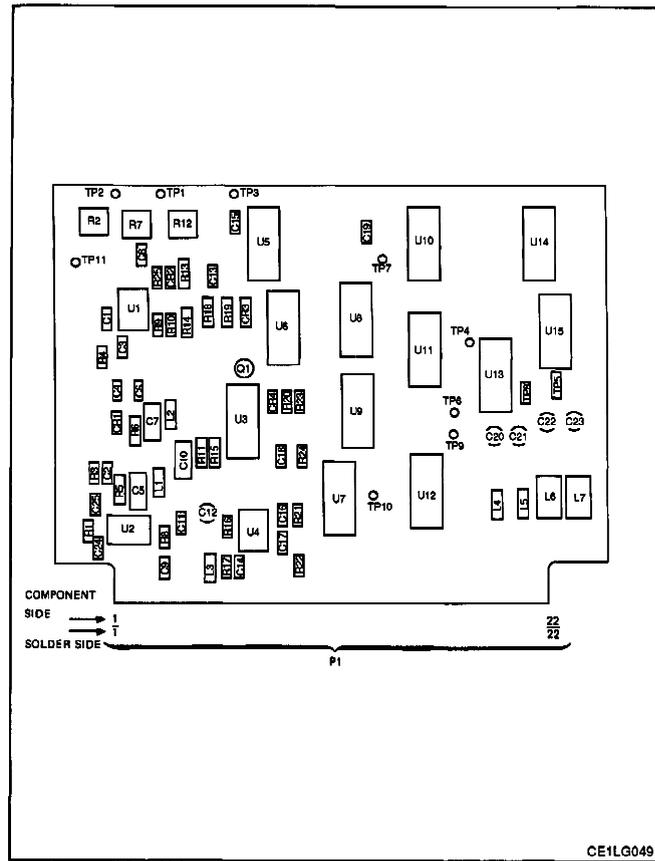


Part of Figure 8-34. A11 IF Limiter Assembly

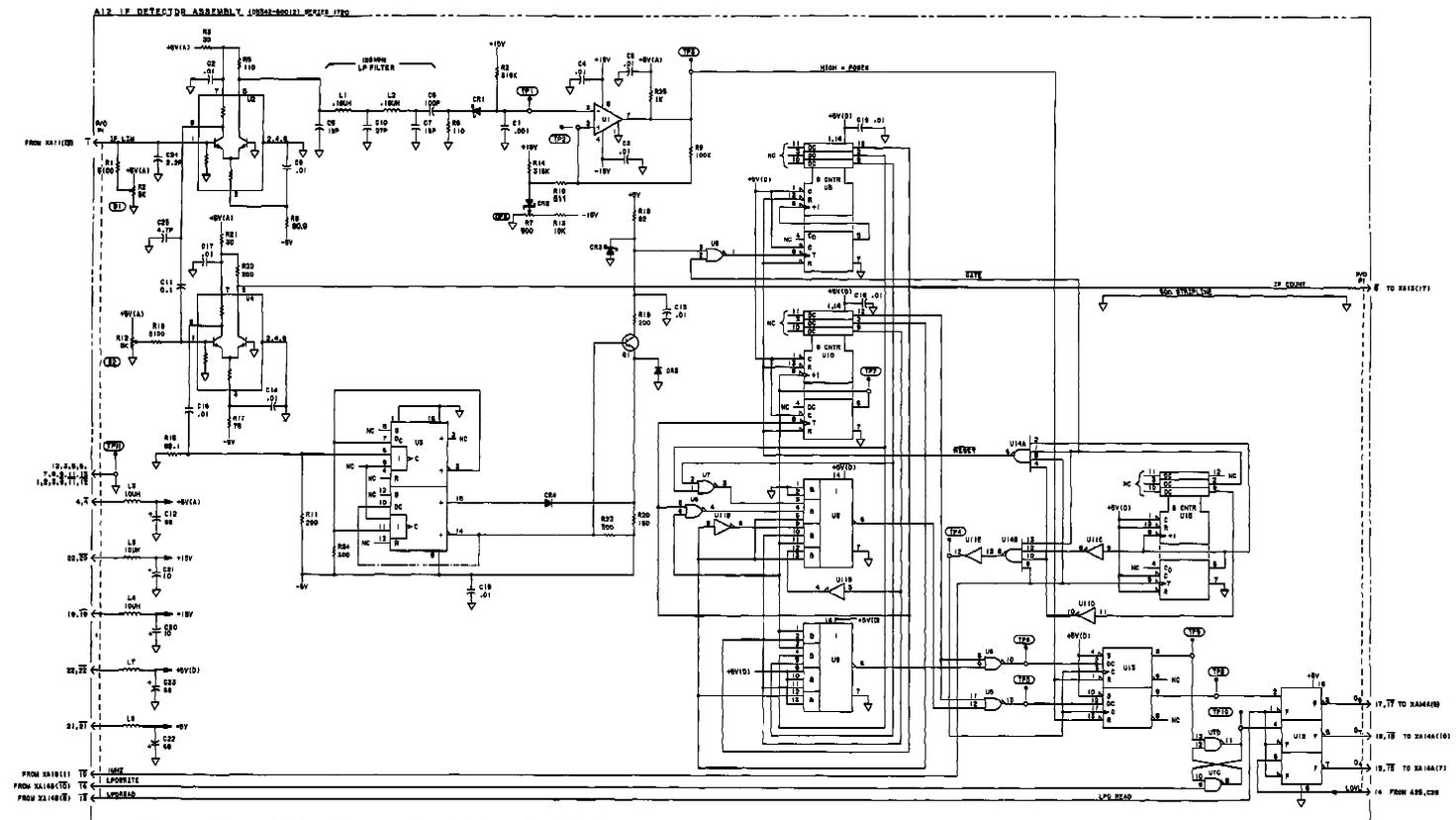
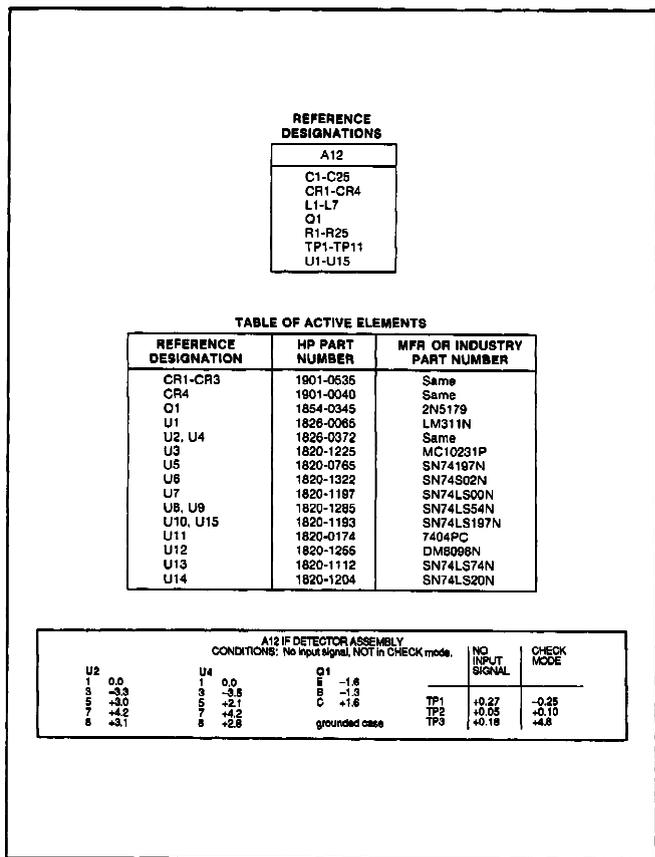


CE1LG048

FO Figure 8-34. A11 IF Limiter Assembly

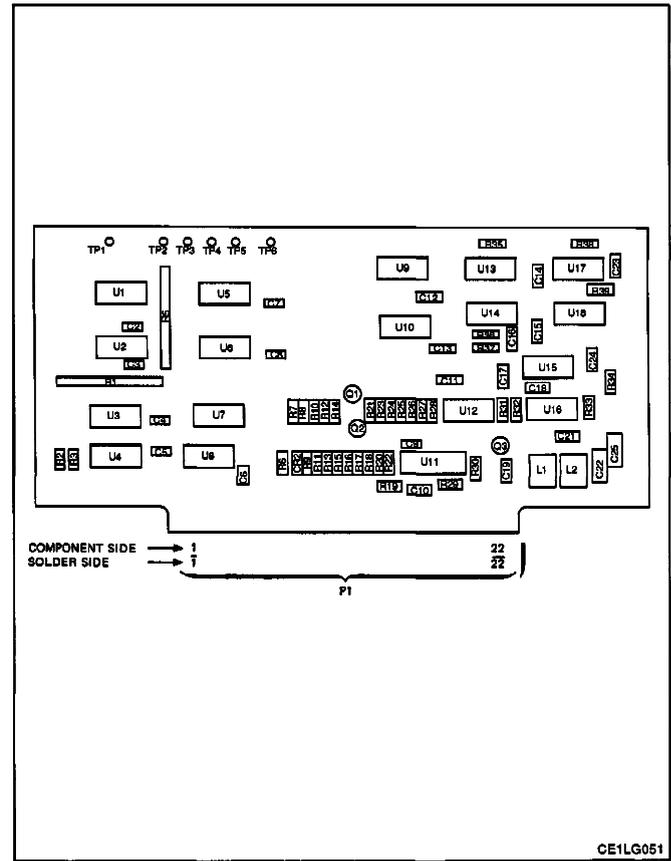


Part of Figure 8-35. A12 IF Detector Assembly



CE1LG050

FO Figure 8-35. A12 IF Detector Assembly



CE1LG051

Part of Figure 8-36. A13 Counter Assembly

REFERENCE DESIGNATIONS

A13	
C1-C25	
CR1, CR2	
L1, L2	
Q1, Q2	
R1-R34	
TP1-TP8	
U1-U18	

Deleted: C1, C20, CR1, R4

TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
CR1, CR2	1901-0040	Same
Q1, Q2	1354-0071	Same
U1, U2	1820-2316	Same
U3, U7	1820-1199	SN74LS04N
U4	1820-1112	SN74LS74N
U5, U6, U9, U10		SN74LS253N
U8	1820-1197	SN74LS00N
U11	1820-1850	MC10212P
U12, U16	1820-1223	MC10231P
U13, U14	1820-1251	SN74LS196N
U17, U18	1820-1251	SN74LS196N
U15	1820-1052	MC10125L

A13 COUNTER ASSEMBLY
CONDITIONS: No Input signal; SAMPLE RATE to HOLD.

Q1	Q2	Q3
-1.5	-1.5	-1.5
-0.5	-0.5	-0.5

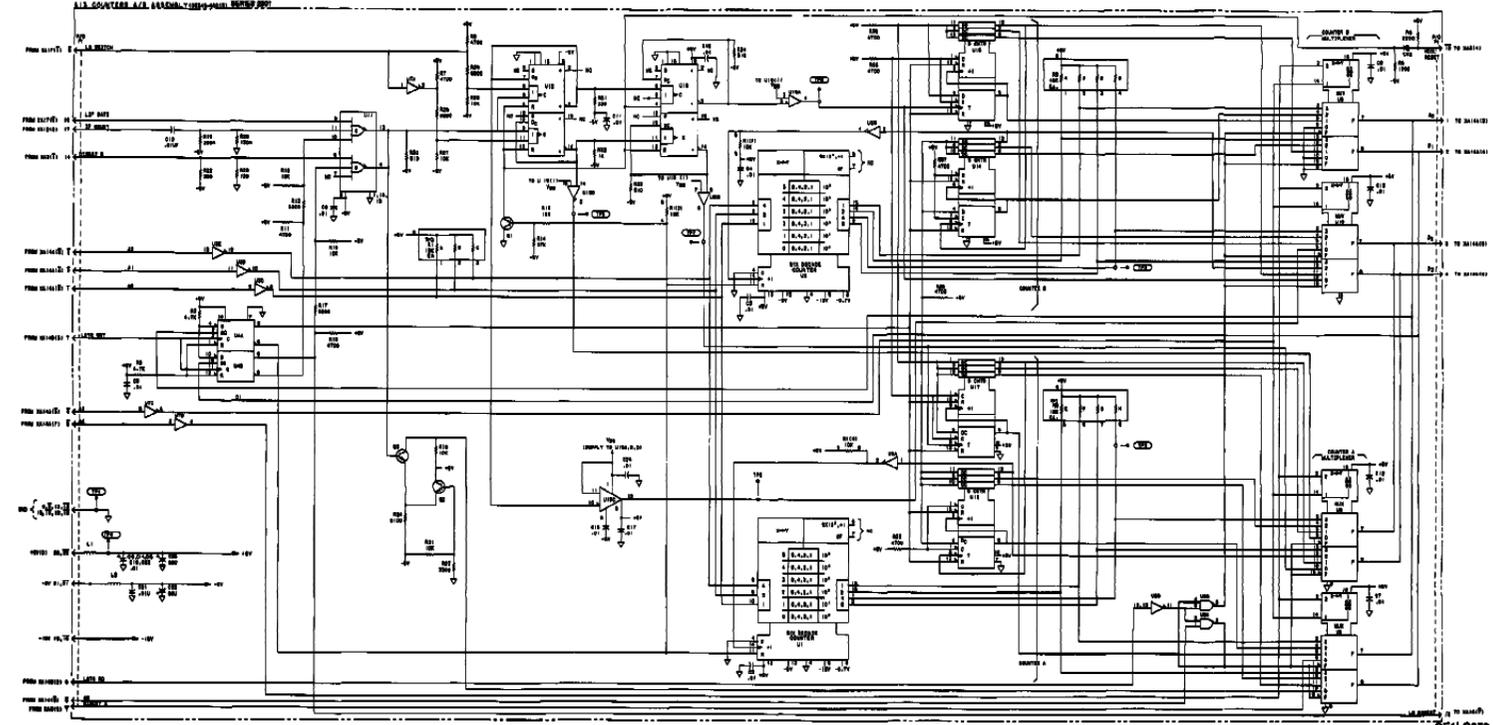


Figure 8-36. A13 Counter Assembly
FP 8-155

REFERENCE DESIGNATIONS

A14
C1-C24
CR1-CR3
L1
R1-R21
S1, S2
TP1-TP6
U1-U24

TABLE OF ACTIVE ELEMENTS

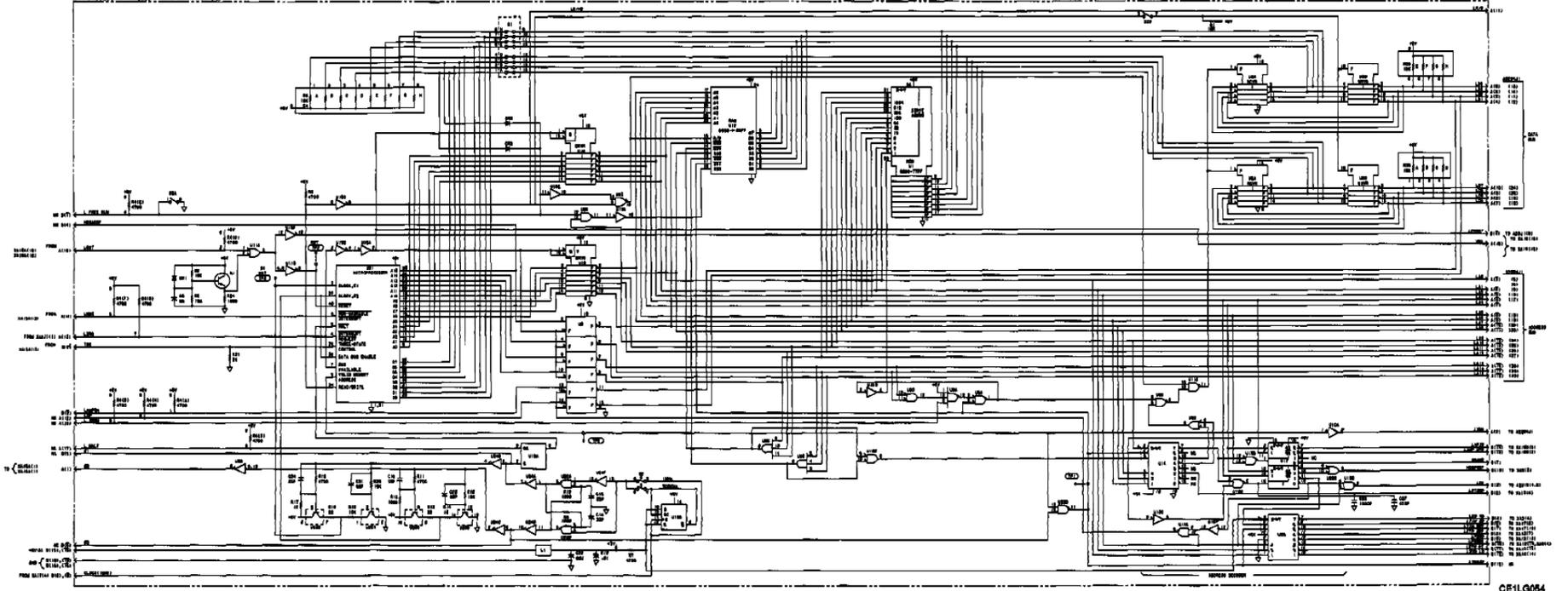
REFERENCE DESIGNATION	HP PART NUMBER	MFG OR INDUSTRY PART NUMBER
CR1-CR3	1801-0040	Same
Q1	1884-0874	Same
U1	1818-0898	Same
U2, U3	1820-1081	AM8726
U4	1818-0897	Same
U5, U22	1820-1197	SN74LS00N
U6	1820-1144	SL362PC
U7	1818-0706	Same
U8	1820-1255	DM8098N
U9	1820-1202	6LS10PC
U10, U15, U24	1820-1198	SN74LS04N
U11	1820-1425	SN74LS192N
U12	1818-0136	MC9810L-1
U13	1820-1206	7SL332A
U14	1820-1240	SN74S138N
U16, U18	1820-1388	DM8098N
U17	1820-1072	SN74S199N
U19	1820-1112	SN74LS14N
U20	1820-1240	SN74S138N
U21	1820-1480	MC6800L
U23	1820-1804	MPC8542

AN MICROPROCESSOR ASSEMBLY

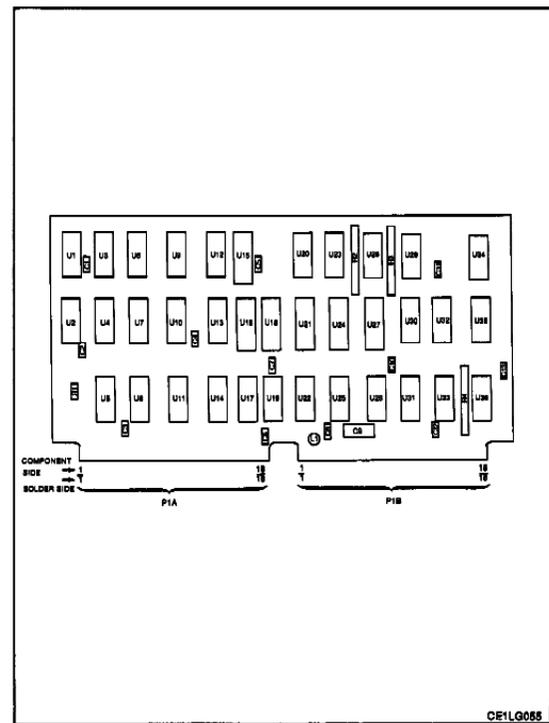
Legend Chart:
With the kit setup described in Table A4, page 1, 2, 3, the following symptoms should be observed:

SYM	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15	U16	U17	U18	U19	U20	U21	U22	U23	U24
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16

*Refer to Table A4.



CE1LG054
FD Figure 8-37. A14 Microprocessor Assembly



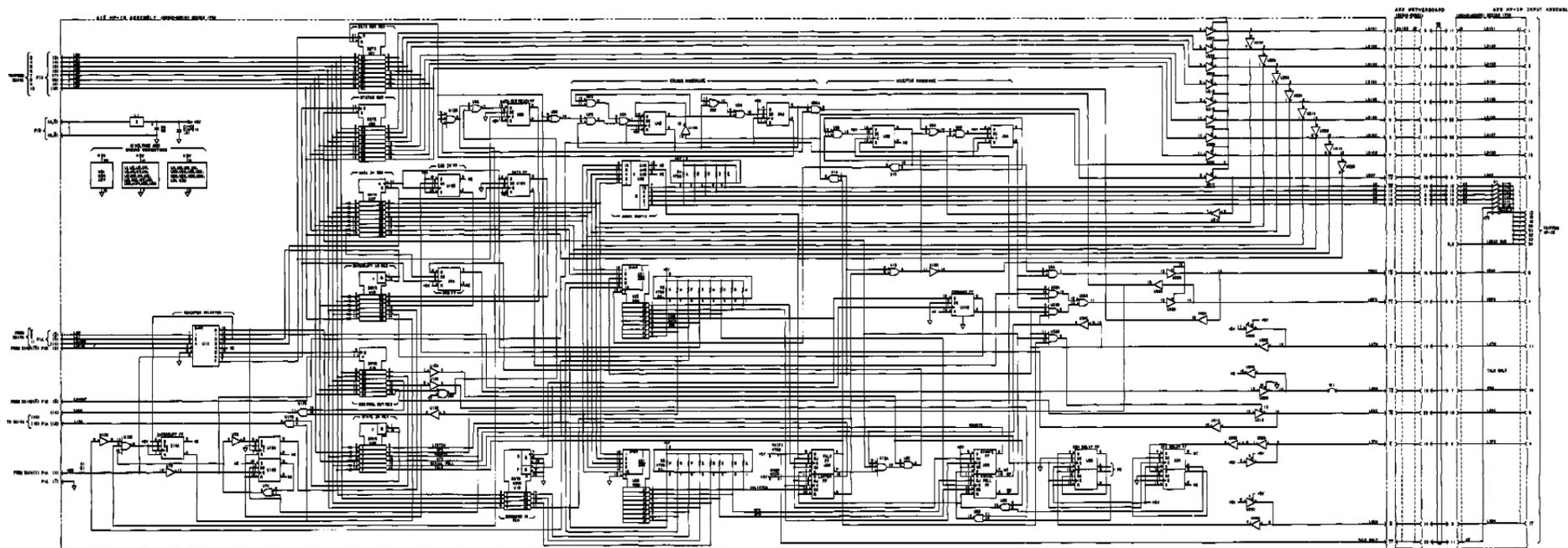
Part of Figure 8-38. A15 HP-IB Assembly

REFERENCE DESIGNATIONS

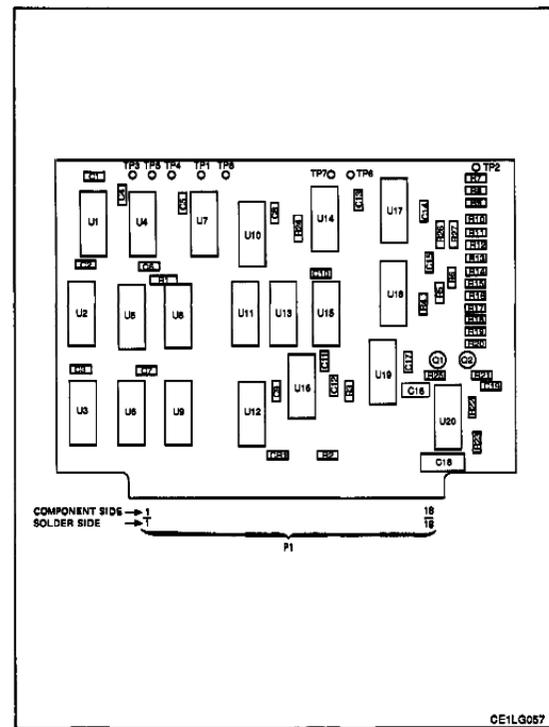
A15
C1-C3
L1
R1-R4
U1-U36

TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	HP PART NUMBER	MPG OR INDUSTRY PART NUMBER
U1, U36	1820-1197	SN74LS00N
U2, U5, U6, U9	1820-1144	9LS02PC
U3, U4, U7	1820-1112	SN74LS74N
U10, U14, U19, U24, U26		
U7	1820-1211	SN74LS88N
U11	1820-1216	SN74LS138N
U12	1820-1206	SN74LS27N
U13	1820-1199	SN74LS04N
U15	1820-1885	DM74LS175N
U16	1820-1196	AM74LS174N
U17	1820-1198	SN74LS03N
U18, U30	1820-1369	DM8090N
U20, U29	1820-1282	SN74LS108N
U21, U24, U27	1820-1887	SN74LS374PC
U22, U25, U28, U31	1820-1869	MC3448P
U23	1818-1154	Same
U28	1818-1155	Same
U32	1820-1202	9LS10PC
U33	1820-0804	93L24PC



OE1L0056



CE1LG057

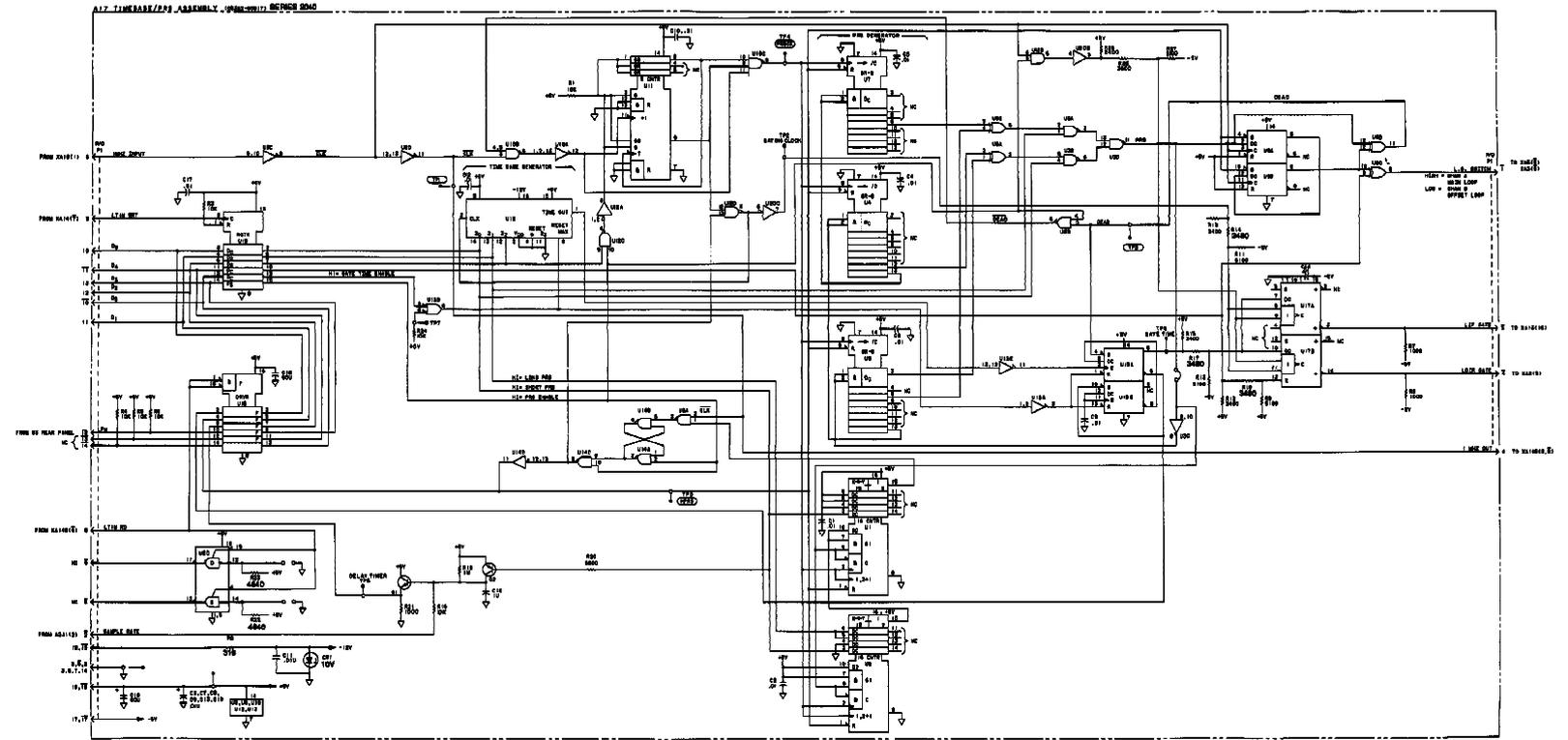
Part of Figure 8-41. A17 Timing Generator Assembly

REFERENCE DESIGNATIONS

A17
C1-C19
CR1
Q1, Q2
R1-R23
TP1-TP8
U1-U20

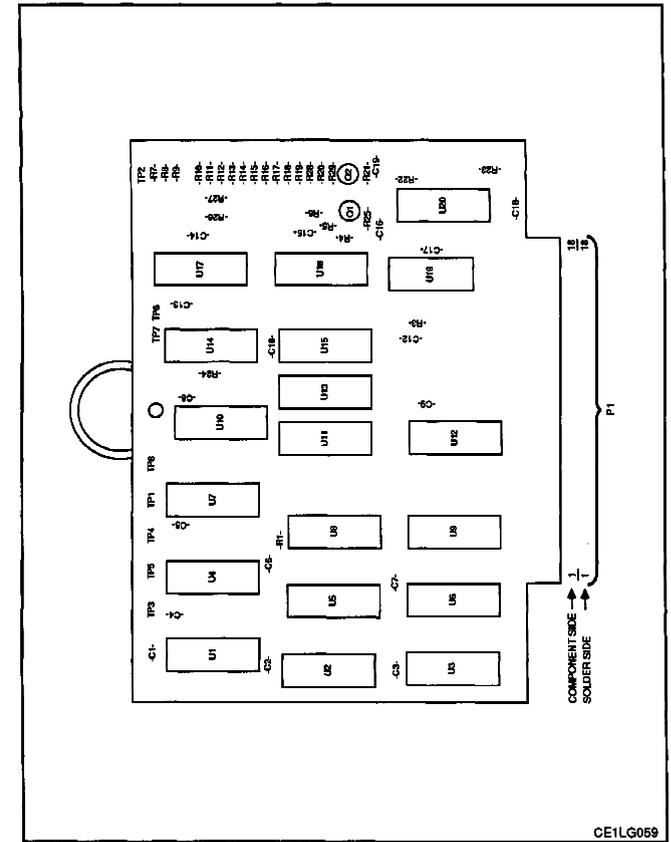
TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	MP PART NUMBER	MPR OR INDUSTRY PART NUMBER
CR1	1902-3182	F27268
Q1	1854-0860	S795740
Q2	1853-0036	Same
U1, U2	1820-1430	AM74LS161N
U3, U6, U12, U13	1820-1197	SN74LS00N
U4, U5, U7	1820-1433	SN74LS164N
U8	1820-1211	SN74LS66N
U9, U14, U15	1820-1112	SN74LS74N
U10	1820-1202	9LS10PC
U11	1820-1442	SN74LS290N
U16	1820-1180	MK3009P
U17	1820-1225	MC10231P
U18	1820-1254	DMB095N
U19	1820-1196	AM74LS174N
U20	1820-1255	DMB090N



CE1G068

FO Figure 8-41. A17 Timing Generator Assembly

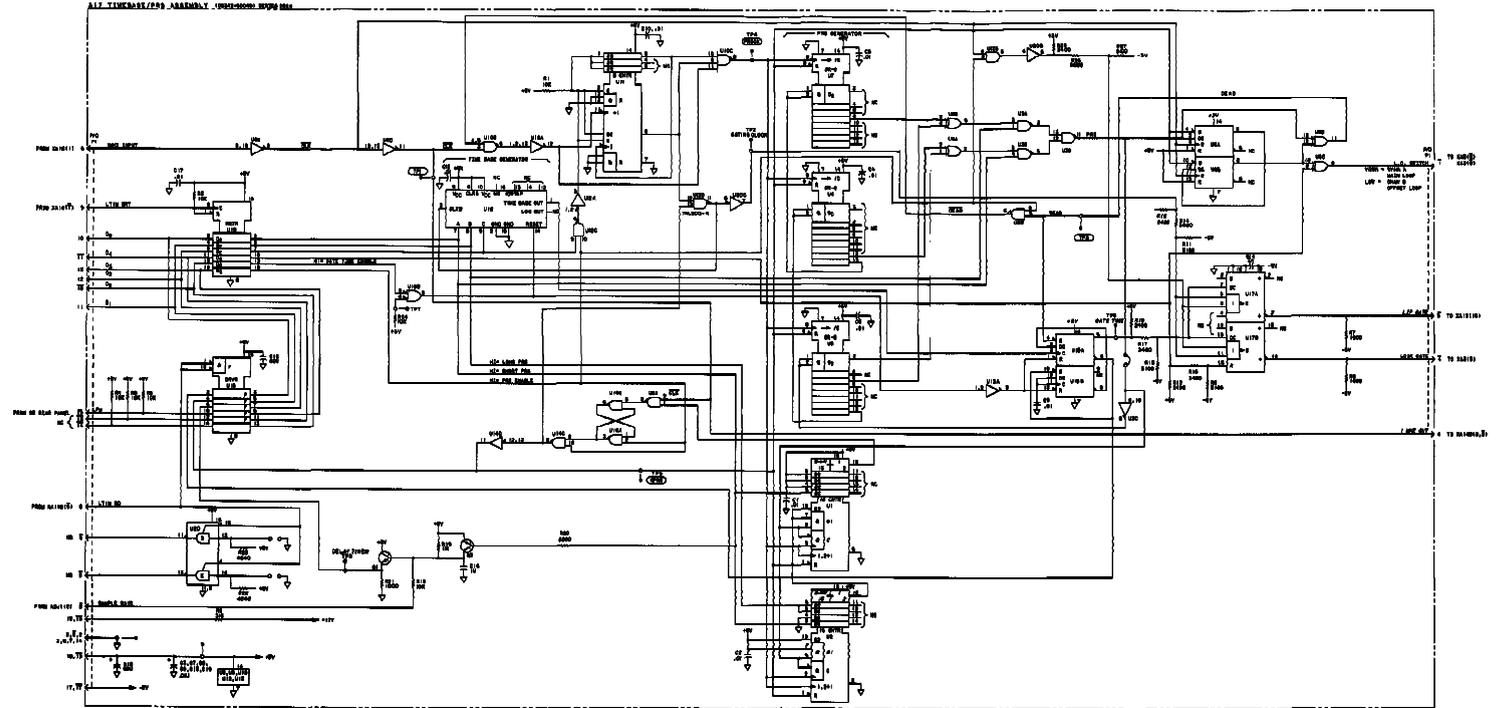


Part of Figure 8-41A. A17 Timing Generator Assembly

REFERENCE DESIGNATIONS
A17
C1-C10, C12-C19
Q1-Q2
R1, R3-R9
TP1-TP10
U1-U20

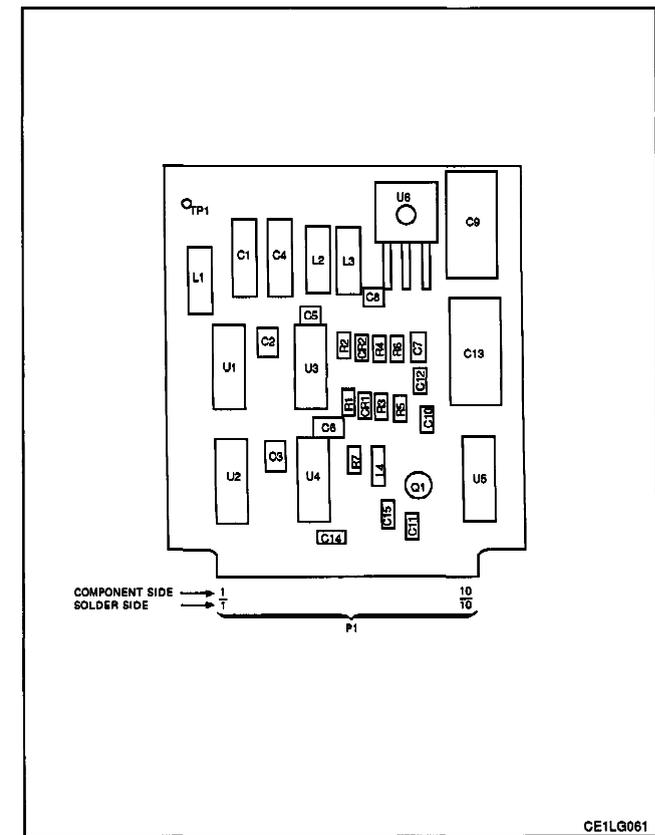
TABLE OF ACTIVE ELEMENTS

REFERENCE DESIGNATION	HP PART NUMBER	MFR OR INDUSTRY PART NUMBER
Q1	1854-0560	SP36740
Q2	1853-0036	1853-0036
U1, U2	1820-1430	SN74LS161N
U3, U8, U12-U14	1820-1197	SN74LS00N
U4, U5, U7	1820-1433	SN74LS164N
U6	1820-1211	SN74LS86N
U9, U15	1820-1112	SN74LS74N
U10	1820-1202	9LS10PC
U11	1820-1442	SN74LS290N
U16	1DB9-0003	1DB9-0003
U17	1820-1225	MC10231P
U18	1820-1254	DM8095N
U19	1820-1196	AM74LS174N
U20	1820-1255	DM8098N

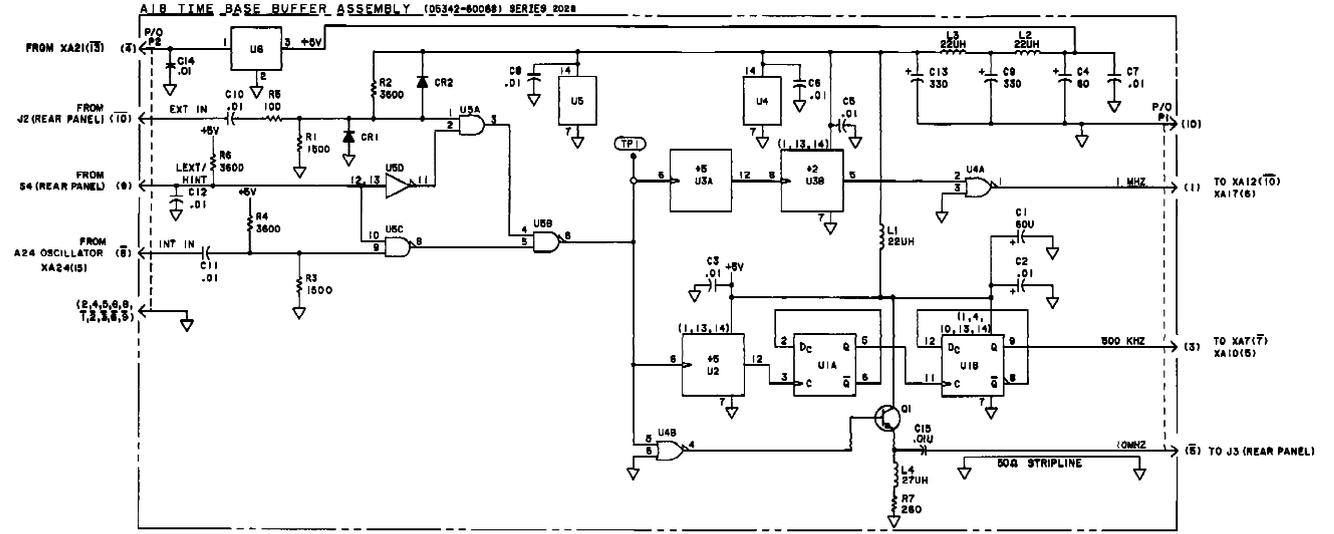
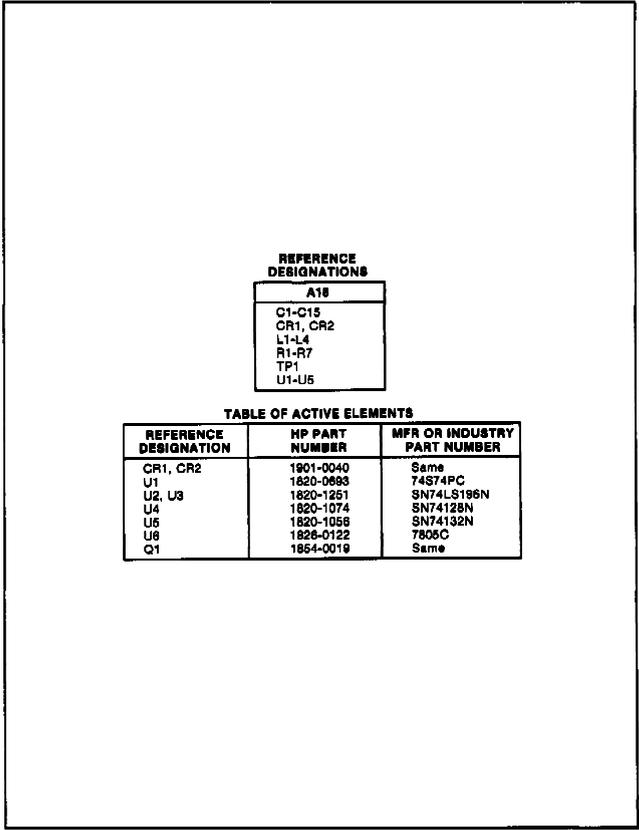


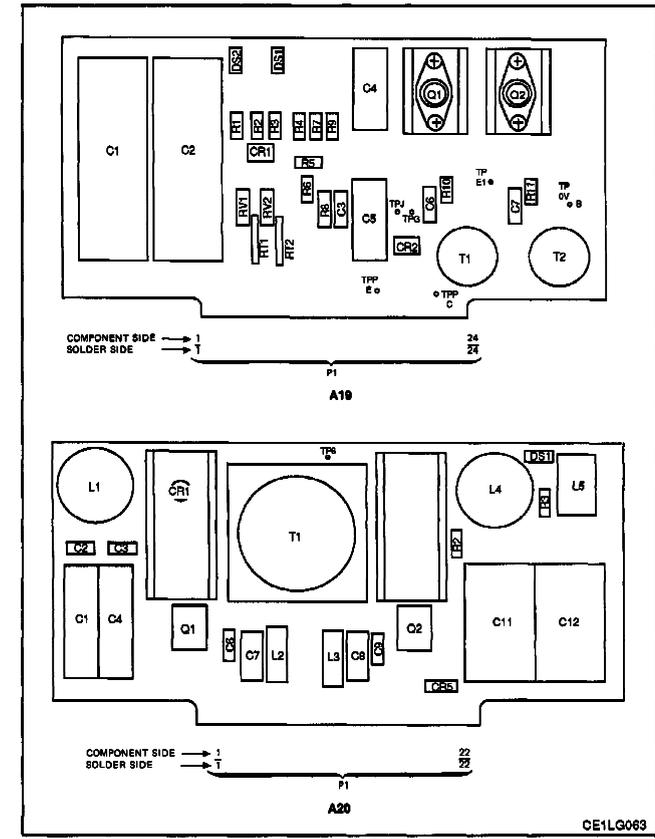
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FO Figure 8-41A. A17 Timing Generator Assembly (SERIES 2826 AND HIGHER)

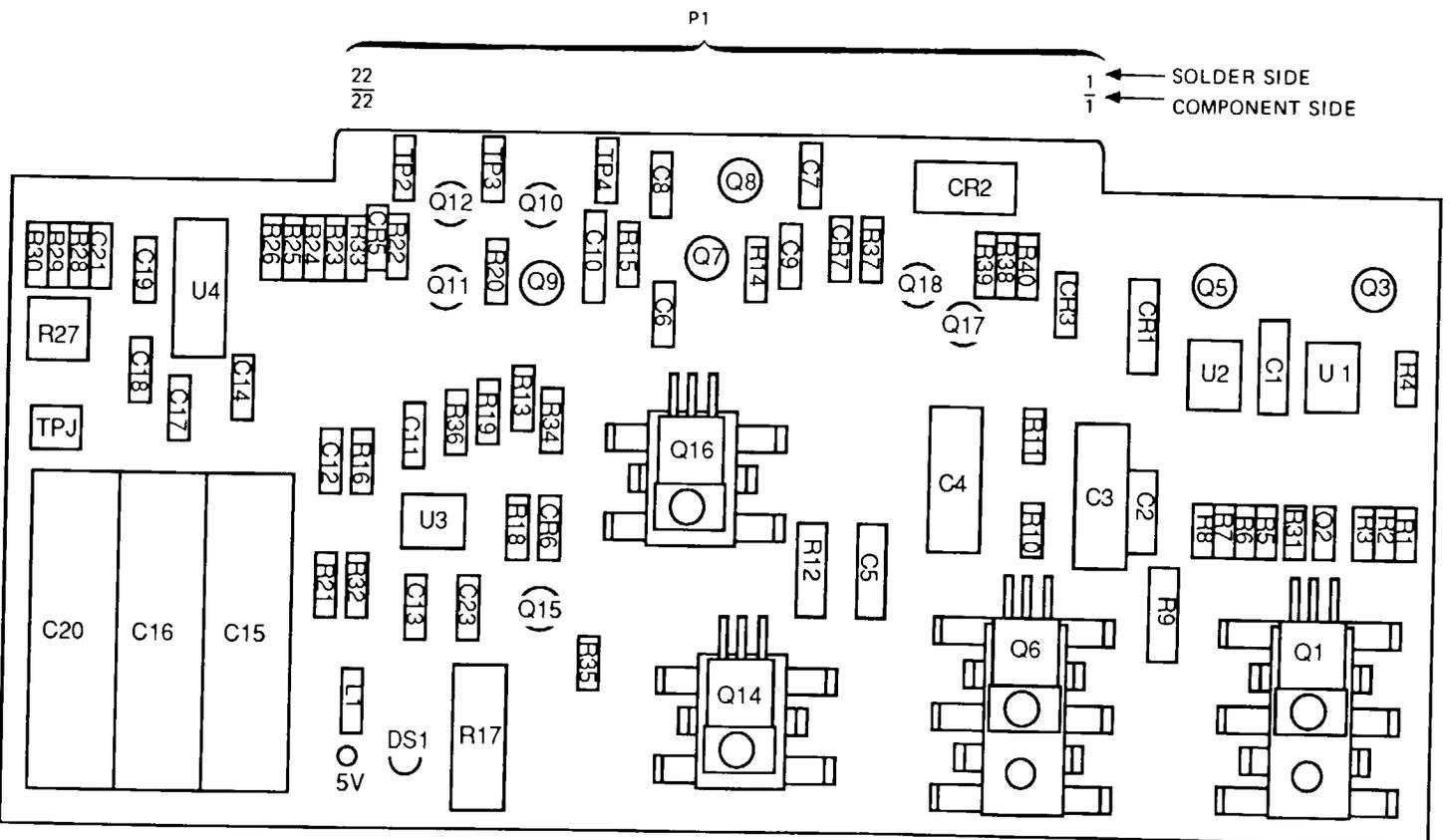


Part of Figure 8-42. A18 Time Base Buffer Assembly



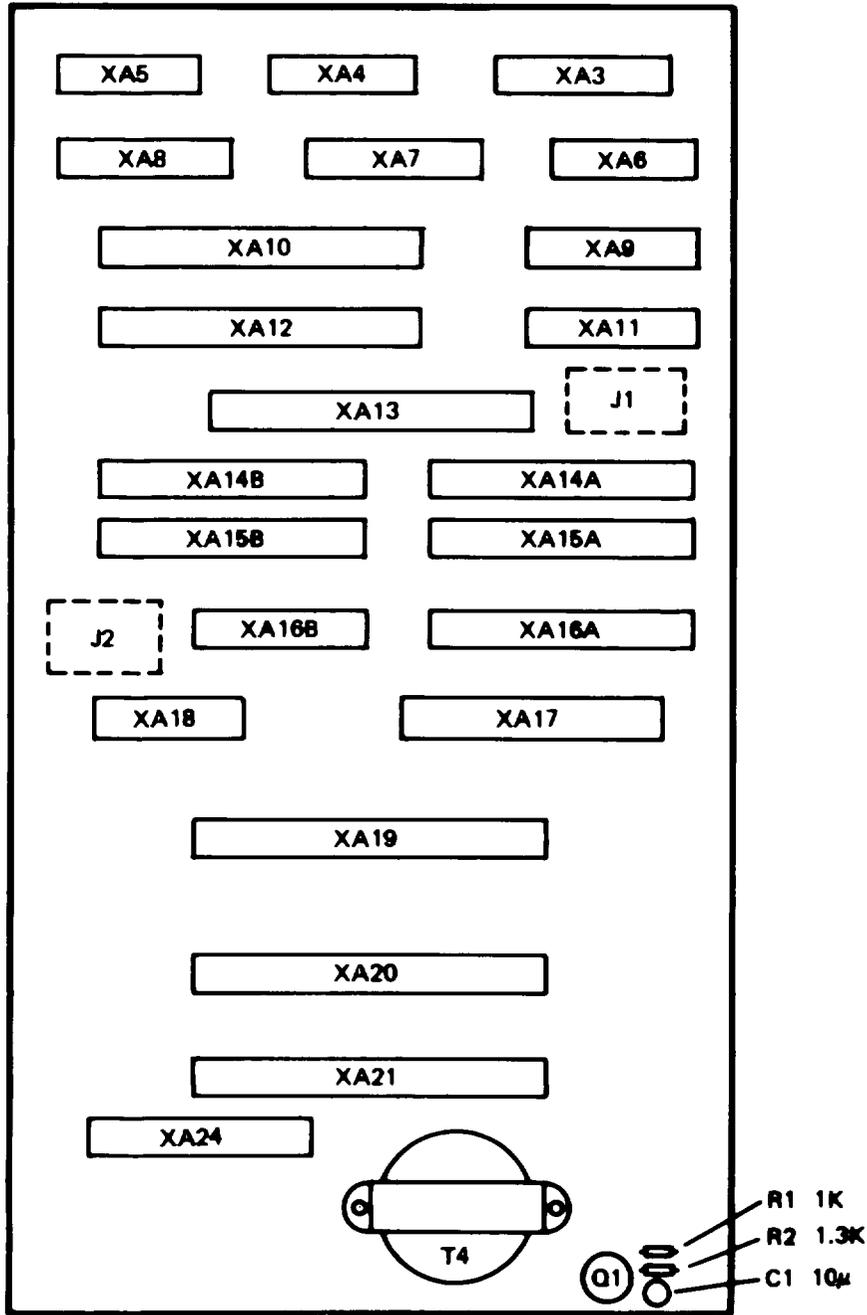


Part of Figure 8-43. A19 through A23 Power Supply, Switch Driver, and Motherboard Assemblies



Part of Figure 8-43. A19 through A23 Power Supply, Switch Driver, and Motherboard Assemblies

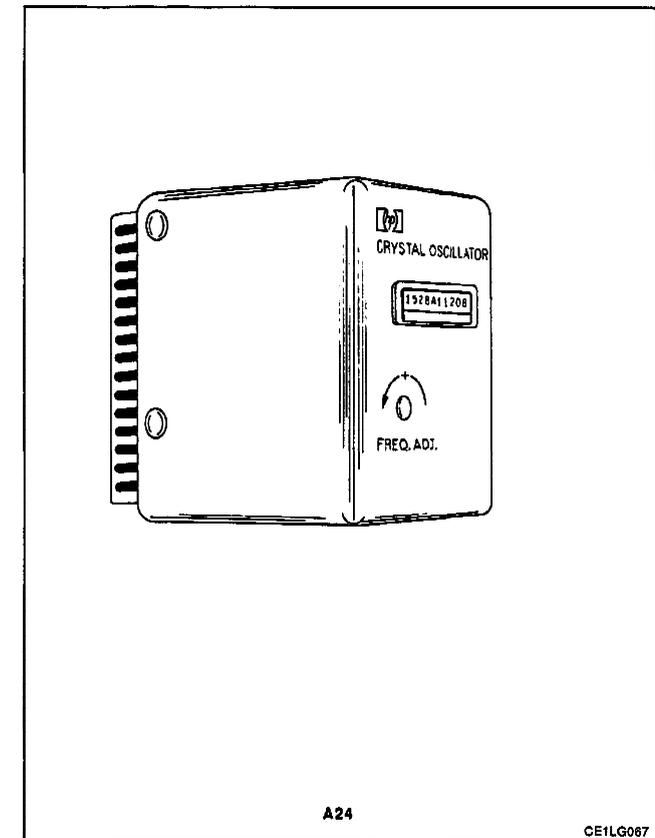
CE1LG064



A22 Motherboard Assembly

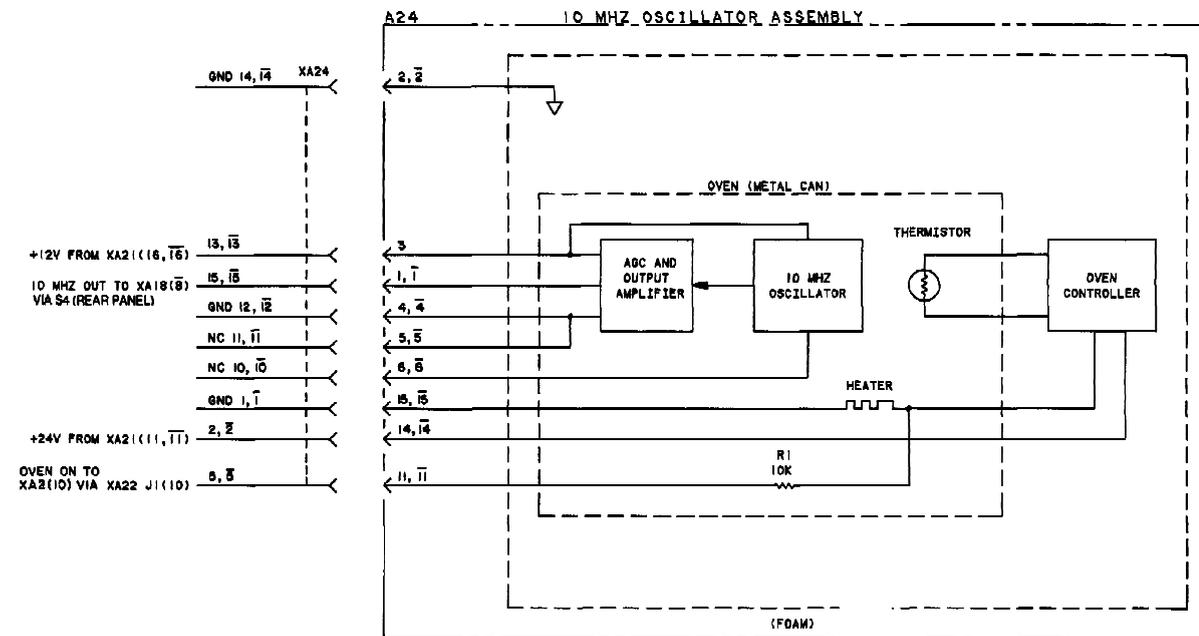
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Part of Figure 8-43. A 19 through A23 Power Supply, Switch Driver, and Motherboard Assemblies



Part of Figure 8-44. A24 Oscillator Assembly

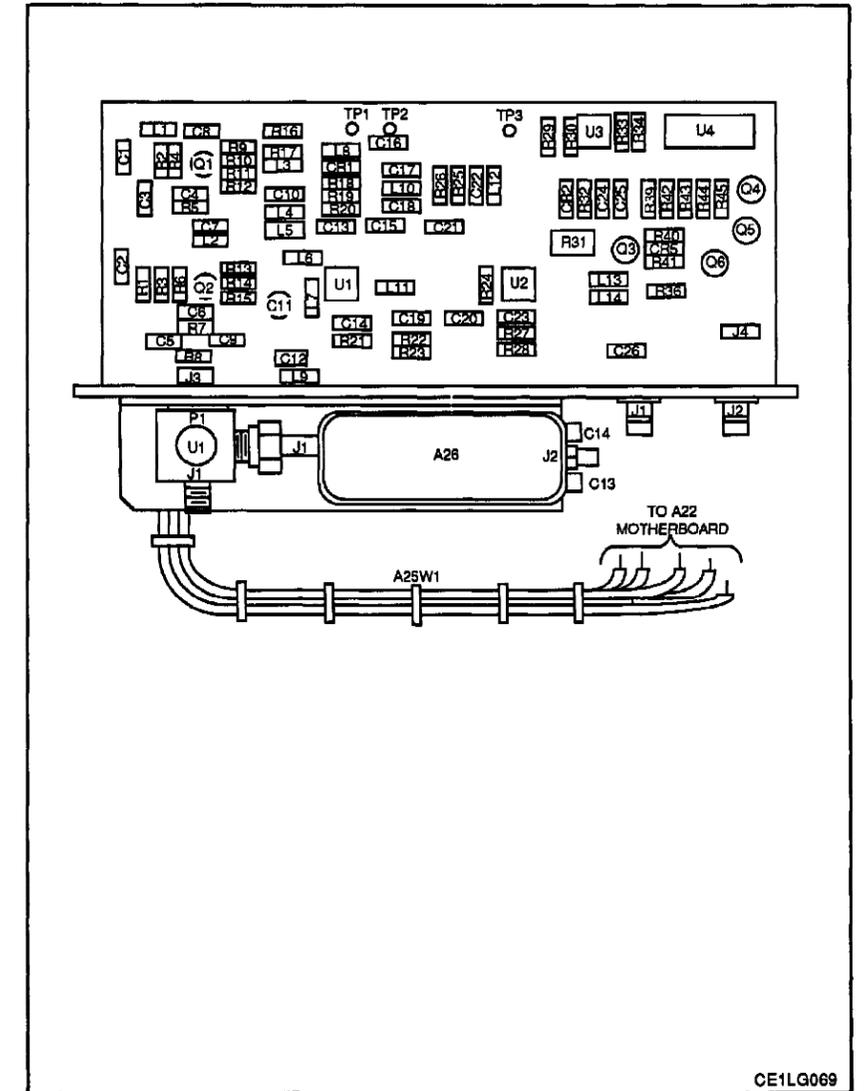
- NOTES:
1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED, ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
 2. UNLESS OTHERWISE INDICATED:
RESISTANCE IN OHMS;
CAPACITANCE IN FARADS;
INDUCTANCE IN HENRIES
 3. ~~DELETED~~
 4. ~~DELETED~~
 5. ~~DELETED~~
- SEE APPENDIX G IN THIS MANUAL FOR ADDITIONAL REPAIR INFORMATION ON THE A24 OSCILLATOR ASSEMBLY



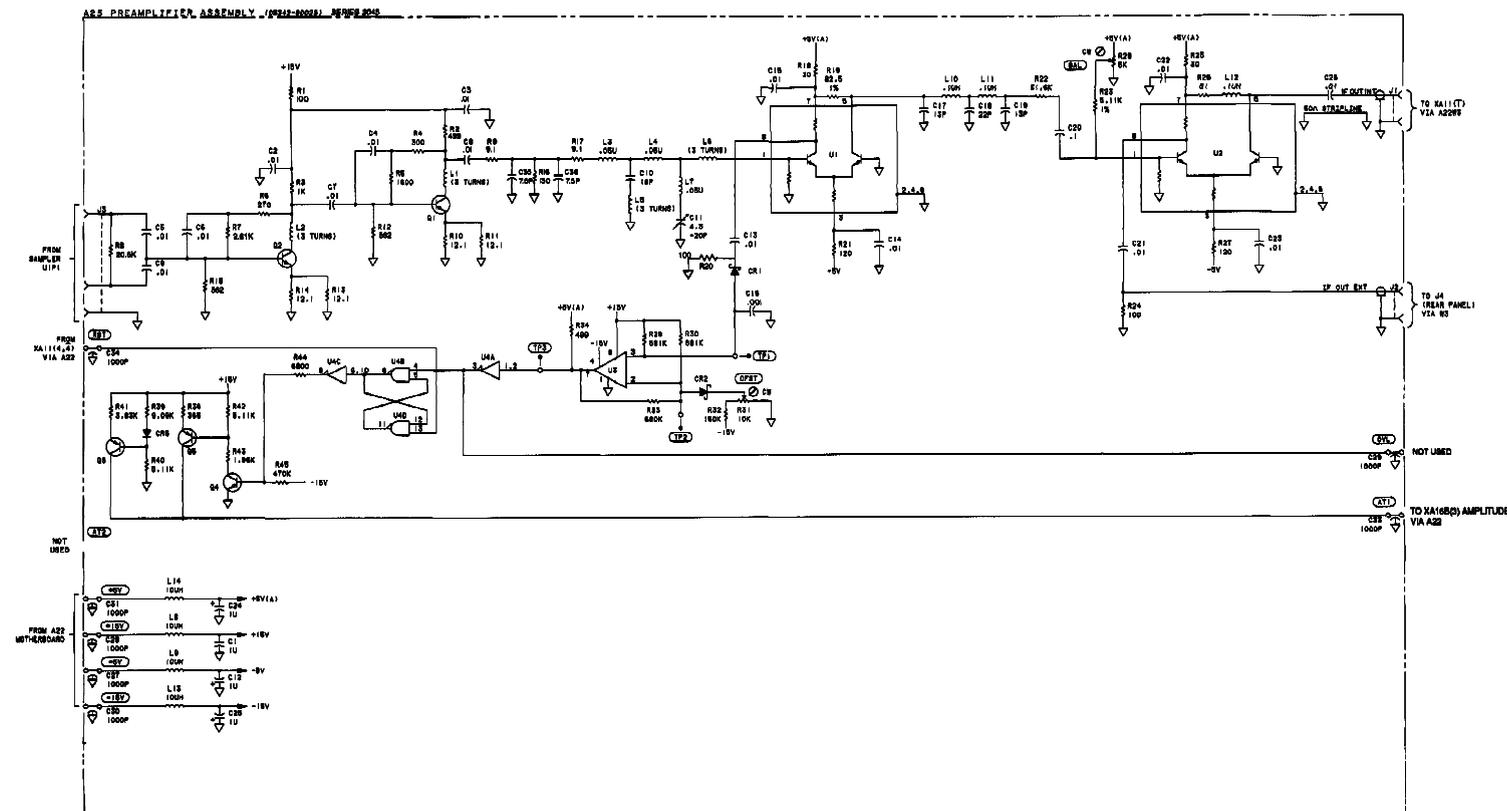
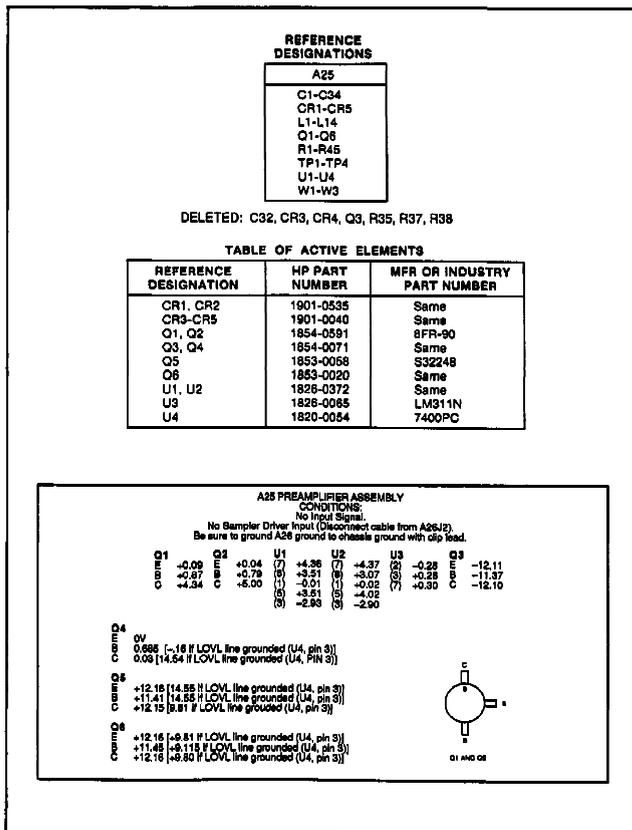
CE1LG068

FO Figure 8-44. A24 Oscillator Assembly

FP 8-169

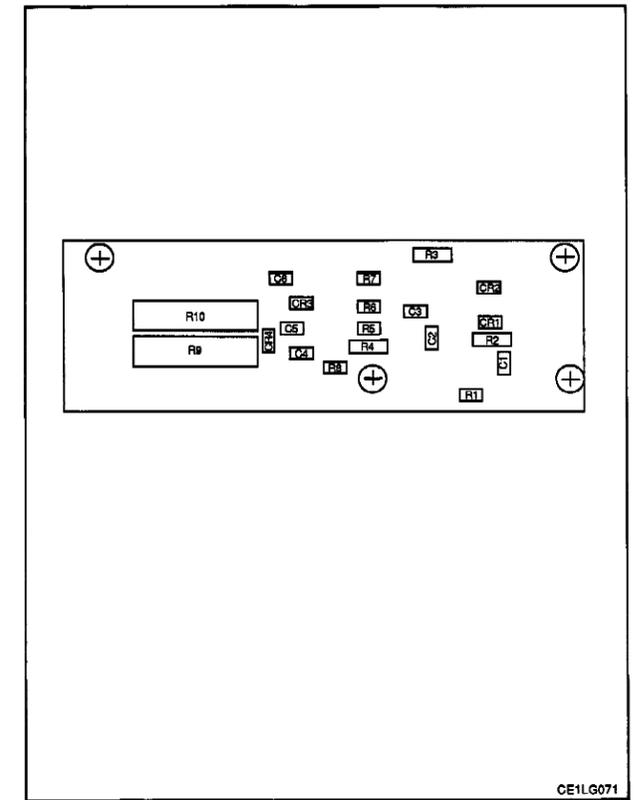


Part of Figure 8-45. A25 Preamp Assembly



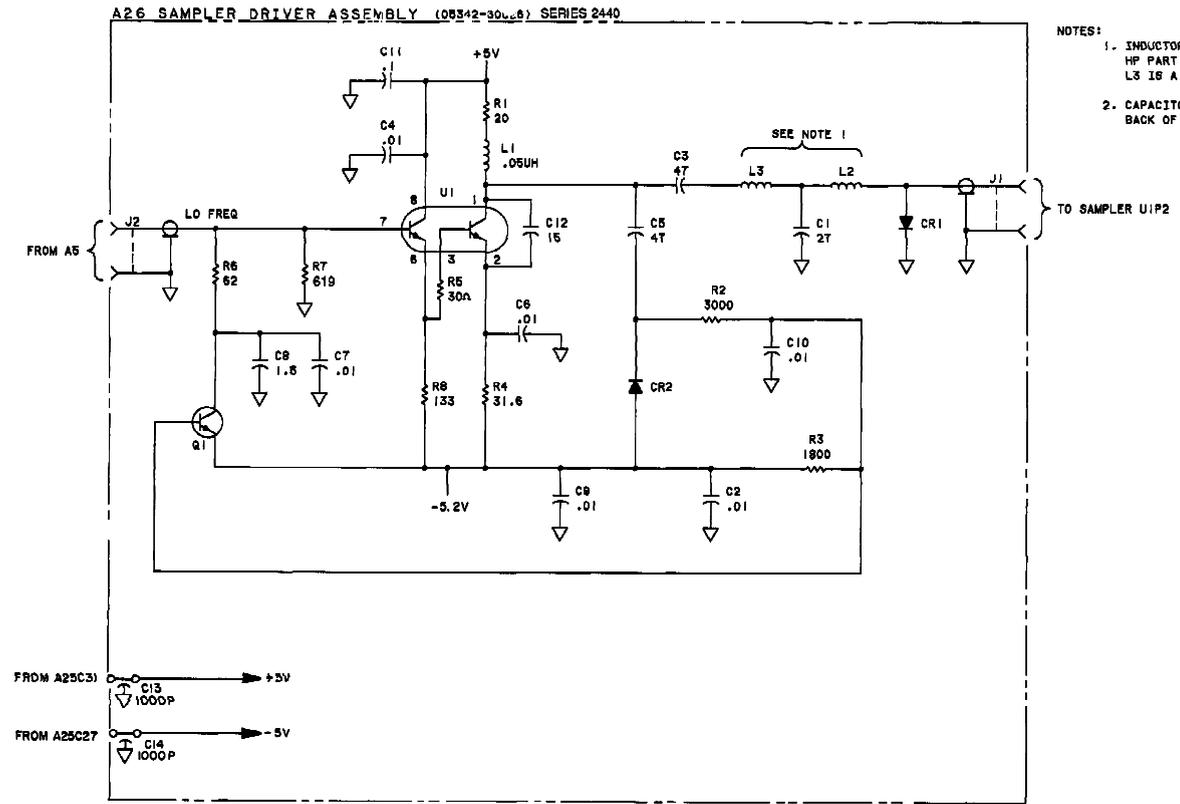
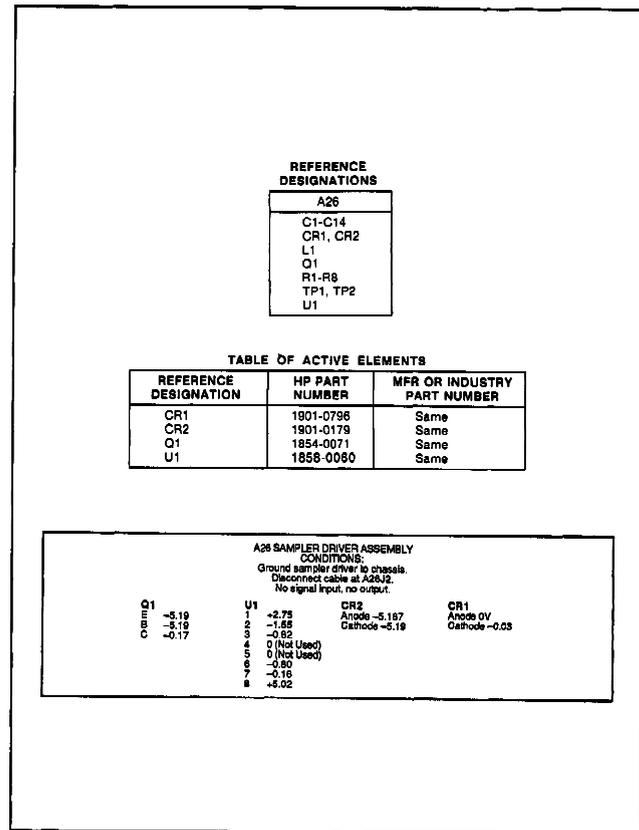
CE1LG070

FO Figure 8-45. A25 Preamplifier Assembly



CE1LG071

Part of Figure 8-46. A26 Sampler Driver Assembly



APPENDIX A REFERENCES

A-1. SCOPE.

This appendix lists all forms, field manuals, technical manuals, and miscellaneous publications referenced in this manual.

A-2. FORMS.

Transportation Discrepancy Report (TDR)	Form SF361
Report of Discrepancy (ROD)	Form SF364
Product Quality Deficiency Report	Form SF 368
Recommended Changes to Equipment Technical Manuals	DA Form 2028-2

A-3. TECHNICAL MANUALS.

Unit and Intermediate Direct Support and General Support Repair Parts and Special Tools List, for Microwave Frequency Counter TD 1225A(V)2/U	TM 11-6625-301 4-24P
Procedures for Destruction of Electronics Materiel to Prevent Enemy Use (Electronics Command)	TM 750-244-2

A-4. MISCELLANEOUS.

The Army Maintenance Management System (TAMMS)	DA Pam738-750
Consolidated Index of Army Publications and Blank Forms	DA Pam 25-30
First Aid for Soldiers	FM21-11

MAINTENANCE ALLOCATION CHART

Section I. INTRODUCTION

B-1. GENERAL.

a. This appendix provides a general explanation of all maintenance and repair functions authorized at various maintenance levels for the TD 1225A(V)2/U.

b. The Maintenance Allocation Chart (MAC) in Section II designates overall authority and responsibility for the performance of maintenance functions on the identified end item or component. The application of the maintenance functions to the end item or component will be consistent with the capacities and capabilities of the designated maintenance levels.

c. Section III lists the tools and test equipment (both special tools and common tool sets) required for each maintenance function as referenced from section II.

d. Section IV contains supplemental instructions and explanatory notes for a particular maintenance function,

B-2. MAINTENANCE FUNCTIONS. Maintenance functions will be limited to and defined as follows:

a. Inspect. To determine the serviceability of an item by comparing its physical, mechanical, and/or electrical characteristics with established standards through examination.

b. Test. To verify serviceability and to detect incipient failure by measuring the mechanical or electrical characteristics of an item and comparing those characteristics with prescribed standards.

c. Service. Operations required periodically to keep an item in proper operating condition, i. e., to clean (includes decontaminate, when required), preserve, drain, paint, or to replenish fuel, lubricants, chemical fluids, or gases.

d. Adjust. Maintain or regulate within prescribed limits, by bringing into proper or exact position, or by setting the operating characteristics to the specified parameters.

e. Align. To adjust specified variable elements of an item to bring about optimum or desired performance.

f. Calibrate. To determine the cause and corrections to be made or adjusted on instruments or test measuring and diagnostic equipment used in precision measurement . This consists of comparisons of two instruments, one of which is a certified standard of known accuracy, to detect and adjust any discrepancy in the accuracy of the instrument being compared.

g. Remove/install. To remove and install the same item when required to perform service on other maintenance functions. Install may be the act of emplacing, seating, or fixing into position an item, part, module (component or assembly) in a manner to allow the proper functioning of the equipment or system.

h. Replace. To remove an unserviceable item and install a serviceable counterpart in its place. Replace is authorized by the MAC and is shown as the 3d position code of the SMR code.

i. Repair, The application of maintenance services (inspect, test, service, adjust, align, calibrate, and/or replace) including fault location/troubleshooting, removal/installation, and disassembly/assembly procedures, and maintenance actions (welding, grinding, riveting, straightening, facing, remachining, or resurfacing) to identify troubles restore serviceable to an item by correcting specific damage, fault, malfunction, or failure in a part, subassembly, module (component or assembly), and item or system.

j. Overhaul. That periodic maintenance effort (service/ action) prescribed to restore an item to a completely serviceable/operational condition as required by maintenance standards in appropriate technical publications (i.e., DMWR) Overhaul is normally the highest degree of maintenance performed by the Army. Overhaul does not normally return an item to like new condition.

k. Rebuild. Consists of those services/ actions necessary for the restoration of unserviceable equipment to a like new condition in accordance with original manufacturing standards. Rebuild is the highest degree of material maintenance applied to Army equipment. The rebuild operation includes the act of returning to zero those age measurements (hours, miles, etc.) considered in classifying Army equipment/ components.

B-3. EXPLANATION OF COLUMNS IN THE MAC, SECTION II.

a. Column 1, Group Number. Column 1 lists functional group code numbers, the purpose of which is to identify maintenance significant components, assemblies, subassemblies and modules with the next higher assembly. End item group number shall be "00".

b. Column 2, Component/ Assembly. Column 2 contains the noun names of components, assemblies, subassemblies, and modules for which maintenance is authorized.

c. Column 3, Maintenance Function. Column 3 lists the functions to be performed on the item listed in column 2.

d. Column 4, Maintenance Level. Column 4 specifies, by the listing of a work time figure in the appropriate subcolumn (s), the level of maintenance authorized to perform the function listed in column 3. This figure represents the active time required to perform that maintenance function at the indicated level of maintenance, If the number or complexity of the tasks within the listed maintenance function vary at different levels, appropriate work time figures will be shown for each level. The work time figure represents the average time required to restore an item (assembly, subassembly, component, module, end item or system) to a serviceable condition under typical field operating conditions. This time includes preparation time (including any necessary disassembly/assembly time), troubleshooting/fault location time and quality assurance/ quality control time in addition to the time required to perform the specific tasks identified for the maintenance functions authorized in the maintenance allocation chart. The symbol designations for the various maintenance levels are as follows:

UNIT

C — Operator/ Crew

O — Organizational Maintenance

INTERMEDIATE

F — Direct Support Maintenance

H — General Support Maintenance

L — Specialized Repair Activity

DEPOT

D — Depot Maintenance

e. Column 5, Tools and Equipment. Column 5 specifies by code, those common tool sets (not individual tools) and special tools, TMDE, and support equipment required to perform the designated function.

f. Column 6, Remarks, This column shall, when applicable, contain a letter code, in alphabetic order which shall be keyed to the remarks contained in Section IV.

B-4. EXPLANATION OF COLUMNS IN TOOL AND TEST EQUIPMENT REQUIREMENTS, SECTION III.

a. Column 1, Reference Code. The tool and test equipment code correlates with a code used in the MAC, Section 11, Column 5.

b. Column 2, Maintenance Level. The lowest level of maintenance authorized to use the tool or test equipment.

c. Column 3, Nomenclature. Name or identification of the tool or test equipment.

d. Column 4, National Stock Number. The National Stock Number of the tool or test equipment.

e. Column 5, Tool Number. The manufacturer's part number.

B-5. EXPLANATION OF COLUMNS IN REMARKS, SECTION IV.

a. Column 1, Reference Code. The code recorded in column 6, Section II.

b. Column 2, Remarks. This column lists information pertinent to the maintenance function being performed as indicated in the MAC, Section II.

**SECTION II. MAINTENANCE ALLOCATION CHART
FOR
ELECTRONIC COUNTER, TD-1225A(V)2/U**

(1) GROUP NUMBER	(2) COMPONENT/ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE LEVEL					(5) TOOLS AND EQPT.	(6) REMARKS
			UNIT		INTERMEDIATE		DEPOT		
			C	O	F	H	D		
00	ELECTRONIC COUNTER TD-1225	INSPECT		0.1				1	A
		TEST				1.0		4-18	
		ADJUST				1.5		4-18	
		REPAIR				2.0		2-18	B
		REPLACE				0.2		3	
01	CRYSTAL OSCILLATOR ASSY A24	REPAIR					1.0	4-18	C
		INSPECT				0.1			A
		TEST				0.5		4-18	
		REPLACE				0.2		3	
		REPAIR					1.0	4-18	C

**SECTION III. TOOL AND TEST EQUIPMENT REQUIREMENTS
FOR
ELECTRONIC COUNTER, TD-1225A(V)2/U**

Tool OR Test EQUIPMENT REF CODE	Maintenance CATEGORY	NOMENCLATURE	NATIONAL/NATO STOCK NUMBER
1	0	TOOL KIT, ELECTRONIC EQUIPMENT TK-101/G	180-00-064-5178
2	H,D	TOOL KIT, ELECTRONIC EQUIPMENT TK-105/G	180-00-610-8177
3	H,D	TOOL KIT, ELECTRONIC EQUIPMENT,NT TK-100/G	5180-00-605-0079
4	H,D	SIGNAL GENERATOR SG-763/U HP 652A	525-00-054-3483
		SIGNAL GENERATOR SG-1121(A) 1/U	525-00-007-6661
		HP 8620A MAIN FRAME WITH PLUG-INS	525-01-018-6548
		HP PART NO. 86222A/B, 86290A/B/C (18.6 GHz)	525-01-040-0919
5	H,D	VOLTMETER, SAMPLING ME-416/U , HP 3406A	525-00-113-3491
6	H,D	SIGNAL GENERATOR, SG-1112 (V) 1/U, HP 8640B-004 or EQUIVALENT (500 KHz-512 MHz)	525-00-566-3067
7	H,D	OSCILLOSCOPE SYSTEM AN/USM-281C , TEKTRONIX 7603N11S or EQUIVALENT	625-00-106-9622
8	H,D	PULSE GENERATOR, SG-1105, HP 8013B or EQUIVALENT	625-01-010-3524
9	H,D	SIGNAL GENERATOR, SG-1093/U, HP 8640B or EQUIVALENT	525-00-487-2878
10	H,D	POWER SUPPLY, PP-7547/U (HP 6113A)	130-00-225-1682
11	H,D	MULTIMETER HP 3490A	1625-01-010-925:
12	H,D	REPAIR KIT PRINTED CIRCUIT MK-772/U	5999-00-757-7Q4,
13	H,D	SERVICE ACCESSORY KIT HP 10842A	6625-01-614-8723
14	H,D	TRANSISTOR TEST SET TS-1836D/U	6625-00-138-7320
15	H	MULTIMETER, AN/PSM-45	5625-01-139-2512
16	H,D	ISOLATION TRANSFORMER GIS-1000 (80089)	5950-01-110-2924
17	H,D	EXTENDER BOARD HP 05342-600034 (for A-21 (CXT CARD) CALIBRATION	
18	H,D	EXTENDER BOARD HP 05342-60035 (for A-19 CKT CARD) CALIBRATION	

**SECTION IV. REMARKS
FOR
ELECTRONIC COUNTER, TD-1225A(V)2/U**

REFERENCE CODE	REMARKS
A	VISUAL INSPECTION
B	REPAIR OF END ITEM IS ACCOMPLISHED BY REPLACEMENT OF MODULES, CIRCUIT CARD ASSEMBLIES, FUSES, CABLE ASSEMBLIES, CABLES, OR CHASSES MOUNTED COMPONENTS
C	REPAIR OF A24 IS ACCOMPLISHED BY REPLACEMENT OF COMPONENTS

APPENDIX C A24 OSCILLATOR REPAIR

SECTION I INTRODUCTION

C-1. SCOPE.

C-2. This appendix contains instructions for the repair of the A24 Crystal Oscillator Assembly. Throughout this appendix the A24 Crystal Oscillator Assembly is referred to as either the Instrument, Oscillator, or 10811A.

C-3. GENERAL.

C-4. This appendix contains three sections. Section I contains general information. Section II contains the post repair adjustments, Section III contains the necessary repair information including principles of operation, troubleshooting procedures, and diagrams.

SECTION II ADJUSTMENTS

C-5. INTRODUCTION.

Adjustments for the 10811A Oscillator are provided in paragraph 5-32,

SECTION III SERVICE

C-6. INTRODUCTION

C-7. This section contains theory of operation, a detailed troubleshooting procedure, and a schematic diagram.

C-8. SCHEMATIC DIAGRAM SYMBOLS AND REFERENCE DESIGNATORS

C-9. Figure C-1 shows the symbols used in the schematic diagram. At the bottom of Figure C-1, the system for reference designators, assemblies, and subassemblies is shown.

C-10. REFERENCE DESIGNATORS

C-11. Theory of Operation

C-12. The overall theory of operation for the 10811A starts with paragraph C-14. The detailed theory of operation starts with paragraph C-18.

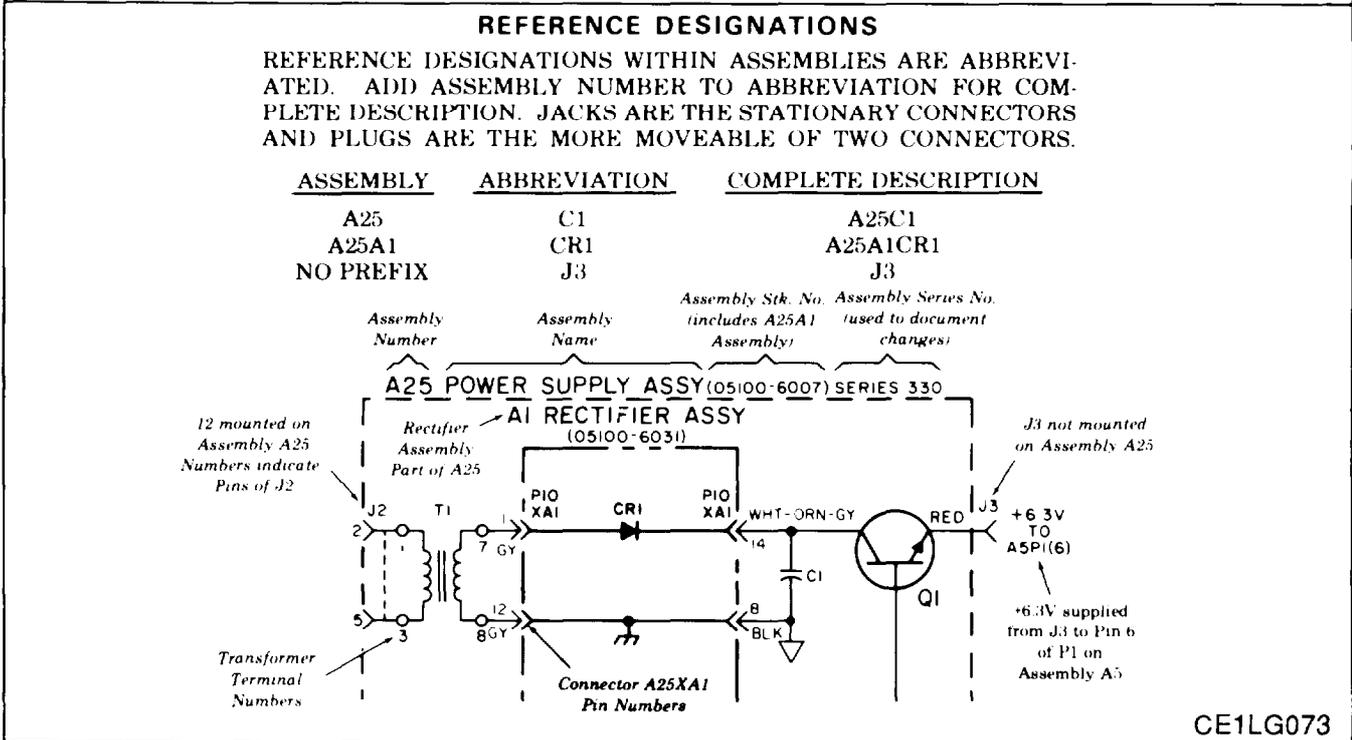
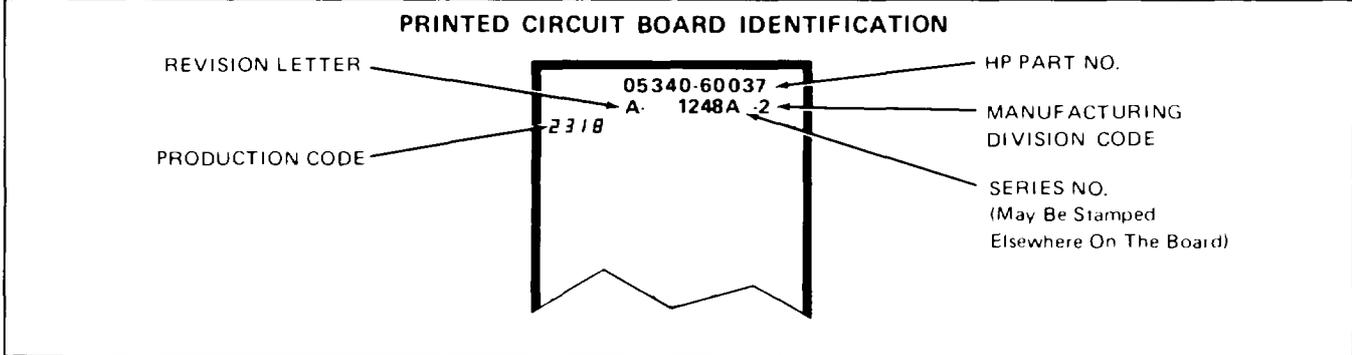
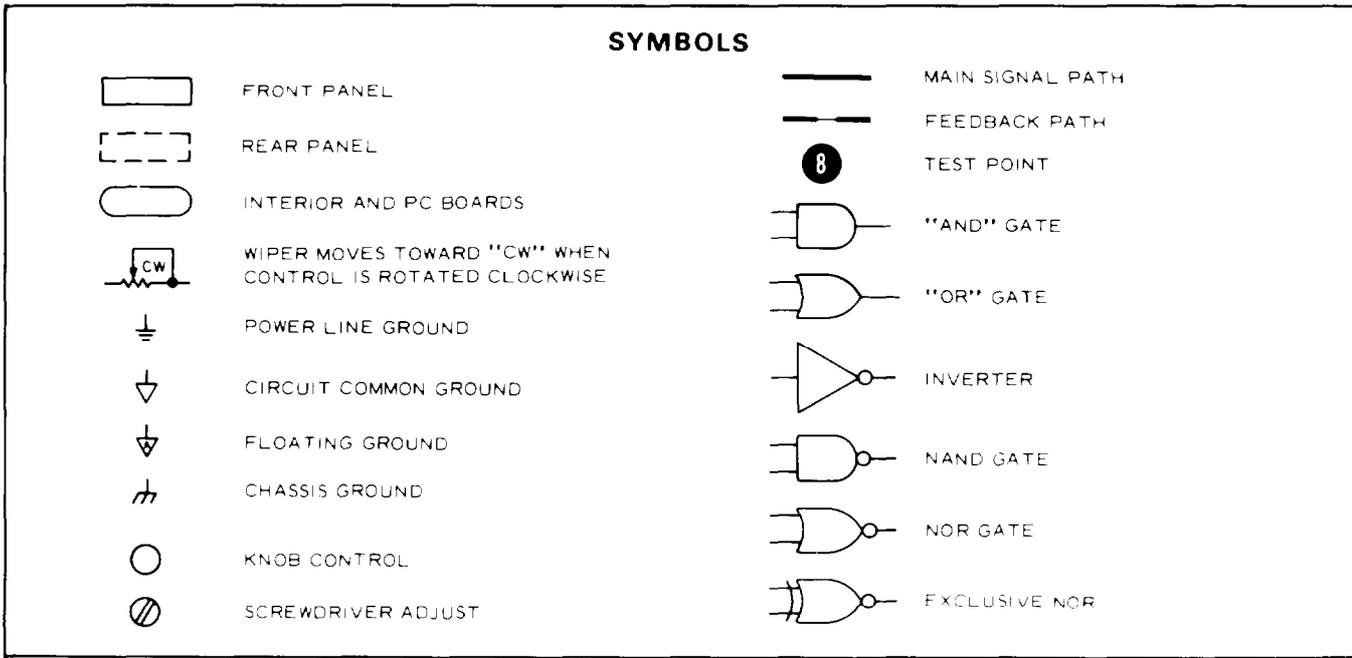
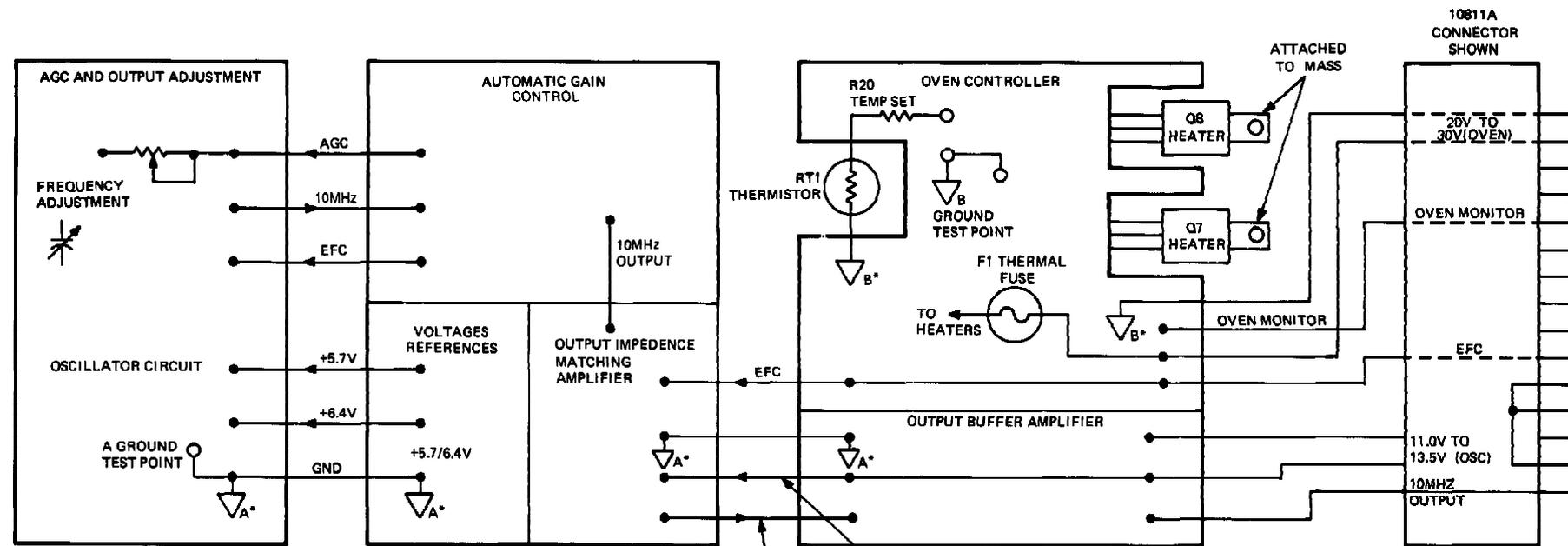


Figure C-1. Schematic Diagram Notes



A GROUND POINT FOR TESTING OSCILLATOR, AGC, OUTPUT AMPLIFIER AND VOLTAGE REFERENCE

B GROUND POINT FOR TESTING OVEN CONTROLLER

* A AND B GROUNDS MAY BE TIED TOGETHER OR FLOATED AT DIFFERENT POTENTIALS EXTERNAL TO THE OSCILLATOR.

10MHZ TO OUTPUT AMP +11.0 TO +13.5V

C-13. OVERALL BLOCK DIAGRAM THEORY

C-14. The 10811A Quartz Crystal Oscillator is an extremely stable, compact, low-power source of 10 MHz. The crystal, along with the oscillator, circuit buffer amplifier, and oven control circuits are all mounted inside a thermally insulated housing.

C-15. A detailed block diagram of the 10811A oscillator is shown in Figure C-2.

C-16. The 10811A oscillator is divided into three sections with each section connected by a .010-inch thick flexible circuit. Three small circuit boards are bonded to the flexible circuit to provide support in the areas where components are located. The arrangement allows the unit to be easily disassembled and operated in the disassembled state on the service bench.

C-17. The three sections can be divided into the following subsections (Figure C-2):

1. Main Oscillator
2. Automatic Gain Control
 - Voltage Reference (+5.7V and +6.4V)
 - Output Impedance Matching Buffer
3. Output Buffer Amplifier
 - Oven Controller

C-18. MAIN OSCILLATOR THEORY OF OPERATION

C-19. The 10811A oscillator is a Colpitts-type crystal oscillator which uses the crystal as the series inductor. Figure C-3A shows the basic block diagram of a Colpitts-type oscillator. Figure C-3B shows the basic equivalent components of the oscillator.

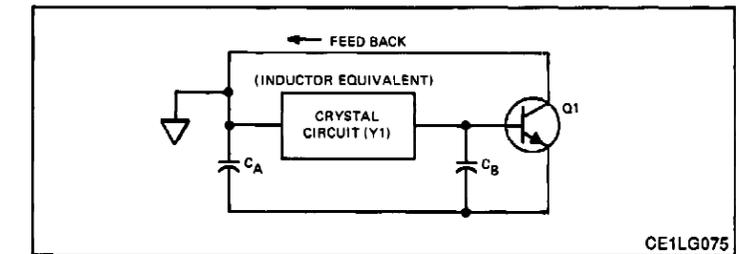


Figure C-3A. Basic Colpitts-Type Oscillator

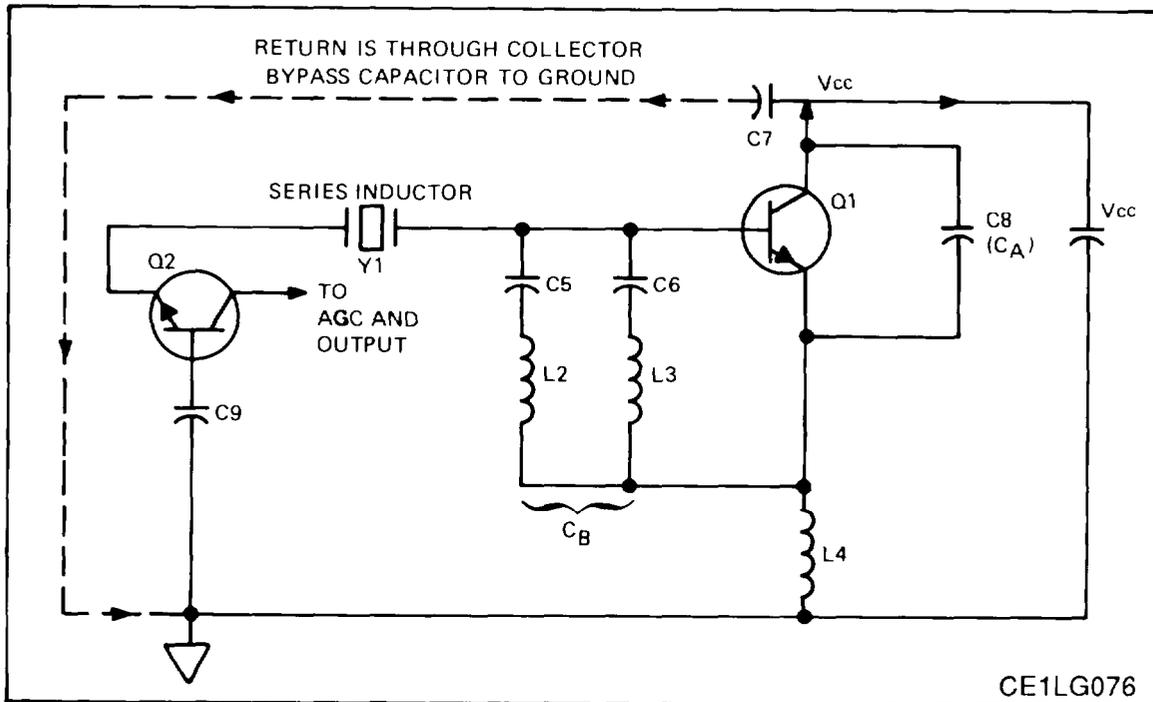


Figure C-3B. Main Oscillator Schematic Design

C-20. Comparing Figure C-3A and C-3B, we find Y1 is the inductor, capacitor CA is C8 and CB is the combination of C5, L2, C6, and L3. C5 is a dc blocking capacitor. Its reactance is very low, so the combination of these components can be redrawn as in Figure C-4. The crystal Y1 is a "third overtone" crystal and is operated at 10 MHz. To keep the circuit from oscillating at the crystal's fundamental, or at a different overtone, the mode suppression network of C5, L2, C6, L3 appears capacitive only at frequencies between 9 MHz and 10.5 MHz. Below and above this frequency range, the network appears inductive. This does not allow the proper phase shift around the loop and thus suppresses oscillations at all frequencies other than 10 MHz. It should be noted that any reactance in series with the crystal will cause a change in frequency.

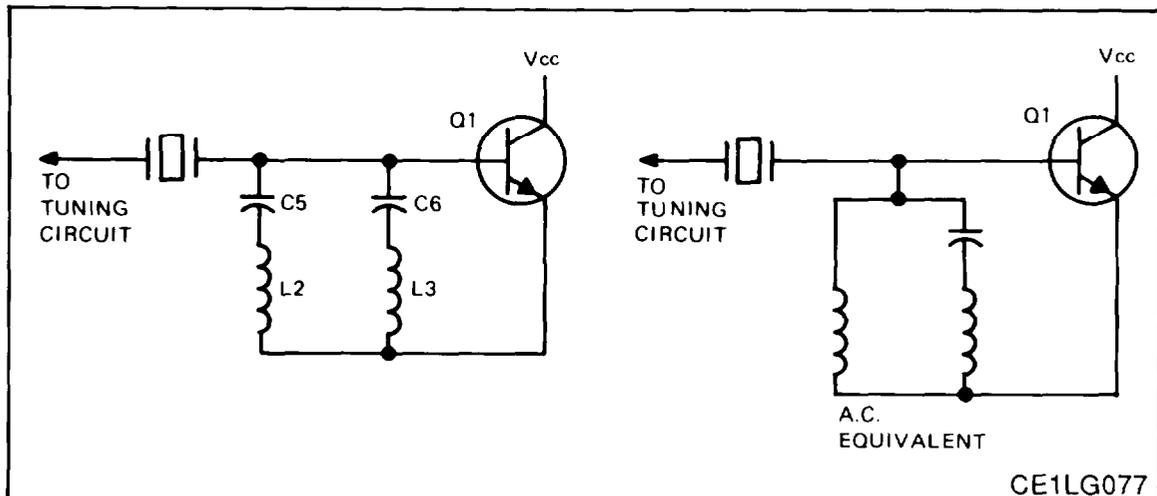


Figure C-4. Mode Suppression

C-21. Figure C-5 show the equivalent crystal circuits with the tuning capacitor C1.

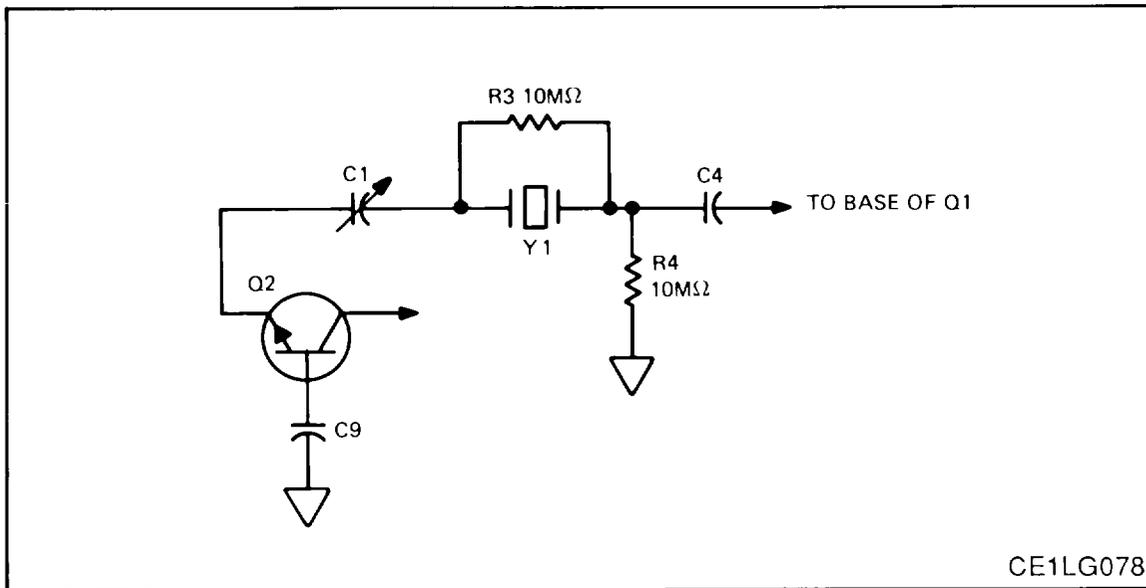


Figure C-5. Frequency Tuning Circuit

C-22. C1 tuning capacitor is available from the top of the oscillator outer housing. The change in reactance of C1 allows the oscillator's frequency to be varied over a 20 Hz (2×10^{-6}) range. C9 and C4 are dc blocking capacitors.

C-23. ELECTRONIC FREQUENCY CONTROL (EFC)

C-24. To allow for a fine tuning control, a varactor (CR1) is added in parallel with C1 tuning capacitor. See Figure C-6. The varactor's capacitance depends on the dc voltage applied to it (reverse bias). The EFC voltage range is +5 volts to -5 volts, giving a fine tuning range of = 1 Hz (1×10^{-7}). Since one side of the varactor is tied to a reference (6.4V), a full +5 volts applied to the EFC input will still keep CR1 reverse biased. C2 and C3 are again dc blocking capacitors to keep the EFC current from flowing in to the crystal circuit. Note: if the EFC input is not used, it must be connected to ground to keep any noise from modulating the EFC line and causing frequency changes.

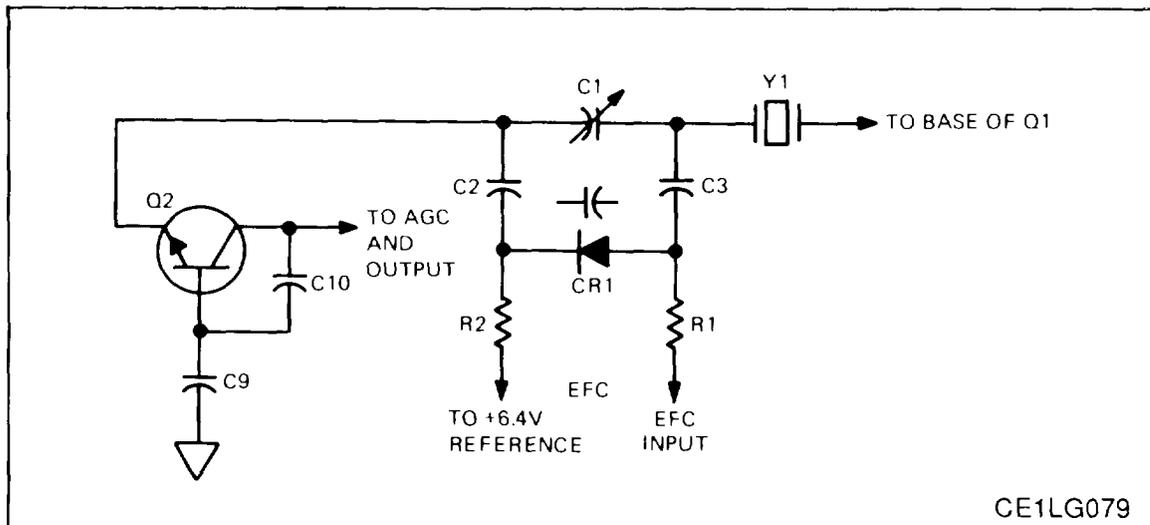


Figure C-6. EFC

C-25. AUTOMATIC GAIN CONTROL (AGC)

C-26. The output for the AGC (and output amplifiers, discussed later) is taken across capacitor C10, and is applied to Q3. Since C10 is effectively in series with the crystal, the current passing through the crystal also passes through C10. The voltage across C10 is therefore proportional to the current through the crystal. As the output of the oscillator changes, the output of the peak detector circuit changes. This change in the AGC voltage changes the voltage applied to the base of Q1 and stops the impending output voltage change. A peak detector circuit formed by C12, C13, CR4 and CR5 is used to develop a dc voltage to control the crystal current. This negative control voltage forms the lower half of a voltage divider for the base of Q1 (R6 and R7). Controlling the bias current and the gain of Q1. Thus AGC action controls the output signal level. (See Figure C-7).

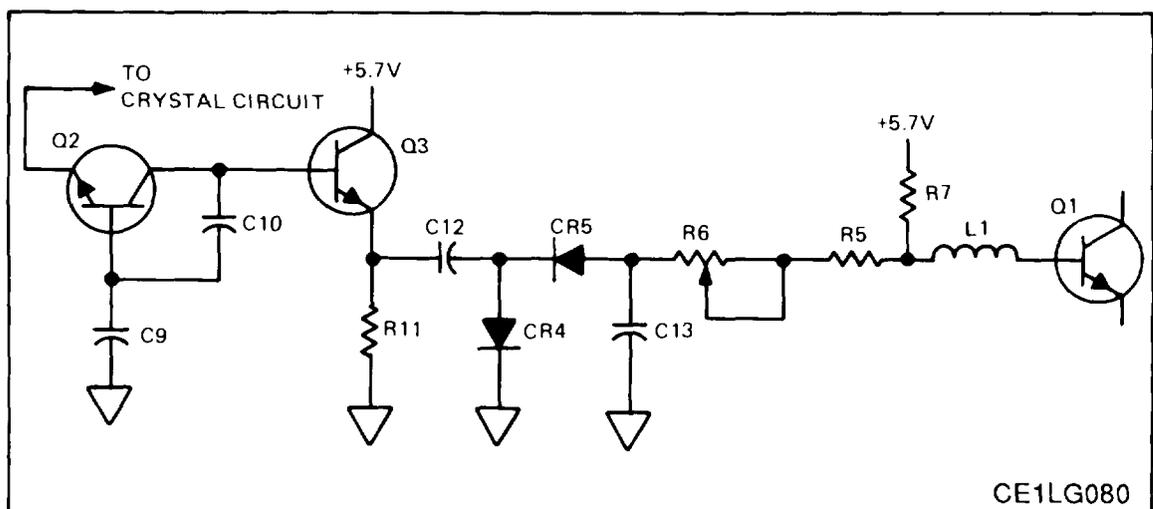


Figure C-7. Automatic Gain Control (AGC)

C-27. By adjusting the AGC voltage with R6 the amplitude for the output (at the base of Q3) can be set. R5 sets the AGC limit when R6 is at its minimum resistance,

C-28. RF OUTPUT IMPEDANCE MATCHING AND OUTPUT BUFFER

C-29. The signal for the output amplifiers is taken from the same point as the AGC (across C10). The voltage is buffered by Q5 which is an impedance matching stage. Resistors R14 and R15 set the dc bias level while C14 allows the ac to bypass R14. The signal is then applied to the output buffer stage of Q9. Resistor R40 provides a 50 Ω source impedance when transformed by T1. Typical gain from Q9 base to collector is approximately 2. See Figure C-8.

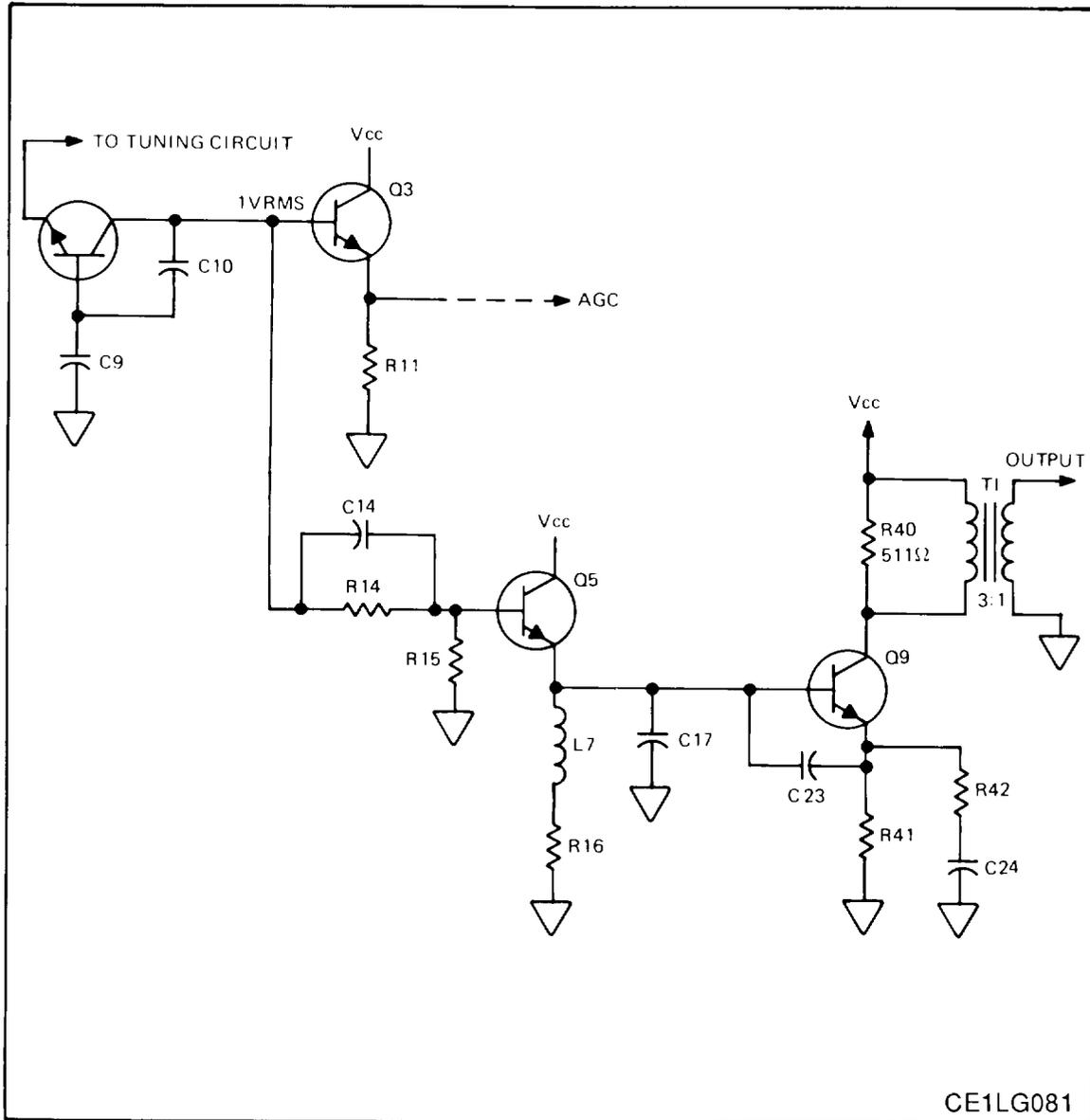


Figure C-8. Output Amplifiers

C-30. VOLTAGE REFERENCES (5.7V AND 6.4V)

C-31. Constant current diode CR2 feeds 1 mA to zener diode CR3 providing 6.4V dc for the EFC varactor reference. R12 and C15 form a filter to attenuate noise from the zener diode. R13 provides current limiting for Q5 if the 5.7V line is shorted. See Figure C-9.

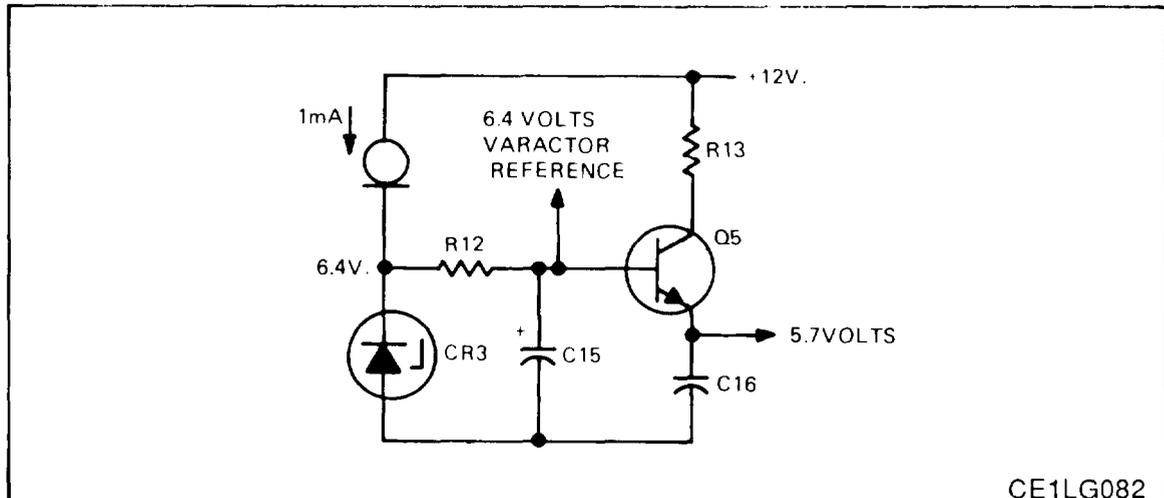


Figure C-9. Voltage References

CE1LG082

C-32. OVEN HEATER AND CONTROLLER THEORY**NOTE**

In the following theory of operation the term OVEN MASS will be used to describe the cast aluminum block in which the crystal and crystal electronics are located. The exploded view of the oscillator shows the oven mass.

C-33. The purpose of the oven is to shield the oscillator crystal and electronics from normal ambient temperature changes. The oven controller does this by maintaining a constant oven temperature which is higher than the highest expected ambient temperature.

C-34. Three main blocks make up the oven circuits. See Figure C-10.

1. Thermistor
2. Amplifier (controller)
3. Heaters

C-35. In the 10811 A oven, a thermistor (RT1) is secured with epoxy into a hole in the oven mass. U3 is the amplifier and Q7 (not shown) and Q8 are the heaters. It is the thermistor that senses the oven mass temperature. Since it is in one leg of the bridge circuit, when the mass temperature changes slightly, a voltage change occurs across the bridge (RT1, R18, R19, R20, R21). Amplifier U3 boosts this voltage change and then uses it to control the current through Q7 and Q8. The current flowing through transistors Q7 and Q8 causes a power dissipation in the form of heat, and it is this heat that warms the oven mass. Therefore, when the mass temperature starts to change, the heaters are told to adjust their power to cancel the impending temperature change.

C-36. WARM-UP: GENERAL OPERATION. If the oscillator has been off for several hours, the mass and thermistor will be at the ambient temperature. Assuming this is below the normal oven operating temperature (80 to 84°C) the resistance at the thermistor RT1 is higher than that of R18+R20 and therefore $V_1 > V_2$. This causes the output of U3 to be $\approx (V_{cc} - 1.5V)$ and supply base current to Q8 through Q6. A separate circuit limits the collector current of Q8 and is described later. As the oven mass warms up, the thermistor's resistance gets lower causing both V_2 and V_1 to lower (V_2 lowers because V_0 lowers due to RT1 getting smaller). V_1 decreases at a faster rate than V_2 and eventually $V_1 = V_2$ when $RT1 = R20 + R18$. At this time, the oven controller "cuts back" and begins to operate in a linear mode, adjusting the collector current in Q8 (and therefore the power dissipated in Q7 and Q8) to keep the oven precisely at its set temperature.

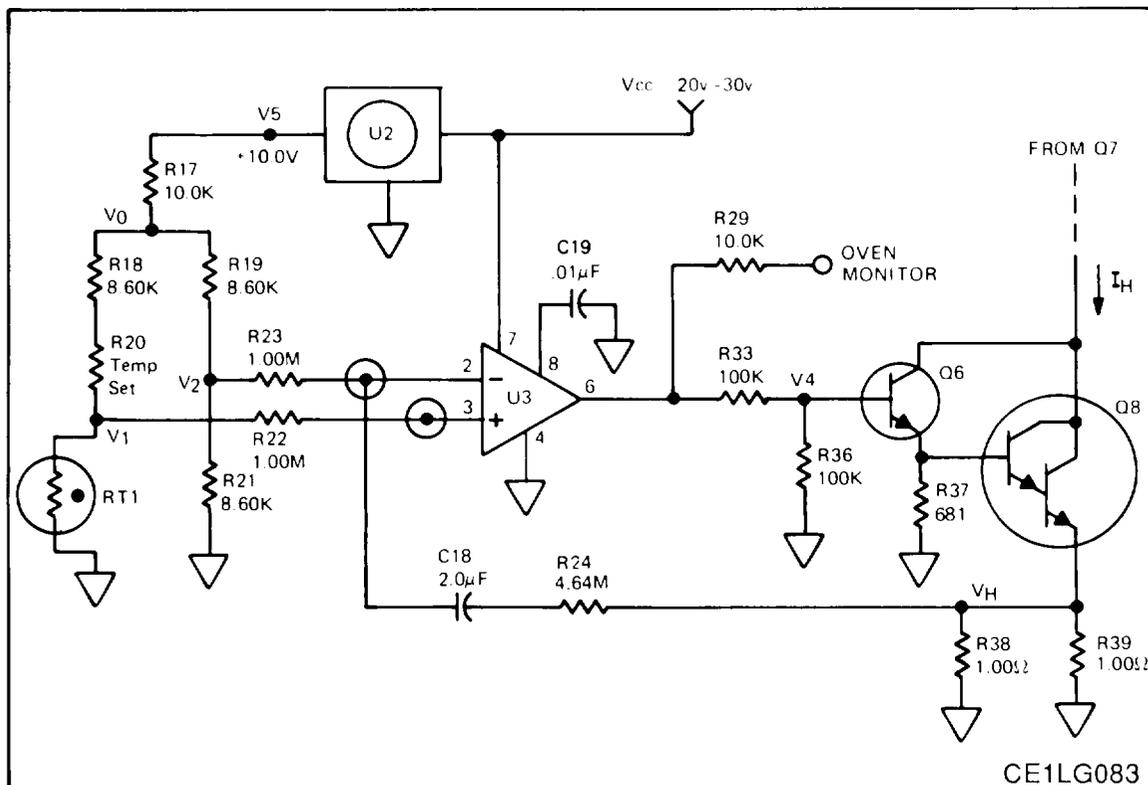


Figure C-10. Oven Control Circuits

C-37. The purpose of R17 is mainly to reduce the power dissipated in the thermistor which causes it to self-heat above the oven operating temperature.

C-38. R38 and R39 in parallel provide a means of sensing the heater current, I_H . During warm-up, the voltage across them, V_H , is used in the current limit circuit (described later). During normal, linear operation, V_H is essentially the feedback point for the oven controller loop.

C-39. Q6 is necessary primarily for the condition when the oscillator has been stored at -55°C . Since U3 (at -55°C) cannot supply enough base current for Q8, Q6 gives the added current gain required.

C-40. PRECISION VOLTAGE REFERENCE

C-41. U2 is a 10.0V voltage reference. It provides a stable voltage source for the bridge and U1. A change in the bridge reference voltage changes the voltage across the thermistor and hence, the power it dissipates. See Figure C-10.

C-42. OVEN CONTROLLER TURN-ON CURRENT LIMITING

C-43. Figure C-11 shows the turn-on current limiting circuit. From an initial turn-on condition the thermistor senses the oven temperature to be low. To correct this situation the amplifier attempts to drive heavy amounts of current through Q7 and Q8 heaters. If allowed to continue this way, excessive current will flow; much more than is practical or necessary for warm-up. Amplifier U1 and associated components limit the current during warm-up to a practical value. When V_{cc} is applied to the oven, U1B forces V_H to equal V_3 by sinking the base current from Q6. By sensing V_{cc} , the circuit transforms the heater transistors into what appears to be a fixed heater resistance of $47\ \Omega$ typical.

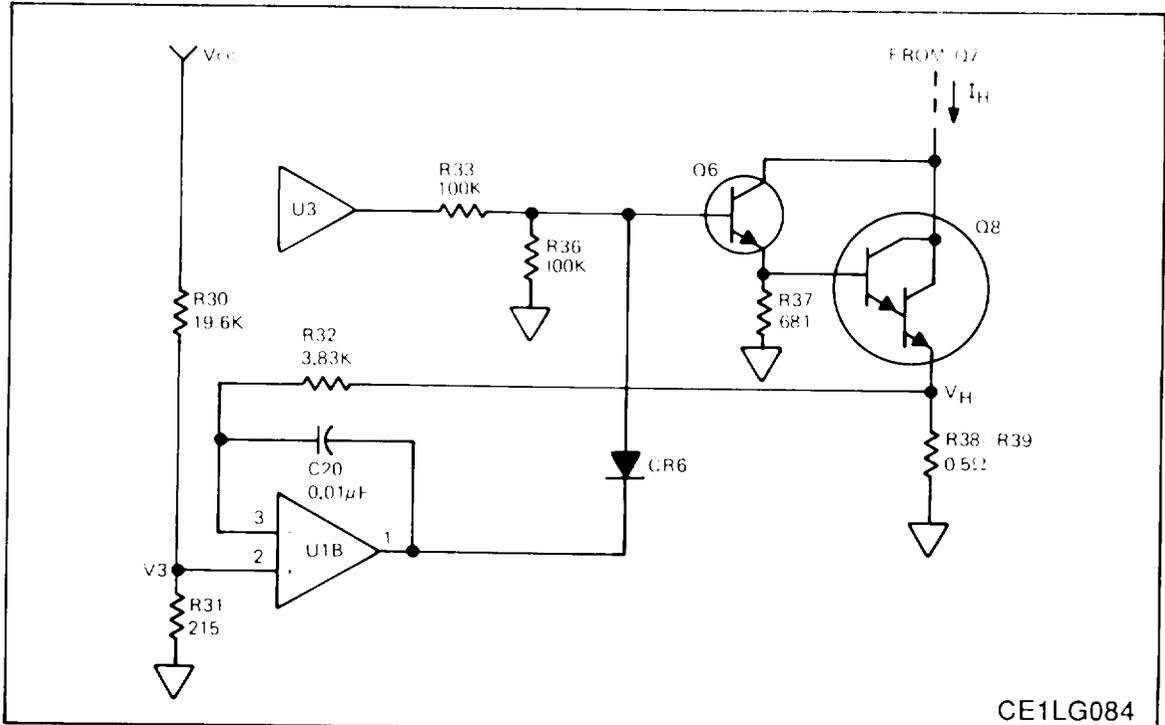


Figure C-11. Turn-on Current Limit Circuit

C-44. HEATER TRANSISTOR BALANCE

C-45. Because heater transistors Q7 and Q8 are not equally spaced from the crystal, it is necessary to offset the power dissipation between the two transistors. Figure C-12 shows a simplified schematic of this circuit. Amplifier U1A references a voltage divider across V_{cc} (R25, R26) and a divider referenced to the mid-point between the heater transistors. From this U1A controls the base current of Q7 to insure the voltage at the mid-point between the heater transistors is a constant percentage of V_{cc} ($V_4 \approx 0.57 V_{cc} \pm 2\%$).

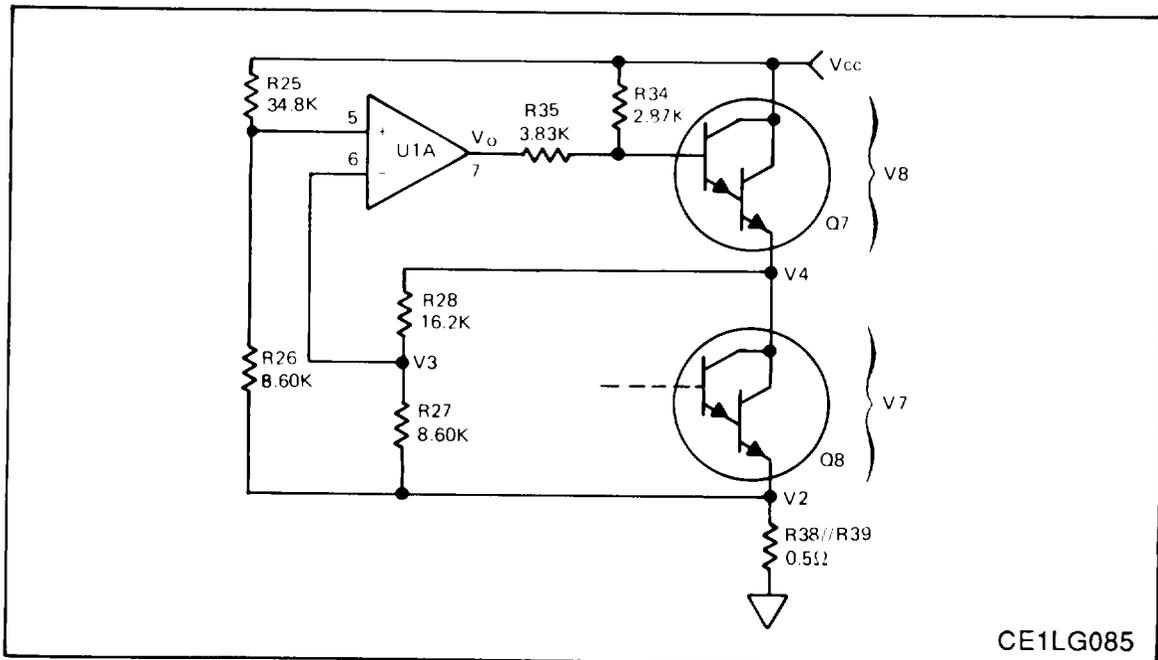


Figure C-12. Heater Transistor Balance Circuit

C-46. REPAIR AND TROUBLESHOOTING

C-47. Inspection

C-48. The 1081 1A should be inspected for indications of mechanical and electrical defects. Electronic components that show signs of overheating, leakage, frayed insulation, and other signs of deterioration should be checked and a thorough investigation of the associated circuitry should be made to verify proper operation. Mechanical parts should be inspected for excessive wear, looseness, misalignment, corrosion, and other signs of deterioration.

CAUTION

Proper static handling techniques must be employed when servicing semiconductor products. The voltage susceptibility of all I.C. and transistor families are well below levels commonly found in service environments, Exercise care and observe standard static precautions.

C-49. REPAIR

C-50. Printed Circuit Component Replacement

C-51. To prevent damage to the plating and the replacement component, apply heat sparingly, and work carefully. See CAUTION below.

C-52. Replacing Integrated Circuits

C-53. Following are two recommended methods of replacing integrated circuits:

- a. **SOLDER GOBBLER.** This is the best method. Solder is removed from board by a soldering iron with a hollow tip connected to a vacuum source.
- b. **CLIP-OUT.** Clip the leads as close to the component as possible. With a soldering iron and longnose pliers, carefully remove the leads from each hole. Then clean the holes.

CAUTION

The flex circuitry used in the 10811 A oscillator requires special attention to soldering iron tip temperature and the length of time heat is applied. A low wattage ($\approx 25W$) iron with a temperature control should be used. The tip temperature should be held below 500°C. Care should be taken to be sure that the iron is not held on the circuit longer than necessary. Components should be removed by clipping the leads and then gently removing them. Do not use force when removing components. Following these precautions will insure that repairs can be easily made without damaging the flex circuit. Also, components should not be arbitrarily removed for troubleshooting or replacement unless there is reasonable confidence in the component's failure.

WARNING

THE OSCILLATOR'S INTERNAL OVEN MASS TEMPERATURE MAY BE AS HIGH AS 85°C (185°F). TO AVOID SERIOUS BURNS DO NOT REMOVE OSCILLATOR CIRCUITS AND/OR OVEN MASS ASSEMBLY FROM THE OUTER CAN UNTIL THE OSCILLATOR HAS SUFFICIENTLY COOLED (APPROXIMATELY ONE HOUR WITH BOTTOM COVER AND FOAM INSULATOR REMOVED). THE OUTER HOUSING TEMPERATURE IS NOT A RELIABLE INDICATION OF THE INTERNAL TEMPERATURE.

C-54. The troubleshooting is arranged to allow the technician to quickly find the defective component(s) without unnecessary removal of components.

C-55. TROUBLESHOOTING

C-56. Failures in the 10811A can be divided into two sections:

1. Failure of the oscillator's circuits.
2. Failure in the oven controller circuits.

C-57. Failures in the oscillator circuits can be divided into the following problems:

1. No output.
2. Output amplitude is too low or high.
3. Output is distorted (contains excessive harmonics).
4. Output is off frequency (high or low).
5. Output has excessive noise or frequency stability does not meet specifications.

C-58. Poor frequency stability can be difficult to troubleshoot, and many times the oscillator is not at fault. Environmental conditions can affect stability and should be ruled out first.

C-59. Failures in the oven circuitry can be divided into the following problems:

1. No oven current (heat).
2. Excessive oven current (>600 mA).
3. Oven does not cut back after warm-up (this will open the thermal fuse if allowed to continue).
4. Oven does not regulate at the proper temperature. (This can be the cause for poor frequency stability).

C-60. Since the main oscillator and oven control power supply inputs are separate from each other, the defective circuit can be operated without applying power to the complete oscillator.

C-61. Determine which section is defective (oven or oscillator circuit), then proceed as described in the following troubleshooting section. The two circuits can be investigated separately.

1. Remove top cover and insulator described in:
 - a. 10811 A paragraphs C-64.

CAUTION

With the cover and foam insulator removed to thermal fuse cannot protect the oven circuit from thermal runaway. Caution should be used at all times.

C-62. DISASSEMBLY FOR TROUBLESHOOTING AND REPAIR

C-63. Perform steps 1 through 3 for the 10811A oscillator
Once these steps are completed, follow steps 6 through 10.

C-64. For the 10811A Oscillator:

Step 1. Remove the three screws securing the bottom cover to the outer housing, and remove bottom cover.

Step 2. Remove the two screws securing the pc edge connector to the outer housing.

Step 3. Remove the foam sheet to expose the oven controller circuit board.

If troubleshooting the oven controller, stop here and go to paragraph C-67. Go to Step 6 only if the trouble is in the oscillator circuit.

Step 4. Deleted

Step 5. Deleted

Step 6. Using a long, small diameter tool, remove the complete oscillator assembly by inserting the tool into the tuning capacitor access hole (labeled FREQ. ADJUST) and pushing on the capacitor until the circuit can be grasped and removed freely.

CAUTION

Do not remove the circuits by pulling on the edge connector or flexible circuit. Damage to the flexible circuit may occur.

Step 7. Using a posidrive screwdriver, remove the two screws securing the heater transistors to the oven mass. Remove the washers and transistor insulators.

NOTE

When reassembling the oven mass the heater transistor screws must be tightened to a torque of 0.6 newton metres (5 in. -lbs.)

Step 8. Tilt the oven controller assembly back and remove the foam insulator between the oven controller assembly and the oven mass. Be careful not to break the two black thermistor wires attached to the oven controller assembly.

Step 9. Remove the eight screws (four each side) securing the covers to the oven mass assembly.

Step 10. Use two of the screws from each cover (removed in Step 9) to secure the boards to the mass for troubleshooting.

C-65. Go to paragraph C-83, Oscillator Troubleshooting. When reassembling unit, reverse the above procedure.

C-66. SPECIAL PARTS REPLACEMENT CONSIDERATIONS

C-67. Several mechanical parts and components must be replaced as a pair or require special consideration. They are:

- a. Oven mass assembly and thermistor: If the thermistor (RT1) is found to be defective, the thermistor and oven mass assembly must be replaced as one item.
- b. Crystal and Temperature Set Resistor: The replacement crystal for Y1 will be accompanied by the **required temperature set resistor (R20)** for the oven. This resistor must be installed with the new crystal. The crystal and R20 can be ordered using HP Part Number 10811-60108. If the temperature set resistor is found to be defective only, it must be replaced with the same value and tolerance. If the temperature set resistor (R20) is unreadable, the value required can be determined by finding the oven temperature value marked on the crystal (Y1). The required resistor can then be determined from

Table C-1. Temperature Set Resistor List

OVEN TEMP °C	RESISTOR VALUE	PART NUMBER
80.0	1.33K	0698-7239
80.1	1.29K	0698-6981
80.2	1.25K	0698-6973
80.3	1.21K	0698-7238
80.4	1.18K	0698-3512
80.5	1.15K	0698-4469
80.6	1.10K	0698-7237
80.7	1.07K	0698-4196
80.8	1.04K	0698-6970
80.9	1.00K	0698-7236
81.0	968	0698-0096
81.1	931	0698-4465
81.2	909	0698-7235
81.3	866	0698-3495
81.4	825	0698-7234
81.5	787	0698-4014
81.6	750	0698-7233
81.7	715	0698-3700
81.8	681	0698-7232
81.9	649	0698-4460
82.0	619	0698-7231
82.1	600	0757-1100
82.2	562	0698-7230
82.3	511	0698-7229
82.4	500	0698-5852
82.5	464	0698-7228
82.6	422	0698-7227
82.7	383	0698-7226
82.8	348	0698-7225
82.9	316	0698-7224
83.0	287	0698-7223
83.1	261	0698-7222
83.2	215	0698-7220
83.3	196	0698-7219
83.4	162	0698-7217
83.5	121	0698-7214
83.6	100	0698-7212
83.7	61.9	0698-7207
83.8	34.8	0698-7201
83.9	0	8159-0005
84.0	0	8159-0005

Table C-1. When Y1 is replaced, the nut which secures it to the oven mass should be tightened to a torque of 0.6 newton-metres (5 in.-lbs.). This will insure maximum heat transfer without overstressing the crystal package.

c. Deleted

d. Oven heater transistors Q7 and Q8: Holding screws for Q7 and Q8 must also be torqued to a specific force of 0.6 newton-metres (5 in.-lbs.). There are several available posidrive torquing screwdrivers.

C-68. OVEN CONTROLLER TROUBLESHOOTING

C-69. General

C-70. The oven controller section consists of three major circuits and a 10V voltage reference for increased stability of sensitive circuits. Figure C-13 shows the major circuits and active components involved in their operation.

C-71. The temperature sense circuit monitors the temperature of the oven mass and reduces the power drawn by the oven heater transistors when the oven mass has reached operating temperature. After power cut-back, this circuit monitors the oven mass temperature and controls the power in the heaters to maintain the constant temperature. The thermistor (RT1) has a negative temperature coefficient. At room temperature the thermistor resistance is approximately 100K ohms, while at operating temperature (~82°C) the resistance is approximately 9K ohms. Shorting the thermistor to oven common makes the oven mass appear too hot to the temperature sense circuit. This in turn causes the temperature sense circuit to shut off power to the oven heaters. This technique is used in the troubleshooting procedure.

C-72. The warm-up current limit circuit controls the maximum current the oven may draw during warm-up (380 to 490 mA with 20V dc oven input). This circuit is only active during the warm-up phase of the oven circuit operation.

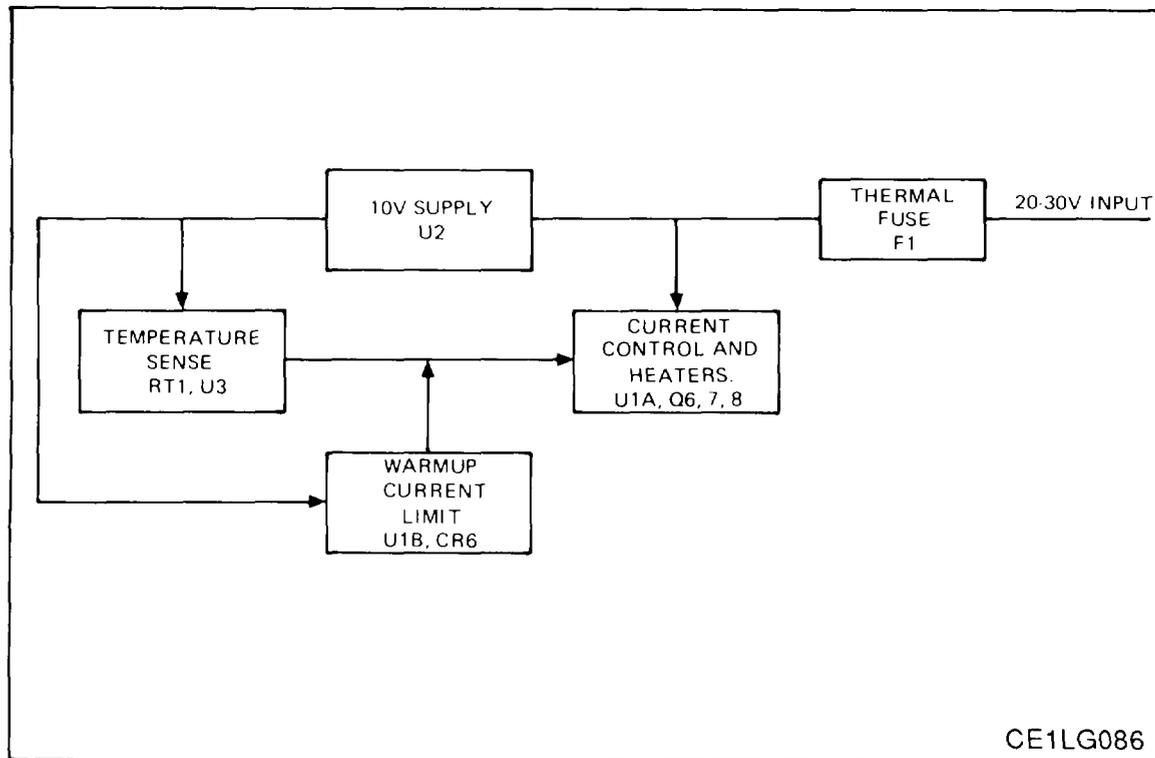


Figure C-13. Oven Controller Block Diagram

C-73. Normal Operation

C-74. When the oven is tested under normal conditions (~25°C ambient temperature) it will initially draw 380 to 490 mA. After 5 to 10 minutes the oven current will start to drop. Over the next 10 to 15 minutes the oven current will fall to the 60 to 150 mA range where it will stabilize. The oven circuit should not oscillate.

WARNING

DO NOT OPERATE THE OVEN CIRCUITS WHEN THE OVEN MASS IS OUTSIDE OF THE OSCILLATOR INSULATED HOUSING. DOING SO WILL OVERHEAT THE OSCILLATOR CIRCUITS INSIDE THE OVEN MASS AND CAUSE PERMANENT DAMAGE. ALL OVEN TEST POINTS ARE AVAILABLE WITH THE OVEN MASS AND OVEN CONTROLLER CIRCUIT INSIDE THE HOUSING.

WHEN OSCILLATOR COVER AND INSULATOR ARE REMOVED THERMAL FUSE WILL NOT PROTECT CIRCUIT FROM OVERHEATING. APPLY OVEN POWER ONLY WHEN ACTUALLY MAKING MEASUREMENTS FOR TROUBLESHOOTING OR AS DIRECTED IN TROUBLESHOOTING TREE, TABLE C-2.

C-75. TROUBLESHOOTING

C-76. Table C-2 is a troubleshooting tree for the oven circuits. The troubleshooting procedure separates the different functional circuits by monitoring the oven supply current during different operating conditions. For example, if the warm-up current is excessive, this indicates a trouble in the warm-up current limit circuit, or the current control and heater circuit. If shorting the thermistor reduces the current being drawn from the power supply, this indicates the current control circuit is operating and the problem is most likely in the warm-up current limit circuit.

C-77. As with most troubleshooting trees this is intended to be a guide to the trouble area. It is not a substitute for technical skill in isolating the faulty components.

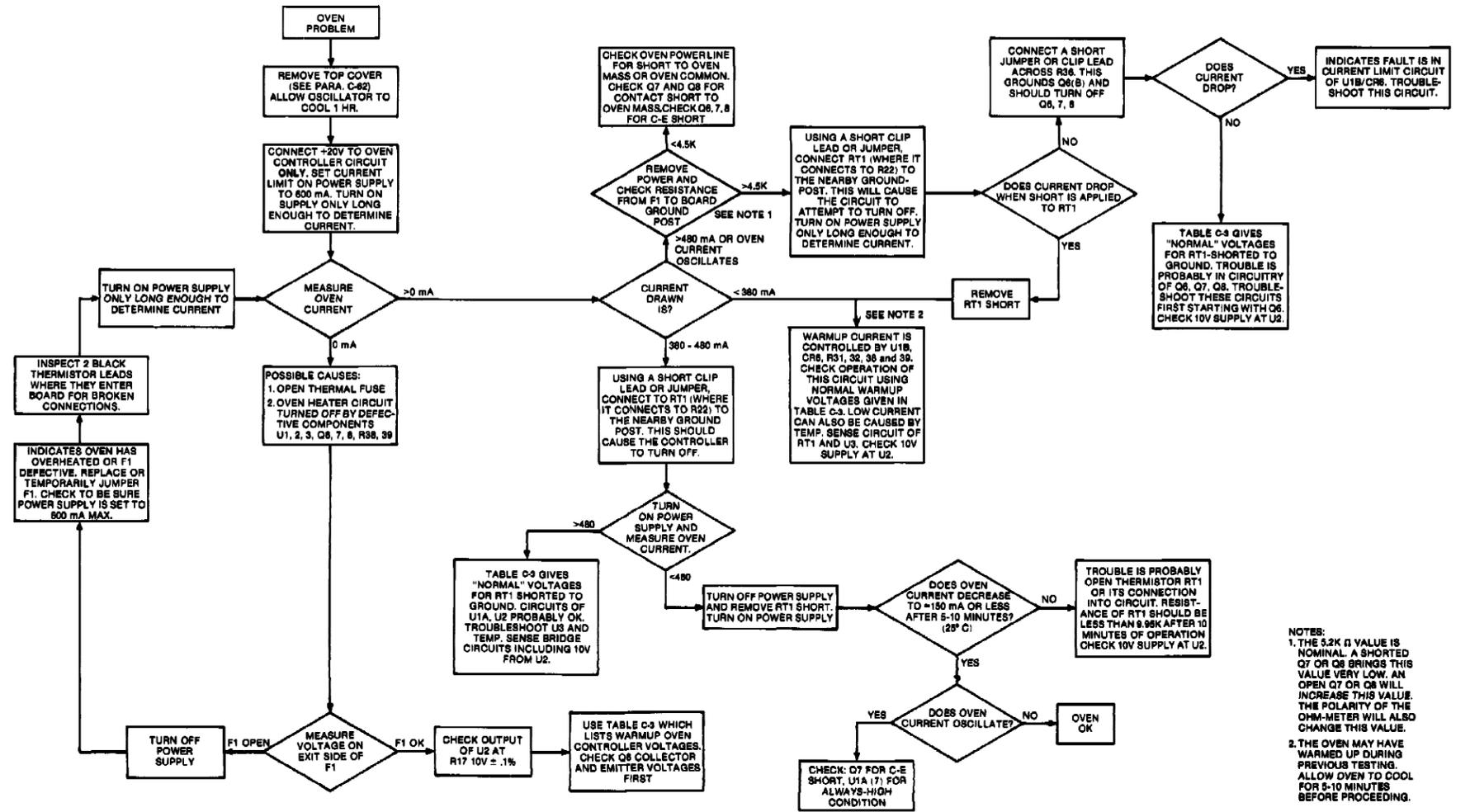
C-78. Table C-3(next to schematic diagram) gives normal circuit voltages during warm-up, operation, and when thermistor RT1 is shorted to ground. Use this table during troubleshooting.

C-79. Troubleshooting Cautions

C-80. When oven current is excessive, turn on the power supply only long enough to make the necessary measurements. Do not leave power on if the oven is drawing excessive current. With the housing cover and foam insulator removed, the thermal fuse (F1) cannot protect the circuits in the oven mass from overheating and damage.

C-81. Flex Damage

C-82. If a tear in the flex circuit occurs, the tear can continue until a trace is broken. To stop a tear, use a pair of scissors and cut around the tear. **DO NOT CUT A SHARP CORNER** as this will cause a stress concentration allowing the tear to start again. A hole punch may also be used. Punch a hole in the flex so as to remove the forward end of the tear.



NOTES:
1. THE 5.2K Ω VALUE IS NOMINAL. A SHORTED Q7 OR Q8 BRINGS THIS VALUE VERY LOW. AN OPEN Q7 OR Q8 WILL INCREASE THIS VALUE. THE POLARITY OF THE OHM-METER WILL ALSO CHANGE THIS VALUE.
2. THE OVEN MAY HAVE WARMED UP DURING PREVIOUS TESTING. ALLOW OVEN TO COOL FOR 5-10 MINUTES BEFORE PROCEEDING.

FO Table C-2 Oven Controller Troubleshooting Tree

C-83. OSCILLATOR TROUBLESHOOTING

C-84. The oscillator circuits are relatively simple and straightforward. The following paragraphs will briefly describe the major circuit areas, a troubleshooting outline, and some helpful suggestions to make the troubleshooting process easier. The oscillator consists of four sections. They are:

1. Oscillator Q1, Q2, and associated circuitry.
2. AGC Q3, CR4, CR5, and R6.
3. Output circuit Q5, Q9.
4. 5.7V power supply CR2, CR3, and Q4.

The oscillator is the signal source. Its output level is controlled by the AGC. The 5.7V power supply provides an extra-stable clean voltage source for the oscillator circuits. The output circuits provide a high level signal capable of driving a 50 to 1K ohm load.

C-85. NORMAL OPERATION

C-86. The output of the oscillator circuit at Q2(C) is a 10 MHz undistorted sine wave with an amplitude of approximately 2.8V p-p. The AGC voltage (measured at CR5-C13 junction) is approximately -1.5V. The 10 MHz signal passes through Q5 to Q9(B) at about the same level. The voltage gain of amplifier Q5 (base to collector) is approximately 2 with a 50-ohm load on the output. The output of transformer T1 is approximately 1.5V p-p. All 10 MHz signals found in the 10B11A will be undistorted sine waves unless otherwise noted in Table C-4 (next to the schematic diagram).

C-87. OSCILLATOR TROUBLESHOOTING TECHNIQUES

C-88. When troubleshooting the oscillator section, remove the oven mass from the housing and the covers from the oven mass as described in paragraph C-64. Connect 12V to the oscillator section. Set the power supply current limit to 60 mA. Do not apply power to the oven circuit.

C-89. Initial troubleshooting and probing should be done on the backside of the boards (trace side) while they are secured to the oven mass (see paragraph C-64, step 10). This way the circuits are more easily handled. When the fault is isolated to a few components, the unit may then be disassembled for final troubleshooting and repair.

C-90. Helpful Hints

1. Most points in the oscillator circuits cannot be measured with a dc voltmeter. The reactance of the voltmeter probe and leads will load the circuit and give false readings. Instead, use an oscilloscope with a high input impedance probe for these measurements. Table C-4 (oscillator section normal voltages) indicates when a dc voltmeter can be used.
2. Before reinstalling the oven mass into the housing, adjust the output amplitude (with R6) to 0.53V into a 50-ohm load. Although this value is slightly below normal, the output will increase slightly when the unit is reassembled and is at normal operating temperatures.
3. If a tear in the flex circuit occurs, go to paragraph C-81 for repair instructions.

C-91. TROUBLESHOOTING INFORMATION

C-92. Symptoms of failures in the oscillator sections will generally fall into one of the following categories:

1. No output.
2. Output amplitude is low or high.
3. Output is distorted (contain excessive harmonics).
4. Excessive drift of output frequency.
5. Time domain frequency stability (short-term stability) does not meet specifications.

C-93. Troubleshooting of these faults will be discussed in the following paragraphs.

C-94. NO OUTPUT. This is usually easy to repair by simple signal tracing. Localized fault finding (to actual defective component) can be somewhat more difficult if the problem is in the main oscillator circuit (Q1, Q2, and AGC). If the fault appears to be in the oscillator section and does not yield to normal troubleshooting techniques, measure the AGC voltage at the junction of CR5-C13 (see Note 7 on Table C-4, Oscillator Normal Voltages). If this voltage appears normal, the problem may be a defective quartz crystal (Y1). To verify this possibility, obtain a 10 μ H (HP Part No. 9100-2265) and a 12 μ H inductor (9100-2242). Use the HP numbered parts as these have been tested in the circuit. On the oscillator board, remove the red and blue wires connecting the crystal to the board. Place the 12 μ H inductor in place of these wires. With 12V applied to the circuit, adjust the FREQ ADJUST (C1), and amplitude control (R6) for a good sine wave signal.

NOTE

At some settings of C1 and/or R6, intermittent oscillations may appear. Some minor adjustment of C1 and/or R6 should clear this. If this fails, replace the 12 μ H inductor with the 10 μ H inductor and repeat the C1/R6 adjustment.

If replacing the crystal with an inductor produces oscillation, this is a very good indication of a defective crystal. When replacing crystal Y1, read paragraph C-67(b), Special Parts Considerations. If the circuit will still not oscillate, the problem is most likely one of the oscillator circuit elements.

C-95. OUTPUT AMPLITUDE HIGH OR LOW. Many times this can be cured by the adjustment of R6 as described in paragraph 5-32. If the correct amplitude cannot be obtained with this adjustment, monitor the signal at Q2(C) with an oscilloscope and set R6 to obtain an amplitude of 2.8V p-p. Then check Q5 and Q9 stages. If the Readjustment isn't effective, you should suspect the AGC circuitry (Q3, CR4, CR5, C5, C6, R5, R6, R7, or Q1).

C-96. OUTPUT DISTORTION. Check the distortion with a spectrum analyzer (see Table C-2 step 2. for procedure). If the distortion products are harmonically related to 10 MHz, trace the signal to the distorting stage. If the distortion is not harmonically related to the 10 MHz output:

1. Check the mode suppression components of L2/C5 and/or L3/C6. These components suppress oscillations at all frequencies other than 10 MHz.
2. Check for spurious oscillations from the amplifier stages and oscillator transistors.

C-97. EXCESSIVE DRIFT OF OUTPUT FREQUENCY. When a quartz crystal oscillator has not been operated for a long period of time, or if it has been subjected to severe thermal or mechanical shock, the oscillator may take some time to stabilize. In most cases, the crystal will

drift and then stabilize at or below the specified rate within a few days after being turned on. In isolated cases, depending on the amount of time the oscillator has been off and the environmental conditions it has experienced, the 10811A may take up to 1 week to reach the specified aging rate. This should be taken into consideration if the drift rate of the unit is out of specifications. If the unit has had sufficient time to stabilize but is still out of specification, the most likely cause of excessive drift is a defective crystal (Y1). If Y1 is to be replaced, read paragraph C-67(b). Other possible causes are unstable C3 and/or C8.

C-98. TIME DOMAIN STABILITY (SHORT-TERM STABILITY) OUT OF SPECIFICATION. Measurement of time domain stability is somewhat difficult and exacting. If the 10811A fails this test, be sure no signal sources other than the test reference are operating near the measurement system, as these can cause interference with the measurement. Other sources of error are vibration, nearby electrical equipment, poor shielding, or motors that can radiate signals into the 10811A. The failure to connect the EFC input (to ground) can cause poor frequency stability as can a noisy voltage being used for the EFC control. If another oscillator is available (known to be good), verify the accuracy of the measurement system. This could save considerable troubleshooting time.

C-99. Two other possibilities external to the oscillator are the oven and oscillator power supplies. These must be stable in order for the circuits to function properly.

C-100. When troubleshooting this condition, carefully monitor the output waveform. Check for distortion or intermittent distortion, small amplitude variations (there should be none), or spurious oscillations on the output signal. Use a spectrum analyzer for this test (see Table C-3, step 3). These symptoms can be more readily traced than small frequency fluctuations.

C-101. Almost any of the circuits can cause poor short-term stability. However, the most probable cause is crystal Y1. Other possible causes are the oven controller circuit (keeps changing temperature) or defective frequency determining components (CR1, C1, C3, C8, or instability in the 5.7V supply). Q1 and Q2 are also good suspects. Instability can also be caused by the AGC circuit, but this is usually visible as output amplitude variations or instability on the output waveform.

C-102. To check oven stability, allow the 10811 A to operate normally away from drafts or sudden temperature changes. Allow the unit to warm up for at least 1-hour then connect a sensitive recorder or digital voltmeter to the OVEN MONITOR OUTPUT. Once the oven has stabilized, the monitor voltage should not vary more than 100-200 μ V when measured over 3- to 4-minute periods. Causes of oven instability are temperature sensing elements RT1, U2, U3, and associated components.

Table C-3. Oven Circuit Voltages*

VOLTAGE POINT	OVEN AT OPERATING TEMP.	OVEN COLD (JUST AFTER TURN-ON)	RT1 GROUNDED
Q6B	1.6	2.	.25
Q6C	11.4	11.4	11.4
Q6E	1.	1.3	0
Q7B	12.5	12.7	11.9
Q7C	20.	20.	20.
Q7E	11.4	11.4	11.4
Q8B	1.	1.3	0
Q8C	11.4	11.4	11.4
Q8E	.07	.23	0
U1 Pin 1	8.9	1.8	8.9
U1 Pin 2	.07	.23	0
U1 Pin 3	.2	.23	.2
U1 Pin 5	4.	4.1	3.8
U1 Pin 6	4.	4.1	3.8
U1 Pin 7	3.3	4.8	1.5
U2 Pin 2	10.	10.	10.
U3 Pin 6	3.5	19.0	.5

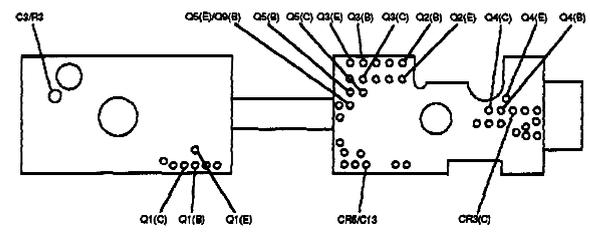
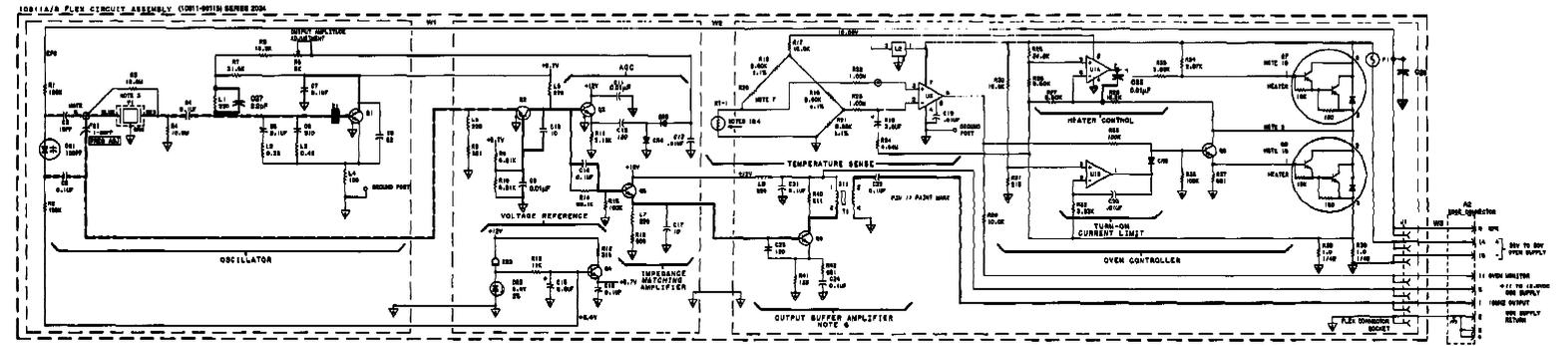
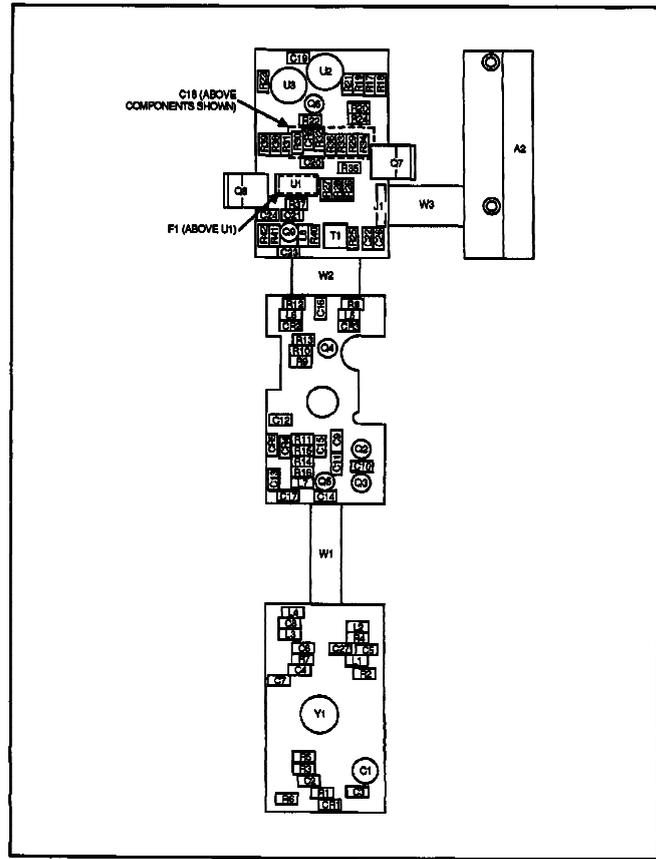
* Voltage readings taken with oven supply voltage of 20V dc and insulating foam and cover removed. Voltages are approximate and will vary slightly from unit-to-unit.

Table C-4. Oscillator Section Normal Voltages (see Notes 1,2,3)

VOLTAGE POINT	NORMAL VOLTAGES		REMARKS
	AC (p-p)	DC	
C3/R3	1 to 4	—	Note 8
CR5/C13	—	-1.5	Notes 4 and 7
CR3(C)	0	6.3	Note 4
Q1(B)	1	.75	Note 8
Q1(C)	0	5.5	Note 4
Q1(E)	.9	.03	Note 8
Q2(B)	0	2.7	Note 4
Q2(C)	2.7	5.6	Note 8
Q2(E)	.06	2	Notes 4 and 5
Q3(B)	2.7	5.6	Note 8
Q3(C)	0	11.8	Note 4
Q3(E)	2.4	4.9	Notes 4 and 6
Q4(B)	0	6.3	Note 4
Q4(C)	0	10.3	Note 4
Q4(E)	0	5.6	Note 4
Q5(B)	2.7	3.1	Note 8
Q5(C)	0	11.8	Notes 8 and 9
Q5(E)	2.8	2.6	Note 8
Q9(B)	2.8	2.8	Note 8, 9
Q9(C)	5.1	11.8	Note 8, 9
Q9(E)	2.5	1.9	Note 8

NOTES:

- All voltages taken with 12V oscillator supply.
- Voltages are approximate and will vary slightly from unit-to-unit.
- All ac voltages are sine waves except Q2(E) and Q3(E).
- This dc voltage may be measured with a standard dc voltmeter. All other voltages should be measured with an oscilloscope and high impedance probe to minimize circuit loading.
- Waveform is  .06v.
- Waveform is slightly flattened on the bottom
- This is the AGC voltage. Value shown is nominal with oscillator operating. If the oscillator is not oscillating, the AGC voltage will be +2.5V.
- Measure both ac and dc voltages with an oscilloscope and a high impedance probe to minimize circuit loading.
- AC voltage at Q9(C) measured with 50-ohm load on the output.



NOTES:

1. WHEN RECONNECTING THE THERMISTOR LEADS:
 - a. REMOVE AND PROTECT FROM THE OVER HEAT.
 - b. INSERT THE THERMISTOR LEADS IN THE SAME HOLES ALL THE WAY THROUGH THE HOLES IN THE FLEX CIRCUIT. THE OSCILLATOR SHOULD BEAT AGAINST THE FLEX CIRCUIT BOARD AS SHOWN BELOW.
2. THE VOLTAGE AT BRIDGE/COIL SHOULD BE OPEN OVER SUPPLY. THE SAME 2.0V. SEE NOTE 4.
3. SEE PARAGRAPH CATHODE BEARING REPLACING THE CRYSTAL. IT, WHEN REINSTALLING THE CRYSTAL INTO THE OVER HEAT, TIGHTEN RESISTANCE NOT TO 1 TORQUE OF 1.5-1.8 INCH-POUNDS.
4. THERMISTOR BODY TEMPERATURE RESISTANCE IS APPROXIMATELY 100K. THERMISTOR IS PART OF FROG BOARD U11 AND CANNOT BE REPLACED SEPARATELY. RESISTANCE BETWEEN THERMISTOR AND OVER HEAT SHOULD BE GREATER THAN 100 OHMS OVER.
5. THIS AREA OF THE BRIDGE BOARD IS HIGH IMPEDANCE. THE AREA MUST REMAIN CLEAN.
6. THE VOLTAGE FROM FROG BOARD TO BRIDGE/COIL IS APPROXIMATELY 1.5V. A 50 OHM LOAD ON THE OUTPUT.
7. R48 IS SELECTED TO MATCH CRYSTAL Y1. IF Y1 IS DAMAGED, THE SUPPLIER CAN NOT BE USED. SEE PARAGRAPH CATHODE.
8. ALL VALUES OF CAPACITANCE IN 20% TOLERANCE AND DIMENSIONS IN 0.005-INCHES UNLESS OTHERWISE SPECIFIED.
9. ALL VOLTAGES MEASURED WITH 1K TO THE OSCILLATOR CIRCUITS AND 50K TO THE OVER CIRCUITS.
10. WHEN REINSTALLING R7 AND R8 OVER THE OVER HEAT, ISOLATE THE BRIDGE BOARD TO 200-400 OHM RESISTANCE. IF R7 AND R8 ARE TO BE REPLACED, SEE PARAGRAPH CATHODE.



CE1LG087



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PAGE NO	PARA-GRAPH	FIGURE NO	TABLE NO
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2-25	2-28		
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3-10	3-3		3-1
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5-6	5-8		
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F03

IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:

Recommend that the installation antenna alignment procedure be changed throughout to specify a 2° IFF antenna lag rather than 1°.

REASON: Experience has shown that with only a 1° lag, the antenna servo system is too sensitive to wind gusting in excess of 25 knots, and has a tendency to rapidly accelerate and decelerate as it hunts, causing strain to the drive train. Hunting is minimized by adjusting the lag to 2° without degradation of operation.

Item 5, Function column. Change "2 db" to "3db."

REASON: The adjustment procedure for the TRANS POWER FAULT indicator calls for a 3 db (500 watts) adjustment to light the TRANS POWER FAULT indicator.

Add new step f.1 to read, "Replace cover plate removed in step e.1, above."

REASON: To replace the cover plate.

Zone C 3. On J1-2, change "+24 VDC to "+5 VDC."

REASON: This is the output line of the 5 VDC power supply. +24 VDC is the input voltage.

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