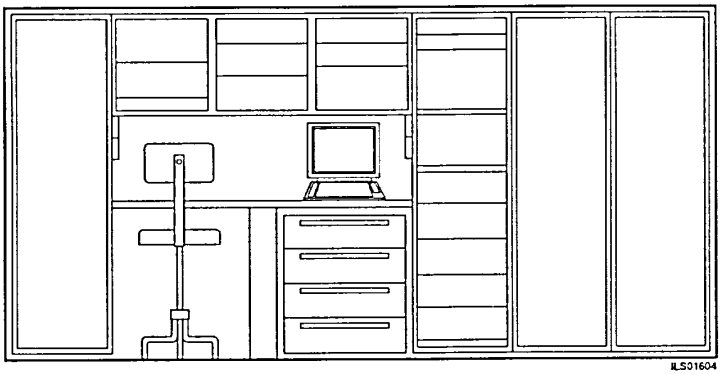
TECHNICAL MANUAL

OPERATOR, UNIT AND DIRECT SUPPORT MAINTENANCE MANUAL

FAST DIRECTION FINDING TEST SET GROUP

OQ-493/USD



Headquarters, Department of the Army

July 1994

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5 SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK

1. DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL
2. IF POSSIBLE, TURN OFF THE ELECTRICAL POWER
3. IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH, OR LIFT THE PERSON TO SAFETY USING A DRY WOODEN POLE OR A DRY ROPE OR SOME OTHER INSULATING MATERIAL
4. SEND FOR HELP AS SOON AS POSSIBLE
5. AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION

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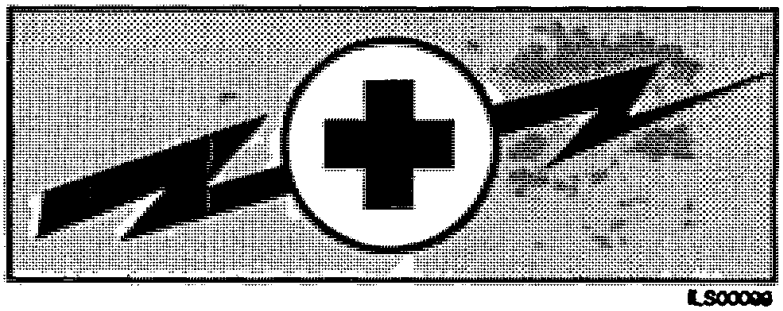
SAFETY SUMMARY

WARNING



WARNING

Do not connect more than two LRUs (the digital processor T/S and the LRU under test) to power junction box C5A6 at the same time. If more than two LRUs are connected simultaneously to power junction box C5A6, power supplies C5A9 and C5A10 can be overloaded. Overloading the power supplies can cause a fire or explosion that is harmful to personnel and can damage equipment.

WARNING

Trichlorotrifluoroethane, trichloroethane, and similar chemical solvents are no longer used for ordinary cleaning of equipment. These substances threaten public health and the environment by destroying ozone in the earth's upper atmosphere. Suitable nonhazardous cleaning materials are used instead (i.e., use a clean cloth dampened with water and a mild detergent or with an approved substitute solvent).

WARNING

Extremely high current can be generated by accidentally shorting voltages to ground. Conductive jewelry, especially rings and watches, that could come in contact with the hardware should be removed.

WARNING

Before performing any repair procedure, power must be removed from the digital processor T/S by disconnecting cables from connectors 114 and J15.

WARNING

High voltage and low voltage/high current are used in the operation of this equipment. Ensure that all power is disconnected from connectors J14 and J15 when any maintenance procedure is performed. When performance test/troubleshooting procedure is being performed, care must be taken to avoid contacting high-voltage connections or grounding the high-current sources when operating this equipment. Injury or death may result if personnel fail to observe safety precautions.

Caution

This equipment contains parts and assemblies sensitive to damage by electrostatic discharge (ESD). Use ESD precautionary procedures when touching, removing, or inserting printed circuit card assemblies.

ESD
CLASS 1

GENERAL HANDLING PROCEDURES FOR ESDS ITEMS

- Use wrist ground straps or manual grounding procedures.
- Keep ESDS items in protective covering when not in use.
- Ground all electrical tools and test equipment
- Periodically check continuity and resistance of grounding system.
- Use only metallized solder suckers.
- Handle ESDS items only in protected areas.

MANUAL GROUNDING PROCEDURES

- Make certain equipment is powered down.
- Touch ground prior to removing ESDS items.
- Touch package of replacement ESDS item to ground before opening.
- Touch ground prior to inserting replacement ESDS items.

ESD PROTECTIVE PACKAGING AND LABELING

- Intimate covering of antistatic material with an outer wrap of either type 1 aluminized material or conductive plastic film or hybrid laminated bags having an interior of antistatic material with an outer metallized layer.

- Label with sensitive electronic symbol and caution note.

Caution

Be sure to set power switch at power supply C5A9 OFF while removing and installing CCAs in the digital processor T/S.

Caution

When performing steps in the digital processor T/S performance test and troubleshooting procedure, when prompted by the computer via the VDT to replace or reseat a CCA within the digital processor T/S, remove power cable from connector J15 prior to performing that step.

Technical Manual

No. TM 11-6625-3291-13

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, D.C., 1 July 1994

OPERATOR, UNIT, AND DIRECT SUPPORT MAINTENANCE MANUAL FOR FAST DIRECTION FINDING TEST SET 00-493/USD (NSN N/A)(EIC: N/A)

REPORTING OF ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in back of this manual directly to Commander, U.S. Army Communications-Electronics Command and Fort Monmouth, Attn: AMSEL-LC-LM-LT, Fort Monmouth, NJ 07703-5007. A reply will be sent directly to you.

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HOW TO USE THIS MANUAL

HOW DO I FIND INFORMATION?

Front Cover. Use the front cover to quickly find the chapters shown on the front cover of this manual.

Table of Contents. Entries within the main table of contents duplicate the entries on the front cover. This is in case the front cover is torn off.

Chapter and Section Indexes. Indexes are located in the front of each chapter and in the front of lengthy sections.

HOW DO I GET FAMILIAR WITH THE EQUIPMENT?

See chapter 1 for physical and functional descriptions.

DOES THE MANUAL CONTAIN OPERATING INSTRUCTIONS?

In some cases. See chapter 2.

WHAT IS THE EXTENT OF UNIT MAINTENANCE?

See chapter 3. Normally, unit maintenance is limited to quarterly preventive maintenance checks and services.

WHERE IS DIRECT SUPPORT MAINTENANCE?

See chapter 4.

ARE OTHER MANUALS REQUIRED?

Yes. Refer to appendix A for a list. Obtain these manuals through supply channels.

WHAT TOOLS AND EQUIPMENT ARE REQUIRED?

Turn to appendix B (Maintenance Allocation) for a listing.

WHAT ABOUT EXPENDABLE MATERIALS AND SUPPLIES?

Turn to appendix E for a listing. Procure these items through supply channels.

WHAT ACTIONS ARE TAKEN IF MISTAKES ARE FOUND IN THE MANUAL?

See the block at the start of the table of contents.

DO I NEED TO KNOW ANY SPECIAL SAFETY INSTRUCTIONS?

Yes you do. You should read the safety summary at the front of the manual.

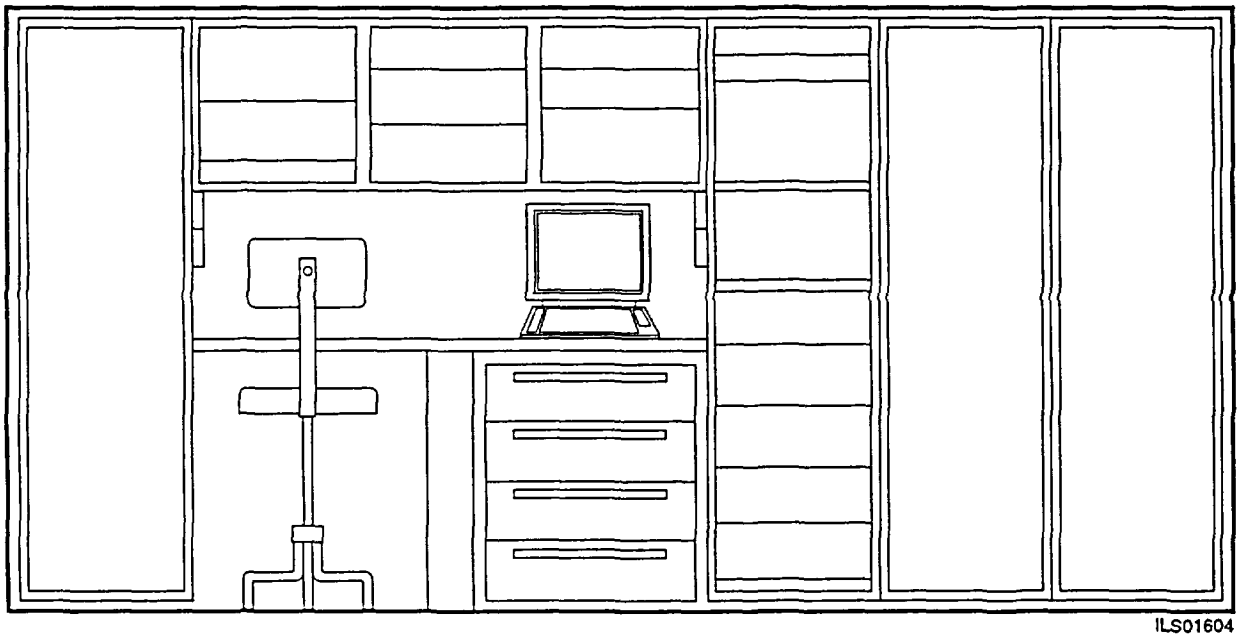

Figure 1-1. Fast Direction Finding Test Set Group OQ-493/USD

CHAPTER 1

INTRODUCTION

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SECTION I. GENERAL INFORMATION

This section provides information about the scope of this manual and general information about forms and administrative items.

1.1 SCOPE

This manual provides operator, unit, and direct support maintenance instructions for Fast Direction Finding Test Set Group OQ-493/USD (figure 1-1), commonly referred to as the FDF T/S group. The FDF T/S group is part of Electronics AN/USM-652, commonly referred to as the Airfield Maintenance Facility (AMF). The FDF T/S group consists of Digital Processor Test Set TS-4204/TSQ-105(V), commonly referred to as the digital processor T/S, and various general purpose test equipment.

The FDF T/S group is used to test and troubleshoot many of the line-replaceable units (LRUs) contained in Surveillance Information Processing Center AN/TSQ-176, commonly referred to as the Integrated Processing Facility (IPF), and Radio Remote Receiving Set AN/ARW-83(V)7, commonly referred to as the Airborne Relay Facility (ARF). In addition, the FDF T/S group may be used to test and troubleshoot certain equipment items that are part of equivalent IPF, ARF, or other similar subsystems.

Included in the manual are general descriptions and data; instructions for installation, operation, and preventive and corrective maintenance; and functional descriptions.

1.2 CONSOLIDATED INDEX OF ARMY PUBLICATIONS AND BLANK FORMS

Refer to the latest issue of DA Pam 25-30 to determine if there are new editions, changes, or additional publications pertaining to the equipment.

1.3 MAINTENANCE FORMS, RECORDS, AND REPORTS

1.3.1 Reports of Maintenance and Unsatisfactory Equipment

Maintenance forms, records, and reports that are to be used by maintenance personnel at all maintenance levels are listed in and prescribed by DA Pam 738-750 as contained in Maintenance Management Update.

1.3.2 Report of Item and Packaging Discrepancies

Fill out and forward SF 364 (Report of Discrepancy (ROD)) as prescribed in AR 735-1 1-2/DLAR 4140.55/SECNAVMATINST 4355.73A/AFR 400-54/MCO 4430.3J.

1.3.3 Transportation Discrepancy Report (TDR) (SF 361)

Fill out and forward Transportation Discrepancy Report (DR) (SF 361) as prescribed in AR 5538/NAVSUPINST 4610.33C/AFR 75-18/MCO P4610.19D/DLAR 4500.15.

1.4 DESTRUCTION OF ARMY MATERIEL

Destruction of Army materiel to prevent enemy use shall be as prescribed in TM 750-244-2.

1.5 PREPARATION FOR STORAGE OR SHIPMENT

Refer to chapter 3 for storage and shipment procedures.

1.6 ADMINISTRATIVE STORAGE

Administrative storage of equipment issued to and used by Army activities will have preventive maintenance performed in accordance with the preventive maintenance checks and services (PMCS) charts before storing. When removing the equipment from administrative storage, the PMCS should be performed to assure operational readiness. Disassembly and repacking of equipment for shipment or limited storage are covered in chapter 3.

1.7 REPORTING EQUIPMENT IMPROVEMENT RECOMMENDATIONS (EIR)

EIRs will be prepared using SF 368 (Quality Deficiency Report). EIRs should be mailed directly to the Commander, U.S. Army Communications-Electronics Command and Fort Monmouth, Attn: AMSELLC-ED-TC, Fort Monmouth, New Jersey 07703-5023. A reply will be furnished directly to you.

SECTION II. EQUIPMENT DESCRIPTION AND DATA

This section describes the equipment characteristics, capabilities, and features; provides descriptions of the FDF T/S group equipment; and provides listings of tabulated data.

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1.8 EQUIPMENT CHARACTERISTICS, CAPABIUTIES, AND FEATURES

Equipment characteristics, capabilities, and features of the FDF T/S group are listed in table 1-1. As mentioned previously, the FDF T/S group is used to test and troubleshoot certain LRUs in the IPF subsystem, certain LRUs in the ARF subsystem, and certain LRUs in other equivalent systems or subsystems.

Table 1-1. FDF T/S Group Characteristics, Capabilities, and Features

CHARACTERISTICS (refer to figure 1-2 and table 1-2):

- Provides automated testing and troubleshooting, under computer control, of certain LRUs in the ARF and IPF subsystems, as listed in table 1-2.
- Provides dc power sources and standard test equipment that functions as an ordinary test bench for manual checkout of other IPF/ARF subsystem LRUs. Manually tested LRUs are also listed in table 1-2.

CAPABILITIES AND FEATURES:

- Automated testing is computer controlled per FDF T/S group test software. Operator interaction with the test software is performed via a video display terminal (VDT).
- During execution of automated tests, setup and operation of FDF T/S group standard test equipment are performed automatically by the FDF T/S group computer.
- Once an automated test has been initiated by the operator, the FDF T/S group does not typically require operator interaction during test execution.
- Certain automated tests are computer directed, meaning that test software prompts the operator with the logical sequencing of required tests to be performed. Other automated tests require the operator to direct the sequence of tests to be performed, as dictated in the LRU maintenance manual for the unit under test (UUT).
- For some automated tests, the pass/fail test result is determined by the FDF T/S group computer. In others, the test results are observed and evaluated by the operator; these test results are input to the FDF T/S group computer via the VDT.
- When the FDF T/S group is used as an ordinary test bench, it supplies dc power sources for manually tested LRUs via supplied power interconnect cables. The FDF T/S group standard test equipment is connected to the UUTs via supplied cables.
- Most individual equipment items in the FDF T/S group contain built-in power-up selftest diagnostics.
- Automated testing and troubleshooting of the FDF T/S group computer are provided to verify correct operation, and to fault isolate to defective internal assemblies per procedures in chapter 4 of this manual.
- Several standard test equipment items in the FDF T/S group perform automatic selfcalibration routines on power-up. These self-calibration routines do not require operator interaction during execution.

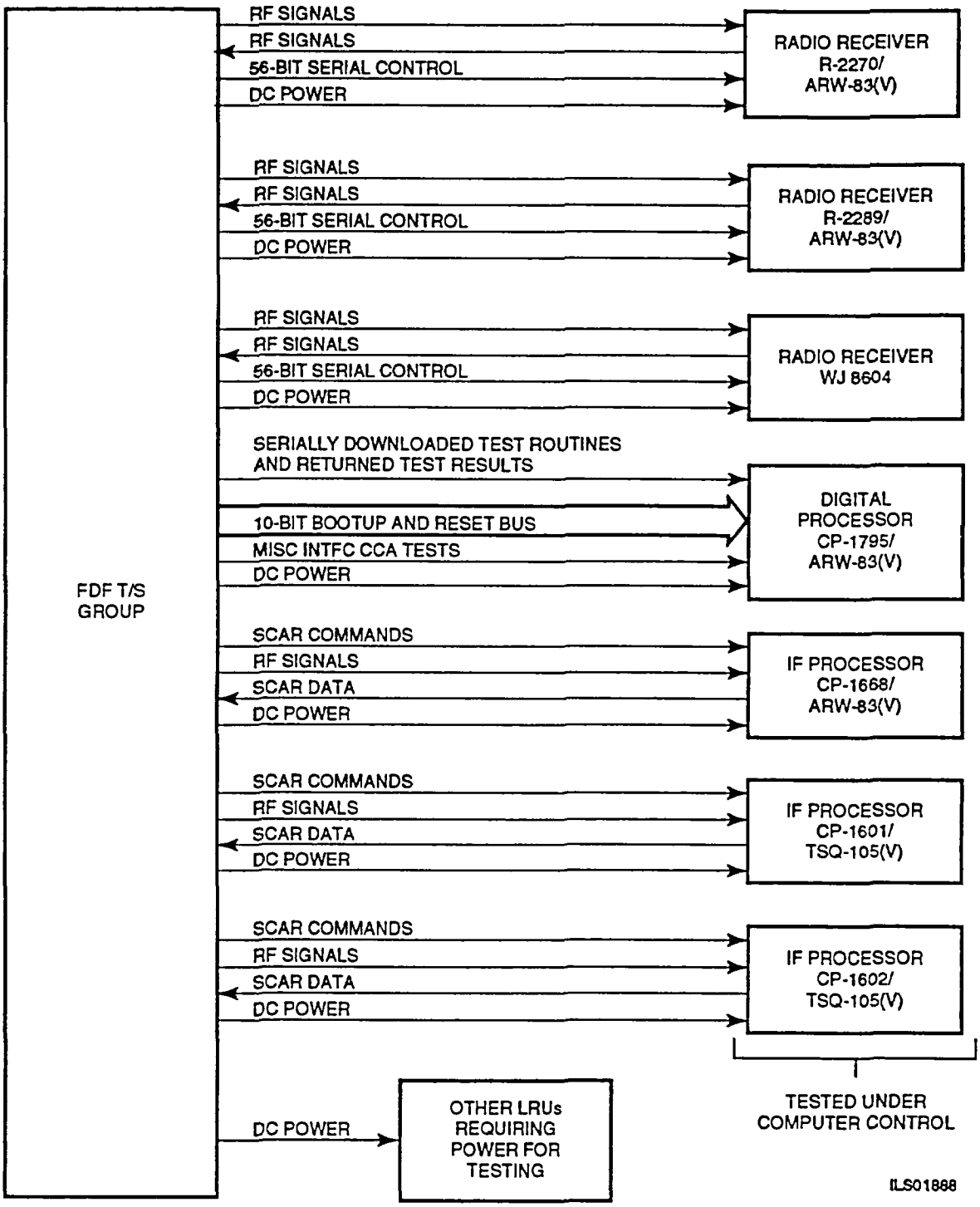

Figure 1-2. FDF TIS Group Interface Block Diagram

Table 1-2. ARF/IPF LRUs Tested by FDF T/S Group

Nomenclature	Common name	Technical manual	Test method
Digital Processor CP-1795/ARW-83(V)	ARF digital processor	TM 11-5865-268-13	Computer-controlled, computer-directed
Radio Receiver R-2270/ARW-83(V)	R-2270 receiver	TM 11-5821-321-13	Computer-controlled, computer-directed and computer-controlled, operator-directed
Radio Receiver R-2289/ARW-83(V)	R-2289 receiver	TM 11-5821-327-13	Computer-controlled, computer-directed and computer-controlled, operator-directed
Radio Receiver WJ-8604	WJ-8604 receiver	TM 11-5821-352-13	Computer-controlled, computer-directed and computer-controlled, operator-directed
RF Processor CP-1606/ARW-83(V)	RF processor	TM 11-5865-236-13	Computer-controlled, computer-directed
IF Processor CP- 1668/ARW- 83(V)	SCAR processor level 0	TM 11-5865-246-13	Computer-controlled, computer-directed
IF Processor CP- 1601/TSQ- 105(V)	SCAR processor level 1	TM 11-5865-245-13	Computer-controlled, computer-directed
IF Processor CP-1602/TSQ-105(V)	SCAR processor level 2	TM 11-5865-238-13	Computer-controlled, computer-directed
Demultiplexer TD-1373/U	Uplink demultiplexer	TM 11-5865-241-13	Manual testing using power supplies and general purpose test equipment
Multiplexer TD-1374A/U	Data multiplexer	TM 11-5865-239-13	Manual testing using power supplies and general purpose test equipment

Table 1-2. ARF/IPF LRUs Tested by FDF T/S Group - Continued

Nomenclature	Common name	Technical manual	Test method
Radio Frequency Distribution Unit SB-4187/ ARW-83(V)	RF distribution unit	TM 11-5865-254-13	Manual testing using power supplies and general purpose test equipment
Frequency Converter CV-3836/ARW-83(V)	SCAR downconverter	TM 11-5865-250-13	Manual testing using power supplies and general purpose test equipment

For purposes of this discussion and those that follow, the FDF T/S group interface to UUTs is described for the LRUs contained in the above IPF and ARF subsystems as the primary application example. Figure 1-2 shows an interface block diagram of the FDF T/S group for the IPF and ARF subsystem LRU UUTs.

Table 1-2 lists the nomenclature for the UUTs that interface with the FDF T/S group, their respective common names, associated technical manuals, and FDF T/S group test method(s) used for LRU testing/troubleshooting.

1.9 LOCATION AND DESCRIPTION OF MAJOR COMPONENTS

Figure 1-3 shows the location of equipment supplied with the FDF T/S group. Table 1-3 lists the FDF T/S group equipment by official name, reference designator, common name, and part number keyed to figure 1-3. Table 1-3 also references publications that provide additional information about the FDF T/S group equipment items.

The FDF T/S group equipment is rack mounted in one relay rack and the three bays of the electronics cabinet. The work table surface holds VDT C4A4 and free-standing equipment items such as the frequency doubler, the transmission/reflection test set, the power splitter, and the minimum loss pad, which do not have reference designators. The relay rack, electronics cabinet, work table, drawers, and chair are not part of the FDF T/S group, but they are provided as part of the AMF, in which the FDF T/S group resides.

The relay rack and cabinet bays are designated 1 thru 7 from left to right, when facing the front of the relay rack and electronics cabinet. Each piece of equipment mounted in the relay rack and electronics cabinet bays has a reference designator.

The reference designator is a combination of the letter of the bay in which a piece of equipment is located and the number of the vertical position occupied by the equipment item in that bay. The equipment items are numbered successively from the top of each bay, beginning with number 1.

The following paragraphs describe the FDF T/S group, as a whole, and its individual equipment items.

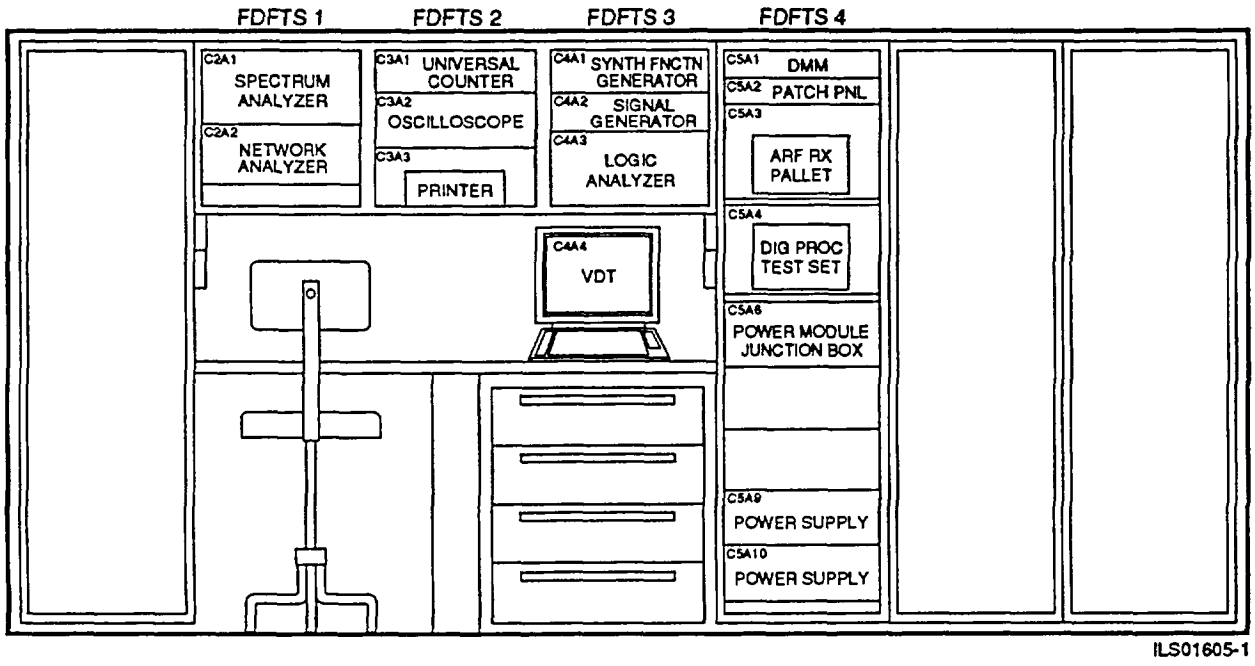

Figure 1-3. FDF TIS Group Equipment Locations

Table 1-3. FDF T/S Group Equipment List

Reference designator	Official nomenclature	Common name/ Ref. TM no.
None	Fast Direction Finding Test Set Group OQ-493/USD 21-186760-1	Fast DF test set (FDF T/S) group TM 11-6625-3291-13 TM 11-6625-3291-23P
C2A1	Spectrum Analyzer HP 8560A, w/Opt 002/003 16-185136-1	Spectrum analyzer TM 11-6625-3286-14 TM 11-6625-3286-24P
C2A2	Network Analyzer HP 8753C 16-185138-1	Network analyzer TM 11-6625-3289-14 TM 11-6625-3289-24P
C3A1	Universal Counter HP 5335A 16-172190-1	Universal counter TM 11-6625-3068-14 TM 11-6625-3068-24P
C3A2	Oscilloscope TEK 2440 16-185139-1	Oscilloscope TM 11-6625-3283-14 TM 11-6625-3283-24P
C3A3	ThinkJet Printer HP 2225A 16-185135-1	Printer TM 11-7025-321-14 TM 11-7025-321-24P
C4A 1	Synthesizer Function Generator SG-1288/G Wavetek 288 16-185133-1	Function generator TM 11-6625-3198-12 TM 11-6625-3198-24P
C4A2	Signal Generator HP 8657B, w/Opt 001 ESL 16-185137-1	Signal generator TM 6625-3281-14 TM 6625-3281-24P
C4A3	Logic Analyzer HP 1650B 16-185140-1	Logic analyzer TM 11-6625-3284-14 TM 11-6625-3284-24P
C4A4	Computer Terminal HP 700/96 C1064W	Video display terminal (VDT) TM 11-6625-3291-13 TM 11-6625-3291-23P
C5A1	Digital Multimeter AN/GSM-64D Fluke 8840A/AF 16-185141-1	Digital multimeter, DMM TM 11-6625-444-14-3 TM 11-6625-444-24P-3

Table 1-3. FDF T/S Group Equipment List - Continued

Reference designator	Official nomenclature	Common name/ Ref. TM no.
C5A2	Patch Panel Trompeter Electronics JS-24WD3SF7/BJ28	Patch panel TM 11-6625-3291-13 TM 11-6625-3291-23P
C5A3	ARF Intercept Receiver Pallet 10-182950-1	ARF intercept receiver (RX) pallet TM 11-5821-352-13 TM 11-5821-352-23P
C5A4	Digital Processor Test Set TS-4204/TSQ-105(V) 10-166609-1	Digital processor T/S TM 11-6625-3291-13 TM 11-6625-3291-23P
C5A6	Power Module Junction Box 10-162550-1 TM 11-6625-3291-23P	Power junction box TM 11-6625-3291-13
C5A9, C5A10	Power Supply Lambda 25699 TM 11-6130-484-23P	Power supplies TM 11-6130-484-13
None	Switch Box INMAC H080000	VDT/STE - PAM switch box
None	Frequency Doubler HP 11721A	Frequency doubler
None	Transmission/Reflection Test Set HP 85044A/B	Transmission/reflection test set TM 11-6625-3282-14
None	Three-Way Power Splitter HP 11850A	Power splitter
None	Minimum Loss Pad HP 11852B	Minimum loss pad
None	N-type Precision RF Cable Set HP 11851B	Precision RF cable set TM 11-6625-3291-13 TM 11-6625-3291-23P
None	50-Ohm N-type Accessory Kit HP 11853A	50-ohm N-type accessory kit TM 11-6625-3291-13 TM 11-6625-3291-23P

Table 1-3. FDF T/S Group Equipment List - Continued

Reference designator	Official nomenclature	Common name/ Ref. TM no.
None	75-Ohm N-type Accessory Kit HP 11855A	75-ohm N-type accessory kit TM 11-6625-3291-13 TM 11-6625-3291-23P
None	ARF Maintenance Kit MX-2648 21-178363-1	ARF maintenance kit TM 11-6625-3291-13 TM 11-6625-3291-23P
None	Ac/Dc Power Cable Kit 21-164447-1	Ac/Dc power cable kit TM 11-6625-3291-13 TM 11-6625-3291-23P
None	Coaxial Cable 09-188941-1 thru -7	Coaxial cable TM 11-6625-3291-13 TM 11-6625-3291-23P
None	Test Signals Cable Kit 1-164448-1	Signal cable kit TM 11-6625-3291-13 TM 11-6625-3291-23P

1.9.1 FDF T/S Group

The FDF T/S group (figure 1-3 and table 1-3) includes the digital processor T/S, which is the computer that controls the test process. Also included in the FDF T/S group are an alphanumeric display computer terminal, commonly referred to as the video display terminal (VDT); power supplies; a power module junction box; a patch panel; and various other items of general purpose test equipment that are used to maintain IPF and ARF LRUs. LRU testing is accomplished by either one of two methods: one is to test certain LRUs manually while using some of the FDF T/S group power supplies and/or general purpose test equipment items in conjunction with other test sets; the other is accomplished by digital processor T/S execution of user-interactive test programs. The test programs are stored in erasable programmable read-only memory (EPROM) contained within the digital processor T/S.

The LRUs tested by the FDF T/S group are listed in table 1-2, along with the test method.

1.9.1.1 Computer-Controlled Testing

During computer-controlled testing, execution of the test programs causes the digital processor T/S to output digital signals that control the operational mode of the LRU under test. Additionally, the test programs generate VDT presentations that are transmitted over a bidirectional serial data link from the digital processor T/S to the VDT. The VDT presentations guide the user through selection and execution of LRU test procedures.

Selection of an LRU test procedure is effected by the user making the appropriate VDT keyboard entry as directed by the instructions and menu displayed on the VDT. After LRU test procedure selection, program-controlled VDT presentations describe the test to be performed, the necessary test interconnections, any required test equipment setups or measurements, and the test responses for an operational LRU.

Program execution is semi-automatic, in that program-prompted user interaction at the VDT keyboard is required to advance a test procedure program. Through user entries at the keyboard, a program can be made to repeat a test procedure, advance to the next step in the test procedure, or terminate the test procedure. Besides responding to user inputs at the VDT, the digital processor T/S automatically performs, via an IEEE standard-488 interface bus, setup and control of certain standard test equipment in the FDF T/S group. For example, the signal generator and function generator outputs are set to the values required by the test selected to be run on an LRU per test software and the LRUs test procedure.

1.9.1.2 Manual Testing of Units

Certain LRUs in the ARF and IPF subsystems are manually tested using the FDF T/S group power supplies and general test equipment. Test information for those LRUs is provided solely in the associated LRU maintenance manual. Typically, the FDF T/S group power supplies, power module junction box, and power cables are used to supply power to the UUT. Other signal and/or coaxial cables from the FDF T/S group cable kits may also be specified in the test setup for the UUT. Procedures for use of the FDF T/S group general test equipment for running manual tests are provided in the LRU maintenance manual for the UUT. In this instance, the FDF T/S group is being used as an ordinary test bench setup for test/troubleshooting of the UUT.

1.9.1.3 Equipment Rack

The equipment comprising the FDF T/S group is mounted in one relay rack and a three-bay electronics cabinet, as shown in figure 1-3. This equipment rack, the work table, drawers, and chair are part of the AMF. Refer to the AMF manual specified in appendix A for mechanical mounting details for the FDF T/S group equipment.

1.9.2 Spectrum Analyzer C2A1

Spectrum analyzer C2AI (HP 8560A) (see figure 1-3) is standard test equipment. The spectrum analyzer is equipped with the HP 909 rack-mounting kit for mounting in the electronics cabinet. The HP 909 option provides side-rails to facilitate moving the unit into and out of the cabinet.

The instrument is controlled by an internal microprocessor and is accessed by the digital processor T/S via its GPIB port For automated testing, the analyzer receives setup/control commands from the digital processor T/S via an HPIB port. For manual testing/setup, it can be operated using its on-screen menus and front-panel controls. The analyzer also has a screen-image print capability and passes print data to printer C3A3, via its HPIB port, when requested by the operator.

The spectrum analyzer permits signal spectra in the 50-Hz to 2.9-GHz frequency range to be displayed for operator analysis and measurement. The spectrum analyzer sweep frequency range (span) can be set to any value between 100 Hz and 2.9 GHz, or it can be set to 0 Hz (if the analyzer is to be used as a manually tuned receiver). However, it should be noted that the analyzer's calibration may not be valid for excessively large frequency spans.

Frequency tuning error is less than ±5 percent over the analyzer's frequency range. Spectral resolution bandwidths (-3 dB) are selectable from 10 Hz to 1 MHz in a 1, 3, 10 sequence; or a 2-MHz resolution bandwidth can be selected.

Input signal amplitude may be displayed either logarithmically or linearly. The analyzer has a 10 x 10 division display graticule. Calibrated logarithmic display range is 10, 5, 2, and 1 dB per division, while linear calibration is 10% of reference level per division.

The spectrum analyzer's input signal amplitude range is -120 to +30 dBm; however, an internal 70-dB step attenuator is provided to reduce use of an external attenuator. The analyzers input attenuator level is selectable in 10-dB steps. Amplitude measurement accuracy is l± dB over the analyzer's frequency range.

For further information on the spectrum analyzer, refer to its associated reference manuals listed in appendix A.

1.9.3 Network Analyzer C2A2

Network analyzer C2A2 (HP 8753C) (see figure 1-3) is standard test equipment. The network analyzer is equipped with an HP 913 rack-mount flange/front handle kit, which permits the unit to be rack mounted in the electronics cabinet. The network analyzer may be moved easily into or out of the electronics cabinet on side-rails fastened to the vertical mounting bars. Refer to the appropriate reference manuals listed in appendix A for further information.

The network analyzer is a radio frequency (RF) stimulus/response system that is used to measure magnitude and phase, insertion loss/gain, and RF path isolation characteristics of linear RF circuits contained in certain LRUs tested by the FDF T/S group. It can also perform attenuation, gain compression, s-parameter, electrical length, group delay, impedance, return loss, and linear phase deviation measurements. For automated testing, the network analyzer receives instrument setup/control commands from the digital processor T/S GPIB port output, via the analyzer's HPIB port. The analyzer also has a screen-image print capability and passes print data to printer C3A3 via its HPIB port when requested by the operator.

The instrument is controlled by an internal microprocessor and is accessed through its HPIB port by the digital processor T/S. For automated testing, the analyzer receives instrument setup/control commands from the digital processor T/S GPIB port output. For manual testing/setup, it can be operated using its on-screen menus and front-panel controls. During manual operation, the operator makes decisions concerning what operational/mode setup the instrument needs to make the desired measurement, and then selects the proper functions using a combination of front-panel buttons and the displayed menus.

On power-up, the network analyzer performs a series of self-calibration routines and self-test diagnostics, which are built into the instrument to aid in fault detection and maintenance. A group of self-calibration and maintenance tests can also be run during normal operation using on-screen service menus.

The network analyzer contains an internally leveled 300-kHz to 3-GHz swept synthesized signal source, having up to 100-mW output power that supplies an RF stimulus to the LRU under test. The source has 1-Hz frequency resolution and can be swept using linear, log, list, power, and CW sweep modes. Test measurements are accomplished by the network analyzer response section, which consists of three tuned 300-kHz to 3-GHz receivers, each having 100 dB of dynamic range. One receiver is used as a reference channel, while the other two receiver channels are used to measure LRU responses to the stimulus provided by the analyzer's signal source. The two receiver channel measurement responses can be simultaneously displayed in overlay or split-screen format on the front-panel color display.

The network analyzer is used with the 50-ohm transmission/reflection test set, the 50-ohm power splitter, and the minimum loss pad to perform a variety of RF transmission and reflection measurements on the LRUs under test. The transmission measurements include insertion loss or gain, insertion phase, and transmission coefficient. The reflection measurements include return loss, from which voltage standing wave ratio (VSWR) can be calculated, and reflection coefficient, from which impedance can be calculated or read from the included Smith chart overlay.

For further information on the network analyzer, refer to its associated reference manuals listed in appendix A.

1.9.4 Universal Counter C3A1

Universal counter C3A1 (HP 5335A) (see figure 1-3) is standard test equipment that is equipped with the HP 913 option, which includes flanges for rack mounting. The universal counter rests on side-rails that facilitate moving the instrument into or out of the electronics cabinet.

The universal counter performs frequency and time interval measurements, and it provides mean averaging, sample selection size, and standard deviation statistical functions, as well as offset, scale, and normalize math functions. It is a three-input channel unit, designated A, B, and C, with matched input amplifiers. The input channels have a ±5 V dc range to minimize use of input attenuators for most input signals, including transistor-transistor logic (TITL).. Channel A can count up to 200 MHz, channel B can count up to 100 MHz, and channel C (option 030) can count up to 1.3 GHz.

Besides measuring frequency, the frequency counter can perform time interval measurements with an accuracy exceeding 2 ns. The unit permits selection of either automatic or manual triggering with adjustable trigger levels that can be monitored on the front-panel display by pressing a front-panel switch. The unit is equipped with a high-stability crystal time base (option 010) to ensure measurement accuracy. For automated testing, the universal counter receives instrument setup/control commands from the digital processor T/S GPIB port output, via the counter's HPIB port. For manual testing/setup, it also can be operated manually using its front-panel controls.

On power-up, the counter performs a series of self-test diagnostics, which are built into the instrument to aid in fault detection and maintenance.

For further information on the universal counter, refer to its associated reference manuals listed in appendix A.

1.9.5 Oscilloscope C3A2

Oscilloscope C3A2 (TEK 2440) (see figure 1-3) is standard test equipment and is equipped with an OPT 1R to permit rack mounting. Side-rails permit the oscilloscope to be moved easily into and out of the electronics cabinet

The oscilloscope is a dual-channel storage instrument with a maximum digitizing rate of 500 Mega samples per second. It is capable of simultaneous acquisition of channel 1 and channel 2 input signals. It has a real-time useful storage bandwidth of 200 MHz for single-event acquisitions, with an equivalent-time bandwidth of 300 MHz for repetitive acquisitions.

The instrument is controlled by an internal microprocessor and is accessed by the digital processor T/S via its GPIB port. For automated testing, the oscilloscope receives instrument setup/control commands from the digital processor T/S GPIB port output. For manual testing/setup, it can be operated using its on-screen menus and front-panel controls. Alphanumeric readouts of the vertical and horizontal scale factors, trigger levels, trigger source, and cursor measurements are displayed at the top of the screen. Menus, which allow the user to select the operating mode, are displayed at the bottom of the screen.

During manual operation, the operator makes decisions concerning what operational/mode setup the instrument needs to make the desired measurement, and then selects the proper functions using a combination of front-panel buttons and the displayed menu.

The two vertical channels of the oscilloscope have calibrated deflection factors from 2 mV to 5 V per division in a 1-2-5 sequence of 14 steps. Use of coded probes having attenuation factors of 1X, 10X, 100X, and 1000X extends the minimum sensitivity to 5,000 V per division (with the 1000X probe) and the maximum sensitivity to 200 μV per division (using a 1X probe in SAVE or AVERAGE expanded mode). VOLTS/DIV readouts are automatically switched to display a correct scale factor when properly coded probes are attached. Each channel can be separately inverted. In SAVE mode, the waveforms

may be both horizontally and vertically repositioned, expanded horizontally and vertically, added to each other, or multiplied together for either XY or YT displays.

Horizontal display modes of A, A INTEN, and B delayed are available. The time base has 29 calibrated SEC/DIV settings in a 1-2-5 sequence from 2 ns per division to 5 seconds per division. An external clock mode is provided that accepts clocking signals from 1 to 100 MHz. The B trace and the intensified zone on the A INTEN trace may be delayed by time with respect to the A trigger, and a DELAY by EVENTS function permits the A display to be delayed by a selected number of B trigger events.

Certain trigger system features of the oscilloscope, such as SOURCE selection, trigger LEVEL control, trigger SLOPE, trigger MODE, and CPLG (coupling), include certain enhancements not normally found in a conventional oscilloscope. Refer to the associated manuals referenced in appendix A for more information on triggering.

Time and voltage cursors are provided for making parametric measurements on the displayed waveforms. Time may be measured either between the cursor positions (DELTA TIME) or between a selected cursor and the trigger point of an acquired waveform (ABSOLUTE). Time cursor readouts are scaled in seconds, degrees, or percentage values. The l/TIME cursors may be scaled in Hertz (Hz), degrees, or percentage.

Voltage cursor measurements on a waveform display can be selected to read either the voltage difference between the cursor positions or the absolute voltage position of a selected cursor with respect to ground. The volts measurement readouts may be scaled in units of volts, decibels (dB), or percent. The voltage cursors and the time cursors may also be coupled to track together (V@T and SLOPE) and assigned to a particular waveform for ease in making peak-to-peak and slope waveform measurements. The units for V@T may be volts, percent, or dB; SLOPE may have units of slope (VOLTS/SEC), percent (VOLTS/VOLT), or dB.

Waveforms may be acquired in NORMAL mode, AVG (averaging) mode, or ENVELOPE mode; the mode chosen depends on the measurement requirements. NORMAL mode continuously acquires and displays successive acquisitions producing a "live" waveform display similar to that seen with an analog oscilloscope. AVG (averaging) mode averages successive acquisitions of a waveform resulting in an improved signal-to-noise ratio of the displayed waveform. ENVELOPE mode saves the maximum and minimum data-point values over a selected number of acquisitions from 1 to 256, or continuously if the CONT (continuous) parameter is selected. The display presents a visual image of the amount of change (envelope) that occurs to a waveshape during the accumulated acquisitions. ENVELOPE mode allows frequency, phase, amplitude, and position changes to be easily identified.

Acquired waveforms can be saved in any of the nonvolatile REF waveform memories. Any or all of the stored reference waveforms can be displayed for comparison with the waveforms currently being acquired. The operator can designate the source and destination of waveforms to be stored by assigning either channel 1 or channel 2 (or the sum or product of the two channels) to any REF memory, or by moving a stored reference waveform from one REF memory to another. During automated testing, one or more reference waveforms may be written into a REF memory location in the oscilloscope by the digital processor T/S, via the GPIB.

The oscilloscope's memory erase (TEKSECURE) feature can be used to destroy current information that may be stored in nonvolatile memory. When an ERASE MEMORY operation is performed, either from the front-panel menu or via the GPIB, the following stored data is deleted: all waveforms saved in reference memories, all AutoStep sequences saved in sequencer memory, the current front-panel setup, and any waveforms saved on screen. The ERASE MEMORY feature also clears all remaining NVRAM memory except those locations storing calibration constants, calibration status/results, and data for the real-time clock.

An on-screen HELP function can be used to display operational information about any front-panel control. When HELP mode is in effect, manipulating almost any front-panel control causes the scope to display information about that control. When HELP is first invoked, an introduction to HELP is displayed on the screen.

The oscilloscope provides an AUTO SETUP function that can be used to automatically set the instrument for a viewable display based on input signal characteristics. The user can specify the particular waveform characteristic that the display is optimized for (front-edge, period, etc.) from a menu displayed when the AUTO SETUP function is executed.

A MEASURE function is provided that automatically extracts parameters from signal input to the scope. In the SNAPSHOT mode, 20 different waveform parameters are extracted and displayed for a single signal acquisition. In continuous extraction mode, up to four parameters are extracted continuously as the instrument continues to acquire signal data.

An AutoStep Sequencer (PRGM key) function allows the operator to save single front-panel setups or sequences of setups for later recall, along with associated flow control and input/output actions. From 100 to 800 front-panel setups (depending on complexity) can be stored in one or more sequences.

The oscilloscope has a screen-image print capability and passes print data to printer C3A3, via its GPIB port, when requested by the operator.

On power-up, the oscilloscope performs a series of self-calibration routines and self-test diagnostics, which are built into the instrument to aid in fault detection and maintenance.

For further information on the oscilloscope, refer to its associated reference manuals listed in appendix A.

1.9.6 Printer C3A3

Printer C3A3 (ThinkJet Printer HP 2225A) (see figure 1-3) is standard desktop-type computer peripheral equipment, and it is mounted on a tray that slides on side-rails fastened to vertical mounting bars in the electronics cabinet.

The printer receives data to be printed through its parallel Hewlett Packard interface bus (HPIB) port. The HPIB port is a listen-only IEEE-488 standard bus port that is connected to the general purpose interface bus (GPIB) port of the digital processor T/S and the HPIB/GPIB ports of the FDF T/S group standard test equipment. All the GPIB/HPIB ports adhere to the IEEE-488 bus standard. To allow transferring/formatting of data to the printer, the sending equipment must have a compatible print/plot driver, in the FDF T/S group, only network analyzer C2A2, oscilloscope C3A2, spectrum analyzer C2A1, and logic analyzer C4A3 have compatible print capabilities, typically implemented as a screen-print feature.

The printer is a quiet, desktop-type, commercial unit that generates crisp 150-cps text/graphics hard copy on ordinary 9.5" by 11.0" perforated-edge fanfold paper. The unit contains an easy-to-replace, disposable print cartridge.

For further information on the printer, refer to its associated reference manuals listed in appendix A.

1.9.7 Function Generator C4A1

Function generator C4A1 (Synthesizer Function Generator SG-1288/G Wavetek 288) (see figure 1-3) is standard test equipment that is equipped with a rack-mounting kit. The rack-mounting kit includes flanges and handles that permit the unit to be fastened to the vertical mounting bars in the electronics cabinet. The unit is equipped with side-rails that allow it to be moved out of or into the electronics cabinet.

The function generator, which has 16-digit resolution, produces precision sine, square, triangle, and ramp output waveforms; and dc. It also contains a wideband sweeper that can cover the instrument's full frequency range. For automated testing, the function generator receives setup/control commands from the digital processor T/S via an GPIB port. For manual testing/setup, it can be operated using its frontpanel controls.

On power-up, the function generator performs a series of self-test diagnostics, which are built into the instrument to aid in fault detection and maintenance.

The function generator can produce a synthesized sinewave output signal over the 20-Hz thru 20-MHz frequency range. The sinewave output can be modulated using an externally generated input AM or FM signal. Additionally, symmetrical and non-symmetrical square and triangle waveforms, as well as negative and positive-going ramps, can be produced. All produced waveforms may be dc or phase offset. The waveforms may be varied in output amplitude from 2-mV to 30 V p-p. Besides fixed-frequency waveform production, the function generator can be used as a wideband phase continuous sweep generator that covers up to the full frequency range.

For further information on the function generator, refer to its associated reference manuals listed in appendix A.

1.9.8 Signal Generator C4A2

Signal generator C4A2 (HP 8657B) (see figure 1-3) is standard test equipment. The signal generator is equipped with an HP 909 rack-mount flange/front handle kit, which permits the unit to be rack mounted in the electronics cabinet. The signal generator may be moved easily into or out of the electronics cabinet on side-rails fastened to the vertical mounting bars.

The signal generator is a programmable synthesized signal generator that provides modulated or unmodulated sinewave output signals with frequencies from 100 kHz to 2060 MHz, at power levels between -143.5 and +13 dBm. The frequency resolution is 1 Hz and power level resolution is 0.1 dB; absolute power level accuracy is better than ±1.5 dB.

Modulation may be generated either internally or externally. Internally generated amplitude modulation (AM) and frequency modulation (FM) rates are 400 Hz and 1 kHz. Externally generated AM rates are 20 Hz to 100 kHz; externally generated FM rates are 5 Hz to 100 kHz. Modulation modes may be simultaneous or mixed (AM-AM, FM-FM, or AM-FM) and may be derived from either internal or external sources.

For automated testing, the signal generator receives setup/control commands from the digital processor T/S via an HPIB port. The output frequency, power level, and modulation characteristics are fully programmable and are controlled by digital processor T/S execution of the FDF T/S group software, as required, for the LRU under test. Besides computer control of signal generator output parameters, manual control of the output parameters may be effected through operator use of the front-panel controls. For manual testing/setup, it can be operated independently, using its front-panel controls.

On power-up, the signal generator performs a series of self-test diagnostics, which are built into the instrument to aid in fault detection and maintenance.

For further information on the signal generator, refer to its associated reference manuals listed in appendix A.

1.9.9 Logic Analyzer C4A3

Logic analyzer C4A3 (HP 1650B) (see figure 1-3) is standard test equipment and is rack-mounted in the electronics cabinet using a (Tektronix part number) 5061-6175 rack-mount kit. The logic analyzer is equipped with side-rails to facilitate moving the instrument into and out of the cabinet.

The 80-channel logic analyzer permits observation of digital data within a serial data stream or a parallel data bus. Either an internal clock or an external clock may be used to observe a particular signal configuration at the time of a selected event occurrence. The logic analyzer can be used for a variety of tests on LRUs. For example, operation of the digital processor T/S serial input/output (L/O) signals can be verified by using the logic analyzer. In addition to FDF T/S group cables, a 16-channel lead set and termination adapter are provided for connecting the analyzer to the UUT.

The logic analyzer is controlled by an internal microprocessor, and it includes a front-panel-accessible 3.5" diskette drive, which is used to load the instrument's operating system on power-up. During automated testing, the analyzer is accessed, via the analyzer's HPIB port, by the digital processor T/S to initiate testing. Logic analyzer test setup and measurement characteristics are fully programmable, and test setup files are loaded from the analyzer's diskette drive, prior to test initiation, per instructions contained in the FDF T/S group software for the LRU under test

For manual testing/setup, the logic analyzer can be operated using its on-screen menus and front-panel controls. The analyzer also has a screen-image print capability and passes print data to printer C3A3, via its HPIB port, when requested by the operator.

On power-up, the analyzer performs a series of self-test diagnostics, which are built into the instrument to aid in fault detection and maintenance.

For further information on the logic analyzer, refer to its associated reference manuals listed in appendix A.

1.9.10 Video Display Terminal (VDT) C4A4

VDT C4A4 (Computer Terminal HP 700/96 C1064W) (see figure 1-3) is tray-mounted on the work surface shelf underneath the electronics cabinet. The VDT is equipped with a detachable, full American Standard Code for Information Interchange (ASCII) keyboard. The soft white phosphor display screen has a capacity of up to 80 lines and 132 columns; 24 lines x 80 columns (1,920 characters) are used in the FDF T/S group application. The VDT has an internal memory capacity of 8 pages. An RS-232-C serial printer port is provided, but it is not used in the FDF T/S group.

The screen displays user-interactive LRU test menus, instructions, and commands resulting from FDF T/S group software execution by the digital processor T/S. The operator responds to the LRU test menus, instructions, and commands by initiating keyboard inputs as directed by the display and/or dictated by the test results.

Communication between the VDT and the digital processor T/S is provided via an RS-232-C serial input/output (SIO) port operating in full duplex at a transmission rate of 4,800 baud.

For further information on the VDT, refer to its associated reference manuals listed in appendix A.

1.9.11 Digital Multimeter C5A1

Digital multimeter C5Al (Fluke 8840A/AF) (see figure 1-3) is standard test equipment. Since the basic size of the instrument is 3.5 x 8.5 x 14.4 inches, the equipment is supplied with the Y8834 offset rack mounting kit The Y8834 kit permits the digital multimeter (DMM) to be rack mounted. The DMM is also equipped with handles and may be moved easily into or out of the equipment rack on side-rails fastened to the vertical mounting bars.

The DMM is a precision, full-function digital multimeter with dc volts, true rms ac volts, resistance, dc current, and true rms ac voltage/current measurement capabilities. It can perform up to 100 measurements per second, is fully programmable, and offers 3.5to 5.5-digit resolution.

The DMM measures dc voltage from 200 mV full scale with 1-μV resolution up to 1000 V with 10-mV resolution. It measures ac voltage from 200 mV full scale with 1-μV resolution up to 700 V with 10-mV resolution. It also performs dc ratio measurements. Current measurement ranges of 2000 mA full scale with 10-μA resolution are provided for de and true rms ac. Resistance measurements can be selected with a maximum range of 20 megohm with 100-ohm resolution down to a 200-ohm range with 1.0-mohm sensitivity.

On power-up, the DMM performs a series of self-test diagnostics, which are built into the instrument to aid in fault detection and maintenance. The self-tests can also be performed during normal operation by pressing the SRQ button on the unit front panel for 3 seconds (minimum).

For automated testing, the DMM receives setup/control commands from the digital processor T/S via a GPIB port. The measurement setup characteristics are fully programmable and are controlled by digital processor T/S execution of the FDF T/S group software, as required for the LRU under test. For manual testing/setup, it can be operated independently, using its front-panel controls.

For further information on the DMM, refer to its associated reference manuals listed in appendix A.

1.9.12 Patch Panel C5A2

Patch panel C5A2 (Trompeter Electronics JS-24WD3SF7/BJ28) (see figure 1-3) contains 24 BNC feed through connectors that facilitate access to rear-panel-mounted connectors on FDF T/S group equipment. The patch panel is bolted to the vertical mounting bars in the equipment rack. No slides are provided for the patch panel.

The panel-mounted BNC connectors provide easy access to /VO signals that are routed to/from rear-panel-mounted connectors on the test equipment included in the FDF T/S group. The patch panel BNC connectors service rear-panel /VO signals on the network analyzer, the function generator, the universal counter, the signal generator, and the spectrum analyzer.

1.9.13 ARF Intercept Receiver Pallet C5A3

ARF intercept receiver pallet C5A3 (10-182950-1) (see figure 1-3) provides a test fixture for fault verification testing of defective WJ-8604 receivers that have been replaced during ARF subsystem testing/troubleshooting. The receiver pallet, which contains no active circuit devices, includes a mechanical mounting tray and power/control/RF signal interconnections for eight receivers, and it is the same equipment item (part number) used to mount and interface the intercept receivers into the ARF subsystem equipment racks. The receiver pallet sits on a shelf that slides on side-rails fastened to vertical mounting bars in the equipment rack and is secured to the shelf by a lower front thumbscrew. The receiver to be tested is installed in slot-3 of the pallet

The pallet provides a complete set of connectors for power/control/RF cable interconnects. FDF T/S group testing uses only the connectors associated with slot-3 of the pallet. In the FDF T/S group, cables are provided to connect the multi-pin power connector (J24) to junction box C5A6, the multi-pin control connector (J21) to the digital processor T/S serial I/O port output connector (J3), and the BNC audio output connector (J22) to standard test equipment. In addition, BNC cables are provided to interconnect standard test equipment to the receiver's RF input connector (RF IN-3 J3), and to the receiver's spectrum display unit output connector (SDU OUT-3 J8).

1.9.14 Digital Processor T/S C5A4

Digital processor T/S C5A4 (TS-4204/TSQ-105(V)) (see figure 1-3) is housed in a metal enclosure that sits in a mounting tray on a shelf which slides on side-rails fastened to vertical mounting bars in the equipment rack. The digital processor T/S is secured to the shelf by a lower front thumbscrew.

The digital processor T/S contains 10 replaceable circuit card assemblies (CCAs). Table 1-4 lists the digital processor T/S equipment supplied. Access to the CCAs is achieved by removing 18 screws that secure a top cover plate to the digital processor T/S.

Table 1-4. Digital Processor T/S C5A4 Equipment List

Reference designator	Official nomenclature/ Part number	Common name
C5A4	Digital Processor Test Set TS-4204/TSQ-105(V) 10-166609-1	Digital processor T/S
C5A4A1	68000 Common CCA 10-166581-1	Common CCA
C5A4A2	68000 Processor CCA 10-166579-1	Processor CCA
C5A4A6	SCAR Interface CCA 10-166332-1	SCAR interface CCA
C5A4A7	Serial Input/Output Interface CCA 10-166578-7	SIO interface CCA
C5A4A8	Data Link Interface CCA 10-166333-4	DLI interface CCA
C5A4A10	Parallel Input/Output Interface CCA 10-166331-1	PIO interface CCA
C5A4A11	General Purpose Interface Bus Interface CCA 10-166587-1	GPIB interface CCA
C5A4A15	256K Erasable Programmable Read-Only Memory CCA 10-154851-3	EPROM CCA
C5A4A16	256K Erasable Programmable Read-Only Memory CCA 10-154851-2	EPROM CCA
C5A4A17	256K Erasable Programmable Read-Only Memory CCA 10-154851-1	EPROM CCA
C5A4A29	Processor Backplane 10-156755-1	Backplane

Table 1-4. Digital Processor C5A4 T/S Equipment List - Continued

Reference designator	Official nomenclature/ Part number	Common name
C5A4A30	Bus Terminator 10-165507-1	Bus term
C5A4B1	Centrifugal Blower 42-902001-013	Blower
C5A4S1	Thermostatic Switch 42-905001-008	Overtemp switch

The digital processor T/S front panel contains 3 TNC connectors, 11 MS27508-type multi-pin or multi-socket connectors, and 1 electromagnetic interference (EMI) filter that is built onto an MS27508-type connector (J15). DC power is applied to the EMI filter via a cable from junction box C5A6. One of the MS27508-type multi-socket connectors (J11) connects the IEEE-488 interface bus from the digital processor T/S to the signal generator and the function generator. Another MS27508-type multi-pin connector (J1) provides the interface connections between the digital processor T/S and the VDT. One MS27508-type 8-pin connector (J14) carries 115 V ac to a rear-panel-mounted centrifugal blower that cools the circuits inside the digital processor T/S. The remaining MS27508-type multi-pin and multi-socket connectors are dedicated for test connections to various LRUs. The three TNC connectors are not used.

The digital processor T/S serves as the FDF T/S group computer, which executes the test program software included with the FDF T/S group. The test programs are stored in EPROM and are loaded automatically into random access memory (RAM) upon power-up of the digital processor T/S. As the digital processor T/S executes the test programs, digital outputs are produced that control the operational mode of the LRU under test.

Additionally, the digital processor T/S uses a GPIB (IEEE Standard-488) port to pass test equipment setup and control commands to the HPIB/GPIB-equipped standard test equipment in the FDF T/S group. For example, the GPIB port is used to adjust the outputs from the FDF T/S group signal generator and function generator to the values required by specific tests on certain LRUs. No HPIB/GPIB port print capability is provided to printer C3A3 by the digital processor T/S, because the digital processor software does not include a print/plot driver routine.

LRU responses to test inputs are, in some cases, analyzed by the digital processor T/S. In other cases, the operator monitors the test responses using FDF T/S group equipment and causes the digital processor T/S to advance or repeat test program execution by making the appropriate entry at the VDT keyboard.

1.9.15 Junction Box CSA6

Junction box C5A6 (Power Module Junction Box 10-162550-1) (see figure 1-3) is a metal enclosure that has 15 connectors (J1 thru J15) mounted on the front panel and 9 connectors (J16 thru J19, J21 thru J25) mounted on the rear panel. The connectors mounted on the rear panel are all MS3102-type multi-pin connectors; they receive the dc voltage

outputs from FDF T/S group power supplies C5A9 and C5A10. The junction box is bolted directly to the equipment rack, and it has no slides.

DC voltages are routed to six terminal boards and a power module (PS 1) inside the junction box. The power module is a dc-to-dc converter that is located in the left rear comer when viewing the junction box from the rear. Access to the power module is gained by removing the screws that secure the cover to the junction box.

The power module dc-to-dc converter output and the six terminal boards are wired to the 15 front-panel-mounted connectors. Eight of the front-panel-mounted connectors are MS27508-type multi-pin or multi-socket connectors; the remaining seven connectors are MS3470-type multi-socket connectors. Either front-panel-mounted connector J3 or J4 is used to supply dc power to the digital processor T/S. The remaining front-panel-mounted connectors are dedicated to supply dc power to certain LRUs tested by the FDF T/S group.

1.9.16 Power Supplies C5A9 and C5A10

Power supplies C5A9 and C5A10 (Lambda 25669) (see figure 1-3) are standard equipment and are identical. The following descriptive information applies to both power supply units.

The power supply is housed in a metal enclosure that has front handles and side flanges to facilitate sliding the power supply into and out of the equipment rack. The unit has 19" rack adapters that are bolted to the vertical mounting bars of the equipment rack. The power supply front panel contains controls and an indicator for measuring the output voltages and currents, and for adjusting the output voltages. One power supply rear-panel connector (J1) accepts 115 Vac for primary power. Three other rear-panel connectors (J2 thru J4) are used to output the developed dc voltages and sensing lines that are supplied to junction box C5A6.

The power supply contains four power modules (designated PSI thru PS4) and associated internal wiring and components. Only the PS 1 thru PS3 modules are connected to internal wiring. The PS4 (28 V dc) module is connected to its associated internal wiring/components in only one of the power supply units; hence, the 28-V dc module in the other unit is not used. All dc power outputs of the unit are current-limited and voltage-regulated.

Power module PSI generates ±5 V dc voltage outputs, while PS2 and PS3 each generate ±15 V dc outputs. The power supply output voltage and current values can be monitored on a front-panel-mounted digital meter. The digital meter displays either the voltage value or the current value that is output from one of the internal power modules and sensed at the junction box. Display of voltage or current is accomplished by appropriately positioning a two-position front-panel slide switch in conjunction with a four-position front-panel rotary switch. The slide switch selects voltage or current to be displayed; the rotary switch selects the output from one of the three power modules.

Each power module output voltage may be set by adjusting one of three front-panel-mounted potentiometers. The output voltages from the power supply are routed to junction box C5A6 for ultimate distribution to the digital processor T/S and/or an LRU under test.

For further information on the power supplies, refer to its associated reference manuals listed in appendix A.

1.9.17 VDTISTE - PAM Switch Box

The VDT/STE - PAM switch box supports use of VDT C4A4 with digital processor T/S C5A4 for FDF T/S group operations. It also allows the VDT to be used for ARF digital processor EPROM load operations using the low-band PAM (programmable adapter module) (C6A3), referred to as the STE - PAM, and its associated PROM programmer (C6A2).

1.9.18 Frequency Doubler

The frequency doubler (HP 11721A) was originally designed as an accessory for the HP 8662A synthesized signal generator and other signal generators that have outputs in the same frequency range. In the FDF T/S group, for example, the frequency doubler can be used with signal generator C4A2 (HP 8657B) or function generator C4A1 (Wavetek 288). The frequency doubler is a free-standing unit that is not mounted into an equipment rack. It is used as an in-line device within test setup cabling.

The frequency doubler uses a balanced full wave rectifier to double 50- to 1300-MHz input signals. The full wave rectifier generates a high amplitude second harmonic of the input while suppressing the fundamental signal at the output.

Conversion loss and spurious signals in the doubler's output are dependent upon the characteristics of the input signal. The frequency doubler is designed to work with signal generators that have a third harmonic suppression level of less than or equal to -50 dBm, and a minimum drive level of +13 dBm +1 dB.

The frequency doubler's output level is not a linear function of its input level. Changes in RF amplitude that constitute amplitude modulation at the doubler input are not exactly reproduced at the output. As a result, amplitude modulation is generally degraded except at very low depths (less than 20% may result in less than 3% AM distortion). Frequency modulation, while not distorted, will be changed by the frequency doubler, in that the peak deviation of the output signal will be double that of the input signal.

For further information on the frequency doubler, refer to its associated reference manuals listed in appendix A.

1.9.19 Transmission/Reflection Test Set

The transmission/reflection test set (HP 85044A/B) is a free-standing unit that is not mounted into an equipment rack. It contains a power splitter and a directional bridge that permit simultaneous transmission and reflection measurements to be made using the network analyzer. The transmission/reflection test set also incorporates a 0- to 70-dB, 10-dB/step attenuator that permits the incident signal level to be reduced without affecting the signal level at the reference input to the network analyzer. The transmission/reflection test set is used to make RF measurements on RF Processor CP-1606/ARW-83(V), Radio Receiver R-2270/ARW-83(V), Radio Receiver R-2289/ARW-83(V), and Radio Receiver WJ-8604.

For further information on the transmission/reflection test set, refer to its associated reference manuals listed in appendix A.

1.9.20 Power Splitter

The power splitter (HP 11850A) is a free-standing unit that is not mounted into an equipment rack. It contains one input port and three output ports. One output port provides the reference output, while the other two ports can be used for independent transmission measurements. The power splitter is used with the network analyzer to perform RF measurements on some of the LRUs in the ARF and IPF subsystems.

1.9.21 Minimum Loss Pad

The minimum loss pad (HP 11852B) is a free-standing equipment item that is not mounted into an equipment rack. It provides low-loss 50- to 75-ohm impedance transformation in RF test setups using the network analyzer or other RF test equipment, as required.

1.9.22 Precision RF Cable Set

The precision RF cable set (HP 11851 B) consists of three 24-inch cables and one 34-inch cable. The 24-inch cables are phase matched to ± degrees; the 34-inch cable is for use with the

transmission/reflection test set. The precision RF cable set is required for accurate phase and gain/loss measurements on LRUs under test.

1.9.23 N-type Accessory Kits
The accessory kits provide a set of precision adapters for N-type coaxial cable connectors used in RF test setups using the network analyzer or other RF test equipment, as required. One kit (HP 11853A) provides adapters for 50-ohm N-type connectors, while the other kit (HP 11855A) provides those required for 75-ohm N-type connectors.

1.9.24 ARF Maintenance Kit
The ARF maintenance kit (21-178363-1) contains a set of tools, adapters, and other items required for general maintenance using the FDF T/S group.

1.9.25 Ac/Dc Power Cable Kit
The ac/dc power cable kit (21-164447-1) contains cables that provide ac power to power supplies C5A9 and C5A10, and other cables that connect the dc voltage outputs from the power supplies to the junction box input connectors. Still other cables provide dc power from various junction box connectors to the input power connectors of the various LRUs tested by the FDF T/S group.

1.9.26 Coaxial Cables
The coaxial cables (09-188941-1 thru -7) connect rear-panel outputs from the function generator, the network analyzer, the signal generator, the spectrum analyzer, and the universal counter to rear patch panel feed through connectors. Thus, ease of access to rear-panel connectors on the general purpose test equipment is provided at the front of the patch panel.

1.9.27 Test Signals Cable Kit
The test signals cable kit (21-164448-1) contains cables that provide 110-V ac power for the blowers in the digital processor T/S and in Digital Processor CP-1795/ARW-83(V). The other cables in the kit transfer test data and control signals from various digital processor T/S connectors to the various LRUs under test. Additionally, responses from some of the LRUs tested by the FDF T/S group are returned over some of the cables for analysis by the digital processor T/S.

1.9.28 FDF T/S Group Equipment Interconnecting Cables
Cables used for FDF T/S group interconnections are supplied as part of the AMF, and hence are not listed or described in this manual. However, a cable interconnect diagram is provided in this manual as figure FO-1. For cable part numbers and other detailed information, refer to the AMF manual listed in appendix A.

1.10 EQUIPMENT DATA

This paragraph provides technical equipment data for FDF T/S group assemblies that are not covered by individual equipment manuals. For information on standard equipment/test equipment items, refer to the associated equipment manuals listed in appendix A. The standard/test equipment items include spectrum analyzer C2A1, network analyzer C2A2, universal counter C3A1, oscilloscope C3A2, printer C3A3, VDT C4A4, logic analyzer C4A3, signal generator C4A2, function generator C4A1, DMM C5A 1, power supplies C5A9 and C5 10, and standalone (non-mounted) items (see table 1-3). For information on the equipment rack and electronics cabinet in which the FDF T/S group equipment items are installed, refer to the technical manual associated with the AMF, which is listed in appendix A.

1.10.1 Patch Panel C5A2
The physical and electrical characteristics and the environmental limitations of patch panel C5A2 are as follows:

PHYSICAL CHARACTERISTICS

Height .....3.50 in (8.89 cm)
Width .....19.00 in (48.26 cm)
Depth .....3.00 in (7.62 cm)
Weight .....8.00 lb (3.64 kg)

ELECTRICAL CHARACTERISTICS

Connectors .....50-ohm BNC-to-BNC bulkhead feed through

ENVIRONMENTAL LIMITATIONS

Temperature:
Operating.....-55 to 100 °C
Nonoperating .....-65 to 125 °C

Humidity .....10 to 90%, non-condensing

1.10.2 ARF Intercept Receiver Pallet C5A3

The physical and electrical characteristics and the environmental limitations of ARF intercept receiver pallet C5A3 are as follows:

PHYSICAL CHARACTERISTICS

Height .....8.75 in (22.23 cm)
Width .....19.00 in (48.26 cm)
Depth .....27.00 in (68.58 cm)
Weight .....15.00 lb (6.82 kg)

ELECTRICAL CHARACTERISTICS

Connectors .....50-ohm BNC-to-BNC bulkhead feed through, multi-pin power and signal

ENVIRONMENTAL LIMITATIONS

Altitude:
Operating .....30,000 ft (9,150 m), maximum
Nonoperating .....53,792 ft (16,400 m), maximum

Temperature:
Operating .....-55 to 100 °C
Nonoperating .....-65 to 125 °C

Humidity .....10 to 95%, non-condensing

1.10.3 Digital Processor T/S C5A4

The physical and electrical characteristics and the environmental limitations of digital processor T/S C5A4 are as follows:

PHYSICAL CHARACTERISTICS

Height	7.88 in (20 cm)
Width	10.25 in (26.03 cm)
Depth	27.00 in (68.58 cm)
Weight	35.00 lb (15.90 kg)

ELECTRICAL CHARACTERISTICS

Input Power Requirements:	
DC voltage/Current	+5 V dc/20 A, +15 V de/1.5 A, -15 V dc/1.5 A, all dc voltages ±5%
Consumption	350 W (nominal)
Blower voltage	11 5 V ac (+5%, -10%), 48 to 440 Hz
Digital Signals:	
Input and output	EIA RS-422, twisted shielded pairs
Basic clock rate	65 kb/s
Logic type	TTL
TTL Levels:	
High (TTL 1)	+2.4 to +5.5 V dc
Low (TTL 0)	0.0 to +0.4 V dc
Internal Common Bus Levels:	
Input logic levels:	
TTL logic low	0.8 V dc, maximum
TTL logic high	2.0 V dc, minimum
Output logic levels:	
TTL logic low	0.4 V dc, maximum
TTL logic high	2.4 V de, minimum
Bus receivers:	
Logic low	0.8 V de, maximum; 200 mA, maximum, at 0 V dc
Logic high	1.7 V de, minimum; 100 mA, maximum, at 2.5 V dc
Ac loading	10 pF, maximum

Bus drivers:
- Logic low .....0.8 V dc, maximum, at 48 mA
- Logic high .....80 mA, maximum, at 3.5 V de
- Ac loading .....10 pF, maximum
- Unit load .....One bus receiver and two bus drivers and <10pF of CCA etch

All bus lines are open collector, resistor-terminated to 3.4 V dc, nominal.

ENVIRONMENTAL LIMITATIONS

Altitude:
- Operating .....30,000 ft (9,150 m), maximum
- Nonoperating .....53,792 ft (16,400 m), maximum

Temperature:
- Operating .....-0 to 43 °C
- Nonoperating .....-20 to 70 °C

Humidity .....10 to 95%, non-condensing

1.10.4 Junction Box C5A6

The physical and electrical characteristics and the environmental limitations of junction box C5A6 are as follows:

PHYSICAL CHARACTERISTICS

Height .....8.70 in (22.10 cm)
Width .....19.00 in (48.26 cm)
Depth .....10.00 in (25.40 cm)
Weight .....25.00 lb (11.36 kg)

ELECTRICAL CHARACTERISTICS

Input Requirements:
- Voltage .....24 to 30 V de (power module) 5, ±12, 15, +28 V dc (junction box)

Current .....1.4 A, full load; 0.9 A, half load
Regulation, line .....0.1% or 10 mV, whichever is greater

Output Requirements:
- Voltage .....+36 V dc (±35 mV), maximum, continuously adjustable between 18 and 50 V de (power module); ±5, ±12, ±15, +28, +36 V dc (junction box)

Regulation, load .....0.1% or 20 mV, whichever is greater

Impedance	DC to 1 kHz, 0.004 x load resistance or 0.04 ohm, maximum; 1 to 10 kHz, 0.015 x load resistance or 0.15 ohm, maximum; 10 to 100 kHz, 0.03 x load resistance or 0.5 ohm, maximum
Overload protection	Automatic protection against output overload or short circuit; output voltage automatically restores to normal when overload is removed.

ENVIRONMENTAL LIMITATIONS

Temperature:	
Operating	-55 to 100 °C
Nonoperating	-65 to 125 °C
Humidity	10 to 90%, non-condensing

SECTION III. TECHNICAL PRINCIPLES OF OPERATION

This section provides functional descriptions of the FDF T/S group equipment.

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1.11 GENERAL

The following paragraphs describe conventions used in this manual and the technical descriptions of the FDF T/S group.

1.11.1 Nomenclature

To simplify the name structure in the following technical descriptions, common names have been assigned to each assembly and subassembly of the FDF T/S group. Refer to tables 1-3 and 1-4 for cross-references between common names and official names.

1.11.2 Digital Signal Names

Where possible, a signal name describes the function performed by the signal. Where an acronym is used in a signal name, refer to the glossary in the back of this manual for its definition.

1.11.3 Component and Pin Identifications

To simplify identification of items in description text and maintenance instructions, the reference designators are used with the reference designator of the largest subassembly/component presented first.
The following are examples of item identification:

- A1, A2, A3 (etc.) used by itself refers to a major subassembly.
- A1A2 refers to subordinate subassembly A2 of major subassembly A1.
- A1A2U2 refers to integrated circuit U2 of subordinate subassembly A2 of subassembly A1.
- A3P2 refers to plug P2 of subassembly A3.
- A3P2-5 refers to pin 5 of plug P2 of subassembly A3.

1.12 FDF T/S GROUP FUNCTIONAL DESCRIPTION

Figure FO-3 shows a functional diagram of the FDF T/S group. The FDF T/S group consists of 10 major standard test equipment units, several minor standalone standard test equipment units, a patch panel, two power supplies, a power supply junction box, an ARF intercept receiver pallet test fixture, and a digital processor T/S with included software (user code). The following paragraphs provide a functional block diagram description of the FDF T/S group. For additional functional information on the equipment described, refer to the appropriate reference manuals listed in appendix A.

1.12.1 Spectrum Analyzer C2A1

Spectrum analyzer C2A1 (figure FO-3, sheet 3) permits signal spectra in the 50-Hz to 2.9-GHz frequency range for an LRU under test to be displayed for operator analysis and evaluation. It is controlled by an internal microprocessor and is accessed by the digital processor T/S via its GPIB port. For automated testing, the analyzer receives setup/control commands from the digital processor T/S via an HPIB port. For manual testing/setup, the analyzer can be operated using its on-screen menus and front-panel controls.

The spectrum analyzer also has a screen-image print capability and passes print data to printer C3A3, via its HPIB port, when requested by the operator.

1.12.2 Network Analyzer C2A2

Network analyzer C2A2 (figure FO-3, sheet 3) is an RF stimulus/response system that is used to measure magnitude and phase, insertion loss/gain, and RF path isolation characteristics of linear RF circuits contained in certain LRUs tested by the FDF T/S group. For automated testing, the network analyzer receives instrument setup/control commands from the digital processor T/S GPIB port output, via the analyzer's HPIB port. The analyzer also has a screen-image print capability and passes print data to printer C3A3, via its HPIB port, when requested by the operator.

The instrument is controlled by an internal microprocessor and is accessed through its HPIB port by the digital processor T/S. For automated testing, the analyzer receives instrument setup/control commands from the digital processor T/S GPIB port output. For manual testing/setup, it can be operated using its on-screen menus and front-panel controls. During manual operation, the operator makes decisions concerning what operational/mode setup the instrument needs to make the desired measurement, and then selects the proper functions using a combination of front-panel buttons and the displayed menu.

To perform insertion loss and phase measurements on some LRUs under test, the network analyzer is used with certain standalone standard test equipment items (i.e., the 50-ohm transmission/reflection test set, the 50-ohm power splitter, and the minimum loss pad).

1.12.3 Universal Counter C3A1

Universal counter C3A1 (figure FO-3, sheet 3) performs frequency and time interval measurements on LRUs under test. During automated testing, the universal counter receives instrument setup/control commands from the digital processor T/S GPIB port output, via the counter's HPIB port. For manual testing/setup, it also can be operated manually using its front-panel controls.

1.12.4 Oscilloscope C3A2

Oscilloscope C3A2 (figure FO-3, sheet 3) is used to measure various signal characteristics on LRUs under test. The instrument is controlled by an internal microprocessor and is accessed by the digital processor T/S via its GPIB port.

For automated testing, the oscilloscope receives instrument setup/control commands from the digital processor T/S GPIB port output. For manual testing/setup, it can be operated using its on-screen menus and front-panel controls. During manual operation, the operator makes decisions concerning what operational/mode setup the instrument needs to make

the desired measurement, and then selects the proper functions using a combination of front-panel buttons and the displayed menu.

The oscilloscope has a screen-image print capability and passes print data to printer C3A3, via its GPIB port, when requested by the operator.

1.12.5 Printer C3A3
Printer C3A3 (figure FO-3, sheet 3) receives data to be printed through its parallel HPIB port. The HPIB port is connected to the GPIB port of the digital processor T/S and the HPIB ports of the FDF T/S group standard test equipment. To allow transferring/formatting of data to the printer, the sending equipment must have a compatible print/plot driver, in the FDF T/S group, only network analyzer C2A2, oscilloscope C3A2, spectrum analyzer C2A1, and logic analyzer C4A3 have compatible print capabilities, typically implemented as a screen-print feature.

The printer is a quiet, desktop-type, commercial unit that generates crisp 150-cps text/graphics hard copy on ordinary 9.5" by 11.0" perforated-edge fanfold paper. The unit contains an easy-to-replace, disposable print cartridge.

1.12.6 Function Generator C4A1
Function generator C4A1 (figure FO-3, sheet 3) produces precision sine, square, triangle, and ramp output waveforms that are input to LRUs under test. For automated testing, it receives setup/control commands from the digital processor T/S via a GPIB port. For manual testing/setup, it can be operated using its front-panel controls.

1.12.7 Signal Generator C4A2
Signal generator C4A2 (figure FO-3, sheet 3) is a programmable synthesized signal generator that provides modulated or unmodulated sinewave output signals to LRUs under test.

For automated testing, the signal generator receives setup/control commands from the digital processor T/S via an HPIB port. The output frequency, power level, and modulation characteristics are fully programmable and are controlled by digital processor T/S execution of the FDF T/S group software. The signal generator also can be controlled manually using the front-panel controls.

1.12.8 Logic Analyzer C4A3
Logic analyzer C4A3 (figure FO-3, sheet 3) permits observation of digital data within a serial data stream or a parallel data bus for an LRU under test. A 16-channel lead set and termination adapter are provided for connecting the analyzer to the UUT.

The logic analyzer is controlled by an internal microprocessor and includes a front-panel-accessible 3.5" diskette drive, which is used to load the instrument's operating system on power-up. During automated testing, the analyzer is accessed, via the analyzer's HPIB port, by the digital processor T/S to initiate testing. Logic analyzer test setup and measurement characteristics are fully programmable, and test setup files are loaded from the analyzer's diskette drive, prior to test initiation, per instructions contained in the FDF T/S group software for the LRU under test.

For manual testing/setup, the logic analyzer can be operated using its on-screen menus and front-panel controls. The analyzer also has a screen-image print capability and passes print data to printer C3A3, via its HPIB port, when requested by the operator.

1.12.9 Video Display Terminal C4A4
Video display terminal (VDT) C4A4 (figure FO-3, sheet 1) is equipped with a detachable, full ASCII keyboard. The soft white phosphor display screen has a capacity of up to 80 lines and 132 columns; 24 lines x 80 columns (1,920 characters) are used in the FDF T/S group application. The VDT has an internal memory capacity of 8 pages.

The screen displays user-interactive LRU test menus, instructions, and commands resulting from FDF T/S group software execution by the digital processor T/S. The operator responds to the LRU test menus, instructions, and commands by initiating keyboard inputs as directed by the display and/or dictated by the test results.

Communication between the VDT and the digital processor T/S is provided via RS-232-C asynchronous communications interface adapter (ACIA) ports on common CCA C5A4A1. The VDT operates in full duplex mode at a transmission rate of 4800 baud. An RS-232-C serial printer port is also provided in the VDT, but it is not used in the FDF T/S group.

1.12.10 Digital Multimeter C5A1

Digital multimeter (DMM) C5A1 (figure FO-3, sheet 3) is a precision, full-function digital multimeter with dc volts, true rms ac volts, resistance, dc current, and true rms ac voltage/current measurement capabilities. During automated testing, the DMM receives setup/control commands from the digital processor T/S via a GPIB port. The measurement setup characteristics are fully programmable and are controlled by digital processor T/S execution of the FDF T/S group software, as required for the LRU under test. For manual testing/setup, the DMM can be operated independently using its front-panel controls.

1.12.11 Patch Panel C5A2

Patch panel C5A2 (figure FO-3, sheet 3) contains 24 BNC feed through connectors that facilitate access to rear-panel-mounted connectors on FDF T/S group equipment. The patch panel BNC connectors service rear-panel I/O signals on the network analyzer, the function generator, the universal counter, the signal generator, and the spectrum analyzer.

1.12.12 ARF Intercept Receiver Pallet C5A3

ARF intercept receiver pallet C5A3 (figure FO-3, sheet 2) provides a test fixture for fault verification testing of defective WJ-8604 receivers that have been replaced during ARF subsystem testing/troubleshooting. It includes a mechanical mounting tray and power/control/RF signal interconnections for eight receivers and is the same equipment item (part number) used to mount and interface the intercept receivers into the ARF subsystem equipment racks. The receiver pallet contains no active circuit devices. The receiver to be tested is installed in slot-3 of the pallet.

The pallet provides a complete set of connectors for power/control/RF cable interconnects. FDF T/S group testing uses only the connectors associated with slot-3 of the pallet. In the FDF T/S group, cables are provided to connect the multi-pin power connector (J24) to junction box C5A6 (J7), the multi-pin control connector (J21) to the digital processor T/S channel A serial I/O port output connector (J3), and the BNC audio output connector (J22) to standard test equipment. In addition, BNC cables are provided to interconnect standard test equipment to the receivers RF input connector (RF IN-3 J3), to the receiver's second IF output (21.4-MHz J11), and to the receiver's spectrum display unit output connector (SDU OUT-3 J8).

1.12.13 Digital Processor T/S C5A4

Digital processor T/S C5A4 (figure FO-3, sheets 1 and 2) contains a microcomputer and various /VO and interface CCAs. The microcomputer consists of common CCA C5A4A1, processor CCA C5A4A2, and EPROM CCAs C5A4A15 thru C5A4A17. EPROM CCAs C5A4A15 thru C5A4A17 contain the user code (software) and VDT displays for the various LRU test procedures.

The user code is executed by an MC68000L8 microprocessor (68000 central processing unit (CPU)) located on processor CCA C5A4A2. Processor CCA C5A4A2 also contains 64 kbytes of local RAM. Common CCA C5A4Al contains 64 kbytes of common RAM, bus timing and control circuits, an interrupt generator, clock circuits, a programmable timer, and ACIAs.

The interface and VO interface CCAs consist of GPIB interface CCA C5A4A1 , PIO interface CCA C5A4A 10, DLI CCA C5A4A8, SIO interface CCA C5A4A7, and SCAR interface CCA C5A4A6. These CCAs provide either communication paths between the digital processor TIS and the LRUs under test or a control path that permits setup and control of the standard test equipment in the FDF T/S group.

1.12.13.1 Digital Processor TIS Common Bus

The digital processor T/S common bus (figure FO-3, sheet 1) interfaces the 16 data lines and 23 address lines of the microprocessor (68000 CPU) on processor CCA C5A4A2 to the other CCAs in the digital processor T/S. Additionally, the common bus includes control timing, and interrupt signal lines that perform various functions. The digital processor T/S common bus signals are described in table 1-5.

1.12.13.2 Digital Processor T/S Interrupt Structure

Digital processor T/S interrupt structure is shown in figure 1-4. Interrupts are requests from peripheral devices (such as SIO interface CCA C5A4A7 and SCAR interface CCA C5A4A6 or common CCA C5A4A 1) that cause the microprocessor on processor CCA C5A4A2 to temporarily suspend current program execution and service the requesting CCA. A CCA can interrupt the microprocessor only when interrupts are enabled. The microprocessor can service interrupts only when the interrupt priority level is enabled. Priority levels for all interface and /UO interface CCAs in the digital processor T/S are a function of the priority level interrupt assigned to a CCA and digital processor T/S backplane wiring. In a group of CCAs assigned the same interrupt priority level, priority is highest for the CCAs electrically closest on the common bus to processor CCA C5A4A2.

1.12.13.2.1 Interrupt Enable Bit

Each interface or I/O interface CCA has an interrupt logic circuit that includes a control status register. The control status register contains an interrupt enable bit that must be set before an interrupt can be requested by that CCA. The interrupt enable bit for each CCA is set during the digital processor T/S initialization routine.

1.12.13.2.2 Interrupt Vector

A different interrupt vector (address pointer in hex code) is assigned to each CCA and hard-coded into the interface/control logic for that CCA. The interrupt vector for a CCA is transmitted to processor CCA C5A4A2 during the interrupt acknowledge sequence, thereby allowing automatic entry into the interrupt service routine for that CCA. The interrupt vector is an 8-bit word containing a hexadecimal number that is multiplied by 4 in the microprocessor. The resultant product vector is the address entry point to the interrupt service routine for that CCA.

1.12.13.2.3 Typical Interrupt Request Cycle

When SIO interface CCA C5A4A7 or SCAR interface CCA CSA4A6 contains data to be passed to processor CCA C5A4A2, then SIO interface C5A4A7 or SCAR interface CCA C5A4A6 requests interrupt service by asserting the BIRQL signal. Although processor CCA C5A4A2 receives the BIRQL signal, the interrupt request cannot be acknowledged until execution of the current instruction is completed. Processor CCA C5A4A2 can acknowledge interrupt requests only between instruction execution cycles.

When execution of the current instruction is completed, processor CCA C5A4A2 responds to the interrupt request by asserting the appropriate interrupt acknowledge (IACKxxL) signal. The active interrupt acknowledge signal is applied to the BIAKIL input of the CCA closest to processor CCA C5A4A2 on the common bus. If the first CCA did not request the interrupt, the interrupt acknowledge signal is passed from the BIAKOL output of the first CCA to the BIAKIL input of the next CCA that has the same interrupt priority level on the common bus. The process of passing the interrupt acknowledge signal through the daisy-chain of CCAs continues until the CCA requesting the interrupt receives the interrupt acknowledge signal. The interrupt acknowledge signal is not passed beyond the CCA requesting the interrupt.

Table 1-5. Digital Processor T/S C5A4 Common Bus Signals

Signal name	Description
BDALO thru BDAL15	Data/address lines 0 thru 15 carry data and addresses when microprocessor is executing a data read or write operation. Address information is asserted first and then data is asserted on BDALO thru BDAL15 lines. Addresses are output from processor CCA C5A4A2, while data may be either input to or output from processor CCA C5A4A2.
BDAL16 thru BDAL22	Extended address lines for addressing SIO interface CCA C5A4A7 and SCAR interface CCA C5A4A6.
BBS7L	Bus bank select 7 line is asserted when microprocessor address bits A13 thru A23 are active, indicating extended addressing is in progress. Bits A13 thru A23 are decoded on processor CCA C5A4A2, and resultant BBS7L signal is routed to interface and 1/O interface CCAs in digital processor T/S. Therefore, interface and /0O interface CCAs need to decode only 16 lower address bits BDALO thru BDAL15, even though extended addressing is in progress.
BRPLYL	Bus reply line indicates that SIO interface CCA C5A4A7, SCAR interface CCA C5A4A6, or an EPROM CCA (C5A4A15, C5A4A16, or C5A4A17) acknowledges receipt of data or interrupt.
BHALTL	Bus halt line, when asserted, causes all microprocessor execution to stop and all external interrupts to be ignored.
BINITL	Bus initialize line resets microprocessor and all CCAs on common bus. BINITL is generated by common CCA C5A4A1 in response to a power-up or reset condition or when the microprocessor executes a RESET instruction. Application of BIN1TL and BHALTL together for 100 milliseconds, minimum, constitutes a complete digital processor T/S reset.
BDMRL	Common bus request for a direct memory access (DMA) operation.
BSACKL	Acknowledge signal driven true to denote common bus ownership.
BDMGIL	Common bus grant in for DMA operation.
BDMGOL	Common bus grant out for DMA operation.
BBUSREQL	Bus request line asserted when one of a number of processor CCAs desires control of common bus. (Not implemented in digital processor T/S, since only one processor CCA is included.)
BBUSGRANTL	Bus grant line that permits one of a number of processor CCAs to gain control of common bus. (Not implemented in digital processor T/S, since only one processor CCA is included.)

Table 1-5. Digital Processor T/S C5A4 Common Bus Signals - Continued

Signal name	Description
BSYNCL	Bus synchronize line indicates that valid address is on BDAL0 thru BDAL22 lines.
BDINL	Bus data in line indicates a microprocessor read cycle is in progress.
BDOUTL	Bus data out line indicates a microprocessor write cycle is in progress.
BWTBTL	Bus write byte line used to differentiate between word or byte operation.
IRQ6L	Interrupt request, priority level 6 line is the highest priority interrupt request that is maskable by the microprocessor.
IRQSL	Interrupt request, priority level 5.
IRQ4L	Interrupt request, priority level 4.
IRQ3L	Interrupt request, priority level 3.
IRQ2L	Interrupt request, priority level 2.
IRQIL	Interrupt request, priority level 1.
IACK07L	Interrupt acknowledge for nonmaskable interrupt.
IACK06L	Interrupt acknowledge for interrupt priority level 6.
IACK05L	Interrupt acknowledge for interrupt priority level 5.
IACK04L	Interrupt acknowledge for interrupt priority level 4.
IACK03L	Interrupt acknowledge for interrupt priority level 3.
IACK02L	Interrupt acknowledge for interrupt priority level 2.
IACK01L	Interrupt acknowledge for interrupt priority level 1.
CPUCLKL	Microprocessor clock (7.8972 MHz for 8-MHz microprocessor).

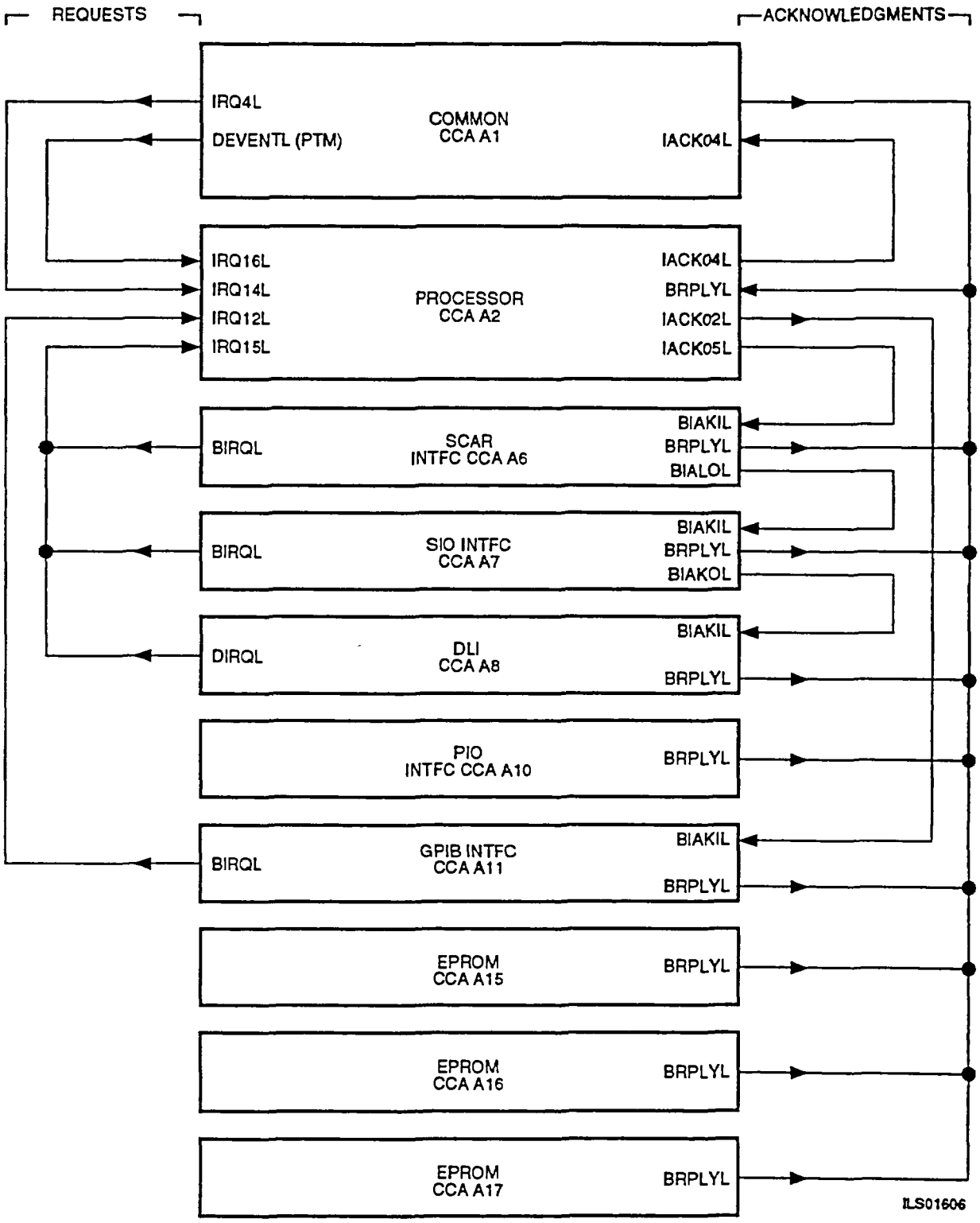

Figure 1-4. Digital Processor T/S C5A4 Interrupt Structure

The CCA requesting the interrupt responds to the interrupt acknowledge signal by asserting BRPLYL. Once BRPLYL is asserted, processor CCA C5A4A2 asserts the BDINL signal to read the interrupt vector placed on the common bus by the CCA requesting the interrupt. When the interrupt vector is placed on the common bus, the CCA requesting the interrupt responds to the BDINL signal by again asserting BRPLYL. When processor CCA C5A4A2 receives and processes the interrupt vector, automatic entry into the interrupt service routine is effected for the CCA requesting the interrupt.

Note

A CCA must assert BRPLYL in response to BDINL or BDOUTL within 16 microseconds, or the microprocessor on processor CCA C5A4A2 enters the halt state. The halt state indicates that a bus error has occurred.

Note

In the following paragraph, reference is made to the user and supervisor operating states of the microprocessor and to S-records. Refer to the Motorola 68000 microprocessor vendor literature for a description of the user and supervisor operating states and S-records.

1.12.13.3 Software

The FDF T/S group software consists of an operating system and two sets of user codes. The operating system executes in the microprocessor supervisor state and has access to all resources of the microprocessor. The operating system services devices within the digital processor T/S and controls task scheduling.

The two sets of user codes include one set that is fetched from the EPROM CCAs and converted from hexadecimal format into S-record format. S-record format is defined by Motorola, Inc., to be used for downloading machine code to the 68000 microprocessor. The S-record format conversion of the hexadecimal user code is cross-loaded from the digital processor T/S to an LRU under test. The LRU under test converts the S-record code back into hexadecimal format and then executes the code to perform the required LRU tests, as described later in this section. The other set of user codes is dedicated for execution only by the digital processor T/S in the microprocessor user state and is downloaded from the EPROM CCAs into local and common RAM during initialization, as described later in this section.

The digital processor T/S executable user code controls digital processor T/S testing of certain LRUs and enables the digital processor T/S to automatically sense and evaluate responses from those LRUs. For other LRUs, the digital processor T/S executable user code controls the operation of the LRU under test, but the operator must manually adjust test equipment and take measurement readings to verify correct LRU performance.

The results of the operator measurements are entered at the keyboard in response to VDT-displayed prompts. The operator measurement results are entered as either pass (P)/fail (F) or yes (Y)/no (N). The FDF T/S group software analyzes the operator test results entries to logically isolate an LRU fault. For testing of all LRUs, at least some operator intervention is required in the form of software-prompted keyboard inputs at the VDT. The operator VDT keyboard inputs may consist of test program selection, termination, and branching, as well as responses regarding operator interpretation of LRU test measurements as directed by VDT displays.

Besides VDT keyboard entries, the operator must accomplish the manual connections between the LRU under test and the FDF T/S group equipment. Additionally, during testing of some LRUs, the operator must use the FDF T/S group test equipment manually to perform certain required LRU performance or troubleshooting measurements not incorporated into

the user code. The following paragraphs functionally describe only the software-controlled operation of the FDF T/S group hardware.

1.12.13.4 Initialization

Initialization of the FDF T/S group consists of powering up all of the included standard test equipment, performing the operational readiness procedures on the standard test equipment as outlined in chapter 2 of this manual, and powering up the digital processor T/S.

During the digital processor T/S initialization process, several important events occur the generation of signals required to initialize the digital processor T/S hardware, resetting the MC68000L8 microprocessor, and executing an initialization routine stored on the EPROM CCAs. The following subparagraphs describe the major events in the digital processor T/S initialization process.

1.12.13.4.1 Initialization of Interface CCAs

When the digital processor T/S is powered up, the power-on reset circuit and the timing and control circuit on common CCA C5A4Al generate bus halt (BHALTL) and bus initialize (BINITL) signals for 100 milliseconds, minimum. The BHALTL and BINITL signals are routed over the common bus to processor CCA C5A4A2. Additionally, the BINITL signal is routed via the common bus to all of the CCAs in the digital processor T/S, except EPROM CCAs C5A4A15 thru C5A4A17. The BINITL signal clears, resets, or presets the internal logic located on SCAR interface CCA C5A4A6, SIO interface CCA C5A4A7, DLI CCA C5A4A8, PIO interface CCA C5A4A10, and GPIB interface CCA C5A4A 11 in the digital processor T/S.

1.12.13.4.2 Resetting Processor CCA C5A4A2

Applying the BHALT and BINITL signals to processor CCA C5A4A2 for 100 milliseconds, minimum, resets the MC68000L8 microprocessor. When reset occurs, the microprocessor address lines are set to zero to access the data in memory location zero, but the digital processor T/S hardware is configured at power-up time to inhibit data from being read out of memory location zero. Instead, data is read by the power-on vector programmable read-only memory (PROM) located on processor CCA C5A4A2.

1.12.13.4.3 Enabling Power-On Vector PROM

The microprocessor two least significant address lines (set to zero) are applied to the low order address inputs of the power-on vector PROM. The other three high order address inputs to the power-on vector PROM are connected to digital processor T/S switch lines 0 thru 3 (SWO thru SW3) which are hard wired to address a particular memory location in the power-on vector PROM.

The power-on vector PROM is enabled for a read operation by a low Q-output from a D-latch on processor CCA C5A4A2. The D-latch Q output is produced when the BHALT signal is applied to the D-latch clear input. Thus, instead of accessing RAM location zero, the MC68000L8 accesses a different memory location that depends on the hard-wired logical states of lines SWO thru SW3.

The accessed memory location in the enabled power-on vector PROM contains a 16-bit word that is read by the microprocessor. The 16-bit word vectors the microprocessor to a jump table that is stored in memory on an EPROM CCA. The jump table contains a branch command that causes the microprocessor to access the entry point of the initialization routine stored on the EPROM CCAs.

1.12.13.5 Initialization Routine Execution

Upon entering the initialization routine, the microprocessor first fetches two double words (32 bits each) that are loaded into the microprocessor supervisor stack pointer and the program counter (PC). The PC contents point to the next instruction to be fetched from the initialization routine. The following subparagraphs describe the initialization of the digital processor T/S software and hardware.

1.12.13.5.1 Software Initialization

After setting up the microprocessor registers, the initialization routine downloads the operating system stored on EPROM CCAs C5A4A15 thru C5A4A17 into the local RAM on processor CCA C5A4A2. After downloading the operating system, the initialization routine downloads the user code containing the test routines for the LRUs. The user code is downloaded from EPROM CCAs C5A4A15 thru C5A4A17 into local and common RAM. However, the VDT menus, directional displays, and fault diagnosis displays associated with the test procedures for the LRUs are not downloaded but are left in EPROM CCAs C5A4A15 thru C5A4A17. The VDT menus and displays are fetched from the EPROM CCAs by the microprocessor as directed by the user code; i.e., the user code, when executed, directs the microprocessor to fetch from EPROM CCAs C5A4A15 thru C5A4A17 the menu or display required for VDT presentation by the current test routine.

1.12.13.5.2 Hardware Initialization

The initialization routine resets the ACIAs on common CCA C5A4A1 and sets the control registers of the ACIAs for the desired digital processor T/S operational characteristics. The programmable timer module (PTM) on common CCA C5A4A1 is set by the microprocessor under initialization routine control. The PTM contains three clock generator channels. Two of the three PTM channels are set to generate clock signals used by the ACIAs to transfer data at the desired baud rate (4800) between the digital processor T/S and the VDT or the ARF digital processor under test.

Additionally, the initialization routine sets the third PTM channel to generate a real-time clock providing a timer interrupt rate that is determined by the operating system. The real-time clock is used by the operating system to time various tasks. Upon termination of the initialization routine, the microprocessor PC points to the user code entry address for the digital processor self-test procedure. The user code causes the first display to be fetched from EPROM and transmitted via the common bus to the ACIAs on common CCA C5A4A1, and then to the VDT. The first display instructs the user to press key L on the VDT keyboard to proceed with the digital processor T/S self-test routine.

1.12.13.6 Digital Processor T/S Self-Test Routine

When the VDT keyboard L key is pressed, the microprocessor begins to execute the digital processor T/S self-test routine. The display TEST SET SELF TEST IN PROGRESS is fetched from an EPROM CCA and passed via the common bus and common CCA C5A4A1 ACIAs to the VDT for display.

The various CCAs in the digital processor T/S are tested by the microprocessor exercising user code, transferring data via the common bus to the input of the CCA under test and then fetching test response data via the common bus from the CCA under test. The response data is analyzed by the microprocessor, under control of the user code, for correct CCA operation with the exception of PIO interface CCA C5A4A10 and GPIB interface CCA C5A4A11.

The digital processor T/S self-test routine first tests the processor CCA C5A4A2 microprocessor instruction set and the local RAM. Then, the common RAM on common CCA C5A4A1 is tested, and each of the EPROM CCAs is tested. After EPROM CCAs C5A4A15 thru C5A4A17 are tested, the I/O and interface CCAs are tested in the following order: SCAR interface CCA C5A4A6, SIO interface CCA C5A4A7, and DLI CCA C5A4A8. Finally, PIO interface CCA C5A4A10 and GPIB interface CCA C5A4A11 are provided with test stimuli. Proper operation of PIO interface CCA C5A4A10 is verified by the user visually observing the logic analyzer display.

Proper operation of GPIB interface CCA C5A4A 11 and the associated IEEE-488 interface bus is verified by the user visually observing the signal generator and function generator output frequencies and power levels on the associated front-panel seven-segment displays. A more comprehensive description of the tests performed by the digital processor T/S self-test routine is presented in chapter 4 of this manual.

1.12.13.7 IEEE-488 Interface Bus

The IEEE-488 interface bus connects the digital processor T/S via GPIB interface CCA C5A4A11 to the standard test equipment in the FDF T/S group. The test equipment are controlled by data and address information that is imbedded in the user code for certain LRU test routines.

The data and address information are passed by the 68000 microprocessor over the common bus to GPIB interface CCA C5A4A11 using an interrupt driven I/O technique. The interrupt driven /VO technique is explained later in this section under the description of DLI CCA C5A4A8, since DLI CCA C5A4A8 permits bidirectional data transfers, while only unidirectional data transfers are performed by GPIB interface CCA C5A4A11.

GPIB interface CCA C5A4A11 controls the IEEE-488 interface bus and talks to the standard test equipment. The test equipment are listeners, only, on the IEEE-488 interface bus. Thus, the data and address information are unidirectional and transferred only towards the test equipment tied to the IEEE-488 interface bus. Some of the eight bus management signals associated with the IEEE-488 interface bus are returned by the test equipment and are monitored by GPIB interface CCA C5A4A11 to verify valid data transfers.

Inside GPIB interface CCA C5A4A11, the general purpose interface adapter (GPIA) performs regular or DMA data transfers over the IEEE-488 bus to (or from, as applicable) the external equipment. Microprocessor data access to the GPIA is provided by the common data buffers via the common bus. The processor controls operation of the CCA through DMA control, address control, and GPIA control functions, which receive common bus control inputs from the processor via the common data buffers.

1.12.13.8 Operator-to-FDF-T/S-Group Interface

The operator-to-FDF-T/S-group interface is a RS-232-C serial interface in the VDT, an interconnecting cable, and ACIAs located on common CCA C5A4A1 in the digital processor T/S. The operator-to-FDF-T/S-group interface permits bidirectional communications between the VDT and the digital processor T/S. In one direction, operator VDT keyboard inputs are transmitted to the digital processor T/S. In the other direction, VDT menus and displays are passed from the digital processor T/S to the VDT for presentation.

1.12.13.8.1 Transmitting Display Data to the VDT

Calls within the user code for the test routine currently under execution cause the microprocessor to fetch the desired VDT display or menu, one byte at a time, from EPROM CCAs C5A4A15 thru C5A4A17. The fetched menu byte is transmitted via the common bus to an ACIA on common CCA C5A4A 1. The ACIA, previously set up for operation during system initialization, transmits the menu or display byte to the VDT at the PTM clock rate of 4800 baud.

1.12.13.8.2 ACIA Functions Monitored During Data Transfers

Each ACIA on common CCA C5A4A1 contains, among other functions, a receive data register, a transmit data register, and a status register. The receive data register is filled with one byte of data whenever a transmission is received from the VDT. The transmit data register is filled with one byte of data whenever the microprocessor transfers one byte of a VDT display from the EPROM CCAs.

The status register contains eight bits. Of the eight bits, two are important to the transfer of data between the VDT and the digital processor T/S. The two bits are the receive data register full (RDRF) and the transmit data register empty (TDRE) bits. When data is received from the VDT, the RDRF status register bit is set high by the ACIA. After the data is read by the microprocessor, the RDRF bit is set low by the ACIA. When data is written from an EPROM CCA into the transmit data register, the TDRE bit is set low by the ACIA.

Internal ACIA functions convert the parallel data byte into serial format for transmission to the VDT. After the data is transmitted to the VDT, the TDRE bit is set high by the ACIA. Since a VDT display is being transmitted one byte at a time,

a subroutine in the user code must continually check the state of the TDRE bit in the ACIA status register. When the TDRE bit goes high, the subroutine transfers another byte of VDT display data from an EPROM CCA to the ACIA. The process continues, byte by byte, until all of the data required for the current VDT screen display is transmitted.

1.12.13.8.3 Transmission of VDT Response to a Displayed Prompt
Operator inputs at the VDT keyboard in response to a displayed prompt are transmitted one byte at a time in the following manner. The user code expects a response to a previously transmitted display prompt Since the user code expects a VDT response, the ACIA status register contents are periodically polled by a user code subroutine. When the user responds to the prompt, eight bits of serial data are transmitted to the ACIA of common CCA C5A4A1. Internal ACIA functions convert the serial data into an 8-bit parallel format byte that is loaded into the ACIA receive data register. When the subroutine senses a high RDRF status register bit, the user code transfers the VDT data byte from the ACIA receive data register into local memory in the digital processor T/S. The microprocessor, under user code control, evaluates the data received from the VDT.

1.12.13.9 Digital Processor T/S Interfaces to LRUs Under Test
Digital processor T/S interfaces to LRUs under test are accomplished through common CCA C5A4A1, PIO interface CCA C5A4A10, DLI CCA C5A4A8, SIO interface CCA CSA4A7, and SCAR interface CCA C5A4A6. Table 1-6 summarizes the digital processor T/S test interfaces.

1.12.13.9.1 Common CCA C5A4A1 Interface
The common CCA C5A4A 1 interface provides an RS-232-C serial link that is used for cross-loading user code test routines which check out the individual CCAs in the ARF digital processor (referred to as the ADPU in the FDF T/S group test menu). For each CCA test, 42 blocks of user code are fetched from EPROM CCAs C5A4A15 thru C5A4A17 by the digital processor T/S microprocessor and are cross-loaded into RAM in the ARF digital processor under test. A microprocessor in the ARF digital processor executes the user code to check out the individual CCAs in the LRU under test. The results of each CCA test are transmitted back to the digital processor T/S via the same RS-232-C serial link used for cross-loading the user code test routines.

1.12.13.9.1.1 Cross-loading User Code to ARF Digital Processor
The user code is cross-loaded in much the same manner as the VDT displays are fetched from EPROM CCAs C5A4A15 thru C5A4A17 and transmitted to the VDT. However, the user code fetched must first be converted from hexadecimal format into S-record format by the microprocessor. The microprocessor typically fetches several bytes (but sometimes less) of user code from an EPROM CCA and converts the code into S-record format. The S-record format code is transferred via the common bus into the common CCA C5A4A 1 ACIA transmit data register.

Internal ACIA functions convert the parallel data bytes into serial format for transmission, one at a time, to the ARF digital processor under test. Meanwhile, a subroutine in the user code continually checks the state of the TDRE bit in the ACIA status register. When the TDRE bit goes high, indicating that the byte transfer to the ARF digital processor is completed, several bytes of user code are fetched from EPROM, converted to S-record format, and loaded one byte at a time into the ACIA transmit data register. The process is continued until 42 blocks of data are cross-loaded into RAM of the ARF digital processor under test. One of the microprocessors in the ARF digital processor under test must first convert the S-record user code into hexadecimal format before execution.

1.12.13.9.1.2 Receiving CCA Test Response from ARF Digital Processor
Test responses from the LRU under test are returned as hexadecimal data rather than in S-format records. Since the digital processor T/S executable user code knows that a 42-block CCA test routine is already cross-loaded into the ARF digital processor under test, the user code expects a test response.

Table 1-6. Digital Processor T/S C5A4 to LRU Under Test Interface Descriptions

Digital processor T/S connector	LRU under test	Interface description
J1	ARF DPU	Serial communications interface between ACIAs on common CCA C5A4Al in digital processor T/S and the common CCA in LRU under test. Communications interface is used to crossload 42 blocks of test data for each individual CCA in LRU under test. CCA test results are returned to digital processor T/S via serial communications interface.
J2	SCAR processor level 0	Serial transfer of SCAR data, command, clock, and load signals at 1-MHz baud rate from output buffers on SCAR interface CCA C5A4A6 in digital processor T/S to LRU under test. One data byte is sent to command LRU under test to take measurements. Test results consist of 20 16-bit (two 8-bit bytes) words returned serially at 1-MHz baud rate from LRU under test to input buffers on SCAR interface CCA C5A4A6 in digital processor T/S.
J3	SCAR processor level 2	Serial transfer of SCAR data, command, clock, and load signals 1-MHz baud rate from output buffers on SCAR interface CCA C5A4A6 in digital processor T/S to LRU under test. One data byte is sent to command LRU under test to take measurements. Test results consist of 64 16-bit (two 8-bit bytes) words returned serially at 1-MHz baud rate from LRU under test to input buffers on SCAR interface CCA C5A4A6 in digital processor T/S. Test results include 44 measurement words plus 20 histogram words.
J3	SCAR processor level 1	Serial transfer of SCAR data, command, clock, and load signals at 1-MHz baud rate via output channel B on SIO interface CCA C5A4A7 in digital processor T/S to LRU under test. In operational mode, one 8-bit byte is transmitted to set up source, and a second 8-bit byte is transmitted to command LRU to take measurements. In maintenance mode, seven 8-bit bytes are transmitted to set up BITE test parameters. Test results consist of 64 16-bit words (two 8-bit bytes) returned serially at 1-MHz baud rate to input channel C on SIO interface CCA C5A4A7 in digital processor T/S. Test results include 34 measurements and 30 unassigned words.
J3	WJ-8604 receiver, R-2270 receiver, R-2289 receiver, and RF processor	A 56-bit serial control word transmitted at 125-kHz baud rate from channel A output of SIO interface CCA C5A4A7 in digital processor T/S.

Table 1-6. Digital Processor T/S C5A4 to LRU Under Test Interface Descriptions - Continued

Digital processor T/S connector	LRU under test	Interface description
J3	ARF DPU	Serial echo test data output from channel B of SIO interface CCA C5A4A7 in digital processor T/S to the DLI CCA, the SCAR interface CCA, and the SIO interface CCA in ARF digital processor (DPU) LRU under test. Serial echo test data is returned from LRU under test to channel C input of SIO interface CCA C5A4A7 in digital processor T/S.
J9	ARF DPU	Serial operational BITE test data and clocks for operational BITE and DLI-1 CCA test outputs from transmitter on DLI CCA C5A4A8 in digital processor T/S. Test results are returned via receiver on DLI CCA C5A4A8 in digital processor T/S.
J11	(Connected to standard test equipment)	IEEE-488 interface bus to control standard test equipment.
J18	ARF DPU	Parallel output from PIO interface CCA C5A4A 10 in digital processor T/S consists of one reset line and nine bootup vector lines for initializing 68000 processors in LRU test.

Therefore, a user code subroutine uses a built-in time delay to periodically poll the ACIA RDRF status register bit. When the ARF digital processor transmits the first 8-bit serial data response to the CCA test, internal ACIA functions convert the serial data into an 8-bit parallel byte. The byte is loaded into the receive data register, and the ACIA RDRF status register bit is set high. When the user code subroutine senses the high RDRF bit, the hexadecimal data byte is fetched by the microprocessor from the receive data register and stored in digital processor T/S RAM.

The process continues until the entire test response is stored into digital processor T/S RAM or a polling timeout occurs. The digital processor T/S microprocessor, operating-under control of the digital processor T/S executable user code, evaluates the test response and transmits the evaluation to the VDT for display and user interpretation.

1.12.13.9.2 PIO Interface CCA C5A4A 10 Interface

PIO interface CCA C5A4A10 provides parallel output data via a cable connected to digital processor T/S front-panel connector J18 for ARF digital processor or antenna control unit testing.

When the ARF digital processor (ADPU) or antenna control unit test procedure is selected from the FDF T/S group main menu, the digital processor T/S microprocessor addresses PIO interface CCA C5A4A10. Once addressed, PIO interface CCA C5A4A10 is enabled to accept a 16-bit parallel word that the microprocessor fetches from memory and transfers via the common bus. Although the parallel word contains 16 bits, only 10 bits have logical significance.

The parallel word is applied through the common data buffers to the channel A first-in first-out (FIFO) memory. The parallel data output from the channel A FIFO memory is latched in the channel A output registers. The latched 16-bit parallel word is applied through the channel A output drivers to digital processor T/S front-panel connector J18 and is routed over an interconnecting cable to the ARF digital processor or antenna control unit under test, as applicable.

During ARF digital processor testing, one of the 10 parallel output bits having logical significance resets the ARF digital processor under test, while the remaining nine output bits initialize the microprocessors inside the ARF digital processor.

1.12.13.9.3 DLI CCA C5A4A8 Interface

DLI CCA C5A4A8 provides an RS-422 bidirectional serial interface via a cable connected to digital processor T/S front-panel connector J9 for ARF digital processor testing. At the ARF digital processor end, the interconnecting cable connects to a DLI CCA in the LRU under test to establish the RS-422 interface.

The RS-422 interface is used when the operational BITE test is selected to be run on the LRU under test. First, the LRU under test is initialized via the RS-422 interface by the digital processor T/S. Then, the digital processor T/S uses the RS-422 interface to request that the LRU under test execute the resident operational BITE test. When operational BITE test execution is completed, the results are transferred via the RS-422 interface from the LRU under test to the digital processor T/S for subsequent display on the VDT. The following subparagraphs describe the overall transfer of data and test results between the digital processor T/S and the LRU under test.

1.12.13.9.3.1 Data Transmission from Digital Processor T/S

Data is normally exchanged between the digital processor T/S and the LRU under test in 10-byte blocks, although all 10 bytes are not always used within a given block. For the operational BITE test, two blocks of data are transmitted from the digital processor T/S to initialize the ARF digital processor under test. An additional data block is transmitted to request execution of the operational BITE test resident in the ARF digital processor under test. The data blocks are transmitted at a baud rate of 998.4 kHz (1 MHz, nominal) which is derived from the DLI CCA C5A4A8 internal clock.

1.12.13.9.3.2 Setting Up DLI CCA C5A4A8 for Data Transmission
Basically, DLI CCA C5A4A8 is set up for data transmission to, or reception from, an LRU under test by an interrupt driven I/O technique incorporated into the operating system.

DLI CCA C5A4A8 registers and logic functions are set up for transmission of the digital processor T/S data by a DLI output driver initiator software module contained in the user code. A driver initiator is included in the user code for each digital processor T/S interface that uses the interrupt driven I/O technique. The DLI output driver initiator is executed by the microprocessor and takes charge of passing data to DLI CCA C5A4A8 for the transmission.

The DLI output driver initiator loads the number of words to be transmitted into the DLI CCA C5A4A8 transmitter address register. The transmitter address register is the lower seven bits in the 128- by 16-bit word data buffer in the transmitter shift register and data buffer function. The number of words to be transmitted (i.e., three blocks of 10 words each, or 30 words) is placed on the common bus by the microprocessor to the common data buffers on DLI CCA C5A4A8.

The 7-bit representation for the 30 words to be transmitted is passed through the device select control data registers function to the transmitter shift register and data buffer function. The seven bits are stored at the bottom of the 128- by 16-bit data buffer.

1.12.13.9.3.3 Transmitting the Three Data Blocks
The DLI output driver initiator manages the loading of the three blocks of data into the DLI CCA C5A4A8 transmitter shift register and data buffer function. The three blocks of data are converted from parallel to serial format by the shift register in the transmitter shift register and data buffer function.

The serial data is simultaneously applied to the sync word detector and cyclic redundancy check (CRC) generator/checker function and the memory timing and control interface function. The CRC bits and sync word are appended to the serial data bits by the memory timing and control function.

The transmission (TX) send output from the memory timing and control function is applied through the transmitter output buffer to digital processor T/S connector J9. The J9 connector output is carried over an interconnecting cable to a DLI CCA receiver in the ARF digital processor under test.

1.12.13.9.3.4 Data Reception by Digital Processor T/S
After transmitting the ARF digital processor initialization and request for operational BITE execution, the digital processor T/S user code expects a test response from the ARF digital processor under test. The test response is contained in four blocks of data. To be able to receive the response, the digital processor T/S must configure DLI CCA C5A4A8 for data reception.

1.12.13.9.3.5 Setting Up DLI CCA C5A4A8 for Data Reception
Once again, as in data transmission, the DLI input driver initiator must set up the DLI CCA C5A4A8 registers and logic functions for data reception. The receiver address register is the lower seven bits in the 128- by 16-bit word data buffer in the receiver shift register and data buffer function. The number of words to be received (i.e., four blocks of 10 words each, or 40 words) is placed on the common bus to the common data buffers on DLI CCA C5A4A8 by the microprocessor executing the DLI input driver initiator module. The 7-bit representation for the 40 words to be transmitted is passed through the device select control data registers function to the receiver shift register and data buffer function. The seven bits are stored at the bottom of the 128- by 16-bit data buffer.

1.12.13.9.3.6 Receiving the Test Response
The four blocks of test response data are output by a transmitter located within a DLI CCA in the ARF digital processor under test to the digital processor T/S DLI CCA receiver input buffer function.

The serial data stream is routed through the clocks and receiver busy flag function to the sync word detector and CRC generator/checker function on DLI CCA C5A4A8. The sync word detector and CRC generator/checker function detects the sync word and verifies the CRC sum appended to the serial data. The receiver (RX) data output from the sync word detector and CRC generator/checker function is applied to the receiver shift register and data buffer function. The receiver shift register and data buffer function converts the serial data into a 16-bit parallel word format that is stored in the data buffer.

After receiving, converting, and storing the test response data, DLI CCA C5A4A8 requests an interrupt. When the interrupt is honored by the microprocessor, DLI CCA C5A4A8 places an interrupt vector number on the common bus to the microprocessor. The microprocessor multiplies the interrupt vector number by 4 to obtain the interrupt vector address. The interrupt vector address points to the DLI input driver continuator software module that acts as an interrupt service routine to service the interrupt request.

When the interrupt is serviced, the 16-bit parallel data stored in the receiver shift register and data buffer function is applied over internal DLI CCA C5A4A8 bus LROO thru LR15 to the common data buffers function. The resultant common data buffers function output is routed over the common bus to the microprocessor for evaluation by the user code and ultimate display on the VDT for user interpretation.

1.12.13.9.4 SIO Interface CCA C5A4A7 Interface

The SIO interface CCA C5A4A7 interface provides two RS-422 serial transmitter channels and one RS-422 serial receiver channel for communicating with an LRU under test. The two transmitter channels are referred to as channel A and channel B, while the receiver channel is referred to as channel C.

SIO interface CCA C5A4A7 is accessed by the digital processor T/S microprocessor invoking the interrupt driven 1/0 routines within the operating system as previously described for DLI CCA C5A4A8. The following subparagraphs describe the data reception and transmission operations for SIO interface CCA C5A4A7. Refer to table 1-6 for summaries of the various LRUs serviced by input and output channels of SIO interface CCA C5A4A7.

1.12.13.9.4.1 Data Reception

Prior to the data reception, the SIO input driver initiator associated with the user code test routine sets up the SIO interface CCA C5A4A7 registers and logic functions to receive incoming data.

Data received from an LRU under test is applied over RS-422 lines to the channel C receiver input buffers function at a baud rate determined by the transmitter clock in the LRU under test. The most significant bit (MSB) of the data is received first. The receiver input buffer's output data is applied to the test/normal multiplexer (MUX) function.

During normal operation, the serial data is passed through the test/normal MUX function and stored in the receiver input RAM data buffer, under control of the data access control logic function. The receiver input RAM data buffer has 4096 bits of data storage capacity to minimize the number of microprocessor interrupts required for data transfers.

After the received data is stored in the input RAM data buffer, SIO interface CCA C5A4A7 requests an interrupt. When the interrupt is honored by the microprocessor, SIO interface CCA C5A4A7 places an interrupt vector number on the common bus to the microprocessor. The microprocessor multiplies the interrupt vector number by 4 to obtain the interrupt vector address. The interrupt vector address points to the SIO input driver continuator software module that acts as an interrupt service routine to service the interrupt request.

When the interrupt is serviced, the received data is shifted from the receiver input RAM data buffer by the data access shift register function under control of the data access control logic. The data access shift register function supplies the

resultant parallel data through the common data buffers via the common bus to the microprocessor.

1.12.13.9.4.2 Data Transmission
When data is to be transmitted to an LRU under test, the user code SIO output driver initiator sets up the SIO interface CCA C5A4A7 registers and logic functions for a data transmission operation.

Data to be transmitted to an LRU under test is passed over the common bus by the microprocessor to the common data buffers of SIO interface CCA C5A4A7. The common data buffer output data are loaded into the data access shift register function and converted to serial format. The resulting data access shift register serial data output is shifted into the transmitter output RAM data buffer function under control of microprocessor commands loaded into the data access control logic function by the SIO output driver initiator software module.

The transmitter output RAM data buffer function provides two buffer sections that each provide 2047 bits of data storage capacity to minimize the number of microprocessor interrupts required for data transfers.

Final composition of the serial output data stream for channel A or B is performed by transmitter A control logic or transmitter B control logic, respectively. The serial output data streams for channels A and B are applied, MSB first, from the transmitter output RAM buffers function through the transmitter output buffers function to the LRU under test. The data transmission rates for channels A and B are set by jumpers on SIO interface CCA C5A4A7 for 125 and 998.4 kHz (1 MHz, nominal), respectively.

1.12.13.9.5 SCAR Interface CCA C5A4A6 Interface
SCAR interface CCA C5A4A6 provides a digital processor T/S interface for testing SCAR processor level 0 and SCAR processor level 2. SCAR interface CCA C5A4A6 contains two serial output channels: a SCAR command data channel and SCAR receiver command data channel. Only the SCAR receiver command data channel is used by the digital processor T/S to transmit test commands to the LRU under test. LRU test results are received by a serial input channel provided on SCAR interface CCA C5A4A6.

SCAR interface CCA C5A4A6 is enabled for operation by the microprocessor using a polling technique incorporated into the FDF T/S group user code. The following subparagraphs describe how test commands are transmitted to the LRU under test and how test responses are received from the LRU under test. Table 1-6 summarizes the input and output signals passed through digital processor T/S connector J2 between SCAR interface CCA C5A4A6 and the LRU under test.

1.12.13.9.5.1 Transmission of Test Commands
Transmission of test command requests begins with the microprocessor executing the appropriate user code routine and applying the parallel format command requests onto the common bus. The test command data is applied through the SCAR interface CCA C5A4A6 common data buffers onto the CCA internal DATAOOH thru DATA15H bus. The command data output by the common data buffers is stored in the receiver command channel RAM function. Once stored, the command data is converted to serial format per interface commands previously stored in the command/control logic. The serial command data is passed along with associated clock and load strobe signals through the SCAR receiver and SCAR processor output buffers function to digital processor T/S connector J2 at a baud rate of 998.4 kHz. The serial command data, clock, and load strobe signals are routed over an interconnecting cable from digital processor T/S connector J2 to the LRU under test.

1.12.13.9.5.2 Reception of Test Responses
Responses to the serial test command data are output by the LRU under test and received at the SCAR data channel input buffer along with associated clock and load strobe signals. The serial input data rate is 998.4 kHz. The serial input data is passed through the test/normal MUX to the serial data input

channel function. The clock and load strobe signals associated with the input test response data are used to load the data into the serial data input channel function on SCAR interface CCA C5A4A6. The test response data is converted from serial to parallel format and is stored pending retrieval by the microprocessor.

1.12.14 Junction Box C5A6

Junction box C5A6 (figure FO-3, sheet 3) receives the de supply voltages and sense lines from power supplies C5A9 and C5A10 and supplies the voltages to LRUs under test and the digital processor T/S using supplied FDF T/S group cables.

Figure FO-2 is the wiring diagram for the junction box. Junction box C5A6 accepts the de voltage outputs from power supplies C5A9 and C5A10 at rear-panel-mounted connectors. The dc voltages are connected to terminal blocks within the junction box. The terminal blocks are also connected to pins on front-panel-mounted connectors that are dedicated for use by specific LRUs under test or the digital processor T/S. Additionally, the junction box contains a Lambda dc-to-dc converter that accepts the +28 V dc output from power supply C5A9 or C5A10 and produces +36 V dc for use by certain LRUs under test.

1.12.15 Power Supplies C5A9 and C5A10

Power supplies C5A9 and C5A10 (figure FO-3, sheet 3) are standard equipment and are identical. Internally, each power supply contains four power modules (designated PS 1 thru PS4) and associated internal wiring and components, but only PS 1 thru PS3 modules are connected to internal wiring; the PS4 (28 V dc) module is connected to its associated internal wiring/components in only one of the power supply units, namely C5A9. All dc power outputs of the unit are current-limited and voltage regulated. Power module PSI generates ±5 V dc voltage outputs, while PS2 and PS3 each generate ±15 V dc outputs. The power supply output voltage and current values can be monitored on a front-panel mounted digital meter. The digital meter displays either the voltage value or the current value that is output from one of the internal power modules and sensed at the junction box. Display of voltage or current is accomplished by appropriately positioning a two-position front-panel slide switch in conjunction with a four-position front-panel rotary switch. The slide switch selects voltage or current to be displayed; the rotary switch selects the output from one of the three power modules.

Each power module output voltage may be set by adjusting one of three front-panel-mounted potentiometers. The output voltages from the power supply are routed to junction box C5A6 for ultimate distribution to the digital processor T/S and LRUs under test.

1.12.16 VDT/STE - PAM Switch Box

The VDT/LBP switch box supports use of VDT C4A4 with digital processor T/S C5A4 for FDF T/S group operations. It also allows the VDT to be used for ARF digital processor EPROM load operations using STE PAM (C6A3) and its associated PROM programmer (C6A2). The PAM and PROM programmer are part of the primary mission equipment (PME) test capability of the AMF. Refer to the AMF manual referenced in appendix A for full details.

CHAPTER 2
OPERATING INSTRUCTIONS

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SECTION I. CONTROLS AND INDICATORS

2.1 SCOPE

This chapter provides operating instructions for the FDF T/S group. Included in this chapter are descriptions of the operator/crew controls and indicators, as well as typical test setup procedures and diagrams for all line-replaceable units (LRUs) tested by the FDF T/S group.

2.2 OPERATOR/CREW CONTROLS AND INDICATORS

The FDF T/S group equipment has no controls and indicators except for the general purpose test equipment. Refer to the appropriate manuals listed in appendix A for the location and use of the controls and indicators incorporated into the general purpose test equipment.

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2.3 GENERAL

This section provides FDF T/S group initial setup, power-up, self-test, and operational readiness/verification procedures. These procedures are to be performed prior to any LRU testing. They also are to be performed if an FDF T/S group failure is noted during LRU test operation or, alternatively, during routine organizational maintenance activities.

General LRU test descriptions and typical setup diagrams are also provided in this section of the manual. The LRU test descriptions discuss the various automated LRU testing capabilities provided by the FDF T/S group. The overall manual-testing facilities of the FDF T/S group are also described.

2.4 OPERATING PROCEDURES

The initial setup, power-up, self-test, and operational readiness/verification procedures described in the following paragraphs are to be performed prior to any LRU testing. They also are to be performed if an FDF T/S group failure is noted during LRU test operation or, alternatively, during routine unit maintenance activities.

When a fault occurs during operation, the power-up, self-test, and operational readiness/verification procedures in this section should be performed to locate defective equipment items within the FDF T/S group. Procedures herein adhere to the FDF T/S group maintenance philosophy specified in the maintenance allocation chart (MAC) provided in appendix B.

If a standard equipment item (namely, test equipment units, printer unit, or VDT) is determined to be faulty during operation, the unit is replaced by unit maintenance personnel. Replacement of these items requires the configuration of the GPIB/HPIB addresses as shown in table 2-1. Repair of the defective unit is performed at depot level.

Table 2-1. GPIB/HPIB Address Configuration

Unit name and position	GPIB/HPIB address
Spectrum analyzer C2A1	27
Network analyzer C2A2	16
Universal counter C3A1	03
Printer C3A3	06
Function generator C4A1	17
Signal generator C4A2	07
Logic analyzer C4A3	08

If a power supply, the power junction box, the patch panel, the ARF intercept receiver pallet, or the digital processor T/S is determined to be faulty during operation, replacement or repair (as applicable) is performed by direct support maintenance personnel per procedures provided in chapter 4 and elsewhere in this manual.

Note

The following operational procedures are started with all FDF T/S group equipment items installed and powered down (shut down).

2.4.1 Initial Setup, Power-up, and Self-Tests

To perform initial setup, power-up, and self-test procedures, proceed as follows:

1. Perform the following steps in the order given:
   a. that FDF T/S group equipment is connected per procedure outlined in chapter 3 and cabling diagram in figure FO-1.
   b. that all FDF T/S group equipment is plugged into ac strips and that ON/OFF switches on ac strips are ON.
   c. that cable W18 from digital processor T/S C5A4 connector J14 is plugged into ac strip, and that blower C5A4B 1 on digital processor T/S is operating properly (blower air is exhausted through unit's front panel).
   d. up printer, general purpose test equipment, and VDT in the order given below, and note equipment responses indicated. As applicable, also check that cooling fans are functioning properly as each equipment item is powered up.

(1) Printer C3A3. Printer responds by running its built-in self-test, which includes moving of print head assembly. No operational status is displayed while self-tests are executed. When self-tests complete successfully, printer power-on (PWR) indicator lights.

If PWR indicator flashes, a failure or error occurred during self-tests. Replace printer C3A3, and refer defective printer to depot for repair.

(2) Spectrum Analyzer C2A1. Spectrum analyzer responds by running its built-in self-tests. No operational status is displayed while self-tests are executed. When self-tests complete successfully, no failures/errors are noted on analyzer display and analyzer displays a red graticule grid screen and begins a built-in self-alignment routine.

Alignment routine displays LO ADJUST STATUS: , and the following messages appear underneath the heading as they are executed: AMPLTD DATA, XFER ROLLER, OFFSET ROLLER, MAIN ROLLER, ROLLER SENS., DONE.

Next, routine displays IF ADJUST STATUS: , and the following messages appear underneath the heading as they are executed: AMPLITUDE, 300KHZ RBW, 1-MHZ RBW, 2-MHZ RBW, 100-KHZ RBW, 30-KHZ RBW, 10-KHZ RBW, 3-KHZ RBW, l-KHZ RBW, 300-HZ RBW; then 10-, 30-, 100-HZ RBW is displayed.

When alignment routine has successfully completed, the message HP 8560A, COPYRIGHT 1989, REV # 920122 is displayed, analyzer is set to a 30-kHz frequency setting with a span of 0 Hz, and a trace is displayed that shows ambient noise only.

If failures or errors occur during self-tests or self-alignment routine, replace spectrum analyzer C2A1. Refer defective spectrum analyzer to depot for repair.

(3) Network Analyzer C2A2. Network analyzer responds by running its builtin self-tests and displays: *hp*. When self-tests complete successfully, no failures/errors are noted on analyzer screen and message SELF TEST PASSED is displayed. A normal measurement screen also appears on display showing ambient noise traces only.

If failures or errors occur during self-tests, replace network analyzer C2A2. Refer defective network analyzer to depot for repair.

(4) Universal Counter C3A1. Universal counter responds by running its builtin self-tests. No operational status is displayed while most of the self-tests are executed. However, all indicators and display segments light during display self-test. When self-tests complete successfully, no failures/errors are indicated (such as blinking indicators) and counter's indicators reflect last signal measurement that was performed prior to last shutdown.

If failures or errors occur during self-tests, replace universal counter C3A1. Refer defective universal counter to depot for repair.

(5) Oscilloscope C3A2. Oscilloscope responds by running its built-in selftests and displays RUNNING SELF-TEST; GPIB status indicators light. When self-tests complete successfully, no failures/errors are noted on oscilloscope display and a normal measurement screen appears on display showing ambient noise traces only.

If failures or errors occur during self-tests, replace oscilloscope C3A2. Refer defective oscilloscope to depot for repair.

(6) Function Generator C4A1. Function generator responds by running its built-in self-tests. The message WAVETEK SG 1288/G is displayed while self-tests are executed. When self-tests complete successfully, no failures/errors are indicated (such as error code in alphanumeric display), and function generator display reflects last signal setup that was performed prior to last shutdown when Frequency or Amplitude buttons are pressed.

If failures or errors occur during self-tests, replace function generator C4A1. Refer defective function generator to depot for repair.

(7) Signal Generator C4A2. Signal generator responds by running its built-in self-tests. No operational status is displayed while most of self-tests are executed. However, all indicators and display segments light during display self-test. When self-tests complete successfully, no failures/errors are indicated (such as blinking indicators), and signal generator indicators reflect last signal setup that was performed prior to last shutdown.

If failures or errors occur during self-tests, replace signal generator C4A2. Refer defective signal generator to depot for repair.

(8) Logic Analyzer C4A3. Logic analyzer responds by running its built-in self-tests as follows: ROM test, RAM test, interrupt test, display test, keyboard test, acquisition test, threshold test, and disk test. When selftests complete successfully, no failures/errors are noted on analyzer display, and the response LOADING SYSTEM FILE appears. This message indicates that analyzer's operating system files are being loaded from operating system diskette (P/N 01650-13531). If no load errors occur, the System Configuration screen appears on display.

If failures or errors occur during self-tests or operating system load, replace logic analyzer C4A3. Refer defective logic analyzer to depot for repair.

(9) Digital Multimeter (DMM) C5A1. DMM responds by running its built-in self-tests. No operational status is displayed while most of self-tests are executed. However, all indicators and display segments light during display self-test. When self-tests complete successfully, no failures/errors are indicated, such as an error code or blank display.

If failures or errors occur during self-tests, replace DMM C5A1. Refer defective DMM to depot for repair.

(10) VDT C4A4. VDT responds by running its built-in self-tests. No operational status is displayed while self-tests are executed. When

self-tests complete successfully, VDT sounds an audible beep, cursor is displayed on upper left corner of screen, and function key definitions are displayed at bottom of screen.

If VDT does not beep, or if display is not as described above, a failure or error occurred during self-tests. In this case, replace VDT C4A4. Refer defective VDT to depot for repair.

e. If VDT does not function properly in the following substeps, replace VDT and refer defective VDT to depot for repair. Set up VDT C4A4 for operation as follows:

(1) If not done already, enable REMOTE MODE by pressing function key F4 asterisk is shown on REMOTE MODE function key display).

Ensure that all other modes are disabled (no asterisks shown on other function key displays). To disable a mode, just press its associated function key.

(2) Press System key; then press function key F8 (configuration keys). Press function key F3 to access terminal communication parameters.

(3) Set terminal PARITY to NONE.

(4) Set terminal BAUD RATE to 4800.

(5) Set RECV/PACE to XON/XOFF.

(6) Press function key Fl to return to on-line mode.

Note

The FDF T/S group software contained in the digital processor T/S does not recognize lowercase characters.

(7) Press CAPS button on VDT keyboard.

(8) Verify that all other pushbutton switches are not pressed.

Note

In the following step, when power supplies C5A9 and C5Al0 are switched on, VDT displays start of digital processor T/S self-test routine that is described paragraph 2.4.2 (Self-Test, Operational Readiness/Verification). Ignore the self-test results in the following preliminary steps; they are discussed later.

f. Set front-panel ON/OFF switches on power supplies C5A9 and C5A10 to ON.

g. Connect DMM C5A1 to digital processor T/S connector pins J2-12 (+5 V de) and J2-13 (ground).

h. Adjust power supply C5A9 front-panel 5-V de potentiometer so that DMM indicates +5.0 (±0.05) V dc at digital processor T/S connector pins J2-12 and J213.

i. If no indication is received on DMM, set power supply C5A9 front-panel rotary switch to position 1 and METER SELECTION switch to VOLTS. If power supply front-panel seven-segment indicator does not show 5.0 V de, refer to direct support maintenance to replace power supply C5A9. Refer defective unit to depot for repair. If seven-segment indicator does show 5 V dc, use a different multimeter to re-perform steps g and h. If indication on different multimeter is present, replace DMM C5Al. Refer defective DMM to depot for repair.

j. If not done already, set front-panel METER SELECTION switches on power supplies C5A9 and C5A10 to VOLTS.

k. Set power supply C5A9 front-panel rotary switch to position 2 and adjust frontpanel 15-V potentiometer 2 so that 15.0 (±0.2) V dc is indicated on front-panel seven-segment indicator.

i. Set power supply C5A9 front-panel rotary switch to position 4 and adjust power supply front-panel 28-V potentiometer so that 28.0 (±0.2) V dc is indicated on front-panel seven-segment indicator.

m. Set power supply C5A10 front-panel rotary switch to position 1 and adjust frontpanel 5-V potentiometer 1 so that 5.0 (±0.1) V dc is indicated on front-panel seven-segment indicator.

n. Set power supply C5A10 front-panel rotary switch to position 4 and adjust power supply front-panel 28-V potentiometer so that 28.0 (±0.2) V dc is indicated on front-panel seven-segment indicator. Initial setup, power-up, and self-test procedure for the FDF T/S group is now complete.

2. If, in step 1 above, power supply front-panel seven-segment indicator does not show proper voltages during adjustments, refer to direct support maintenance to replace applicable power supply unit. Refer defective unit to depot for repair.

2.4.2 Self-Test, Operational Readiness Nerification

The following additional self-test and operational readiness/verification procedures must be performed in the order given to verify proper operation before testing any LRUs. They also are to be performed if an FDF T/S group failure is noted during LRU test operation or, alternatively, during routine unit maintenance activities.

Note

Perform initial setup, power-up, and self-test procedures presented in the preceding paragraph before beginning the additional self-test, operational readiness/verification procedures below.

2.4.2.1 Network Analyzer C2A2

To verify proper operation of network analyzer C2A2, proceed as follows:

1. network analyzer operational readiness/verification test as follows:
   a. Press INSTRUMENT STATE SYSTEM key on network analyzer front panel.
   b. On right side of network analyzer screen display, press SERVICE MENU key. Next, press TESTS key and then SYS VER TESTS.

c. Press EXECUTE TEST key. The message TEST 27 Sys Ver Init DONE is displayed upon successful completion of tests.

d. Press INTERNAL TESTS key on right side of screen display; then press EXECUTE TEST key. The message TEST 0 ALL INT PASS is displayed upon successful completion of tests.

2. If a fault/error message appears in step 1 above, replace network analyzer C2A2. Refer defective network analyzer to depot for repair.

2.4.2.2 Universal Counter C3A1

To verify proper operation of universal counter C3A1, proceed as follows:

1. universal counter operational readiness/verification test as follows:

Note

The universal counter requires a minimum warm-up time of 20 minutes.

a. Press front-panel CHECK key momentarily. Verify that all display annunciators, except STBY and A and B INPUT trigger, cycle on and off. Press any function key to return unit to normal operation.

b. Connect a BNC coaxial cable from patch panel C5A2 COUNTER TIME BASE OUT connector J2 to universal counter front-panel INPUT A connector.

c. Press front-panel Z=1M/50 ohms key for INPUT A to 50 ohm. Verify that all other INPUT A group keys are off.

d. Repeat steps b and c for universal counter INPUT B.

e. Press and hold front-panel CHECK key for approximately 3 seconds. Verify that all universal counter front-panel annunciators light for approximately 10 seconds. Successful completion of test is indicated by FE PASS message on display. If test fails, a numbered fail message is displayed. Test in progress is a continuous loop. Press any front-panel function key to exit test loop and return to normal operation.

Note

If time base signal does not trigger universal counter, check for signal presence using oscilloscope C3A2 (as described in the next paragraph below). If signal is present, universal counter is faulty.

2. If a fault/error is observed in step 1 above, replace universal counter C3A1. Refer defective universal counter to depot for repair.

2.4.2.3 Oscilloscope C3A2

To verify proper operation of oscilloscope C3A2, proceed as follows:

1. Perform oscilloscope operational readiness/verification test as follows:

a. Connect connector J2 (COUNTER TIME BASE output) on patch panel C5A2 to channel 1 input connector, using BNC cable.

b. SETUP AUTO key on oscilloscope front panel. Verify that oscilloscope auto setup feature functions correctly, and that a signal is displayed on trace 1.

c. that a 10 (±0.1) MHz cw signal of 3.4 (±0.1) V p-p is displayed on oscilloscope.

2. If a fault/error message appears in step 1 above, replace oscilloscope C3A2. Refer defective oscilloscope to depot for repair.

2.4.2.4 Spectrum Analyzer C2A1

To verify proper operation of spectrum analyzer C2A 1, proceed as follows:

1. spectrum analyzer operational readiness/verification test as follows:

Note

The spectrum analyzer requires a minimum warm-up time of 5 minutes.

a. Connect 300-MHz CAL OUTPUT connector to INPUT 50-ohm connector on spectrum analyzer front panel, using BNC cable and N-type to BNC adapter on INPUT connector.

b. Press FREQUENCY key on spectrum analyzer front panel, and subsequently enter 300 MHz on DATA keypad.

c. Press SPAN key, and enter 100 kHz on DATA keypad. Verify that 300-MHz signal is displayed on analyzer screen, as shown in figure 2-1.

d. Press MARKER MKR key to activate marker, then press MARKER PEAK SEARCH key. CAL signal center frequency and amplitude are then displayed on screen. Verify that CAL signal is 300 (t±0.0005) MHz and that signal amplitude is greater than -11 dBm.

e. Proceed as follows:

(1) Press analyzer COPY key to print screen on printer C3A3. Verify that spectrum analyzer screen prints correctly, as shown in figure 2-1.

(2) If spectrum analyzer screen print does not print, check that printer HPIB address in spectrum analyzer is 27. If not, change it to 27. If O.K., then press PRINT key on logic analyzer C4A3. If screen does not print, check HPIB cable from logic analyzer to printer. If logic analyzer screen does not print, replace printer C3A3. If logic analyzer screen prints correctly, check HPIB cable from spectrum analyzer to printer, then replace spectrum analyzer C2A1.

f. spectrum analyzer front-panel INPUT 50-ohm connector to patch panel C5A2 connector J2 (COUNTER TIME BASE), using BNC cable.

g. analyzer AMPLITUDE key and enter reference level of 20 dBm on DATA keypad. Press FREQUENCY key and enter 10 MHz on DATA keypad. Verify that a 10-MHz signal is displayed on screen, as shown in figure 2-2.

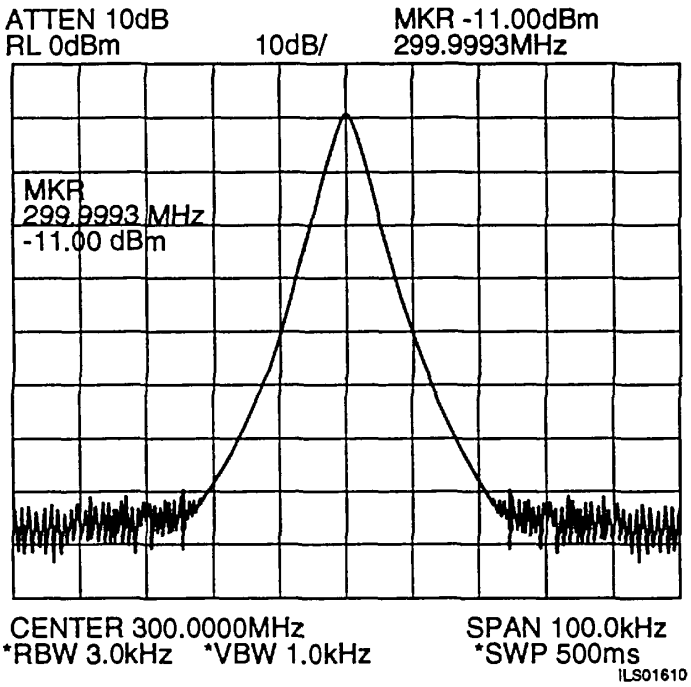

Figure 2-1. 300-MHz Spectrum Analyzer Waveform Screen

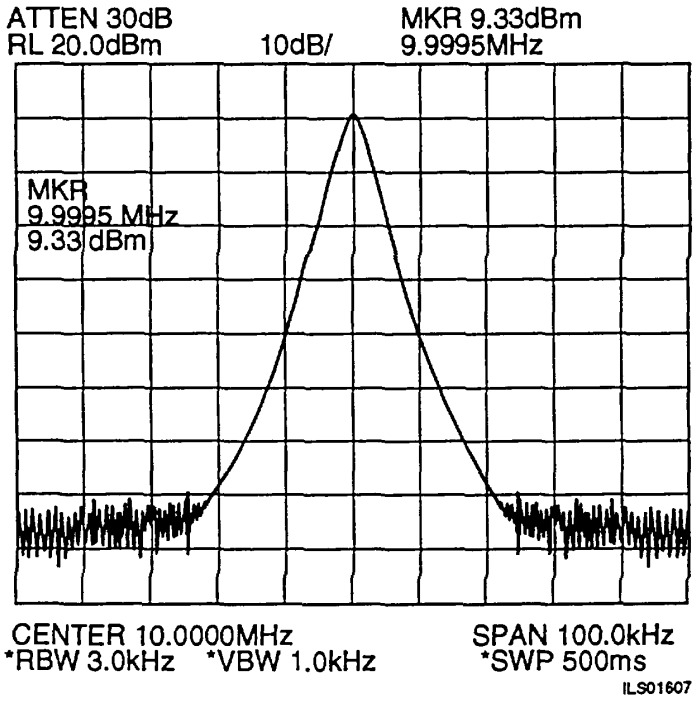

Figure 2-2. 10-MHz Spectrum Analyzer Waveform Screen

h. Press MARKER MKR key to activate marker function; then press MARKER PEAK SEARCH key. Verify that test signal is 10 (±0.001) MHz with amplitude greater than +9 dBm.

i. Connect analyzer front-panel INPUT 50-ohm connector to function generator C4A '"Unbalanced" Function Output, using BNC cable.

j. Proceed as follows:

(1) Press analyzer AMPLITUDE key and enter reference level of 0 dBm on DATA keypad. Press FREQUENCY key and enter 765.4 kHz on DATA keypad. Verify that a 765.4-kHz cw signal is displayed on screen, as shown in figure 2-3.

(2) If signal is not present, use oscilloscope C3A2 to verify function generator output. If signal is not present on oscilloscope, replace function generator. If signal is present on scope (but not on spectrum analyzer), replace spectrum analyzer.

k. Press MARKER MKR key to activate marker function; then press MARKER PEAK SEARCH key. Verify that test signal is 765.4 (±2.0) kHz with amplitude of -21 (±0.5) dBm.

2. If a fault or error appears in step 1 above, replace spectrum analyzer C2A1 indicated. Refer defective spectrum analyzer to depot for repair.

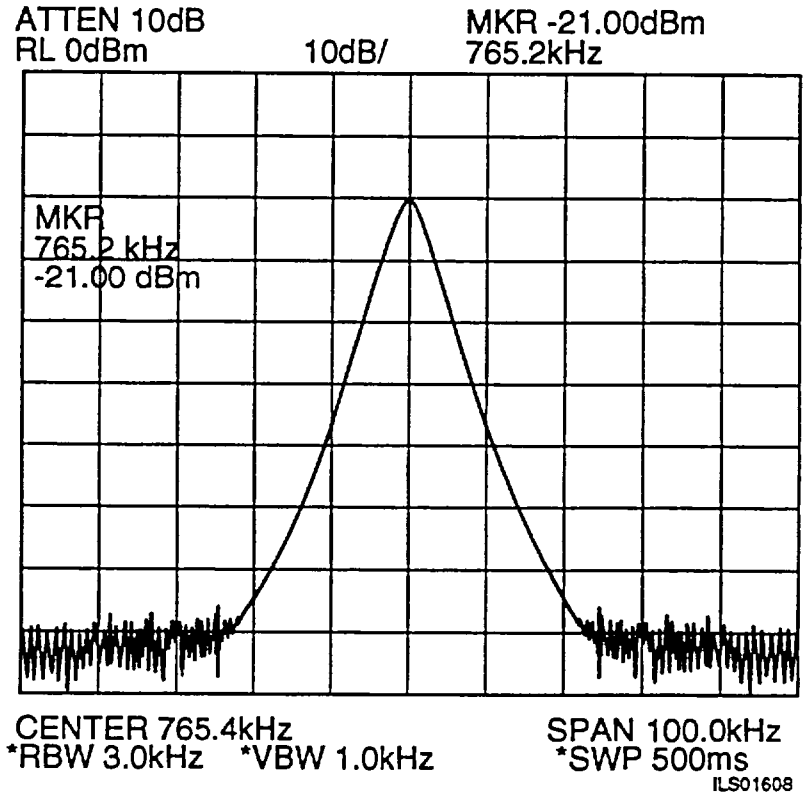

Figure 2-3. 765.4-kHz Spectrum Analyzer Waveform Screen

2.4.2.5 Signal Generator C4A2

To verify proper operation of signal generator C4A2, proceed as follows:

1. Perform signal generator operational readiness/verification test as follows:

Note
The signal generator requires a minimum warm-up time of 20 minutes.

a. Set signal generator POWER pushbutton switch to ON.

b. Verify that all front-panel indicators light for approximately 3 seconds while internal memory check of RAM and ROM is being executed. If front-panel indicators remain lit, signal generator is defective.

c. Verify that front-panel displays indicate a carrier frequency of 123.45 MHz at an output amplitude of -67.0 dBm, and no modulation. Verify that none of frontpanel indicators are lit except for dBm annunciator.

d. Press CARRIER AMPTD key and enter 0 dBm on DATA keypad.

e. Connect signal generator RF OUTPUT connector to universal counter C3A1 INPUT A connector, using a BNC cable.

f. Set Z = 1-MOhm key for A INPUT on universal counter.

g. Set signal generator output frequency and level as follows:

(1) Press CARRIER FREQ pushbutton.

(2) Enter 111.1111 MHz on DATA keypad.

(3) Verify that FREQUENCY display indicates 111.1111 MHz.

(4) Press CARRIER AMPTD pushbutton.

(5) Enter -10 dBm on DATA keypad.

(6) Verify that AMPLITUDE display indicates -10.0 dBm.

h. Verify that universal counter C3AI indicates a measured frequency of 111.1111 MHz.

i. Set signal generator incremental frequency value as follows:

(1) Press CARRIER FREQ pushbutton.

(2) Press INCR SET pushbutton.

(3) Enter 111.1111 MHz on DATA keypad.

j. Press and release CARRIER FREQUENCY step-up key (arrow points up).

k. Verify that universal counter indicates measured frequency of 222.2222 MHz.

l. Disconnect signal generator RF OUTPUT from universal counter INPUT A connector.

m. Connect signal generator RF OUTPUT connector to spectrum analyzer C2A1 INPUT 50-ohm connector, using BNC cable.

n. Set signal generator output frequency and amplitude as follows:

(1) Press CARRIER FREQUENCY pushbutton.

(2) Enter 0. 1 MHz on DATA keypad.

(3) Press CARRIER AMPTD pushbutton.

(4) Enter 0 dBm on DATA keypad.

o. Proceed as follows:

(1) Press spectrum analyzer C2A1 front-panel FREQUENCY key and enter 100 kHz on DATA keypad. Press SPAN key and enter 50 kHz on DATA keypad. Press AMPLITUDE key and enter +20 dBm REF level on DATA keypad. Press MARKER MKR key; then press MARKER PEAK SEARCH key. Verify that 100-kHz signal generator output signal is displayed on analyzer display, as shown in figure 2-4.

(2) If signal is not present, replace signal generator.

p. Proceed as follows:

(1) Press spectrum analyzer SPAN key and enter 2 MHz on DATA keypad. Verify that 100-kHz fundamental and harmonics are displayed on analyzer display, as shown in figure 2-5.

(2) If signal generator output spectra is not correct, replace signal generator.

2. If a fault or error appears in step 1 above, replace signal generator C4A2. Refer defective signal generator to depot for repair.

2.4.2.6 Digital Processor TIS C5A4

To verify proper operation of digital processor T/S C5A4, proceed as follows:

1. Perform digital processor T/S operational readiness/verification test as follows:

Note

If the digital processor T/S fails the self-test procedure, refer to the FDF T/S group performance test in chapter 4. While performing the digital processor T/S self-test to verify operational readiness of the equipment, press VDT key Q, R, or L, as appropriate, but do not press VDT key C. VDT key C is pressed during the FDF T/S group performance test to determine the cause of DLI CCA C5A4A8 failure.

a. Connect a 16-channel lead set and termination adapter to POD1 input of logic analyzer C4A3.

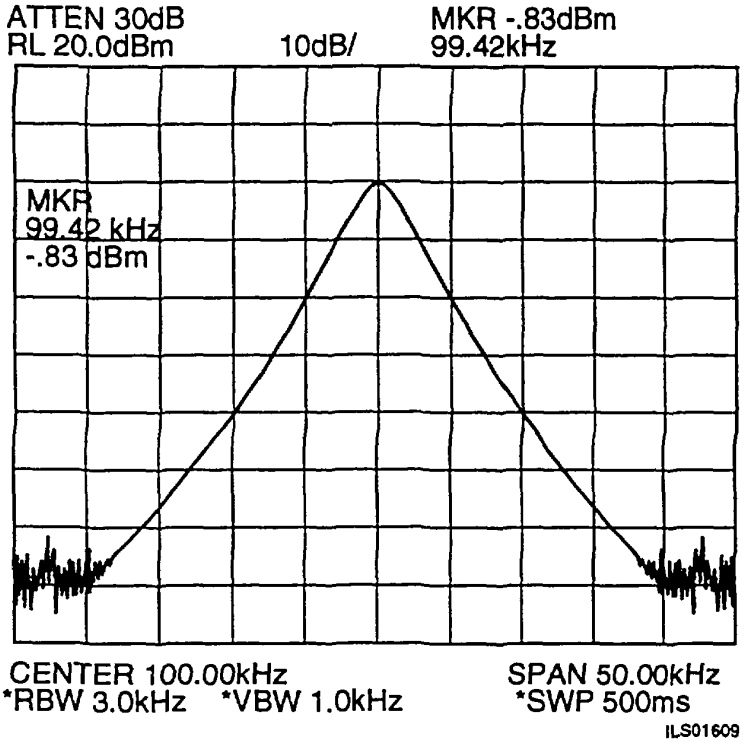

Figure 2-4. 100-kHz Spectrum Analyzer Screen

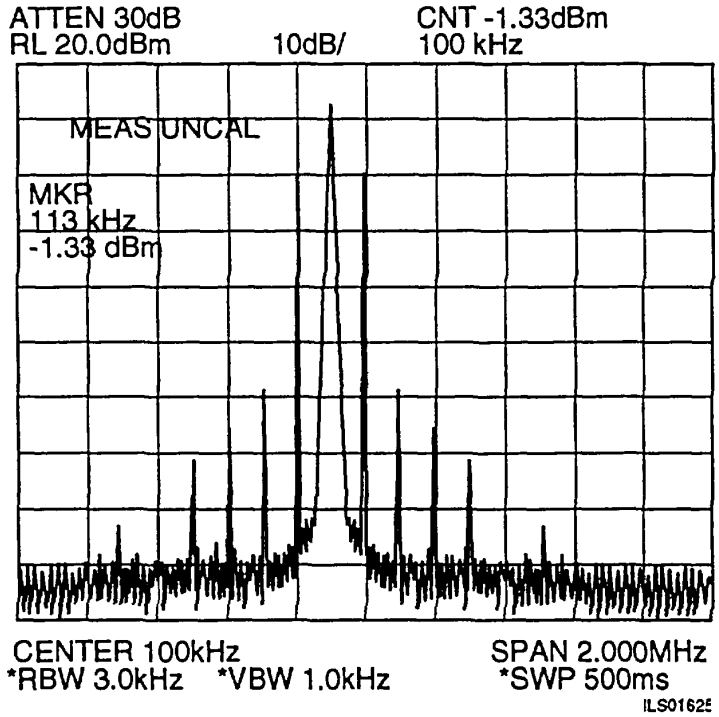

Figure 2-5. 100-kHz Fundamental/Harmonic Spectrum Analyzer Screen

b. Connect cable W15 connector P1 to digital processor T/S connector J18 (PIO port). Connect pins on other end of cable W15 to POD-1 lead set, channels 0 thru 11 per cable tags on each pin lead. If necessary, refer to cable connection details shown in digital processor T/S test setup in figure 4-1.

c. Verify that SYSTEM CONFIGURATION screen is displayed on logic analyzer. If not, power down analyzer, then power up again. After restart, self-tests, and operating system load, analyzer displays SYSTEM CONFIGURATION screen.

d. Load logic analyzer PIO-TEST setup file from operating system diskette as follows:

(1) Press logic analyzer I/O MENU key.

(2) Move cursor to Disk Operations field and press SELECT key; then select From File entry box, select PIO-TEST, and press SELECT key.

(3) Move cursor to Execute field and press SELECT key; then move cursor to Continue option field, and press SELECT key. In turn, analyzer responds by loading test setup file. After file has been loaded, the message "Load operation complete" is displayed.

(4) Move cursor to Done option field, and press SELECT key.

e. Press RUN key on logic analyzer. Analyzer responds by displaying Timing Waveform screen for the test, and the message "waiting for trigger" is displayed at top of screen.

Note

In the following procedure, if a digital processor T/S bus error occurs, the message BUS ERROR DETECTED ON TEST SET DPU is displayed on the VDT. If the bus error is caused by a fault in the digital processor T/S, pressing any key resets the digital processor T/S and causes the self-test procedure to continue until the fault is isolated. If the bus error is caused by a primary power source failure, the self-test procedure must be restarted from the beginning by simultaneously pressing the control (CTRL) and R keys on the VDT keyboard.

For general descriptive information about error messages associated with digital processor testing, and how to resolve them and/or proceed with testing, refer to paragraph 2.5 (Digital Processor Error Messages).

f. Digital processor T/S test screen should now be displayed on VDT C4A4. Simultaneously press control (CTRL) and R keys on VDT keyboard to reset digital processor T/S; then press VDT key L to continue procedure.

Note

The digital processor T/S self-test routine does not exercise the drivers on PIO interface CCA C5A4A10 and GPIB interface CCA C5A4A11 contained in the digital processor T/S.

g. Verify that VDT display indicates that all digital processor T/S C5A4 CCAs, except GPIB interface CCA C5A4A11 and PIO interface CCA C5A4A10, have passed self-test procedure.

If test passes, proceed to step i. If any failures or errors occurred during self-tests, proceed as follows:

(1) Power down digital processor T/S by setting POWER switches on power supplies C5A9 and C5A10 to OFF and proceeding as follows:

(a) Disconnect cable connector W3P2 from connector J15 of digital processor under test.

(b) Disconnect cable connector W14P1 from primary power source that is connected to connector J14 of digital processor under test.

(2) Remove digital processor T/S chassis top cover per procedure in chapter 4.

(3) Verify that digital processor T/S CCAs are properly seated in their respective slots.

(4) Power up digital processor T/S by setting POWER switches on power supplies C5A9 and C5A10 to ON and proceeding as follows:

(a) Reconnect cable connector W14P1 to primary power source that is connected to connector J14 of digital processor under test.

(b) Reconnect cable connector W3P2 to connector J15 of digital processor under test.

h. Proceed as follows:

(1) Re-perform steps f and g. If digital processor T/S passes self-tests, proceed to step i.

(2) If failures/errors are still shown on VDT, replace digital processor T/S and refer defective unit to direct support maintenance.

i. Proceed as follows:

(1) Verify that signal generator C4A2 is tuned to 123.45 MHz at -67 dBm. Verify that function generator C4A1 is tuned to 765.43 kHz at -21.1 dBm. If readouts are correct, proceed to step j.

(2) If readouts on both units are incorrect, GPIB interface CCA C5A4A11 is defective; replace digital processor T/S and refer defective unit to direct support maintenance.

(3) If readouts on only one of the units is incorrect, replace applicable unit and refer defective unit to depot for repair.

j. Verify that parallel interface signals displayed on logic analyzer C4A3 are alternating 12-bit 1010 and 0101 bit patterns (alternating positive and negative going pulses), as shown in figure 2-6. If patterns are correct, proceed to step 1.

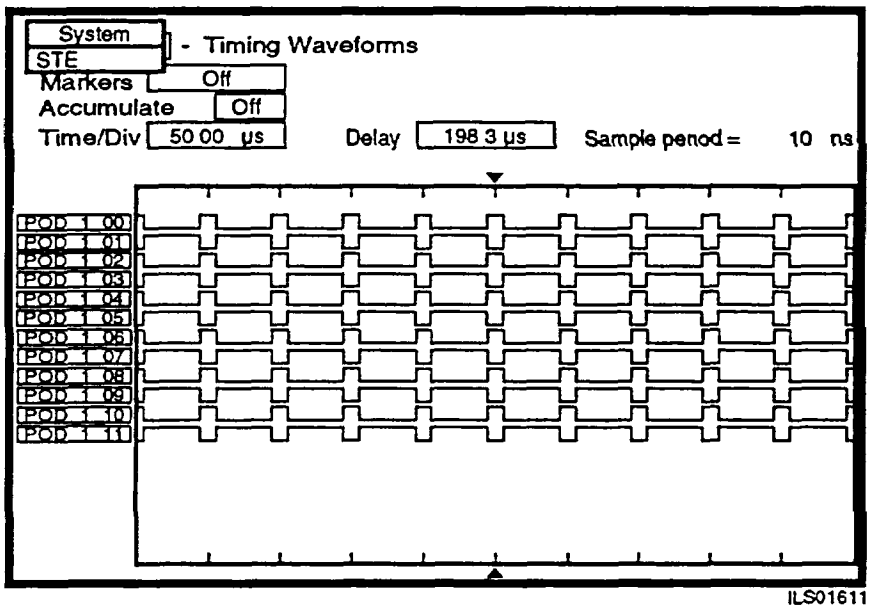

Figure 2-6. Parallel Output Waveform Logic Analyzer Screen

k. If one or more signals are absent or incorrect on logic analyzer C4A3 display, PIO interface CCA C5A4A10 is probably defective; replace digital processor T/S and refer defective unit to direct support maintenance. Repeat steps f thru j on replacement digital processor T/S; if indication still abnormal, replace logic analyzer and refer defective unit to depot for repair.

l. If digital processor T/S successfully completes self-test procedure outlined in preceding steps, press VDT key Q. When VDT key Q is pressed, FDF T/S group main menu is displayed on VDT, as shown in figure 2-7.

2. FDF T/S group self-test/operational readiness procedures are now complete. To proceed with LRU testing, press VDT key associated with desired LRU test procedure and proceed to appropriate LRU test reference information in the paragraphs that follow. LRU test setups, test equipment requirements, and maintenance operating procedures are contained in the technical manual for each LRU tested using the FDF T/S group (see table 1-2).

```
GRCS FDF TEST SET SOFTWARE VERSION 3.0

HIT THE APPROPRIATE KEY TO PROCEED TO THE TEST OF YOUR
CHOICE.  THE TEST SET DPU CAN BE RESET FROM ANY PROMPT BY
HITTING"CTL-R".

A - ADPU TESTING
T - TSDPU TESTING
0 - SCAR 0 PROCESSOR TESTING
1 - SCAR 1 PROCESSOR TESTING
2- SCAR 2 PROCESSOR TESTING
R - RF PROCESSOR TESTING
D - R2270 DUAL CHANNEL RECEIVER TESTING
S - R2289 SINGLE CHANNEL RECEIVER TESTING
V - R8604 SINGLE CHANNEL RECEIVER TESTING
U - RCU SIMULATOR
```

Figure 2-7. FDF T/S Group Main Test Menu

2.5 DIGITAL PROCESSOR ERROR MESSAGES

When certain types of faults are encountered in the digital processor T/S or the ARF digital processor (referred to as the ADPU in the FDF T/S group test menu), test execution is halted and an error message is displayed on the VDT. From the software viewpoint, the faults are detected through the exception processing feature of the MC68000L8 microprocessors in either the digital processor T/S or the ARF digital processor under test. Some possible faults that can be detected by exception processing include software errors, bus errors, processing errors due to power surges and transients, spurious interrupts, incorrect interrupt handling, and other faults from a number of different sources.

2.5.1 Exception Processing/Error Message Types Two basic types of error messages are displayed on the VDT for exception processing faults: bus error messages and exception processing messages. Bus error messages are described in subsequent paragraphs. All other errors detected from exception processing cause the VDT to display one of the two following messages: EXCEPTION PROCESSING HAS BEEN INITIATED ON THE TEST SET DPU or EXCEPTION PROCESSING HAS BEEN INITIATED ON THE DPU UNDER TEST. In addition to one of the two preceding messages, the message EXCEPTION VECTOR = XX is displayed for test system programming purposes and is to be ignored by the operator. The message HIT ANY KEY TO RESET DPU is also displayed.

2.5.2 Operator Response to Exception Processing/Error Messages To handle the detected exception processing fault, the operator must press any key on the VDT keyboard. If the detected fault is in the digital processor T/S, pressing any key on the VDT keyboard resets the digital processor T/S. When the digital processor T/S is reset, the operator must re-initiate the performance test step being performed on the LRU under test when the fault occurred If the detected

fault is in an ARF digital processor under test, test execution continues automatically from the performance test step in progress when the fault occurred.

2.5.3 Bus Errors

Three types of bus errors may occur during computer-controlled testing of the digital processor T/S or the ARF digital processor. Bus errors can be caused by primary power source failure, surges, and transients, as well as a fault in the digital processor T/S or a faulty or improperly seated CCA in the ARF digital processor. The following subparagraphs describe the various types of bus errors associated with each digital processor and the method to be used by the operator in handling each bus error.

2.5.3.1 Digital Processor T/S

When a bus error is detected in the digital processor T/S, a BUS ERROR DETECTED ON TEST SET DPU message is displayed on the VDT. If the bus error is caused by a fault in the digital processor T/S while the self-test procedure is being executed, pressing any key at the VDT keyboard resets the digital processor T/S and causes the self-test procedure to continue until the fault is isolated. The operator follows the fault isolation instructions and repairs the fault in accordance with instructions in procedures within this chapter, or per direct support maintenance procedures in chapter 4. After the fault is repaired, the LRU test in progress at the time the fault occurred is re-initiated.

2.5.3.2 ARF Digital Processor

Two types of bus errors can occur during LRU testing of the ARF digital processor. These bus errors are indicated by the VDT displaying either a BUS ERROR DETECTED ON DPU UNDER TEST message or an ACCESS OF XXXXXXCCA IN SLOT AXX CAUSED BUS ERROR message. If BUS ERROR DETECTED ON DPU UNDER TEST is displayed, the operator presses any key at the VDT keyboard. The FDF T/S group software then attempts to reset the digital processor under test and continues with the test in progress to isolate the fault in the LRU under test. If ACCESS OF XXXXXXCCA IN SLOT AXX CAUSED BUS ERROR is displayed, perform the following steps:

1. Disconnect cable connector W3P2 from connector J15 of digital processor under test.
2. Disconnect cable connector W14P1 from primary power source that is connected to connector J14 of digital processor under test.
3. Remove cover from digital processor under test.
4. Verify that indicated CCA is properly seated in correct slot connector.
5. Reconnect cable connector W14Pl to primary power source that is connected to connector J14 of digital processor under test.
6. Reconnect cable connector W3P2 to connector J15 of digital processor under test.
7. Press key C at VDT keyboard to continue test in progress before bus error occurred and to isolate fault in LRU under test.

2.6 LRU TEST OPERATIONAL DESCRIPTIONS

The following paragraphs describe general operational and functional capabilities provided for the LRUs that are tested by, or use the equipment included in, the FDF T/S group. Operational and functional limitations are also described, along with general instructions for use of the FDF T/S group during LRU testing.

Information for LRUs that use automated test capabilities of the FDF T/S group includes a brief description of the tests performed by the digital processor T/S. Each description contains a list of the

FDF T/S group general purpose test equipment used to check out and troubleshoot the LRUs that are tested under computer control.
Manually tested LRUs are those that do not use computer-directed or computer-controlled test features of the digital processor T/S. For these LRUs, the FDF T/S group typically only provides de power from power junction box C5A6 through supplied interconnect cables. Additionally, certain pieces of FDF T/S group standard test equipment may be used to test these LRUs.

This technical manual only summarizes the available dc power capabilities and limitations associated with manually tested LRUs. It does not describe what test equipment is used for manually tested LRUs, cable setups for manual testing, or applicable test capabilities and limitations of the standard test equipment. This information, as applicable, is contained in the technical manual for each LRU that is manually tested using the FDF T/S group. These manuals are referenced in table 1-2.

WARNING

Do not connect more than two LRUs (the digital processor T/S and the LRU under test) to power junction box C5A6 at the same time. If more than two LRUs are connected simultaneously to power junction box C5A6, power supplies C5A9 and C5A10 can be overloaded. Overloading the power supplies can cause a fire or explosion that is harmful to personnel and can damage equipment.

Note

Whenever a user prompt appears on the VDT display during execution of any FDF T/S group software procedure, the digital processor T/S may be re-initialized. Reinitialization is accomplished by simultaneously pressing the VDT CTRL (control) and R keys on the VDT keyboard. Re-initialization invokes the digital processor T/S self-test routine. After execution of the digital processor T/S self-test routine, FDF T/S group software proceeds at the user's prompt to the main menu shown in figure 2-7. The user may then select the desired test procedure.

2.6.1 ARF Digital Processor

The following paragraphs provide a brief test description, a list of the test equipment required, and a typical test setup diagram for the ARF digital processor.

2.6.1.1 Test Description

The ARF digital processor (ADPU) computer-controlled test procedures can be selected from the main test menu (figure 2-7) by pressing VDT key A.

After selecting the ARF digital processor computer-controlled tests from the main menu, the ARF digital processor test menu is displayed, as shown in figure 2-8. One of three main types of tests may be selected from the ARF digital processor test menu. The three main types of tests are the ARF digital processor built-in test equipment (BITE) tests, the ARF digital processor CCA-level fault isolation test, and the individual CCA tests.

2.6.1.1.1 Operational BITE RAM Test

The operational BITE RAM test reads a memory location, complements the contents of that memory location, exclusive ORs the contents of the memory location with the original data, and complements the exclusive OR result. If the resultant value is zero, the memory location tested passes the test. The final (resultant value) contents of the memory location under test is complemented again to return the contents to the original state before the test began. The entire RAM is tested. A PASS/FAIL result is returned to the digital processor T/S for display on the VDT.

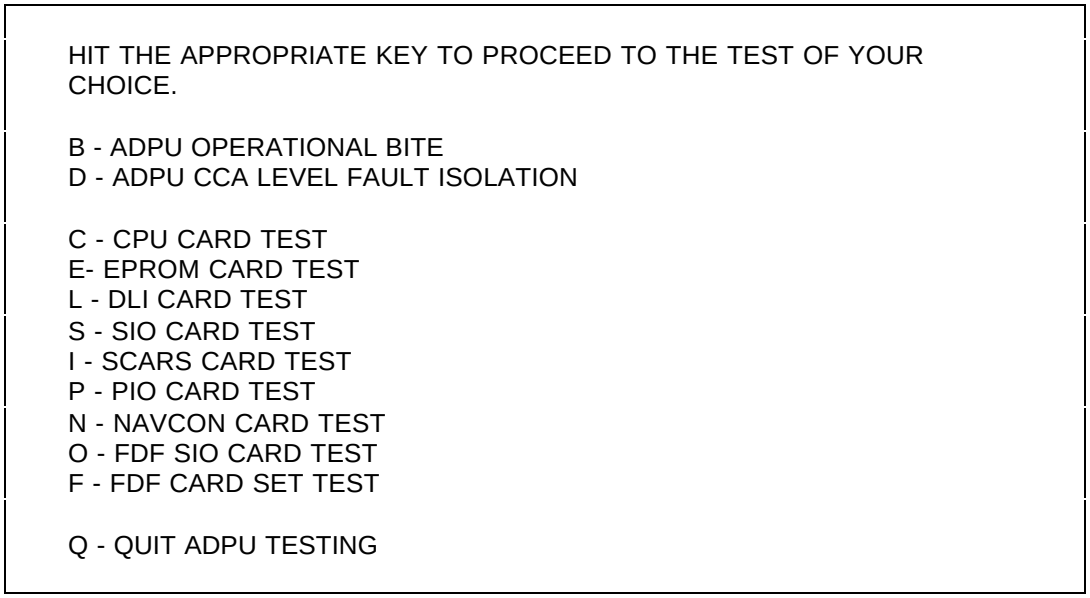

Figure 2-8. ARF Digital Processor Test Menu

2.6.1.1.2 Operational BITE MC68000 Instruction Set Test The operational BITE MC68000 instruction set test checks the operation of the MC68000 instruction set on each 68000 processor CCA. The PASS/FAIL test results are returned to the digital processor T/S for display on the VDT.

2.6.1.1.3 Operational BITE EPROM Test
The operational BITE EPROM test module contains a starting address and an ending address of the EPROM to be tested. The contents of the EPROM from the starting address to the ending address are summed and compared to a checksum value. The checksum value for each EPROM CCA is contained in address area EI0000 thru E10100 located on the first EPROM CCA in the ARF digital processor, and it is stored at the time data is written into the first ARF digital processor EPROM CCA. Address area E10000 thru El0100 also contains an ARF tail number and a catalog that maps where EPROM data is to be stored in ARF digital processor RAM.

If the sum of the EPROM CCA memory contents compares to the checksum stored in memory location E10000 thru El0100, the EPROM CCA passes the test. If the EPROM CCA under test is not present in the ARF digital processor, the test fails. A PASS/FAIL indication is transmitted to the digital processor T/S for display on the VDT.

2.6.1.1.4 Operational BITE Serial I/0 Interface Test

The digital processor T/S requests the ARF digital processor to execute the test (via the interconnected ACIA serial ports). In turn, the request causes an operational routine to be downloaded from ARF digital processor EPROM to ARF digital processor RAM. The operational routine is executed by processor CCA Al (CPU number 7) in the ARF digital processor. The routine performs interrupt, data loopback, and echo tests on the SIO interface CCA in the ARF digital processor.

The interrupt test checks for asserted internal CCA interrupts, which are generated by the input channel, and the two output channels, when they are full of data and also when they are unloaded.

The data loopback test selects the SIO interface CCAs internal data loopback test mode, which connects an output channel (first A, then B) to input channel C. A test data message of 216 bytes (the largest used, typically) is loaded into the output channel of the CCA and then transmitted to the input channel, where it is stored for processor retrieval and evaluation. If any of the expected interrupts are not received, or if returned data does not match transmitted data, the SIO interface CCA under test fails the loopback test. The PASS/FAIL results of the SIO interface CCA internal loopback test are recorded in ARF digital processor RAM and are later passed to the digital processor T/S.

It should be noted that since the CCAs internal loopback data path bypasses the drivers and receivers on the CCA, the drivers and receivers are not tested; all other functional devices within the CCA are tested.

However, to test the receivers and drivers, an echo test is performed by the digital processor T/S.

The echo test involves transmitting 216 bytes of data out the B channel transmitter on the digital processor T/S SIO interface CCA to the receiver input of the SIO interface CCA in the ARF digital processor under test. The 216 bytes of data are then routed through the SIO interface CCA receiver circuits to the ARF digital processor common CCA, via the common bus, during a common CCA read operation.

Next, the common CCA writes the same 216 bytes of data (just read) from the SIO interface CCA back to the same SIO interface CCA, via the common bus. The data written is then output via SIO interface CCA transmitter channel A or B, as appropriate to the test, to the receiver input of the digital processor T/S SIO interface CCA.

Then the digital processor T/S compares the data returned to the original data that was transmitted. If the transmitted and returned data disagrees, the ARF digital processor SIO interface CCA fails the echo test. The echo test is run continuously until the operator presses VDT key S. The echo test results are updated continually on the VDT display by the digital processor T/S.

2.6.1.1.5 Operational BITE SCAR Interface Test

The operational BITE SCAR interface CCA test checks interrupts, the receiver command channel, and the SCAR command channel. The test uses a loopback technique similar to the operational BITE SIO interface CCA test previously described. That is, an output channel is connected to an input channel before the drivers and after the receivers. Thus, the SCAR interface CCA drivers and receivers are not tested. If a driver or receiver is faulty, this test does not detect the fault.

The length of the test data sent through the receiver command channel is 56 bits. The length of the data sent through the SCAR command channel is 8 bits. Since the SCAR interface CCA incorporates a pipelined structure, the test must be performed twice. The first time, the test data is entered into the pipeline; the second time, the test of the CCA circuits is performed. If the transmitted data does not compare to the received data, the CCA fails the test. The PASS/FAIL test results are stored in ARF digital processor RAM and are then passed to the digital processor T/S for display on the VDT.

2.6.1.1.6 Operational BITE NA VCON Interface Test
The NAVCON interface CCA test configures the NAVCON CCA into internal self-test mode. The NAVCON self-test performs several tests, consisting of an internal memory test, an external memory test, a serial loop test, and a parallel loop test. If any of the tests fail, the NAVCON CCA is considered to have failed the operational BITE test. A PASS/FAIL result is returned to the ARF digital processor RAM and is then transmitted to the digital processor T/S for subsequent display on the VDT.

2.6.1.1.7 Individual CCA Tests
The ARF digital processor individual CCA tests consist of software test routines that are independently selected by pressing one of the following VDT keys shown in figure 2-8: C, E, L, S, I, P, N, O, or F. Depending on the VDT key pressed, a particular test routine is downloaded from the EPROM in the digital processor T/S to RAM in the ARF digital processor. Each test routine comprises typically 42 blocks of data, and downloading requires approximately 5 minutes.

After downloading is completed, processor CCA Al in the ARF digital processor (CPU number 7, or the highest number processor as determined by the bus arbitration logic) executes the CCA test routine that was downloaded. The test routine includes any special FDF T/S group test setup instructions for, or manual measurements to be performed on, the CCA under test. Required test setup and manual measurement instructions are indicated in the VDT test screens.

Upon completion of the selected ARF digital processor CCA test, a CCA PASS/FAIL condition is passed to the digital processor T/S for display on the VDT.

2.6.1.1.8 CCA-Level Fault Isolation Test
The ARF digital processor CCA-level fault isolation test executes all of the individual ARF digital processor CCA tests listed at the bottom of the display shown in figure 2-8. Test routines for the individual CCAs are downloaded from digital processor T/S EPROM and executed by processor CCA A1 (CPU number 7) in the ARF digital processor.

The order of CCA testing is not necessarily performed in the same order as the listing of CCA tests presented in the menu shown in figure 2-8. Rather, the order of CCA testing is determined by the results obtained and is analyzed by the processor CCA in the digital processor T/S. That is, the digital processor T/S controls the tests and determines the next CCA to be tested by analyzing the results of the previous tests.

While the digital processor T/S controls and analyzes the tests, processor CCA Al in the ARF digital processor actually executes the tests on the CCAs. Test screens on the FDF T/S VDT instruct the user when a test setup is to be changed and what manual measurements are to be taken.

The results of the ARF digital processor CCA-level fault isolation test are displayed on the VDT, along with corrective action to be performed by the user.

2.6.1.2 Test Equipment Used
The following test equipment is used to perform the LRU performance and module-level tests on the ARF digital processor:

1. Video display terminal C4A4
2. Oscilloscope C3A2
3. Function generator C4A1
4. Logic analyzer C4A3

5. DMM C5A1
6. Power junction box C5A6
7. Power supply C5A9
8. Digital processor T/S C5A4
9. Precision RF cable set (HP 11851 B)
10. Power splitter (HP 11850A)
11. Logic analyzer lead set
12. Digital processor extender card (P/N 10-160160-1) (used for NAVCON CCA test)
13. FDF T/S group power cable kit (ESL 21-164447-1)
14. FDF T/S group test signals cable kit (ESL 21-164448-1)

2.6.1.3 Typical Test Setup
Figure 2-9 shows a typical test setup diagram for the ARF digital processor. Refer to ARF digital processor performance test and troubleshooting procedures in TM 11-5865-268-13 for the actual test setup and instructions to be followed.

2.6.2 SCAR Processor Level 0
The following paragraphs provide a brief test description, a list of test equipment used, and a typical test setup diagram for SCAR processor level 0.

2.6.2.1 Test Description
The SCAR processor level 0 computer-controlled test procedure can be selected by pressing VDT key 0 when the FDF T/S group main menu (figure 2-7) is displayed. Pressing VDT key 0 causes the SCAR processor level 0 test menu to be displayed. The SCAR processor level 0 test menu provides the test operator with a choice of either performance testing or aligning the LRU. The following subparagraphs describe the LRU test and the LRU alignment.

2.6.2.1.1 SCAR Processor Level 0 Test
The SCAR processor level 0 test is an LRU-level test that performs measurements on test reference signals and compares the results of the measurements to established test parameters. The test performs measurements on the 20 spectral measurement channels within the SCAR processor level 0.

The 20 signals analyzed by the SCAR processor level 0 are provided from the FDF T/S group signal generator and function generator. The function generator modulates the signal generator signal as required by the LRU test . Both the signal generator outputs and the function generator outputs are set automatically by the FDF T/S group software executed by the digital processor T/S.

The digital processor T/S sends one serial byte to the SCAR processor level 0 to set up the various LRU parameters (such as dwell time) for testing. After testing is completed, the SCAR processor level 0 serially transmits the test response caused by the signal generator input and the digital processor T/S control byte back to the digital processor T/S. The test response consists of twenty 16-bit words.

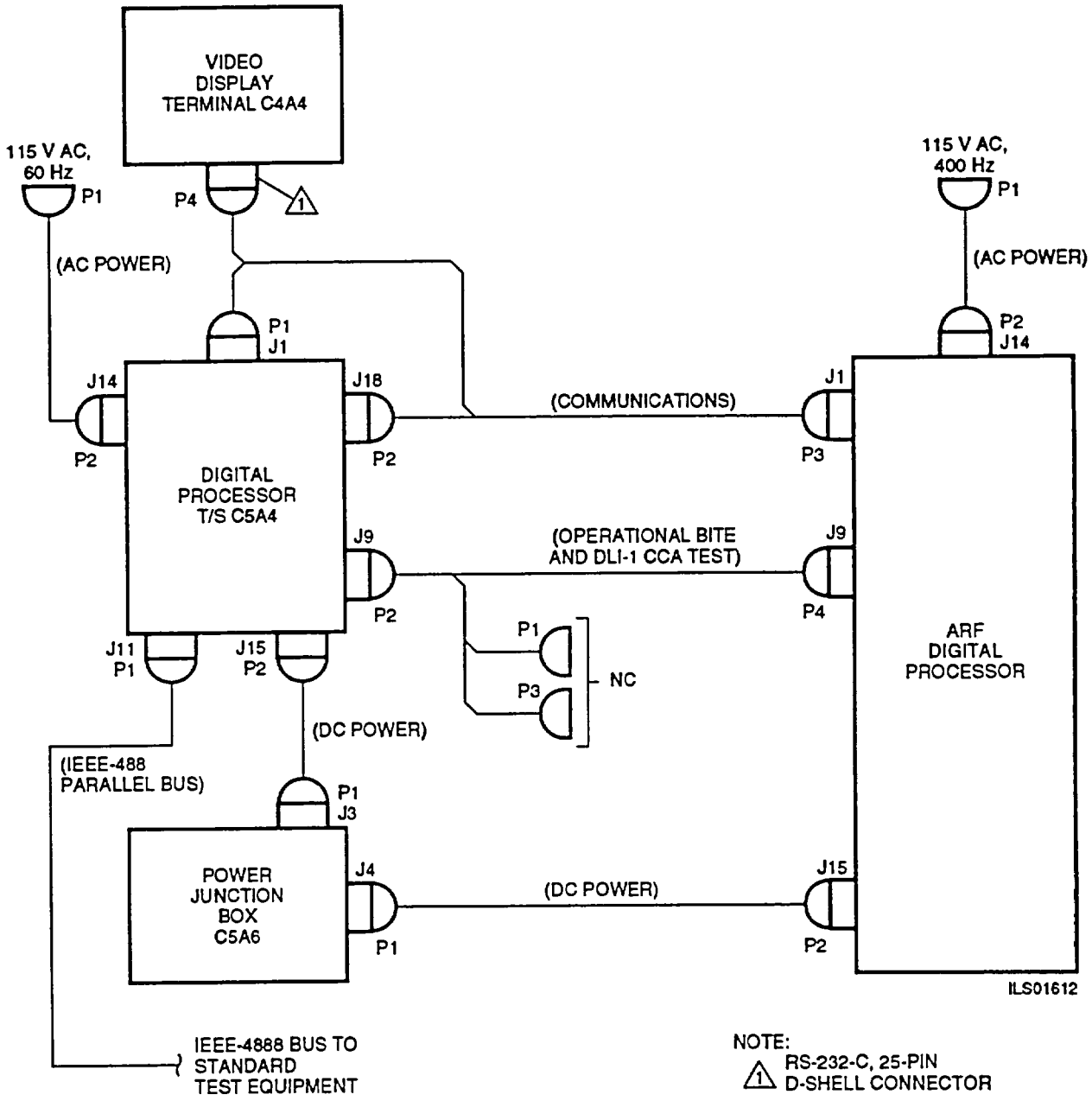

Figure 2-9. Typical ARF Digital Processor Test Setup

The digital processor T/S analyzes the SCAR processor level 0 16-bit word responses. If any of the measurements is not within the established test parameters, then that measurement fails. The results of the SCAR processor level 0 test and any failed measurements are displayed on the VDT.

Troubleshooting (fault isolation) can be initiated following the SCAR processor level 0 LRU test.

Troubleshooting requires manual probing of the chassis to isolate the fault to the CCA level.

2.6.2.1.2 SCAR Processor Level 0 Alignment
Since misalignment of the SCAR processor level 0 may cause failures during LRU testing, the alignment procedure is to be performed prior to LRU performance testing. During the alignment procedure, the FDF T/S group software controls alignment setup and signal generation. However, manual probing of the chassis and adjustment of CCA components are required during the alignment process.

The SCAR processor level 0 alignment procedure involves checking of source voltages, setting of multiplexer selection, alignment of the analog-to-digital converter, alignment of the downconverter, alignment of spectrum analyzer filter channels, alignment of integrators, and alignment of detectors.

2.6.2.2 Test Equipment Used The following test equipment is used to perform the LRU performance and CCA-level tests on the SCAR processor level 0:

1. Video display terminal C4A4
2. Spectrum analyzer C2A1
3. Function generator C4A1
4. Signal generator C4A2
5. DMM C5A1
6. Power junction box C5A6
7. Power supplies C5A9 and C5A10
8. Digital processor T/S C5A4
9. FDF T/S group power cable kit (ESL 21-164447-1)
10. FDF T/S group test signals cable kit (ESL 21-164448-1)

2.6.2.3 Typical Test Setup
Figure 2-10 is a typical test setup for the SCAR processor level 0 LRU test. Refer to SCAR processor level 0 performance test and troubleshooting procedures in TM 11-5865-246-13 for the actual test setup and instructions to be followed.

2.6.3 SCAR Processor Level 1 The following paragraphs provide a brief test description, a list of the test equipment used, and a typical test setup diagram for the SCAR processor level 1.

2.6.3.1 Test Description
The SCAR processor level 1 computer-controlled test procedure can be selected by pressing VDT key 1 when the FDF T/S group main menu (figure 2-7) is displayed. Pressing VDT key 1 causes the SCAR

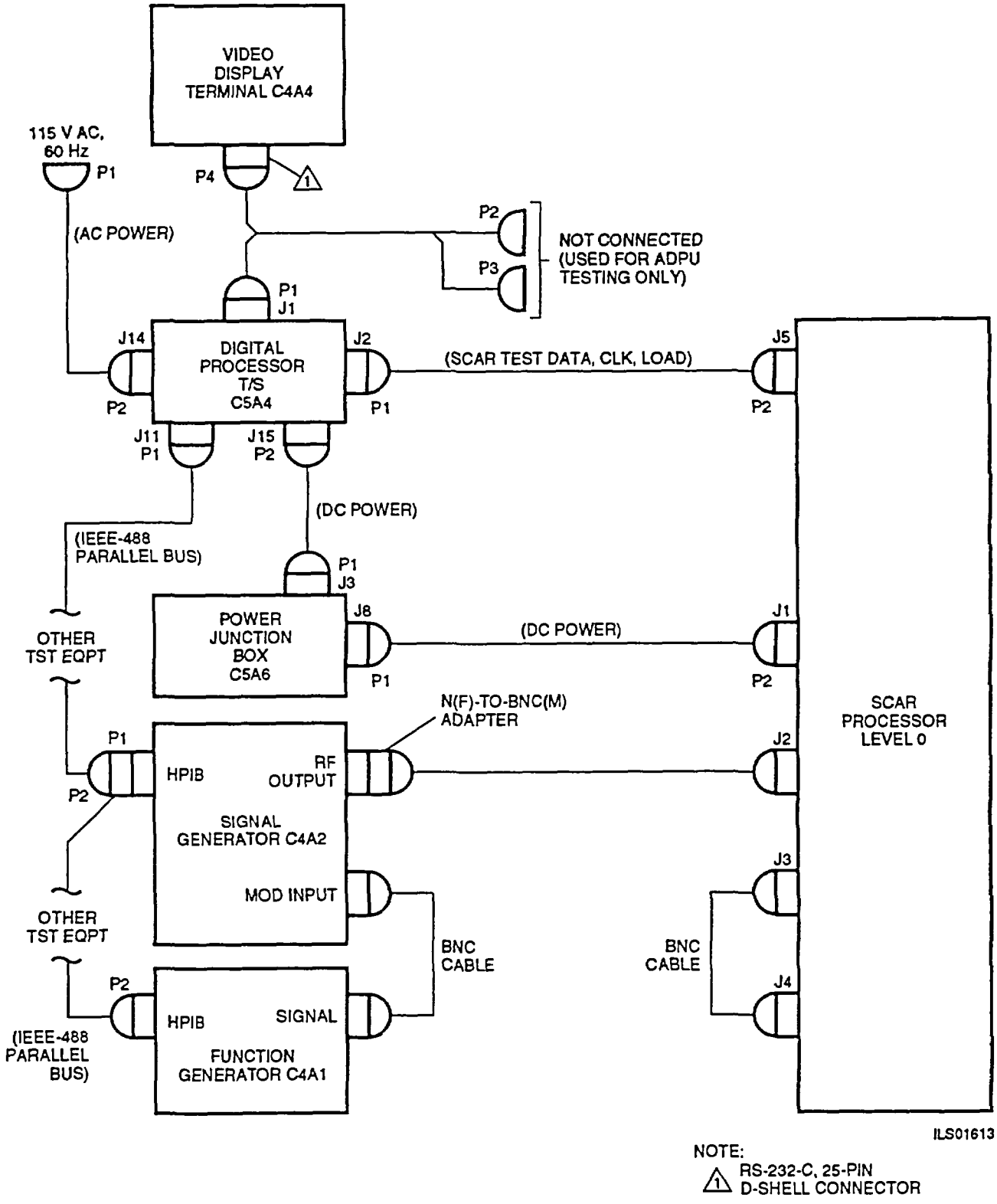

Figure 2-10. Typical SCAR Processor Level 0 Test Setup

processor level 1 test menu to be displayed. The SCAR processor level 1 test menu provides the test operator with a choice of either performance testing or aligning the LRU. The following subparagraphs describe the LRU test and the LRU alignment.

2.6.3.1.1 SCAR Processor Level I Test

The SCAR processor level 1 test is an LRU-level test that performs measurements on test reference signals and compares the results of the measurements to established test parameters. The test performs SCAR measurements on 34 different test signals. Each test signal exercises one of 20 spectral measurement channels within the SCAR processor level 1 or one of 14 waveform measurements generated by the SCAR processor level 1. The test also checks out the BITE circuit within the LRU.

The signals analyzed by the SCAR processor level 1 are provided from signal generator C4A2 and function generator C4A1. The function generator modulates the signal generator signal as required by the LRU test. Both the signal generator outputs and the function generator outputs are set automatically by the FDF T/S group software executed by the digital processor T/S.

The digital processor T/S sends one serial byte to the SCAR processor level 1 to set up the various LRU parameters (such as dwell time) for testing. After testing is completed, the SCAR processor level 1 serially transmits the test response caused by the signal generator input and the digital processor T/S control byte back to the digital processor T/S. The test response consists of sixty-four 16-bit words.

The digital processor T/S analyzes the SCAR processor level 1 16-bit word responses. If any of the measurements is not within the established test parameters, then that measurement fails. The results of the SCAR processor level 1 test and any failed measurements are displayed on the VDT.

Troubleshooting (fault isolation) can be initiated following the SCAR processor level 1 LRU test. Troubleshooting requires manual probing of the chassis to isolate the fault to the CCA level.

2.6.3.1.2 SCAR Processor Level 1 Alignment

Since misalignment of the SCAR processor level 1 may cause failures during LRU testing, the alignment procedure is to be performed prior to LRU performance testing. During the alignment procedure, the FDF T/S group software controls alignment setup and signal generation. However, manual probing of the chassis and adjustment of CCA components are required during the alignment process.

The SCAR processor level 1 alignment procedure involves checking of source voltages, setting of multiplexer selection, alignment of the source control, alignment of spectrum analyzer filter channels, alignment of integrators, and alignment of detectors.

2.6.3.2 Test Equipment Used

The following test equipment is used to perform the LRU performance and CCA-level tests on the SCAR processor level 1:

1. Video display terminal C4A4
2. Spectrum analyzer C2A1
3. Function generator C4A1
4. Signal generator C4A2
5. DMM C5A1
6. Power junction box C5A6

7. Power supplies C5A9 and C5A10

8. Digital processor T/S C5A4

9. FDF T/S group power cable kit (ESL 21-164447-1)

10. FDF T/S group test signals cable kit (ESL 21-164448-1)

2.6.3.3 Typical Test Setup

Figure 2-11 is a typical test setup for the SCAR processor level 1 LRU test. Refer to SCAR processor level 1 performance test and troubleshooting procedures in TM 11-5865-245-13 for the actual test setup and instructions to be followed.

2.6.4 SCAR Processor Level 2

The following paragraphs provide a brief test description, a list of the test equipment used, and a typical test setup diagram for the SCAR processor level 2.

2.6.4.1 Test Description

The SCAR processor level 2 computer-controlled test procedure can be selected by pressing VDT key 2 when the FDF T/S group main menu (figure 2-7) is displayed. Pressing VDT key 2 causes the SCAR processor level 2 test menu to be displayed. The SCAR processor level 2 test menu provides the test operator with a choice of either performance testing or aligning the LRU. The following subparagraphs describe the LRU test and the LRU alignment.

2.6.4.1.1 SCAR Processor Level 2 Test

The SCAR processor level 2 test is an LRU-level test that performs measurements on test reference signals and compares the results of the measurements to established test parameters. The test performs SCAR measurements on 32 different test signals. Each test signal exercises one of 20 spectral measurement channels within the SCAR processor level 2 or one of 12 waveform measurements generated by the SCAR processor level 2.

The signals analyzed by the SCAR processor level 2 are provided from signal generator C4A2 and function generator C4A 1. The function generator modulates the signal generator signal as required by the LRU test. Both the signal generator outputs and the function generator outputs are set automatically by the FDF T/S group software executed by the digital processor T/S.

The digital processor T/S sends one serial byte to the SCAR processor level 2 to set up the various LRU parameters (such as dwell time) for testing. After testing is completed, the SCAR processor level 2 serially transmits the test response caused by the signal generator input and the digital processor T/S control byte back to the digital processor T/S. The test response consists of sixty-four 16-bit words.

The digital processor T/S analyzes the SCAR processor level 2 16-bit word responses. If any of the measurements is not within the established test parameters, then that measurement fails. The results of the SCAR processor level 2 test and any failed measurements are displayed on the VDT.

Troubleshooting (fault isolation) can be initiated following the SCAR processor level 2 LRU test. Troubleshooting requires manual probing of the chassis to isolate the fault to the CCA level.

2.6.4.1.2 SCAR Processor Level 2 Alignment

Since misalignment of the SCAR processor level 2 may cause failures during LRU testing, the alignment procedure is to be performed prior to LRU performance testing. During the alignment procedure, the FDF T/S group software controls alignment setup and signal generation. However, manual probing of the chassis and adjustment of CCA components are required during the alignment process.

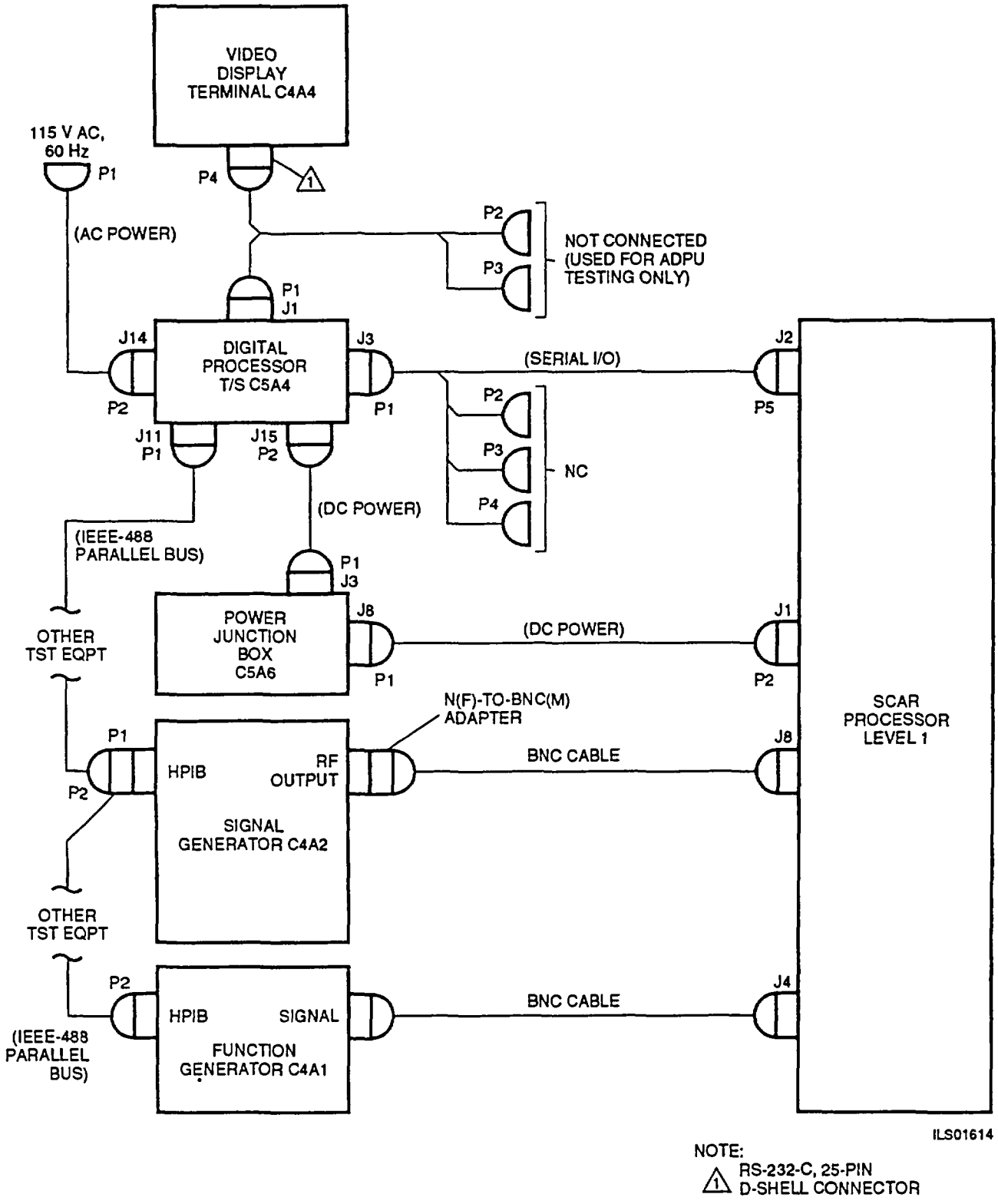

Figure 2-11. Typical SCAR Processor Level 1 Test Setup

The SCAR processor level 2 alignment procedure involves checking of source voltages, setting of multiplexer selection, alignment of the analog-to-digital converter, alignment of the histogram, alignment of spectrum analyzer filter channels, alignment of integrators, and alignment of detectors.

2.6.4.2 Test Equipment Used

The following test equipment is used to perform the LRU performance and CCA-level tests on the SCAR processor level 2:

1. Video display terminal C4A4
2. Spectrum analyzer C2A1
3. Function generator C4A1
4. Signal generator C4A2
5. DMM C5A1
6. Power junction box C5A6
7. Power supplies C5A9 and C5A10
8. Digital processor T/S C5A4
9. FDF T/S group power cable kit (ESL 21-164447-1)
10. FDF T/S group test signals cable kit (ESL 21-164448-1)

2.6.4.3 Typical Test Setup

Figure 2-12 is a typical test setup for the SCAR processor level 2 LRU test. Refer to SCAR processor level 2 performance test and troubleshooting procedures in TM 11-5865-238-13 for the actual test setup and instructions to be followed.

2.6.5 RF Processor

The following paragraphs provide a brief test description, a list of the test equipment used, and a typical test setup diagram for the RF processor.

Note

The test procedures displayed on the VDT refer to the RF processor electronic component assemblies (ECAs) as modules. In the following test description, module is used in place of ECA so the descriptive text agrees with the VDT displays.

2.6.5.1 Test Description

The RF processor computer-controlled test procedure can be selected by pressing VDT key R when the VDT displays the FDF T/S group main menu (figure 2-7). The RF processor tests provided include an overall LRU performance test and a module-level test. The LRU performance test measures insertion loss through the RF processor, channel-to-channel phase tracking, and the BITE oscillator output spectrum.

VHF/UHF channel-to-channel phase tracking and insertion losses in RF paths, from the RF processor's eight VHF inputs and eight UHF inputs through to the two LRU outputs, are measured using network analyzer C2A2, the power splitter, and the precision RF cable set. Printer C3A3 is used to generate network analyzer screen hard copies of the phase tracking for each RF processor channel with respect to

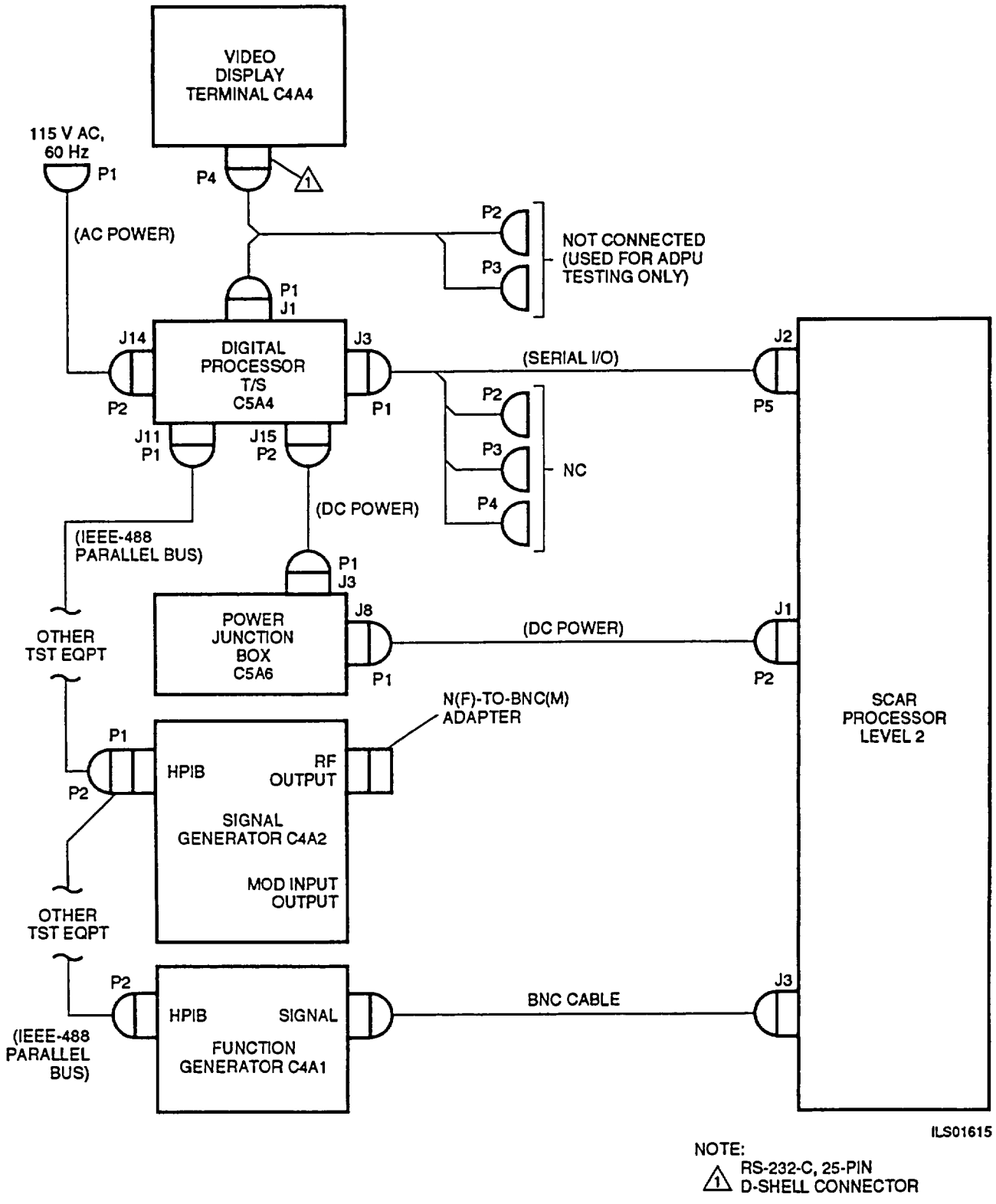

Figure 2-12. Typical SCAR Processor Level 2 Test Setup

the other channels. Spectrum analyzer C2A1 is used to monitor the BITE oscillator output frequency spectrum.

The digital processor T/S generates the necessary command word bit configurations needed to control RF processor operation during the LRU performance test. More specifically, the digital processor T/S commands control the BITE oscillator and the switching circuits that route the network analyzer's RF output signal through the RF processor's internal signal paths.

When the LRU performance test detects a fault, the operator uses the module-level test to locate the defect. The module-level test consists of individual procedures that isolate the RF processor fault to a replaceable module. The module-level procedures use DMM C5A1 to measure voltages and the network analyzer and transmission/reflection test set to measure insertion loss and return loss of the RF processor's internal subassemblies.

The RF processor LRU-or module-level test can be selected only when the RF processor test menu is displayed on the VDT. At that time, pressing VDT key L causes the FDF T/S group software to branch to the LRU test procedure, while pressing VDT key M causes the software to branch to the module-level test procedure.

Note

The RF processor computer-controlled LRU and module-level tests are not designed to isolate faulty RF cables.

2.6.5.2 Test Equipment Used

The following test equipment is used to perform the LRU performance and module-level tests on the RF processor:

1. Network analyzer C2A2
2. Video display terminal C4A4
3. Spectrum analyzer C2A1
4. DMM CSA1
5. Power junction box C5A6
6. Power supplies C5A9 and C5A10
7. Digital processor T/S C5A4
8. Transmission/reflection test set (HP 85044A)
9. Power splitter (HP 11850A)
10. Precision RF cable set (HP 11851A)
11. FDF T/S group power cable kit (ESL 21-164447-1)
12. FDF T/S group test signals cable kit (ESL 21-164448-1)

2.6.5.3 Typical Test Setup

Figure 2-13 is a typical test setup for the RF processor LRU test. Refer to RF processor performance test and troubleshooting procedures in TM 11-5865-236-13 for the actual test setup and instructions to be followed.

2.6.6 R-2270 Receiver

The following paragraphs provide a brief test description, a list of the test equipment used, and a typical test setup diagram for the R-2270 receiver.

Note

The test procedures displayed on the VDT refer to the R-2270 receiver ECAs as modules. In the following test description, module is used in place of ECA so the descriptive text agrees with the VDT displays.

2.6.6.1 Test Description

R-2270 receiver computer-controlled test procedures can be selected by pressing VDT key D when the VDT displays the FDF T/S group main menu (figure 2-7). The procedures consist of an LRU-level test and module-level tests. The module-level tests are directed by the results of the LRU test.

The LRU test checks the frequency and power level of the channel A and B spectral display unit (SDU) outputs and the frequency and power level of the channel A and B third IF outputs while varying the IF bandwidth, input signal frequency, and power level.

If the R-2270 receiver passes the computer-controlled and -directed portion of the LRU performance test, the operator can decide either to repeat that portion or to continue the remaining LRU tests, which are operator-directed instead of computer-directed. The computer-controlled/operator-directed type of testing is also termed the manual mode of testing. For the R-2270 receiver, the manual mode of testing is entered by selecting option U (RCU simulator) from the FDF T/S group main menu (figure 2-7). In RCU simulator mode, the VDT is used to set up various receiver parameters for additional performance testing.

On the other hand, if the R-2270 receiver fails the computer-controlled and -directed portion of the LRU test, the user can decide either to repeat the LRU test or to proceed to the module-level tests. The module-level tests consist of a series of manual measurements performed by the operator to isolate the R-2270 receiver fault to a particular module. The manual measurements are performed while the digital processor T/S controls R-2270 receiver operation. The digital processor T/S also controls the signal generator output frequency and power levels applied to the R-2270 receiver for many of the module level tests.

Note

The R-2270 receiver computer-controlled LRU- and module-level tests are not designed to isolate faulty RF cables.

2.6.6.2 Test Equipment Used

The following test equipment is used to perform the LRU performance and module-level tests on the R-2270 receiver:

1. Video display terminal C4A4
2. Universal counter C3A1

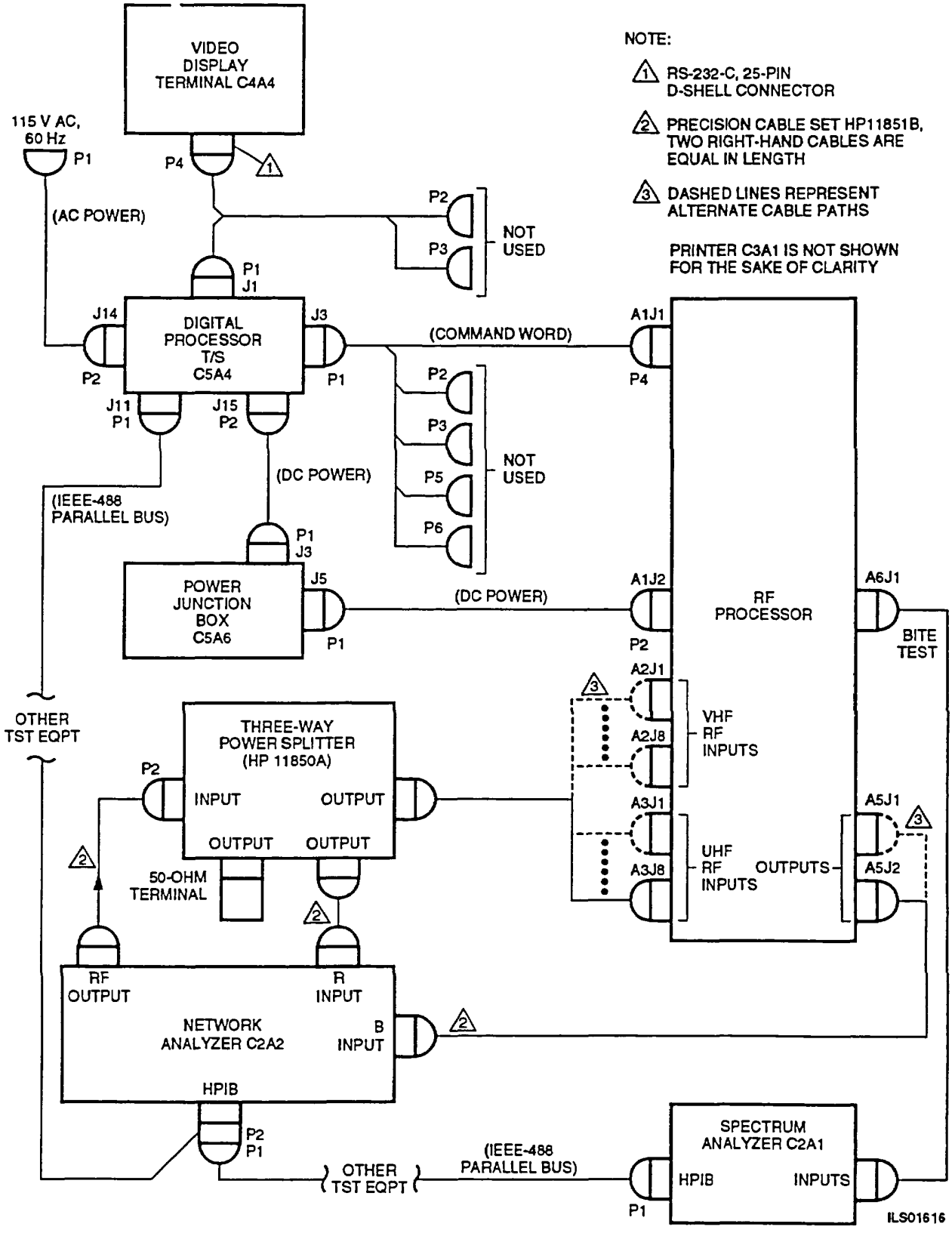

Figure 2-13. Typical RF Processor Test Setup

3. Oscilloscope C3A2
4. Spectrum analyzer C2A1
5. Signal generator C4A2
6. DMM C5A1
7. Power junction box C5A6
8. Power supplies C5A9 and C5A10
9. Digital processor T/S C5A4
10. Variable power supply (HP 6291A) (This item is not part of the FDF T/S group but is specified in the R-2270 receiver performance test procedure in TM 11-5821-321-13.)
11. FDF T/S group power cable kit (ESL 21-164447-1)
12. FDF T/S group test signals cable kit (ESL 21-164448-1)

2.6.6.3 Typical Test Setup

Figure 2-14 is a typical test setup for the R-2270 receiver LRU test. Refer to R-2270 receiver performance test procedures in TM 11-5821-321-13 for the actual test setup and instructions to be followed.

2.6.7 R-2289 Receiver

The following paragraphs provide a brief test description, a list of the test equipment used, and a typical test setup diagram for the R-2289 receiver.

Note

The test procedures displayed on the VDT refer to the R-2289 receiver ECAs as modules. In the following test description, module is used in place of ECA so the descriptive text agrees with the VDT displays.

2.6.7.1 Test Description

R-2289 receiver computer-controlled test procedures can be selected by pressing VDT key S when the VDT displays the FDF T/S group main menu (figure 2-7). The R-2289 receiver test procedures consist of an LRU-level test and module-level tests. The module-level tests are directed by the results of the LRU test.

The LRU test checks the frequency and power level of the SDU output and the frequency and power level of the second IF output while varying the IF bandwidth, the input signal frequency, and the power level. After checking the second IF and SDU outputs, the LRU test verifies proper operation of upper and lower sideband filtering for single sideband (SSB) operation. After checking SSB modes, the test continues by applying frequency modulated (FM) and then amplitude modulated (AM) RF inputs to the receiver FM and AM detection circuits, respectively. The operator is directed to monitor the receiver AUDIO output to verify proper operation.

If the R-2289 receiver passes the computer-controlled and -directed portion (LRU testing) of the performance test, the operator can elect either to repeat that portion or to proceed to the computer controlled and operator-directed manual mode of testing. The manual mode of testing is entered by selecting option U (RCU simulator) from the FDF T/S group main menu (figure 2-7).

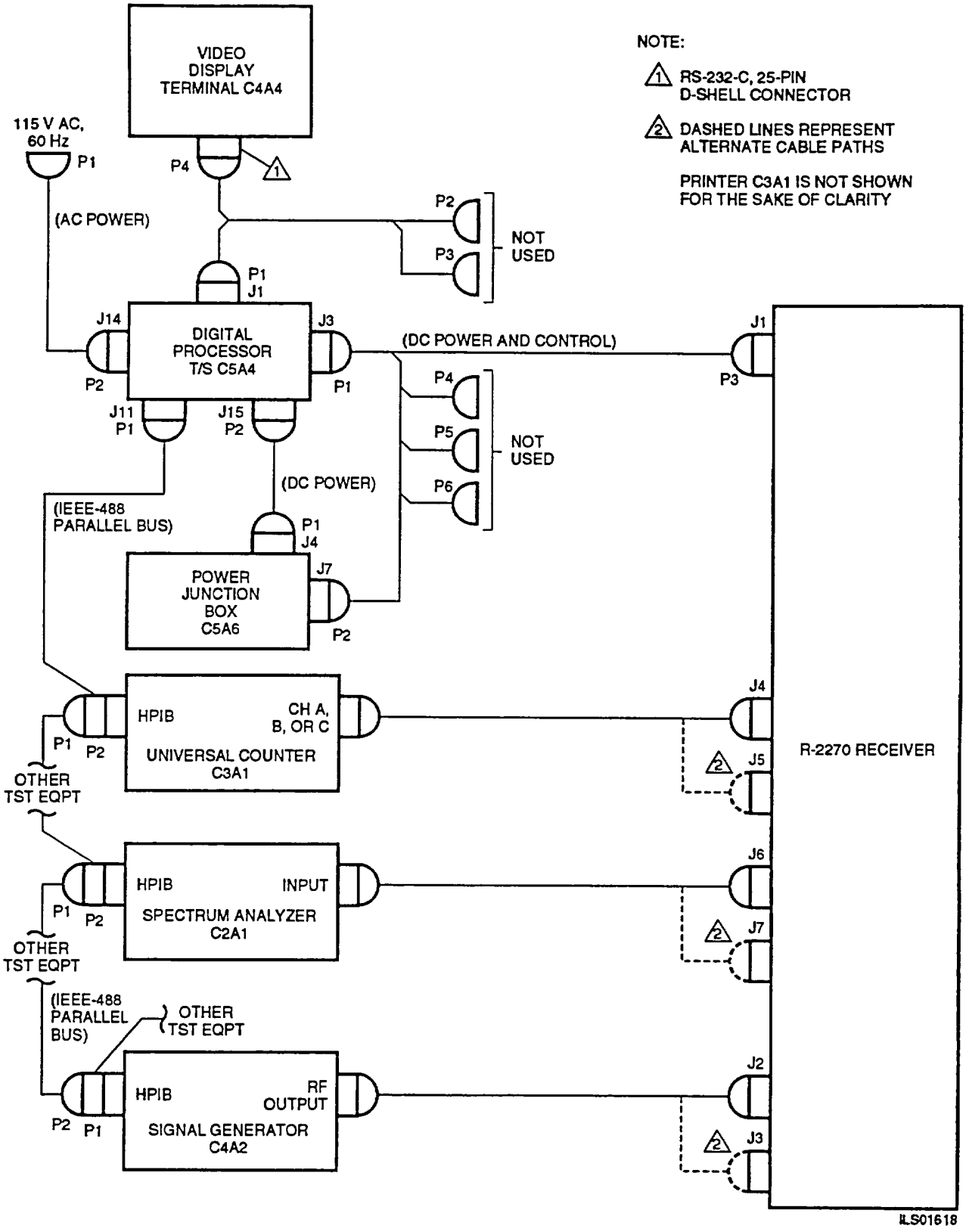

Figure 2-14. Typical R-2270 Receiver Test Setup

In the RCU simulator mode, the VDT is used to set up various R-2289 receiver parameters for additional performance testing. If the R-2289 receiver passes the LRU test, the user can decide either to repeat the LRU test or to return to the FDF T/S group main menu.

If the R-2289 receiver fails the LRU test, the user may either repeat the LRU test or proceed to the module-level tests. The module-level tests consist of a series of manual measurements performed by the operator to isolate the R-2289 receiver fault to a particular module. The digital processor T/S controls R-2289 receiver operation during the manual measurements. The digital processor T/S also controls the signal generator output frequency and power levels applied to the R-2289 receiver for many of the module-level tests and certain other test equipment functions.

Note

The R-2289 receiver computer-controlled LRU-and module-level tests are not designed to isolate faulty RF cables.

2.6.7.2 Test Equipment Used

The following test equipment is used to perform the LRU performance and module-level tests on the R-2289 receiver:

1. Video display terminal C4A4
2. Universal counter C3A1
3. Oscilloscope C3A2
4. Spectrum analyzer C2A1
5. Signal generator C4A2
6. DMM C5A1
7. Power junction box C5A6
8. Power supplies C5A9 and C5A10
9. Digital processor T/S C5A4
10. Variable power supply (HP 6291A) (This item is not part of the FDF T/S group but is specified in the R-2289 receiver performance test procedure in TM 11-5821-327-13.)
11. FDF T/S group power cable kit (ESL 21-164447-1)
12. FDF T/S group test signals cable kit (ESL 21-164448-1)

2.6.7.3 Typical Test Setup

Figure 2-15 is a typical test setup for the R-2289 receiver LRU test. Refer to R-2289 receiver performance test procedures in TM 11-5821-327-13 for the actual test setup and instructions to be followed.

2.6.8 WJ-8604 Receiver

The following paragraphs provide a brief test description, a list of the test equipment used, and a typical test setup diagram for the WJ-8604 receiver. The WJ-8604 receiver test procedure provides only an overall LRU test, since the WJ-8604 receiver is not a field-repairable unit. Typically, this test is

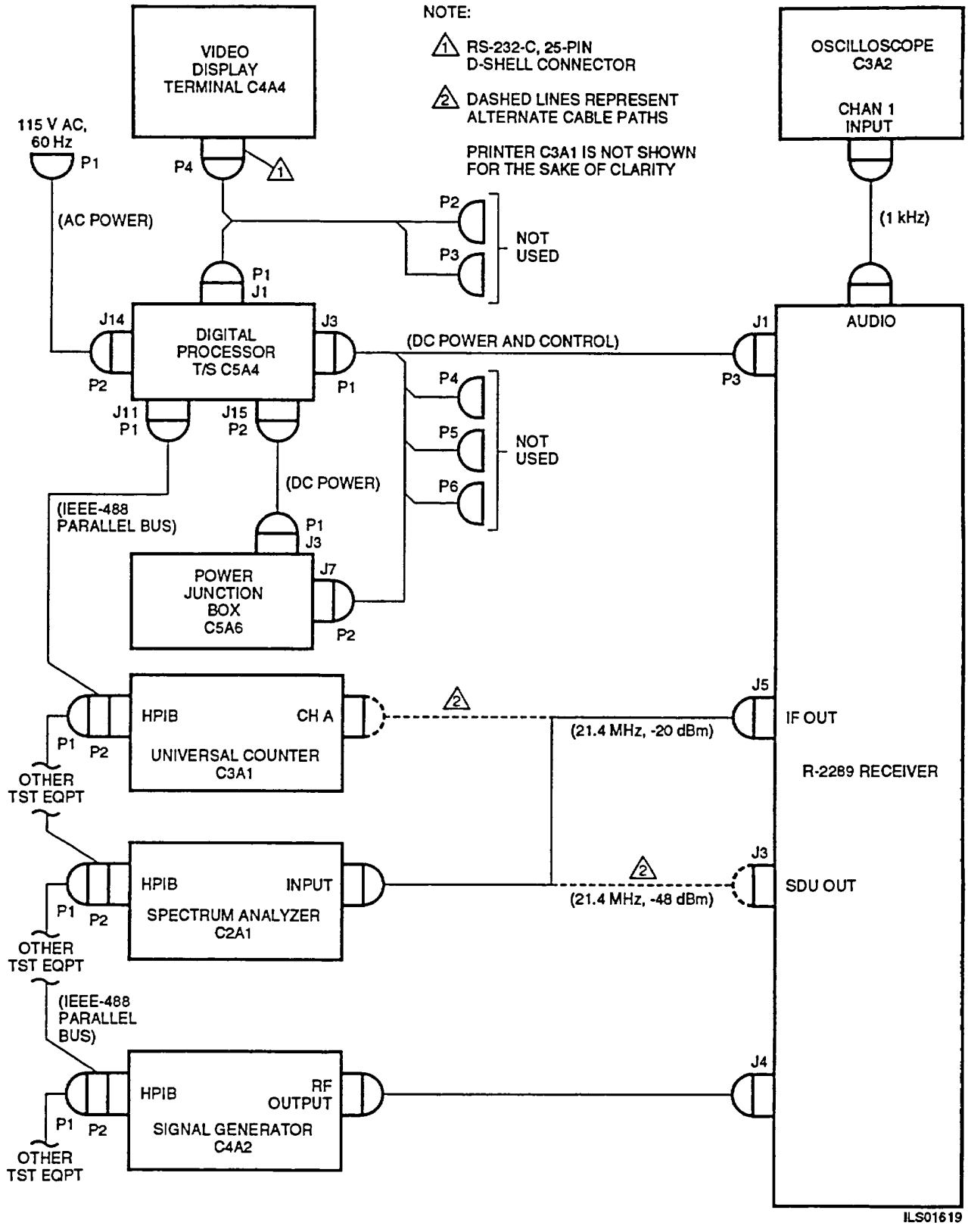

Figure 2-15. Typical R-2289 Receiver Test Setup

performed to verify failures discovered during unit maintenance of an ARF subsystem and to fault locate defective circuits inside the assembly that require depot repair.

Note

The test procedures displayed on the VDT refer to the WJ-8604 receiver ECAs as modules. In the following test description, module is used in place of ECA so the descriptive text agrees with the VDT displays.

2.6.8.1 Test Description

WJ-8604 receiver computer-controlled test procedures can be selected by pressing VDT key V when the VDT displays the FDF T/S group main menu (figure 2-7). The WJ-8604 receiver test procedures consist of an LRU-level test and module-level tests. The module-level tests are directed by the results of the LRU test.

The LRU test checks the frequency and power level of the SDU output and the frequency and power level of the second IF output while varying the IF bandwidth, the input signal frequency, and the power level. After checking the second IF and SDU outputs, the LRU test verifies proper operation of upper and lower sideband filtering for SSB operation. After checking SSB modes, the test continues by applying FM and then AM RF inputs to the receiver FM and AM detection circuits, respectively. The operator is directed to monitor the receiver AUDIO output to verify proper operation.

The digital processor T/S controls WJ-8604 receiver operation during the measurements and also controls test equipment functions, such as the signal generator output frequency and power levels applied to the WJ-8604 receiver for the various tests.

If the WJ-8604 receiver passes the computer-controlled and -directed portion (LRU testing) of the performance test, the operator can elect either to repeat that portion or to proceed to the computer controlled and operator-directed manual mode of testing. The manual mode of testing is entered by selecting option U (RCU simulator) from the FDF T/S group main menu (figure 2-7).

In the RCU simulator mode, the VDT is used to set up various WJ-8604 receiver parameters for additional performance testing. After the WJ-8604 receiver LRU test is completed, the user can decide either to repeat the LRU test or to return to the FDF T/S group main menu.

If the WJ-8604 receiver fails the LRU test, the user may either repeat the LRU test or proceed to the module-level tests. The module-level tests consist of a series of manual measurements performed by the operator to isolate the WJ-8604 receiver fault to a particular module.

Note

The WJ-8604 receiver computer-controlled LRU-and module-level tests are not designed to isolate faulty RF cables.

2.6.8.2 Test Equipment Used

The following test equipment is used to perform the LRU performance and module-level tests on the WJ-8604 receiver:

1. Video display terminal C4A4
2. Universal counter C3A1
3. Oscilloscope C3A2

4. Spectrum analyzer C2A1
5. Signal generator C4A2
6. DMM C5A1
7. Power junction box C5A6
8. Power supplies C5A9 and C5A10
9. Digital processor T/S C5A4
10. ARF intercept receiver pallet C5A3
11. Variable power supply (HP 6291A) (This item is not part of the FDF T/S group but is specified in the WJ-8604 receiver performance test procedure in TM 11-5821-352-13 (ARF subsystem manual).)
12. FDF T/S group power cable kit (ESL 21-164447-1)
13. FDF T/S group test signals cable kit (ESL 21-164448-1)

2.6.8.3 Typical Test Setup

Figure 2-16 is a typical test setup for the WJ-8604 receiver LRU test. Refer to the WJ-8604 receiver troubleshooting procedure in TM 11-5821-352-13 (ARF subsystem manual) for the actual test setup and instructions to be followed.

WARNING

Do not connect more than two LRUs (the digital processor T/S and the LRU under test) to power junction box C5A6 at the same time. If more than two LRUs are connected simultaneously to power junction box C5A6, power supplies C5A9 and C5A10 can be overloaded. Overloading the power supplies can cause a fire or explosion that is harmful to personnel and can damage equipment.

2.6.9 Manually Tested LRUs Powered by FDF T/S Group

A number of other system LRUs derive de power from the FDF T/S group power supplies for test purposes. The LRUs receive the required de power by connecting to power junction box C5A6. The LRUs are not tested under control of the FDF T/S group software and do not connect to the digital processor T/S. Some of the standard test equipment items included in the FDF T/S group may be used during testing of the LRUs that are powered by the FDF T/S group power supplies.

Table 1-2 lists the LRUs that are connected to power junction box C5A6 to receive de power during test but are not tested under computer control by the FDF T/S group. Refer to the TM number given in table 1-2 for the test description and associated test setup diagrams for each LRU not tested automatically on the FDF T/S group equipment.

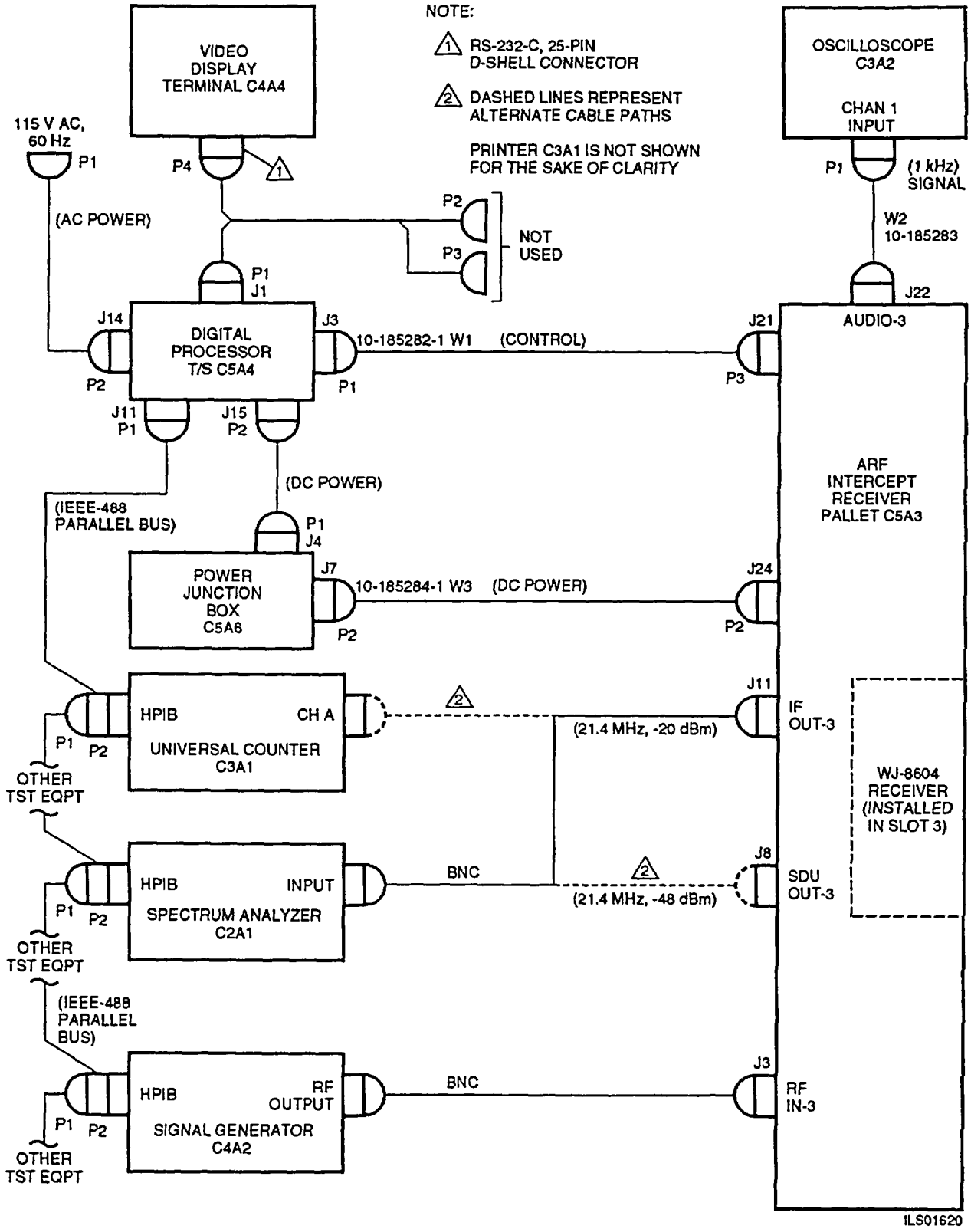

Figure 2-16. Typical WJ-8604 Receiver Test Setup

CHAPTER 3

UNIT MAINTENANCE INSTRUCTIONS

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SECTION I. SERVICE UPON RECEIPT

3.1 CHECKING FOR SHIPPING DAMAGE

The FDF T/S group is originally shipped as installed equipment that is rack mounted in the Airfield Maintenance Facility (AMF). As shipped, standalone equipment items are stowed in drawers under the FDF T/S group work shelf. Replacement units, however, are wrapped in polyethylene and placed in a cardboard box. The box is then filled with polystyrene packing material to minimize shock during transport. The box is sealed and placed in a wooden shipping crate. The crate is then similarly filled with polystyrene packing material. Before unpacking the replacement unit, check the shipping crate for signs of damage incurred during shipment. Report any serious damage on SF 364, Report of Discrepancy (ROD).

3.2 UNPACKING

The procedure for unpacking the equipment is obvious upon inspection.

3.3 CHECKING THE EQUIPMENT

After unpacking the equipment, check it for completeness and modification status as follows:

1. Check equipment against component list on packing slip to see if shipment is complete. Report all discrepancies in accordance with paragraph 1.3. Equipment should be placed in service if a minor assembly or part that does not affect proper functioning is missing.

2. Check to see if equipment has been modified. (Modified equipment will have modification work order (MWO) number on front panel near nomenclature plate.) Also check to see if all currently applicable MWOs have been applied. (Current MWOs pertaining to equipment are listed in DA PAM 25-30.)

Note

For dimensions, weights, and volume of packaged items, see SB 700-20.

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SECTION II. INSTALLATION INSTRUCTIONS

3.4 TOOLS, TEST EQUIPMENT, AND MATERIALS REQUIRED

The following paragraphs describe the items required to install FDF T/S group equipment items in the AMF.

3.4.1 Tools
The tools in a standard maintenance tool kit are sufficient for installing the FDF T/S group equipment items into their 19-inch equipment rack locations in the AMF.

3.4.2 Test Equipment
No test equipment is required for installation of FDF T/S group equipment.

3.4.3 Materials
No materials are required for installation of FDF T/S group equipment.

3.5 INSTALLATION

Installation at the unit and direct support levels consists only of FDF T/S group line-replaceable unit (LRU) replacement during maintenance. As received from the manufacturer, each rack-mounted replacement LRU should already have a rack mounting kit installed (as applicable) and SMRAs secured to its sides, except for patch panel C5A2 and power junction box C5A6, which are mounted only to equipment rack uprights. Each SMRA consists of three parts: an equipment rail (attached to the unit), a rack-mounting rail (attached to cabinet rack), and a slide rail (couples the first two rails together).

Tray-mounted equipment items are mounted on a tray or shelf-mounting provided as part of the AMF. Standalone equipment items do not require installation.

3.5.1 Rack-Mounted Equipment Installation
Equipment locations for the rack-mounted FDF T/S group equipment items are shown in the technical manual for the AMF, which is referenced in appendix A. Cabling interconnections are performed per AMF cabling diagrams, which are also provided in the technical manual for the AMF. If an existing unit is being replaced during maintenance, tag the cables connected to the unit being removed before installing the replacement unit. In turn, use the cable tags as a reference when installing the replacement LRU.

Patch panel C5A2 and power junction box C5A6 are merely secured to rack uprights, using the supplied hardware. Connect cables to these units per cable tags, or as per AMF van cabling diagrams. All other FDF T/S group rack-mounted units have SMRAs and front-panel rack-mount adapters attached.

To install an SMRA-equipped unit into its assigned 19-inch equipment rack location in the AMF, proceed as follows:

1. Extend rails.

2. Align and mate equipment rails on unit with extended slide rails and slide unit part way into equipment rack until each lock lever locks onto its associated rack-mounting rail.

3. Connect FDF T/S group interconnect cabling for unit per AMF van cabling diagrams.

4. When cabling interconnections are complete, press lock-levers on equipment rails and slide unit fully into equipment rack.

5. Secure unit front-panel rack-mount adapters to front of equipment rack with 10-32 x 3/8-inch screws and No. 10 flat washers and Loctite (Item 1, appendix E).

3.5.2 Tray-/Shelf-Mounted Equipment Installation

Equipment locations for the tray-/shelf-mounted FDF T/S group equipment items are shown in the technical manual for the AMF, which is referenced in appendix A. The tray-/shelf-mounted units are printer C3A3, video display terminal (VDT) C4A4, digital processor T/S C5A4, and ARF intercept receiver pallet C5A3.

To install an FDF T/S group tray-/shelf-mounted equipment item into its assigned tray/shelf location in the AMF equipment racks, proceed as follows:

1. If shelf is equipped with SMRAs, remove fastening hardware from rack uprights that secure shelf, and pull shelf out from rack on its slides.

   If shelf does not have SMRAs, proceed to step 2.

2. If an existing unit is being replaced as part of maintenance, tag interconnect cables for later reference. Release unit's tray mounting by turning front thumbscrew(s) counterclockwise; then pull unit forward and upward to remove from tray.

3. Place unit to be installed in front of mounting tray, and slide unit rearwards until hold down pins engage rear-panel holes, or until mounting flanges engage flanges on tray (as applicable). Pull front thumbscrews up over front-panel brackets, or until thumbscrews engage unit mounts (as applicable). Tighten thumbscrews securely by turning clockwise.

4. Connect FDF T/S group interconnect cabling for new/replacement unit per cable tags, or as per AMF cabling diagrams.

5. For shelves without SMRAs, installation is now complete. For shelves with SMRAs, slide shelf fully into equipment rack and fasten with hardware removed in step 1. Apply Loctite (Item 1, appendix E) to hardware when installing.

3.6 INTERCONNECTIONS

Cabling interconnections are performed per AMF cabling diagrams, which are provided in the technical manual for the AMF referenced in appendix A.

SECTION III. PREVENTIVE MAINTENANCE CHECKS AND SERVICES

3.7 GENERAL

Preventive maintenance is the systematic care, inspection, and servicing of equipment to prevent breakdowns and to ensure maximum operational capability. Preventive maintenance is performed at daily, weekly, and monthly intervals, unless otherwise directed by the commanding officer.

3.8 TOOLS, TEST EQUIPMENT, AND MATERIALS REQUIRED

No special tools or test equipment are required. The following tools, test equipment, and materials are required to perform the preventive maintenance procedures.

3.8.1 Tools

The following tools are required to perform preventive maintenance procedures described in this manual:

Army standard	Commercial alternate	Common name
5180-01-195-0855	TK-17/G	Electronic equipment tool kit

3.8.2 Test Equipment

No test equipment is required to perform preventive maintenance procedures described in this manual.

3.8.3 Materials

The following materials are required to perform preventive maintenance procedures described in this manual:

Army standard	Commercial alternate	Common name
8020-00-246-8806	NA	Brush, soft
8305-00-267-3015	NA	Cloth, lint-free
NA	No. 000	Sandpaper
6810-01-310-8303	NA	Alcohol, isopropyl

3.9 PREVENTIVE MAINTENANCE

Preventive maintenance is performed on a routine basis to ensure continuous FDF T/S group performance and condition and to detect impending physical faults before they occur. Defects discovered during operation should be noted for future corrections to be made as soon as operation has ceased. Stop operation immediately if a deficiency is noted during operation that would damage the equipment. Record all deficiencies, together with corrective action taken, on the forms specified in DA PAM 738-750.

3.9.1 Daily Checks

The FDF T/S group, as installed in the AMF, runs continuously. If there is no system/equipment shutdown, daily preventive maintenance is not performed.

3.9.2 Weekly and Monthly Checks

Running of power-up, self-test, and operational verification tests should be performed during periods when the FDF T/S group is not being used to perform performance tests/troubleshooting on units under test (UUTs). Power down (shut down) all FDF T/S group equipment items before beginning the power up, self-test, and operational verification test procedures. However, prior to shutdown, check that the cooling fan(s) on each FDF T/S group equipment item (as applicable) is operating properly. Weekly checks are described in table 3-1; monthly checks are described in table 3-2.

Note

Because most cables are enclosed within the AMF van equipment racks, unit interconnect cable inspections are performed only when equipment is removed and replaced as described in chapter 4.

Table 3-1. Weekly Preventive Maintenance Checks and Services

Step	Item	Description
1	FDF T/S group	Run power-up, self-test, and operational verification procedures, as described in chapter 2.
2	Cooling fans	With FDF T/S group operating, feel front of units that have fans. If hot, check cooling fan(s).
3	Cleanliness	Check each unit for cleanliness as follows:
		a. Remove dust and loose dirt with a clean, soft cloth.
		b. Remove dust or dirt from plugs and jacks with a brush.
		WARNING **Trichlorotrifluoroethane, trichloroethane, and similar chemical solvents are no longer used for ordinary cleaning of equipment. These substances threaten public health and the environment by destroying ozone in the earth's upper atmosphere. Suitable nonhazardous cleaning materials are used instead (i.e., use a clean cloth dampened with water and a mild detergent or with an approved substitute solvent).**
		c. Remove grease, fungus, and ground-in dirt with a cloth dampened (not wet) with water and a mild detergent or with an approved solvent.
4	Cables	Inspect all exterior cables for kinks and strained, cut, frayed, or otherwise damaged insulation.
		Note **Any abnormal conditions should be reported to direct support maintenance personnel.**

Table 3-1. Weekly Preventive Maintenance Checks and Services - Continued

Step	Item	Description
5	Safety wiring	Ensure screws that secure unit front panels to equipment racks are properly tightened and safety wired (as applicable).
6	CCAs	Check that circuit card assemblies (CCAs) are securely mounted in digital processor T/S.
7	Preservation	Inspect exterior surfaces of each unit for chipped paint or corrosion. If necessary, spot-paint surfaces as follows: a. Remove rust and corrosion from metal surfaces by lightly sanding with No. 000 sandpaper. b. Brush two coats of paint on bare metal to protect it from further corrosion. c. Refer to applicable cleaning and refinishing practices specified in TB 43-0118.

Table 3-2. Monthly Preventive Maintenance Checks and Services

Step	Item	Description
1	FDF T/S group	Run power-up, self-test, and operational verification procedures, as described in chapter 2.
2	Cooling fans	With FDF T/S group operating, feel front of units that have fans. If hot, check cooling fan(s).
3	Cleanliness	Check each unit for cleanliness as follows: a. Remove dust and loose dirt with a clean, soft cloth. b. Remove dust or dirt from plugs and jacks with a brush.

Table 3-2. Monthly Preventive Maintenance Checks and Services - Continued

Step	Item	Description
		WARNING **Trichlorotrifluoroethane, trichloroethane, and similar chemical solvents are no longer used for ordinary cleaning of equipment. These substances threaten public health and the environment by destroying ozone in the earth's upper atmosphere. Suitable nonhazardous cleaning materials are used instead (i.e., use a clean cloth dampened with water and a mild detergent or with an approved substitute solvent).** c. Remove grease, fungus, and ground-in dirt with a cloth dampened (not wet) with water and a mild detergent or with an approved solvent.
4	Exterior cables	Inspect all exterior cables for kinks and strained, cut, frayed, or otherwise damaged insulation. **Note** **Any abnormal conditions should be reported to direct support maintenance personnel.**
5	Interconnecting cables	Inspect all unit interconnecting cables for loose, broken, or otherwise damaged connections and for kinks and strained, cut, frayed, or otherwise damaged insulation. **Note** **Any abnormal conditions should be reported to direct support maintenance personnel.**
6	Safety wiring	Ensure screws that secure unit front panels to equipment racks are properly tightened and safety wired (as applicable).

Table 3-2. Monthly Preventive Maintenance Checks and Services - Continued

Step	Item	Description
7	Calibration	Check calibration stickers on each piece of standard test equipment. If current calibration is due to run out during the next month, attach an easily visible tag to unit, indicating that calibration is required. Schedule calibration for affected units. Units requiring calendar calibration are: a. Spectrum analyzer C2A1 b. Network analyzer C2A2 c. Universal counter C3A1 d. Oscilloscope C3A2 e. Function generator C4A1 f. Signal generator C4A2 g. Logic analyzer C4A3 h. Digital multimeter C5A1
8	CCAs	Check that CCAs are securely mounted in digital processor T/S.
9	Preservation	Inspect exterior surfaces of each unit for chipped paint or corrosion. If necessary, spot-paint surfaces as follows: a. Remove rust and corrosion from metal surfaces by lightly sanding with No. 000 sandpaper. b. Brush two coats of paint on bare metal to protect it from further corrosion. c. Refer to applicable cleaning and refinishing practices specified in TB 43-0118.

SECTION IV. CORRECTIVE MAINTENANCE

3.10 GENERAL

This section contains unit-level corrective maintenance instructions for the FDF T/S group. Corrective maintenance consists of identifying defective FDF T/S group equipment items, replacing them as applicable, and/or referring defective items to higher category maintenance as specified in the maintenance allocation chart (MAC) provided in appendix B.

3.11 TOOLS, TEST EQUIPMENT, AND MATERIALS REQUIRED

Corrective maintenance uses the FDF T/S group's internal built-in test (BIT) capabilities. Hence, no special test equipment or materials are required. The following tool kits are required for unit-level corrective maintenance:

Army standard	Commercial alternate	Common name
5180-01-195-0855	TK-17/G	Electronic equipment tool kit
MK-2648	NA	ARF maintenance kit ESL 21-178363-1

3.12 CORRECTIVE MAINTENANCE INSTRUCTIONS

When an FDF T/S group equipment failure is noted during operation, the initial setup, power-up, self test, and readiness/verification procedures described in chapter 2 are to be performed to identify defective units within the FDF T/S group. These checkout procedures adhere to the FDF T/S group maintenance philosophy specified in the maintenance allocation chart (MAC) provided in appendix B.

Specific unit maintenance instructions to be followed for all major FDF T/S equipment items are provided within the setup, power-up, self-test, and operational readiness/verification (checkout) procedures in chapter 2.

When a standard equipment item (i.e., one of the test equipment units, the printer, or the VDT) is determined to be faulty, the defective unit should be replaced by unit maintenance personnel. Repair of the defective unit should be referred to depot-level maintenance.

If a power supply, the power junction box, the patch panel, the ARF intercept receiver pallet, or the digital processor T/S is determined to be faulty, replacement or repair (as applicable) should be performed by direct support maintenance personnel per procedures provided in chapter 4 and elsewhere in this manual.

Note

The operational checkout procedures in chapter 2 require that all major FDF T/S group equipment items are installed in their respective equipment locations and powered down (shut down).

CHAPTER 4
DIRECT SUPPORT MAINTENANCE INSTRUCTIONS

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SECTION I. GENERAL

4.1 SCOPE

This chapter provides instructions for direct support maintenance of the FDF T/S group. The maintenance philosophy is based on the use of built-in test (BIT) capabilities that include line replaceable unit (LRU)and group-level self-test diagnostics and other automated testing. Besides identifying defective LRUs in the group, the automated and BIT capabilities are designed for comprehensive testing and fault isolation of the digital processor T/S to the lowest replaceable circuit card assembly (CCA), as specified in the maintenance allocation chart (MAC) in appendix B.

When an operational defect occurs while performing LRU tests, the power-up, self-test, and operational readiness/verification procedures in chapter 2 are performed (per unit maintenance instructions) to locate defective equipment items within the FDF T/S group.

If a standard equipment item (i.e., one of the test equipment units, the printer, or the video display terminal (VDT)) is determined to be faulty during operation, the unit is replaced by unit maintenance personnel. Repair of the defective unit is performed at the depot level.

If a power supply, the power junction box, the patch panel, or the ARF intercept receiver pallet is determined to be faulty during operation, replacement or limited wiring/cable repair (as applicable) is performed by direct-support-level maintenance. Replacement procedures are per the installation instructions provided in chapter 3. Defective units requiring repair beyond the scope of direct support maintenance are to be referred to depot level.

The digital processor T/S is replaced/repaired by direct support maintenance personnel. Performance testing, troubleshooting, and general maintenance procedures for the digital processor T/S are provided in this chapter. Additionally, this chapter details all test equipment, tools, and materials applicable to direct support maintenance of the digital processor T/S and the FDF T/S group, in general.

4.2 ORGANIZATION

This chapter contains all procedures and reference measurements necessary to determine proper operation of the digital processor T/S, and to isolate digital processor T/S faults to the lowest replaceable defective assembly.

Testing and troubleshooting are performed using integrated test and fault isolation software. Because the software is designed with an integrated test and fault isolation approach, the performance test and fault isolation procedures presented in this chapter are also integrated. Integrating the performance test and fault isolation procedures simplifies the direct support maintenance tasks. Hence, that integrated methodology is reflected in the organization of this chapter.

This chapter also specifies the required tools, test equipment, and materials. Additionally, the test software procedures are described, and reference information for replacement of defective CCAs is given, as well as information covering general maintenance procedures for the digital processor T/S.

Caution

The FDF T/S group equipment contains parts and assemblies sensitive to damage by electrostatic discharge (ESD). Use ESD precautionary procedures when touching, removing, or inserting CCAs.

ESD
CLASS 1

GENERAL HANDLING PROCEDURES FOR ESDS ITEMS

- Use wrist ground straps or manual grounding procedures.
- Keep ESDS items in protective covering when not in use.
- Ground all electrical tools and test equipment
- Periodically check continuity and resistance of grounding system.
- Use only metallized solder suckers.
- Handle ESDS items only in protected areas.

MANUAL GROUNDING PROCEDURES

- Make certain equipment is powered down.
- Touch ground prior to removing ESDS items.
- Touch package of replacement ESDS item to ground before opening.
- Touch ground prior to inserting replacement ESDS items.

ESD PROTECTIVE PACKAGING AND LABELING

- Intimate covering of antistatic material with an outer wrap of either type 1 aluminized material or conductive plastic film or hybrid laminated bags having an interior of antistatic material with an outer metallized layer.
- Label with sensitive electronic symbol and caution note.

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SECTION II. TOOLS AND TEST EQUIPMENT

4.3 TOOLS, TEST EQUIPMENT, AND MATERIALS REQUIRED

4.3.1 Tools

The following tools are required for direct support maintenance of the digital processor T/S and other equipment items within the FDF T/S group:

Army standard	Commercial alternate	Common name
5180-01-195-0855	TK-17/G	Electronic equipment tool kit
MK-2648	NA	ARF maintenance kit
5120-00-165-3912	M22520/1-01	Crimper
5120-00-165-3910	M22520/2-01	Crimper
5120-00-016-6382	M22520/1-02	Crimper turret head assy
5120-00-165-3913	M22520/2-02	Crimper turret head assy
5120-00-915-4587	M8 1969/14-02	Insertion/removal tool
5120-00-915-4588	M8 1969/14-03	Insertion/removal tool

4.3.2 Test Equipment

The following test equipment is required for direct support maintenance of the digital processor T/S and other equipment items within the FDF T/S group:

Army standard	Commercial alternate	Common name
OQ-493/USD	NA	FDF T/S group

4.3.3 Materials

The following materials are required for direct support maintenance of the FDF T/S group:

Army standard	Commercial alternate	Common name
8020-00-246-8806	NA	Brush, soft
8305-00-267-3015	NA	Cloth, lint-free
NA	No. 000	Sandpaper

4.3.4 Test Cables and Fixtures

There are no special test cables and fixtures required to perform the procedures contained in this chapter. All required test cables for FDF T/S group and digital processor T/S performance testing and troubleshooting are included as part of the FDF T/S group.

However, since individual standard equipment items (i.e., the test equipment, the printer, and the VDT) within the FDF T/S group require special test cables, fixtures, and calibration standards to run the LRU performance tests specified in their associated maintenance manuals (listed in appendix A), these items are replaced in the field at the unit maintenance level and are tested/repaired at the depot level.

Depot-level performance tests and troubleshooting procedures, along with lists of required tools, test equipment, materials, test cables, and fixtures for commercial test and computer equipment items, are detailed in the associated maintenance manuals referenced in appendix A.

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4.4 GENERAL

This section contains a description of FDF T/S group automated test and fault isolation facilities and capabilities and an integrated step-by-step performance test and troubleshooting procedure for the digital processor T/S. Each step in the performance test and troubleshooting procedure must be completed in the sequence given. Performance of the digital processor T/S is checked with the unit installed in its respective equipment rack location in the Airfield Maintenance Facility (AMF).

4.5 FDF T/S GROUP FACILITIES AND CAPABILITIES

The FDF T/S group software performs automated testing of the digital processor T/S. All equipment and software required to perform complete operational testing and fault isolation are included in the FDF T/S group.

The FDF T/S group software provides VDT displays that support the entire performance test and fault isolation procedures for the digital processor T/S to guide direct support maintenance personnel. A retest capability is also incorporated into the FDF T/S group software.

The sequence in which CCA fault isolation tests are performed is preset by the FDF T/S group software. Thus, decision making by the test operator is minimized during the automated fault isolation process. Special operator instructions are displayed on the VDT by the FDF T/S group software to provide overall guidance during the test processes and to minimize references to the various LRU technical manuals for the FDF T/S equipment.

4.5.1 Test Operator Interaction

The FDF T/S group VDT displays provide all information necessary for test operator interaction. The information consists of operator instructions, brief test notes, prompts, and test results. The following subparagraphs describe the information provided on the VDT displays.

Note

When using the FDF T/S group VDT, the test operator must ensure that the keyboard is locked into the CAPS LOCK mode, since the FDF T/S software recognizes only uppercase letters. If lowercase letters are entered, the FDF T/S software ignores the input and the operator receives no response on the VDT display.

4.5.1.1 Operator Instructions

Except for certain steps required for initial setup, such as verification and adjustment of power supply voltages, all step-by-step instructions required to perform the performance test and troubleshooting procedure for the digital processor T/S are provided on the VDT displays. The instructions include connection of required cables for the initial test setup and any additional connections required as a result of FDF T/S group software testing.

4.5.1.2 Test Notes

Brief test notes are displayed on the VDT for the digital processor T/S performance test and troubleshooting procedure. The test notes describe the nature of the test to be performed, the implications to the digital processor T/S under test, any limitations of the FDF T/S group software routines, any operator interaction required, and any operator measurements to be taken. Additionally, information concerning test equipment setup and subsequent verification of signal waveforms using the test equipment is described as required.

4.5.1.3 Prompts

Prompts are provided to indicate the current operational status of the software. An example of a software prompt is TEST SET SELF TEST IN PROGRESS.

4.5.1.4 Test Results

The results of the digital processor T/S self-test routine are displayed on the VDT. Instructions are included in the performance test and troubleshooting procedure to guide test operator reactions to the displayed test results. Additionally, in some cases, when a fault is encountered in the digital processor T/S, VDT test result displays include special instructions to be performed by the operator before the self-test procedure is resumed.

4.5.2 Digital Processor T/S Test Procedures

The digital processor T/S test procedures are incorporated into the FDF T/S group software. Basically, the software first checks out processor CCA C5A4A2, common CCA C5A4A1, and EPROM CCAs C5A4A15 thru C5A4A17. Next, the software checks out SIO interface CCA C5A4A7, DLI CCA CSA4AS, and SCAR interface CCA CSA4A6. Finally, the software checks out PIO interface CCA C5A4A10 and GPIB interface CCA C5A4A11 by applying input stimuli to the two CCAs and directing the operator to visually verify the signal generator and function generator output settings as well as the waveforms displayed on the logic analyzer. The following subparagraphs briefly describe the tests performed on the digital processor T/S C5A4 CCA complement by the FDF T/S group software.

4.5.2.1 Processor CCA Instruction Set Test

The FDF T/S group software checks the instruction set on processor CCA C5A4A2. Correct operation of the various 68000 microprocessor instructions is verified by the software.

4.5.2.2 RAM Test

The random access memories (RAMs) on processor CCA C5A4A2 and common CCA C5A4A1 are checked by the software. The software reads a memory location, complements the contents of that memory location, exclusive ORs the contents of the memory location with the original data, and complements the exclusive OR result. If the resultant value is zero, the memory location tested passes the test. The final (resultant value) contents of the memory location under test are complemented again to return the data to the original state before the test began. RAM is tested in this manner throughout the 64 kbytes contained in processor CCA C5A4A2 and common CCA C5A4A1.

If the RAM fails the test, the software displays that information on the VDT for user interpretation. If the RAM passes the test, no display is generated until another digital processor T/S failure is encountered in the self-test routine or until the digital processor T/S passes the self-test routine.

4.5.2.3 EPROM CCA Test

The EPROM software test module contains a starting address and an ending address of the EPROM to be tested. The contents of the EPROM from the starting address to the ending address are summed and compared to a checksum value. The checksum value for each EPROM CCA (C5A4A15 thru C5A4A17) is written into an address area of the EPROM CCA when the data is loaded into the EPROM CCA. If the sum of the EPROM CCA memory contents equals the checksum value, the EPROM CCA passes the test.

If the EPROM CCA fails the test, that information is displayed on the VDT for user interpretation. If the EPROM CCA passes the test, no display is generated by the software until a fault is encountered in the self-test procedure or the digital processor T/S passes the self-test procedure.

4.5.2.4 SIO Interface CCA Test

The SIO interface CCA test checks interrupts generated by the input channel, channels A and B on SIO interface CCA C5A4A7. The data loopback test mode for channels A and B is also tested. The data loopback test mode for channels A and B connects an output channel to an input channel before the drivers and after the receivers on SIO interface CCA C5A4A7. Thus, the SIO interface CCA drivers and receivers are not tested, while the internal CCA receiver and transmitter RAMs, as well as the shift register, multiplexer, and data control logic, are tested.

The internal data loopback test is performed by sending 216 bytes of data via the common bus to SIO interface CCA C5A4A7. The 216-byte message is looped through the SIO interface CCA circuits and then transmitted via the common bus back to processor CCA C5A4A2.

If any of the expected interrupts is not received, or if the returned data does not match the transmitted data, processor CCA C5A4A2 fails the loopback test. If the CCA fails the test, the VDT displays that result. If SIO interface CCA C5A4A7 passes the test, no VDT display is generated until a failure is encountered with another CCA or the digital processor T/S passes the self-test.

4.5.2.5 SCAR Interface CCA Test

The SCAR interface CCA test checks interrupts, the receiver command channel, and the SCAR command channel on SCAR interface CCA C5A4A6. The test uses the loopback technique like the SIO interface CCA test previously described (i.e., an output channel is connected to an input channel before the drivers and after the receivers). Thus, the SCAR interface CCA drivers and receivers are not tested.

The length of the test data sent through the receiver command channel is 56 bits; the length of the data sent through the SCAR command channel is 8 bits. Since SCAR interface CCA C5A4A6 incorporates a

pipelined structure, the test must be performed twice. The first time, the test data is entered into the pipeline; the second time, the test of the CCA circuits is performed.

If the transmitted data does not compare to the received data, the CCA fails the test and a VDT display transmits that information to the test operator. If SCAR interface CCA C5A4A6 passes the test, no display is generated on the VDT until a fault is encountered with another CCA or the digital processor T/S passes the self-test.

4.5.2.6 DLI CCA Test

The following subparagraphs describe the DLI CCA tests incorporated into the FDF T/S group software self-test procedure for the digital processor T/S.

4.5.2.6.1 Output Channel Interrupt Test

The DLI CCA test uses an internal loopback test to check the interrupts and other functions included on DLI CCA C5A4A8. Processor CCA C5A4A2 passes four blocks (40 bytes) of data via the common bus to DLI CCA C5A4A8. The four blocks of data are loaded into the transmitter channel buffer, the transmitter interrupt is enabled, and the transmit bit is set on DLI CCA C5A4A8 by processor CCA C5A4A2. When the transmit channel outputs the data back to the input channel, DLI CCA C5A4A8 asserts an interrupt via the BIRQL daisy-chain to processor CCA C5A4A2. If the output channel interrupt is asserted, DLI CCA C5A4A8 passes that portion of the test.

4.5.2.6.2 Input Channel Interrupt Test

The input channel interrupt test checks operation of the interrupt to processor CCA C5A4A2 when data is received by DLI CCA C5A4A8. The data transmitted by the output channel is passed via the CCA internal data loop path to the CCA receiver input. When the test data is received by the input channel and stored in the input buffer, DLI CCA CSA4A8 asserts the receiver interrupt via the BIRQL daisy-chain to processor CCA C5A4A2. If the receiver interrupt is asserted, DLI CCA C5A4A8 passes that portion of the test.

4.5.2.6.3 Internal Loop Test

The internal loop test is performed by comparing the data received through the input channel to the data sent through the output channel of DLI CCA C5A4A8. If the received data compares to the data transmitted, DLI CCA C5A4A8 passes the internal loop test. If DLI CCA C5A4A8 fails any of the tests described, the VDT displays that information to the test operator. If DLI CCA C5A4A8 passes all tests, no VDT display is generated until either a digital processor T/S CCA C5A4 fault is encountered or the digital processor T/S passes the self-test.

4.5.2.7 PIO Interface CCA Test

The PIO interface CCA test is accomplished by processor CCA C5A4A2 sending two 12-bit signal words, via the common bus, to PIO interface CCA C5A4A10. Each 12-bit signal word is processed by PIO interface CCA C5A4A10 and applied to one of the two parallel output ports. The two 12-bit words are 180° out of phase with each other (i.e., when the first bit of one word is high, the first bit of the other word is low).

The two parallel output ports of the PIO interface CCA are connected to the channels A and B inputs to the logic analyzer. The test operator verifies that the two 12-bit words are simultaneously displayed on the logic analyzer waveform screen and that the two 12-bit words are 180' out of phase. If the logic analyzer display is as stated, PIO interface CCA C5A4A10 passes the self-test.

4.5.2.8 GPIB Interface CCA Test

For the GPIB interface CCA test, processor CCA C5A4A2 transmits control signals and data, via the common bus, to GPIB interface CCA C5A4A11. GPIB interface CCA C5A4A11 uses the common bus data and control signals to produce data and control signals that are applied, via the IEEE-488 interface bus, to the standard equipment in the FDF T/S group.

The IEEE-488 interface bus data and control signals tune the output frequencies and power levels of the function generator and the signal generator to predetermined values, set up and control other test equipment, and also provide for print data passage to printer C3A3.

The test operator visually verifies the correct output frequency and power level values at the signal generator and function generator front-panel displays. If the displays correlate with the predetermined values listed on the VDT display, GPIB interface CCA C5A4A11 passes the self-test.

4.6 PERFORMANCE TEST AND TROUBLESHOOTING

Before beginning this procedure, the initial setup, power-up, self-test, and operational readiness/verification procedures described in chapter 2, paragraph 2.4, should have already been performed to identify defective equipment items in the overall FDF T/S group. This procedure is performed when results of those tests indicate failure of the digital processor T/S, or when a defect in the digital processor T/S or functionally related equipment is suspected.

The standard test and computer peripheral equipment of the FDF T/S group is referred to by common names in the following procedure. Refer to table 1-3 for the common-name-to-official-nomenclature translations.

WARNING

Extremely high current can be generated by accidentally shorting voltages to ground. Conductive jewelry, especially rings and watches, that could come in contact with the hardware should be removed.

Note

The following procedural steps assume that the FDF T/S group equipment is interconnected per procedure outlined in chapter 3 and cabling diagram in figure FO-1. It is also assumed that FDF T/S equipment is powered up.

Note

If applicable, wait 30 minutes (minimum) for standard test equipment to warm up before proceeding with this procedure.

Perform the digital processor T/S performance test and troubleshooting procedure as follows:

1. a. Check (and, if applicable, adjust) 5-V de output on power supply C5A9 as follows:

   (1) Connect DMM C5A1 to digital processor T/S connector pins J2-12 (+5 V dc) and J2-13 (ground).

   (2) If DMM indicates more/less than +5.0 (±0.05) V dc, loosen locknut on power supply C5A9 front-panel 5 V adjustment potentiometer and adjust until DMM C5A1 indicates +5.0 (±0.05) V dc.

   b. If O.K., proceed to step 2.

   c. If indication is abnormal, set power supply C5A9 front-panel METER SELECTION switch to VOLTS and rotary switch to position 1. Remove dc

power cable from digital processor T/S connector J15, and set power supply C5A9 front-panel 5 V adjustment potentiometer to give a front-panel meter display reading of 5.8 (±0.2) V de. If power supply will not adjust to give specified voltage, replace power supply C5A9. If the power supply can be set to specified voltage, proceed to step 6.

2. a. Check (and, if applicable, adjust) 15-V dc output on power supply C5A9 as follows:

   (1) Set power supply C5A9 front-panel rotary switch to position 2.

   (2) If power supply front-panel meter shows more/less than 15.0 (±0.1) V dc, loosen locknut on power supply C5A9 front-panel 15 V adjustment potentiometer and adjust until front-panel display indicates 15.0 (±0.2) V dc.

   b. If O.K., proceed to step 3.

   c. If indication is abnormal, remove dc power cable from digital processor T/S connector J15, and set power supply C5A9 front-panel 15 V adjustment potentiometer to give a front-panel meter display reading of 15.2 (±0.2) V dc. If power supply will not adjust to give specified voltage, replace power supply C5A9. If power supply can be set to specified voltage, proceed to step 6.

3. a. Check (and, if applicable, adjust) 5-V de output on power supply C5A10 as follows:

   (1) Set power supply C5A10 front-panel METER SELECTION switch to VOLTS and rotary switch to position 1.

   (2) If adjustment is needed, loosen locknut on power supply C5A10 front-panel 5 V adjustment potentiometer and adjust until front-panel display indicates 5.0 (±0.1) V de.

   b. If O.K., proceed to step 4.

   c. If indication is abnormal, replace power supply C5A10.

4. a. Check (and, if applicable, adjust) 28-V dc output on power supply C5A10 as follows:

   (1) Set power supply C5A10 front-panel rotary switch to position 4.

   (2) If adjustment is needed, loosen locknut on power supply C5A10 front-panel 28 V adjustment potentiometer and adjust until front-panel display indicates 28.0 (±0.2) V dc.

   b. If O.K., proceed to step 7.

   c. If indication is abnormal, replace power supply C5A10.

Note

In the following steps, the digital processor T/S will be opened, all CCAs removed and then reinstalled one at a time, until cause of the over correct condition is located.

Caution

Be sure to set power switch at power supply C5A9 to OFF in following steps while removing and installing CCAs.

5. a. Check digital processor T/S internal power bus wiring as follows:

   (1) Remove digital processor T/S from shelf in AMF equipment rack, and place unit on work table.

   (2) Remove top and bottom covers of digital processor T/S.

   (3) Remove all plug-in CCAs from card cage.

   (4) Connect test setup as given in figure 4-1, except for logic analyzer connection at digital processor T/S connector J18.

   (5) At power supply C5A9, set power switch to ON.

   (6) At power supply C5A9, observe front-panel meter for normal indication of 5.0 (±0.1) V de or 15.0 (±0.1) V dc.

   b. If O.K., proceed to step 6.

   c. If indication is abnormal, adjust 5 V or 15 V potentiometer, as applicable, for specified voltage. If power supply will not adjust to specified voltage, troubleshoot and repair +5, +15, or -15 V bus wiring in digital processor T/S, as applicable.

6. a. Check digital processor T/S CCAs as follows:

   (1) Turn power supply C5A9 power switch to OFF.

   (2) Install one of CCAs removed in step 5.

   (3) At power supply C5A9, set power switch to ON and observe front-panel meter for normal indication of 5.5 (±0.1) V dc or 15.2 (±0.1) V dc, as applicable.

   b. If O.K., repeat this step until faulty CCA is located.

   c. If indication is abnormal, replace faulty CCA. Repeat steps 6a and 6b to verify repair.

7. a. Check proper operation of power junction box C5A6 dc-to-dc power converter as follows:

   (1) Connect DMM C5A1 to power junction box test points C5A6J7-J (+) and C5A6J7-K (-)

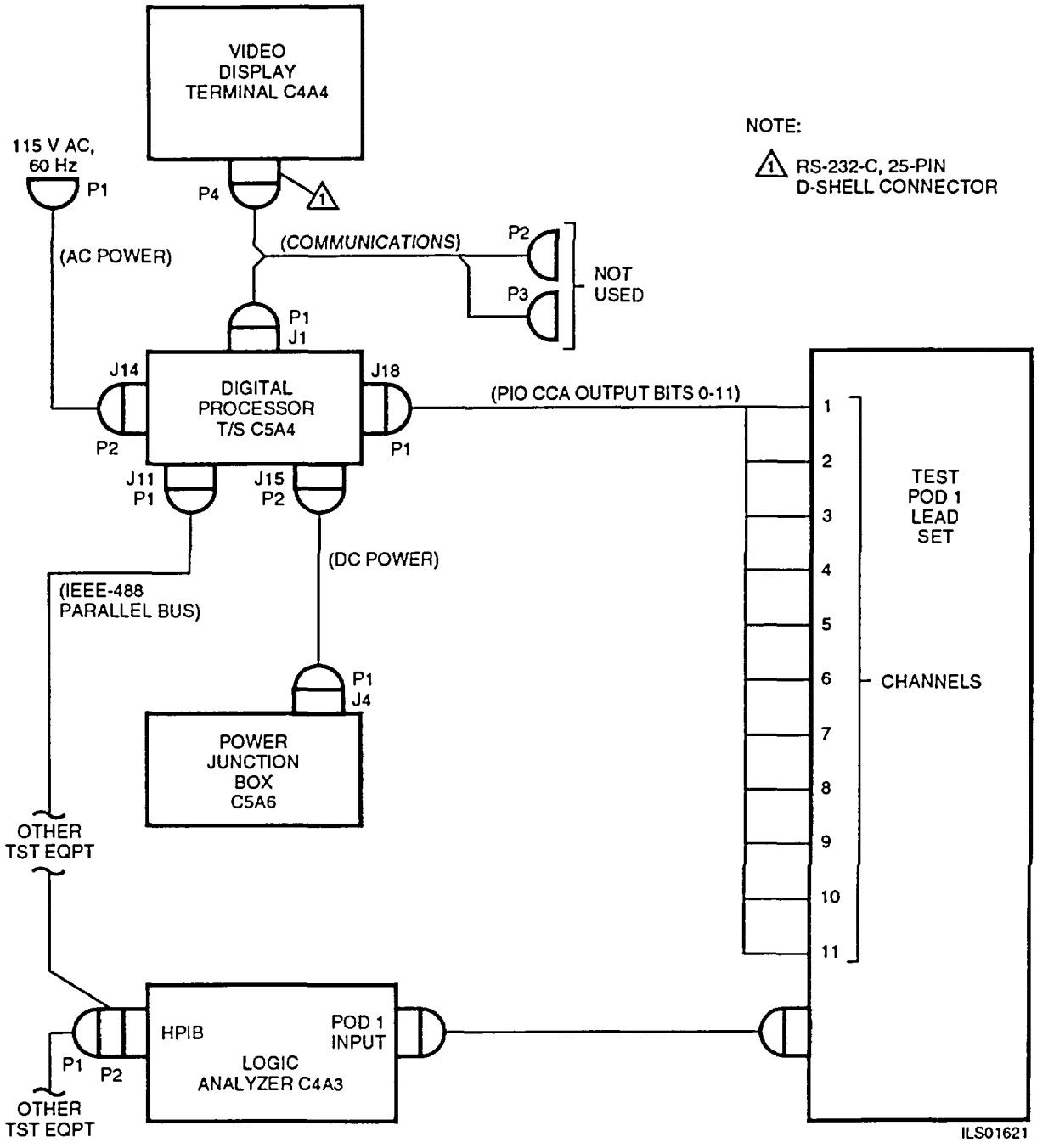

Figure 4-1. Digital Processor T/S C5A4 Test Setup

(2) Measure voltage for normal indication of 36.0 (±0.2) V de.

b. If O.K., proceed to step 8.

c. If indication is abnormal, remove power junction box C5A6 from AMF equipment rack. Remove unit top cover, and inspect condition of internal wiring. If wiring defects are noted, repair wiring and reinstall unit in equipment rack. Then repeat this step to verify repair. If wiring is O.K., or if indication is still abnormal on re-testing, replace power junction box C5A6.

8. a. Check that digital processor T/S cooling blower is properly functioning as follows:

(1) Connect test setup shown in figure 4-1.

(2) Verify operation of blower C5A4B1 by noting presence of cooling air exhaust at digital processor T/S front-panel openings. Normal indication: blower C5A4B1 operating.

b. If O.K., proceed to step 9.

c. If indication is abnormal, replace blower C5A4B1.

Note

In the following step, it is assumed that the digital processor T/S is at normal operating temperature.

9. a. Check continuity of digital processor T/S over-temperature dc power cutoff switch as follows:

(1) Disconnect cable W51 from digital processor T/S connector J14.

(2) Using DMM C5A1, measure resistance between test points J14-E and -F for normal indication of greater than 100 kohms.

b. If O.K., reconnect cable W51 to digital processor T/S connector J14, and proceed to step 10.

c. If indication is abnormal, replace overtemp switch C5A4S 1.

Caution

In the following steps, when prompted by the computer via the VDT to replace or reseat a CCA within the digital processor T/S, remove power cable from connector J15 prior to performing that step.

Note

During execution of following steps, ensure that VDT C4A4 keyboard is operated in CAPS LOCK mode.

10. a. Check digital processor T/S general performance as follows:

(1) Perform digital processor T/S self-test per instructions displayed on VDT C4A4.

(2) Press L key on VDT keyboard to proceed with digital processor T/S self- test routine. The following normal indication message is displayed:

ALL CCAS EXCEPT PIO (A10) AND GPIB (A11) HAVE PASSED SELF-TEST.

b. If O.K., proceed to step 11.

c. If indication is abnormal, isolate digital processor T/S malfunction by noting particular abnormal test response received, as follows:

(1) If no display on VDT C4A4, remove digital processor T/S cover, replace common CCA C5A4A1, and repeat this step.

(2) If VDT displays message:
A SPURIOUS INTERRUPT HAS BEEN DETECTED DURING THE XXXXXXXXX CARD TEST

simultaneously press CRTL and R keys to reset digital processor T/S and repeat this step.

(3) If VDT displays message:

BUS ERROR DETECTED ON TEST SET DPU

press any key to resume self-test procedure and follow fault location instructions on VDT to correct fault.

(4) If VDT display indicates that DLI CCA CSA4A8 test is not receiving correct interrupts, remove digital processor T/S bottom cover and follow instructions displayed on VDT C4A4.

(5) If VDT C4A4 displays message that any of the following are at fault:

SCAR IF CCA C5A4A6
SIO CCA C5A4A7
DLI CCA C5A4A8
Common CCA C5A4A1
EPROM CCAs C5A4A15 thru C5A4A17

remove CCA identified from card cage and reseat CCA in its respective slot of card cage. Press CTRL and R keys to reset digital processor T/S; then repeat this step. If self-test response is still abnormal, replace failed CCA indicated on VDT.

(6) For any other abnormal test responses received, replace processor CCA C5A4A2 and repeat this step to verify repair.

Note

In the following two steps, the frequency and output level displays must be selected alternately, as only one or the other is displayed at any one time.

11. a. Check signal generator C4A2 frequency and output level displays for the following:

    (1) 123.45 MHz

    (2) -67 dBm

    b. If O.K., proceed to step 12.

    c. If indication is abnormal, proceed as follows:

    (1) Remove top cover of digital processor T/S.

    (2) Remove and reseat GPIB interface CCA C5A4A11.

    (3) Press R key to repeat self-test procedure.

    (4) Repeat steps 10 and 11. If indication is still abnormal, replace GPIB interface CCA C5A4A11; then repeat steps 10 and 11 to verify repair.

12. a. Check function generator C4A1 frequency and output level displays for the following:

    (1) 765.43 kHz

    (2) -21.1 dBm

    b. If O.K., proceed to step 13.

    c. If indication is abnormal, proceed as follows:

    (1) Remove top cover of digital processor T/S.

    (2) Remove and reseat GPIB interface CCA C5A4A11.

    (3) Press R key to repeat self-test procedure.

    (4) Repeat steps 10 thru 12. If indication is still abnormal, replace GPIB interface CCA C5A4A11; then repeat steps 10 thru 12 to verify repair.

13. a. Perform digital processor T/S PIO CCA performance test, as follows:

    (1) See digital processor T/S test setup shown in figure 4-1. Connect cable W15 connector P1 to digital processor T/S connector J18 (PIO port). Connect other end of cable to POD-1 lead set, channels 0 thru 11 per cable tags on each pin lead.

    (2) Verify that SYSTEM CONFIGURATION screen is displayed on logic analyzer. If not, power down analyzer and re-power up. After restart,

self-tests, and operating system load, analyzer will display SYSTEM CONFIGURATION screen.

(3) Load logic analyzer PIO-TEST setup file from operating system diskette as follows:

(a) Press logic analyzer I/O MENU key.

(b) Move cursor to Disk Operations field and press SELECT key; then select "from file" entry box and press SELECT key.

(c) Enter filename PIO-TEST, move cursor to Done option field, and press SELECT key.

(d) Move cursor to Execute field and press SELECT key; then move cursor to Continue option field and press SELECT key. In turn, analyzer responds by loading test setup file. After file has been loaded, message "load operation complete" is displayed.

(e) Move cursor to Done option field and press SELECT key.

(4) Press RUN key on logic analyzer. Analyzer responds by displaying Timing Waveform screen for test, and the message "waiting for trigger" is displayed at top of screen.

(5) Simultaneously press CTRL and R keys on VDT keyboard to reset digital processor T/S. Then press VDT key L to continue procedure.

(6) Verify that VDT displays the message:

ALL CARDS EXCEPT PIO (A10) AND GPIB (A111) HAVE PASSED SELF TEST

If a different (abnormal) message is received, repeat step 10.

(7) Verify that parallel interface signals displayed on logic analyzer C4A3 are alternating 12-bit 1010...and 0101...bit patterns (alternating positive- and negative-going pulses), as shown in figure 2-6 in chapter 2.

b. If waveform display is correct, proper operation of digital processor T/S has been verified. Press VDT key Q to return to FDF T/S group main menu, which is shown in figure 2-7 in chapter 2.

c. If one or more signals are absent or incorrect, proceed as follows:

(1) Remove top cover of digital processor T/S.

(2) Remove and reseat PIO interface CCA C5A4A10.

(3) Press R key to repeat self-test procedure; then repeat this step. If one or more PIO waveform signals are still absent or incorrect, replace PIO interface CCA C5A4A10. Repeat step to verify repair.

4.7 DIGITAL PROCESSOR ERROR MESSAGES

When certain types of faults are encountered in the digital processor T/S, test execution is halted and an error message is displayed on the VDT. From the software viewpoint, the faults are detected through the exception processing feature of the MC68000L8 microprocessors in the digital processor T/S under test. Some possible faults that can be detected by exception processing include software errors, bus errors, processing errors due to power surges and transients, spurious interrupts, incorrect interrupt handling, and other faults from a number of different sources.

4.7.1 Exception Processing/Error Message Types

Two basic types of error messages are displayed on the VDT for exception processing faults: bus error messages and exception processing messages. Bus error messages are described in subsequent paragraphs. All other errors detected from exception processing cause the VDT to display the following message: EXCEPTION PROCESSING HAS BEEN INITIATED ON THE TEST SET DPU. In addition to the preceding message, the message EXCEPTION VECTOR = XX is displayed for test system programming purposes and is to be ignored by the operator. The message HIT ANY KEY TO RESET DPU is displayed also.

4.7.2 Operator Response to Exception Processing/Error Messages

To handle the detected exception processing fault, the operator must press any key on the VDT keyboard. This resets the digital processor T/S and causes the digital processor T/S self-test to be executed.

4.7.3 Bus Errors

Three types of bus errors may occur during computer-controlled testing of the digital processor T/S. Bus errors can be caused by primary power source failure, surges, and transients, as well as a faulty or improperly seated CCA. When a bus error is detected in the digital processor T/S, a BUS ERROR DETECTED ON TEST SET DPU message is displayed on the VDT. If the bus error is caused by a fault in the digital processor T/S while the self-test procedure is being executed, pressing any key at the VDT keyboard resets the digital processor T/S, causing the self-test procedure to continue until the fault is isolated. The operator follows the fault isolation instructions and repairs the fault in accordance with instructions in procedures within this chapter. After the fault is repaired, the LRU test in progress at the time the fault occurred can be re-initiated.

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SECTION IV. MAINTENANCE OF THE EQUIPMENT

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4.8 GENERAL

This section provides digital processor T/S general maintenance procedures that are the responsibility of direct support maintenance personnel. The section contains instructions for general inspection and cleaning, for removal of top and bottom covers, and for replacement of defective assemblies.

After completing any repair action, perform the tests described in paragraph 4.6 to verify proper operation of the digital processor T/S before returning it to service.

4.9 GENERAL MAINTENANCE PROCEDURES

To perform general maintenance on digital processor T/S C5A4, remove the top and bottom covers as given in paragraph 4.10.1 and perform the following inspection and cleaning procedures.

4.9.1 Inspection

Proceed as follows:

1. Inspect exterior of unit for dirt, corrosion, dents, scratches, and chipped paint.
2. Check cable and CCA connectors for correct pin depth.
3. Inspect interior of unit for dirt, corrosion, and foreign objects.
4. Inspect interior of unit for burned, frayed, short-circuited, broken, or loose wires. Inspect for kinks and strained, cut, frayed, or otherwise damaged insulation.
5. Inspect cable and CCA connectors for broken or shorted wires.
6. Inspect for loose or missing screws from connectors or chassis.

4.9.2 Cleaning

Proceed as follows:

1. Remove dust and loose dirt from exterior surfaces with a clean, soft cloth.

2. Remove dust and dirt from cable and CCA connectors, internal wiring, and other surfaces with a soft brush.

WARNING

Trichlorotrifluoroethane, trichloroethane, and similar chemical solvents are no longer used for ordinary cleaning of equipment. These substances threaten public health and the environment by destroying ozone in the earth's upper atmosphere. Suitable nonhazardous cleaning materials are used instead (i.e., use a clean cloth dampened with water and a mild detergent or with an approved substitute solvent).

3. Remove grease and/or ground-in dirt with a cloth dampened water and a mild detergent or with an approved solvent.

4.10 DIGITAL PROCESSOR T/S MAINTENANCE PROCEDURES

The following paragraphs provide procedures for removal of top and bottom covers and replacement of assemblies within the digital processor T/S. Figure 4-2 shows the digital processor T/S component locations. The components shown in this figure are labeled by their applicable reference designations.

WARNING

Before performing any repair procedure, power must be removed from the digital processor T/S by disconnecting cables from connectors J14 and J15.

4.10.1 Top and Bottom Cover Removal

To remove the top and bottom covers of the digital processor T/S, proceed as follows:

1. Disconnect power from connectors J14 and J15.
2. Remove 18 screws that secure top cover.
3. Remove top cover.
4. Repeat steps 2 and 3 for bottom cover.

WARNING

High voltage and low voltage/high current are used in the operation of this equipment. Ensure that all power is disconnected from connectors J14 and J15 when any maintenance procedure is performed. When performance test/troubleshooting procedure is being performed, care must be taken to avoid contacting high-voltage connections or grounding the high-current sources when operating this equipment. Injury or death may result if personnel fail to observe safety precautions.

4.10.2 Digital Processor T/S CCA Replacement

When the performance test and troubleshooting procedure in paragraph 4.6 directs maintenance personnel to replace one of the CCAs in the digital processor T/S, perform the following procedures. A11 CCAs are replaced in an identical manner.

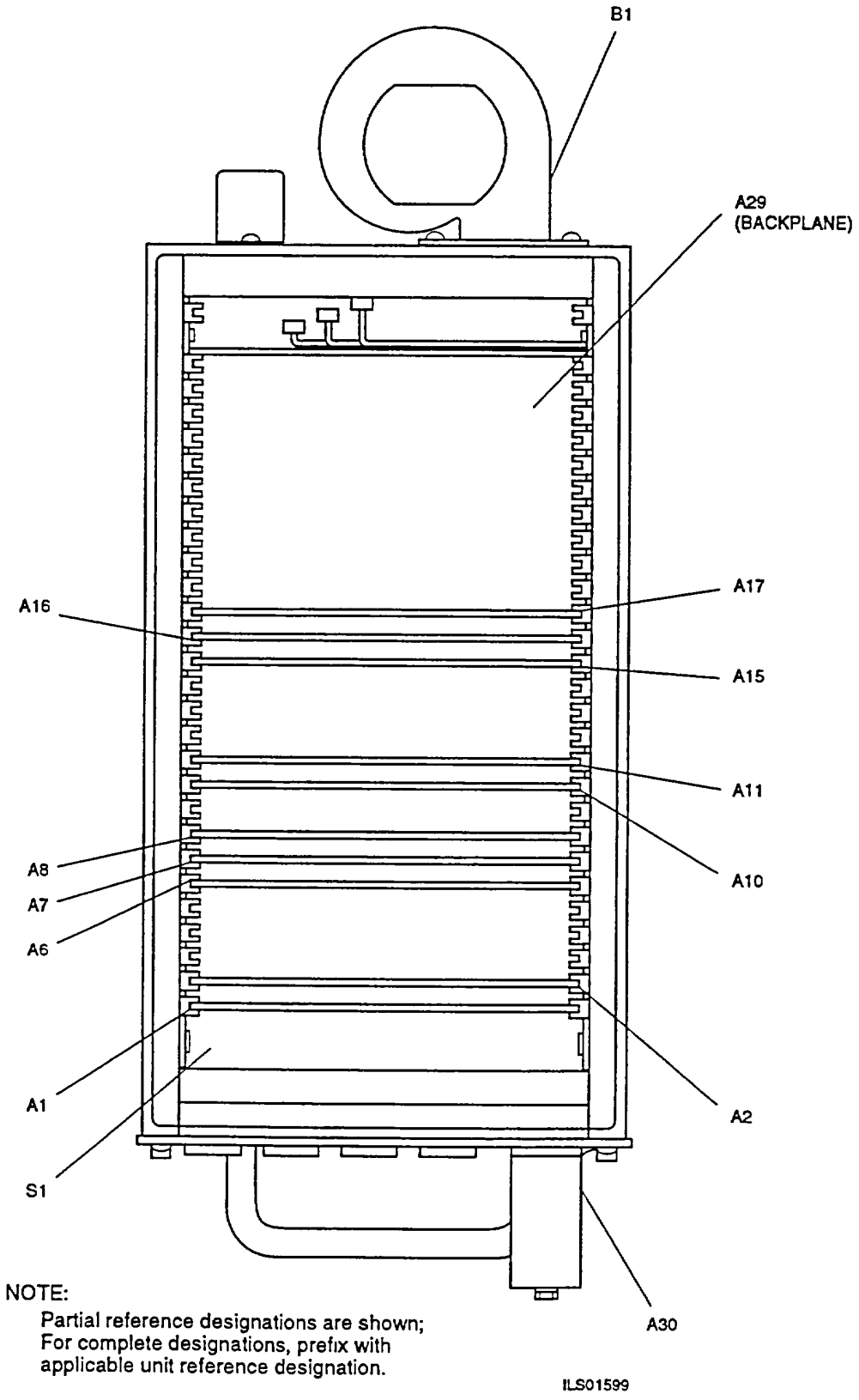

Figure 4-2. Digital Processor T/S C5A4 Component Locations

To replace a CCA, proceed as follows:

1. Using special tool in ARF maintenance kit, unlock card holder locks on both sides of CCA to be replaced by rotating in direction pointing away from chassis.

2. Locate card extraction tool (CDC 87399200) included in ARF maintenance kit. Extract CCA to be replaced by inserting Allen wrench attachments on tool into extraction holes in CCA from component side. Holes are located at top of each CCA slide frame. Squeeze card extractor to pull CCA out of backplane connector. Remove extractor, grasp top edge of CCA, and gently lift CCA free of holders and chassis.

3. Slide replacement CCA evenly into holders with component side of CCA facing toward unit's front panel.

4. Press firmly and evenly on top edge of CCA until it is fully seated into backplane connector.

5. Using locking tool, lock card holder locks on both sides of CCA by rotating in direction toward center of chassis.

6. Resume performance test/troubleshooting procedure in paragraph 4.6.

4.10.3 Blower C5A4B1 and Capacitor C5A4C1 Subassembly Replacement

The digital processor T/S has a centrifugal blower, designated C5A4B1, and its associated capacitor, designated C5A4C1. When the performance test/troubleshooting procedure in paragraph 4.6 calls for replacement of the blower assembly, the associated capacitor should also be replaced.

To replace blower C5A4B 1/capacitor C5A4C1, refer to figure 4-2 and proceed as follows:

1. Loosen rear panel of digital processor T/S by removing 10 screws, flat washers, and lockwashers; grasp blower and pull out for access to plug P22.

2. Disconnect plug P22 from connector J19 and remove rear panel with blower assembly attached.

3. To replace blower C5A4B 1, remove four screws, flat washers, and lockwashers that secure blower; remove blower. To remove capacitor C5A4C1, tag and desolder wires; remove two mounting screws, flat washers, and lockwashers that secure capacitor, and remove capacitor.

4. Place replacement blower in mounting position and secure to rear panel with four mounting screws, flat washers, and lockwashers. Place replacement capacitor in mounting position and secure to rear panel with two mounting screws, flat washers, and lockwashers; resolder wires to capacitor.

5. Reconnect plug P22 to connector J19, being sure to fasten spring clips on connector J19 securely.

6. Mount digital processor T/S rear panel onto chassis by placing it into position and installing 10 mounting screws, flat washers, and lockwashers.

7. Resume performance test/troubleshooting procedure in paragraph 4.6.

4.10.4 Overtemp Indicator C5A4S1 Replacement

Overtemp indicator C5A4S1 is a thermostatic switch that is mounted on the front of the left-side heat sink assembly on the digital processor T/S. To replace overtemp indicator C5A4S1, refer to figure 4-2 and proceed as follows:

1. Remove left-side panel of digital processor T/S by removing 18 mounting screws and lifting panel off.

2. Tag and desolder wires connected to overtemp indicator C5A4S1.

3. Remove overtemp indicator C5A4S1 from left-side heat sink assembly by removing two mounting screws, flat washers, and lockwashers.

4. Place replacement switch in mounting position on left-side heat sink assembly and secure it with two mounting screws, flat washers, and lockwashers.

5. Resolder wires to switch.

6. Replace left-side panel of digital processor T/S by placing it in position and installing 18 mounting screws.

7. Resume performance test/troubleshooting procedure in paragraph 4.6.

APPENDIX A

REFERENCES

A.1 SCOPE

This appendix lists all technical manuals, miscellaneous publications, regulations, and forms referenced in this manual or pertaining to Fast Direction Finding Test Set Group OQ-493/USD (FDF T/S group).

A.2 TECHNICAL MANUALS

Publication number	Title
TB 43-0118	Field Instructions for Painting and Preserving Electronics Command Equipment Including Camouflage Pattern Painting of Electrical Equipment Shelters
TM 11-4940-485-13	Operator, Unit, and Direct Support Maintenance Manual, Electronics Shop AN/USM-652
TM 11-5821-321-13	Operator, Organizational, and Direct Support Maintenance Manual, Radio Receiver R-2270/ARW-83(V)
TM 11-5821-327-13	Operator, Organizational, and Direct Support Maintenance Manual, Radio Receiver R-2289/ARW-83(V)
TM 11-5821-352-13	Operator, Unit, and Direct Support Maintenance Manual, Radio Remote Receiving Set AN/ARW-83(V)7
TM 11-5821-352-23P	Direct Support and General Support Maintenance Repair Parts and Special Tools List (Including Depot Maintenance Repair Parts and Special Tools), Radio Remote Receiving Set AN/ARW-83(V)7 (ARF)
TM 11-5865-236-13	Operator, Organizational, and Direct Support Maintenance Manual, Radio Frequency Processor CP-1606/ARW-83(V)
TM 11-5865-238-13	Operator, Organizational, and Direct Support Maintenance Manual, Intermediate Frequency Processor CP-1602/TSQ-105(V)
TM 11-5865-239-13	Operator, Organizational, and Direct Support Maintenance Manual, Multiplexer TD1374/U, TD1374A/U, and Demultiplexer TD-1375/U
TM 11-5865-241-13	Operator, Organizational, and Direct Support Maintenance Manual, Multiplexer TD-1376/U, TD-1376A/, and Demultiplexer TD-1373/U
TM 11-5865-245-13	Operator, Organizational, and Direct Support Maintenance Manual, Intermediate Frequency Processor CP-1601/TSQ-105(V)
TM 11-5865-246-13	Operator, Organizational, and Direct Support Maintenance Manual, Intermediate Frequency Processor CP-1668/ARW-83(V)

Publication number	Title
TM 11-5865-250-13	Operator, Organizational, and Direct Support Maintenance Manual, Frequency Converter CV-3836/ARW-83(V)
TM 11-5865-254-13	Operator, Organizational, and Direct Support Maintenance Manual, Radio Frequency Distribution Unit SB-4187/ARW-83(V)
TM 11-5865-268-13	Operator, Organizational, and Direct Support Maintenance Manual, Digital Processor Group: Digital Processor CP1795/ARW-83(V) and Digital Processor CP-1604A/TSQ-105(V)
TM 11-5865-306-10	Operator Manual, Surveillance Information Processing Center AN/TSQ-176
TM 11-5865-306-23	Unit and Direct Support Maintenance Manual, Surveillance Information Processing Center AN/TSQ-176
TM 11-5865-307-12	Operator and Unit Maintenance Manual, Special Purpose Detecting System AN/USD-9C
TM 11-6130-484-13	Operator, Unit, and Direct Support Maintenance Manual, Lambda Power Supply 25699
TM 11-6130-484-23P	Direct Support and General Support Maintenance Repair Parts and Special Tools List (Including Depot Maintenance Repair Parts and Special Tools), Lambda Power Supply 25699
TM 11-6625-444-14-3	Operator, Unit, Direct Support, and General Support Maintenance Manual, Fluke 8840A/AF Digital Multimeter
TM 11-6625-444-24P-3	Unit, Direct Support, and General Support Maintenance Repair Parts and Special Tools List (Including Depot Maintenance Repair Parts and Special Tools), Fluke 8840A/AF Digital Multimeter
TM 11-6625-3068-14	Operator, Unit, Direct Support, and General Support Maintenance Manual, HP 5335A Universal Counter
TM 11-6625-3068-24P	Unit, Direct Support, and General Support Maintenance Repair Parts and Special Tools List (Including Depot Maintenance Repair Parts and Special Tools), HP 5335A Universal Counter
TM 11-6625-3198-12	Operator and Unit Maintenance Manual, Wavetek 288 Function Generator/Frequency Synthesizer/Sweeper

Publication number	Title
TM 11-6625-3198-24P	Unit, Direct Support, and General Support Maintenance Repair Parts and Special Tools List (Including Depot Maintenance Repair Parts and Special Tools), Wavetek 288 Function Generator/ Frequency Synthesizer/Sweeper
TM 11-6625-3281-14	Operator, Unit, Direct Support, and General Support Maintenance Manual, HP 8657B Signal Generator
TM 11-6625-3281-24P	Unit, Direct Support, and General Support Maintenance Repair Parts and Special Tools List (Including Depot Maintenance Repair Parts and Special Tools), HP 8657B Signal Generator
TM 11-6625-3283-14	Operator, Unit, Direct Support, and General Support Maintenance Manual, Tektronix 2440 Oscilloscope
TM 11-6625-3283-24P	Unit, Direct Support, and General Support Maintenance Repair Parts and Special Tools List (Including Depot Maintenance Repair Parts and Special Tools), Tektronix 2440 Oscilloscope
TM 11-6625-3284-14	Operator, Unit, Direct Support, and General Support Maintenance Manual, HP 1650B Logic Analyzer
TM 11-6625-3284-24P	Unit, Direct Support, and General Support Maintenance Repair Parts and Special Tools List (Including Depot Maintenance Repair Parts and Special Tools), HP 1650B Logic Analyzer
TM 11-6625-3286-14	Operator, Unit, Direct Support, and General Support Maintenance Manual, HP 8560A Spectrum Analyzer
TM 11-6625-3286-24P	Unit, Direct Support, and General Support Maintenance Repair Parts and Special Tools List (Including Depot Maintenance Repair Parts and Special Tools), HP 8560A Spectrum Analyzer
TM 11-6625-3289-14	Operator, Unit, Direct Support, and General Support Maintenance Manual, HP 8753C Network Analyzer
TM 11-6625-3289-24P	Unit, Direct Support, and General Support Maintenance Repair Parts and Special Tools List (Including Depot Maintenance Repair Parts and Special Tools), HP 8753C Network Analyzer
TM 11-6625-3291-23P	Direct Support and General Support Maintenance Repair Parts and Special Tools List (including Depot Maintenance Repair Parts and Special Tools), Fast Direction Finding Test Set Group OQ493/USD
TM 11-7025-321-14	Operator, Unit, Direct Support, and General Support Maintenance Manual, HP 2225A Thinkjet Printer
TM 11-7025-321-24P	Unit, Direct Support, and General Support Maintenance Repair Parts and Special Tools List (Including Depot Maintenance Repair Parts and Special Tools), HP 2225A Thinkjet Printer

Publication number	Title
TM 55-1500-323-25	Installation Practices for Aircraft Electric and Electronics Wiring
TM 740-90-1	Administrative Storage of Equipment
TO 33A1-15-86-1	Technical Manual, HP 85044A/B Transmission Reflection Test Set

A.3 SUPPLY BULLETINS

Publication number	Title
SB 700-20	Dimensions, Weights, and Volume of Packaged Items

A.4 PAMPHLETS

Publication number	Title
DA Pam 738-750	Maintenance Management Update

A.5 ARMY REGULATIONS

Publication number	Title
AR 55-38	Reporting of Transportation Discrepancies in Shipments
AR 735-11-2	Report of Item and Packaging Discrepancies

A.6 FORMS

Publication number	Title
DA Form 2028	Recommended Changes to Publications
DA Form 2028-2 Test	Recommended Changes to Equipment Technical Manuals
SF 361	Transportation Discrepancy Report (TDR)
SF 364	Report of Discrepancy (ROD)
SF 368	Quality Deficiency Report

APPENDIX B

MAINTENANCE ALLOCATION

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B.1 GENERAL

This appendix provides a summary of the maintenance operations covered in the preceding chapters for Fast Direction Finding Test Set OQ-493/USD (FDF T/S group). It authorizes categories of maintenance for specific maintenance functions on repairable items and components and the tools and equipment required to perform each function. This appendix may be used as an aid in planning maintenance operations.

B.2 MAINTENANCE FUNCTIONS

Maintenance functions will be limited to, and defined, as follows:

B.2.1 Inspect
To determine the serviceability of an item by comparing its physical, mechanical, and/or electrical characteristics with established standards through examination.

B.2.2 Test
To verify serviceability and detect impending failure by measuring the mechanical or electrical characteristics of an item and comparing those characteristics against prescribed standards.

B.2.3 Service
Operations required periodically to keep an item in proper operating condition; i.e., to clean (decontaminate), preserve, drain, paint, or replenish fuel, lubricants, hydraulic fluids, or compressed air supplies.

B.2.4 Adjust
To maintain within prescribed limits, by bringing into proper or exact position, or by setting the operating characteristics to specified parameters.

B.2.5 Align
To adjust specified variable elements of an item to bring about optimum or desired performance.

B.2.6 Calibrate
To determine and cause corrections to be made or to be adjusted on instruments or test-measuring and diagnostic equipments used in precision measurement. Consists of comparisons of two instruments, one of which is a certified standard of known accuracy, to detect and adjust any discrepancy in the accuracy of the instrument being compared.

B.2.7 Install
The act of replacing, seating, or fixing into position an item, part, or module (component or assembly) in a manner to allow the proper functioning of a piece of equipment or a system.

B.2.8 Replace
The act of substituting a serviceable part, subassembly, or module (component or assembly) for an unserviceable counterpart.

B.2.9 Repair
The application of maintenance services or other maintenance actions to restore serviceability to an item by correcting specific damage, fault, malfunction or failure in a part, subassembly, module (component or assembly), end item, or system.

B.2.10 Overhaul
That maintenance effort (service/action) necessary to restore an item to a completely serviceable/operable condition as prescribed by maintenance standards (e.g., DMWR) in appropriate technical publications. Overhaul is normally the highest degree of maintenance performed by the Army.
Overhaul does not normally return an item to like-new condition.

B.2.11 Rebuild
Consists of those services/actions necessary for restoration of unserviceable equipment to a like-new condition in accordance with original manufacturing standards. Rebuild is the highest degree of material maintenance applied to Army equipment. The rebuild operation includes the act of returning to zero those age measurements (hours/miles, etc.) considered in classifying Army equipments/components.

B.2.12 Fault Locate
The act of finding the cause of a malfunction. When applicable to a system, the problem is traced to a piece of equipment. When applicable to a piece of equipment, the problem is traced to an assembly or circuit card assembly (CCA) within the equipment. When applicable to an assembly or CCA, the problem is traced to a component or sealed module.

B.2.13 Disassemble
Removal of modules/components from the equipment for the purpose of performing maintenance tasks (e.g., inspect, test, service, repair, etc.).

B.3 MAINTENANCE ALLOCATION CHART

Table B-I is the maintenance allocation chart (MAC) for the FDF T/S group. The following paragraphs describe the contents of each column in table B-1.

B.3.1 Column 1, Group Number
Column 1 lists group numbers to identify components, assemblies, subassemblies, and modules with the next higher assembly.

B.3.2 Column 2, Component/Assembly
Column 2 lists by formal nomenclature the components, assemblies, subassemblies, and modules for which maintenance is authorized. Each item is followed by its part number and reference designator. The reference designators are applied to all items appearing on the MAC and are similarly applied to the same item in the repair parts and special tools list (RPSTL).

B.3.3 Column 3, Maintenance Function
Column 3 lists the functions to be performed on the item listed in column 2.

B.3.4 Column 4, Maintenance Category
Column 4 specifies, by the listing of a "work time" figure in the appropriate subcolumn(s), the lowest level of maintenance authorized to perform the function listed in column 3. This figure represents the active time required to perform that function at the indicated category of maintenance. If the number or complexity of the task within the listed maintenance function varies at different maintenance categories, appropriate "work time" figures will be shown for each category. The number of man-hours specified by the "work time" figure represents the average time required to restore an item (assembly, subassembly, component, module, end item, or system) to a serviceable condition under typical field operation conditions. This time includes preparation time, troubleshooting time, and quality assurance/quality control time in addition to the time required to perform the specific tasks identified for the maintenance functions authorized in the MAC. The maintenance category subcolumns are as follows:

C-Operator/Crew
O-Organizational
F-Direct Support
H-General Support
D-Depot

B.3.5 Column 5, Tools and Equipment
Column 5 specifies, by code, those common tool sets (not individual tools) and special tools, test and support equipment required to perform the designated function. The code refers to table B-2, which lists the tool and test equipment requirements for the FDF T/S group.

B.3.6 Column 6, Remarks
Column 6 contains, when necessary, an alphabetic reference code leading to additional information (table B-3) pertaining to the item opposite the particular code.

B.4 TOOL AND TEST EQUIPMENT REQUIREMENTS

Table B-2 lists the tool and test equipment requirements for the FDF T/S group. The following paragraphs describe the contents of each column in table B-2.

B.4.1 Reference Code
The numbers in this column coincide with the numbers used in column 5 of table B1.

B.4.2 Maintenance Category
The codes in this column indicate the maintenance category allocated for the tool or test equipment.

B.4.3 Nomenclature
This column lists the noun name and nomenclature of the tools and test equipment required to perform the maintenance functions.

B.4.4 National/NATO Stock Number
This column lists the National/NATO stock number of the specific tool or test equipment.

B.4.5 Tool Number
This column lists the manufacturer's part number of the tool followed by the Federal supply code for manufacturers (five digits) in parentheses.

B.5 REMARKS

Table B-3 lists, when necessary, additional information pertaining to items in the MAC (table B-1). The following paragraphs describe the contents of each column in table B-3.

B.5.1 Reference Code
The codes in this column correspond to the codes in column 6 of table B-1.

B.5.2 Remarks
This column provides any information necessary to clarify items appearing in table B-1. The information opposite any given reference code pertains to the item in table B-1 that is opposite the same reference code in column 6.

Table B-1. Maintenance Allocation Chart for FDF T/S Group Equipment

(1) GROUP NUMBER	(2) COMPONENT/ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE CATEGORY					(5) TOOLS AND EQUPT	(6) REMARKS
			C	O	F	H	D		
00	Fast Direction Finding Test Set 00493/USD	Inspect		0.2				1	
		Service		0.1					
		Test		0.6					
		Test					2.0		
		Replace					4.0		A
		Repair			1.0				F
		Repair					6.0		
01	Patch Panel C5A2	Inspect			0.1			1	
		Test					1.0		
		Replace			0.5			1	
		Repair					2.0		E
02	Power Module Junction Box CSA6	Inspect			0.1				
		Test			0.5				
		Test					0.1	1	
		Repair			1.0			1	B
		Repair					4.0		E
03	Power Supplies CSA9, C5A10	Replace			0.2			1	
		Repair			*				C1
04	Digital Processor Test Set TS-4204/TSQ-105(V) C5A4	Inspect		0.1					
		Service		0.5				1	
		Test		0.2					D
		Test					1.0		
		Replace		0.2				1	
		Repair			0.6			1	B
		Repair					5.0		E
0401	68000 Common CCA C5A4A1	Inspect			0.1			1	
		Test					1.0		
		Replace			0.1			1	
		Repair					4.0		E
0402	68000 Processor CCA C5A4A2	Inspect			0.1			1	
		Test					1.0		
		Replace			0.1			1	
		Repair					4.0		E
0403	SCAR Interface CCA C5A4A6	Inspect			0.1			1	
		Test					1.0		
		Replace			0.1			1	
		Repair					4.0		E

Table B-1. Maintenance Allocation Chart for FDF T/S Group Equipment - Continued

(1) GROUP NUMBER	(2) COMPONENT/ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE CATEGORY					(5) TOOLS AND EQUPT	(6) REMARKS
			C	O	F	H	D		
0404	Serial Input/Output Interface CCA C5A4A7	Inspect			0.1			1	
		Test					1.0		
		Replace			0.1			1	
		Repair					4.0		E
0405	Data Link Interface CCA C5A4A8	Inspect			0.1			1	
		Test					1.0		
		Replace			0.1			1	
		Repair					4.0		E
0406	Parallel Input/Output Interface CCA C5A4A10	Inspect			0.1			1	
		Test					1.0		
		Replace			0.1			1	
		Repair					4.0		E
0407	General Purpose Interface Bus Interface CCA C5A4A11	Inspect			0.1			1	
		Test					1.0		
		Replace			0.1			1	
		Repair					4.0		E
0408	256K EPROM CCA C5A4A 15	Inspect			0.1			1	
		Test					1.0		
		Replace			0.1			1	
		Repair					4.0		E
0409	256K EPROM CCA C5A4A16	Inspect			0.1			1	
		Test					1.0		
		Replace			0.1			1	
		Repair					4.0		E
0410	256K EPROM CCA C5A4A17	Inspect			0.1			1	
		Test					1.0		
		Replace			0.1			1	
		Repair					4.0		E
0411	Digital Processor Backplane C5A4A29	Inspect			0.1			1	
		Test					1.0		
		Replace			0.1			1	
		Repair					4.0		E
	05AC/DC Power Cable Kit	Inspect			0.1				
		Test			0.5				
		Replace			0.5				A
		Repair			*				C2

Table B-1. Maintenance Allocation Chart for FDF T/S Group Equipment - Continued

(1) GROUP NUMBER	(2) COMPONENT/ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE CATEGORY					(5) TOOLS AND EQUPT	(6) REMARKS
			C	O	F	H	D		
06	Test Signals Cable Kit	Test Replace Repair		0.1 0.1	 *				 A C2
07	Frequency Doubler HP 11721A	Replace Repair		0.2	 *				 C3
08	ThinkJet Printer HP 2225A C3A3	Replace Repair		0.2	 *				 C4
09	Network Analyzer HP 8753C C2A2	Replace Repair		0.2	 *				 C5
901	Transmission/Rejection Test Set HP 85044A	Replace Repair		0.2	 *				 C12
10	Computer Terminal/VDT HP 700/96 C1064W C4A4	Replace Repair		0.2			 *		E E
11	Universal Counter HP 5335A C3A1	Replace Repair		0.2	 *				 C6
12	Oscilloscope TEK 2440 C3A2	Replace Repair		0.2	 *				 C7
13	Spectrum Analyzer HP 8560A C2A1	Replace Repair		0.2	 *				 C8
14	Synthesizer Function Generator Wavetek 288 C4A1	Replace Repair		0.2	 *				 C9
15	Signal Generator HP 8657B C4A2	Replace Repair		0.2	 *				 C10

Table B-1. Maintenance Allocation Chart for
FDF T/S Group Equipment - Continued

(1) GROUP NUMBER	(2) COMPONENT/ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE CATEGORY					(5) TOOLS AND EQUPT	(6) REMARKS
			C	O	F	H	D		
16	Logic Analyzer HP 16508 C4A3	Replace Repair		0.2	 *				 C11
17	Digital Multimeter Fluke 8840A/AF C5A1	Replace Repair		0.2	 *				 C13
18	ARF Intercept Receiver Pallet C5A3	Inspect Test Replace Repair Repair			0.1 0.1 1.0 		 1.0 4.0	1 1 1 	 B E

Table B-2. Tool and Test Equipment Requirements

Reference code	Maintenance category	Nomenclature	National/NATO stock number	Tool number
1	O, F	Electronic Equipment Tool Kit TK-17/G	5180-01-195-0855	

Table B-3. Remarks to MAC Items

Reference code	Remarks
A	Item is initial issue only and is not intended to be replaced below depot level.
B	Repair consists of the replacement of CCAs and chassis-mounted components and the replacement of individual connector contacts on cable assemblies:
C1	Refer to TM 11-6130-484-13 (Lambda Power Supply)
C2	Refer to TM 11-4940-485-13 (Airfield Maintenance Facility)
C3	Refer to TM 11-6625-3291-13 (Frequency Doubler HP 11721A)
C4	Refer to TM 11-7025-321-14 (Thinkjet Printer HP 2225A)
C5	Refer to TM 11-6625-3289-14 (Network Analyzer HP 8753C)
C6	Refer to TM 11-6625-3068-14 (Universal Counter HP 5335A)
C7	Refer to TM 11-6625-3283-14 (Oscilloscope TEK 2440)
C8	Refer to TM 11-6625-3286-14 (Spectrum Analyzer HP 8560A)
C9	Refer to TM 11-6625-3198-12 (Function Generator Wavetek 288)
C10	Refer to TM 11-6625-3281-14 (Signal Generator HP 8657B)
C11	Refer to TM 11-6625-3284-14 (Logic Analyzer HP 1650B)
C12	Refer to TO 33A1-15-86-1 (Transmission/Reflection Test Set HP 85044A)
C13	Refer to TM 11-6625-444-14-3 (Digital Multimeter Fluke 8840A/AF)
D	Test consists of power-up, self-test, and computer-directed diagnostics.
E	Return to depot for repair disposition and exchange.

APPENDIX C

COMPONENTS OF END ITEM LIST

C.1 SCOPE

This appendix provides a list of integral components of and basic issue items for Fast Direction Finding Test Set OQ-4931USD (FDF T/S group) to help inventory items required for safe and efficient operation.

C.2 INTEGRAL COMPONENTS OF END ITEM

Table C-1 lists the integral components for the FDF T/S group. These components, when assembled, comprise the FDF T/S group must accompany the equipment whenever the units are transferred or turned in. The illustrations will help you identify these items. The following paragraphs describe the contents of each column of table C-1.

C.2.1 Column 1, Illustration

Column 1 is divided as follows:

C.2.1.1 (A) Figure number

This column indicates the figure number of the illustration on which the item is shown.

C.2.1.2 (B) Item number

This number is used to identify items called out in the illustration.

C.2.2 Column 2, National Stock Number

Column 2 indicates the national stock number assigned to the item, which is used for requisitioning.

C.2.3 Column 3, Description

Column 3 indicates the Federal item name and, if required, a minimum description to identify the item. The part number indicates the primary number used by the manufacturer to control the design and characteristics of the item through its engineering drawings, specifications, standards, and inspection requirements. This number is used to identify an item or range of items.

Following the part number, the Commercial and Government Entity (CAGE) is shown in parentheses.

C.2.4 Column 4, Location

The physical location of each item listed is given in column 4. The list is designed to inventory all items in one area of the major item before moving on to an adjacent area.

C.2.5 Column 5, Usable on Code

Column 5 is not applicable.

C.2.6 Column 6, Qty Reqd (Quantity Required)

Column 6 lists the quantity of each item required for a complete major item.

C.3 BASIC ISSUE ITEMS

Not applicable.

Table C-1. Integral Components of End Item

(1) Illus		(2)	(3)	(4)	(5)	(6)
(A) Fig no.	(B) Item no.	National stock number	Description (Part no. and CAGE)	Location	Usable on code	Qty reqd
1-1		NA	Fast Direction Finding Test Set OQ-493/USD 21-186760-1	NA		1
1-3		7025-01-215-0313	Thinkjet Printer HP 2225A 16-185135-1 (28815)	C3A3		1
1-3		6625-01-276-9421	Synthesizer Function Generator SG-1288/G Wavetek 288 16-185133-1 (28815)	C4A1		1
1-3		6625-01-321-9286	Logic Analyzer HP 1650B 16-185140-1 (28815)	C4A3		1
1-3		6625-01-339-2391	Oscilloscope TEK 2440 16-185139-1 (28815)	C3A2		1
1-3		6625-01-282-8713	Digital Multimeter Fluke 8840A/AF 16-185141-1 (28815)	C5A1		1
1-3		6625-01-127-4955	Universal Counter HP 5335A 16-172190-1 (28815)	C3A1		1
1-3		6625-01-327-3123	Network Analyzer HP 8753C 16-185140-1 (28815)	C2A2		1
1-3		6625-01-323-1443	Spectrum Analyzer HP 8560A, w/Opt 002/003 16-185136-1 (28815)	C2A1		1
		6625-01-247-3963	Transmission/Reflection Test Set HP 85044A/B	None		1

Table C-1. Integral Components of End Item - Continued

(1) Illus		(2)	(3)	(4)	(5)	(6)
(A) Fig no.	(B) Item no.	National stock number	Description (Part no. and CAGE)	Location	Usable on code	Qty reqd
1-3		6625-01-341-3975	Signal Generator HP 8657B, w/Opt 001 16-185137-1 (28815)	C4A2		1
1-3		6130-01-xxx-xxxx	Power Supply Lambda 25699 (80103)	C5A9 C5A10		2
1-3		7025-01-289-1014	Computer Terminal HP700/96 C1064W (28480)	C4A4		1
1-3			Patch Panel Trompeter Electronics JS-24WD35F7/BJ28 (14949)	C5A2		1
1-3			ARF Intercept Receiver Pallet 10-182950-1 (28815)	C5A3		1
1-3		6625-01-236-8966	Digital Processor Test Set TS-4204/TSQ-105(V) 10-166609-1 (28815)	C5A4		1
1-3			Power Module Junction Box 10-162550-1 (28815)	C5A6		1
			Switch Box VDT/STE - PAM			1
		6625-01-140-8523	Frequency Doubler HP11721A (58279)			1
		6625-01-122-3438	Three-way Power Splitter HP11852B			1
		6625-01-127-0094	Minimum Loss Pad HP11852B			1
		5995-01-257-8317	N-Type Precision RF Cable Set HP11551B			1

Table C-1. Integral Components of End Item - Continued

(1) Illus (A) Fig no.	(1) Illus (B) Item no.	(2) National stock number	(3) Description (Part no. and CAGE)	(4) Location	(5) Usable on code	(6) Qty reqd
		5935-01-251-1472	50-Ohm N-Type Accessory Kit HP11853A			1
			75-Ohm N-Type Accessory Kit HP11855A			1
			ARF Maintenance Kit MX-2648 21-178363-1 (28815)			1
			AC/DC Power Cable Kit 21-164447-1 (28815)			1
			Coaxial Cable 09-188941-1 thru -7			7
			Test Signal Cable Kit 21-164448-1			1

APPENDIX D

ADDITIONAL AUTHORIZATION LIST

Not Applicable

APPENDIX E

EXPENDABLE AND DURABLE ITEMS LIST

E.1 SCOPE

This appendix provides a list of expendable supplies and material needed to operate and maintain Fast Direction Finding Test Set OQ-493/USD (FDF T/S group). These items are authorized by CTA 50-970, Expendable Items (except medical, Class V, repair Parts, and Heraldic Items).

E.2 EXPENDABLE SUPPLIES AND MATERIALS LIST

Table E-1 lists the expendable supplies and materials needed for operation of the FDF T/S group. The following paragraphs describe the contents of each column of table E-1.

E.2.1 Column 1, Item Number

Column 1 indicates the number assigned to the entry in the listing. This number is referenced in the narrative instructions to identify the materials (e.g., Use cleaning compound, item 5, appendix E).

E.2.2 Column 2, Level

Column 2 identifies the lowest level of maintenance that requires the listed item.

C-Operator/Crew
O-Organizational Maintenance
F-Direct Support Maintenance
H-General Support Maintenance

E.2.3 Column 3, National Stock Number

Column 3 indicates the national stock number (NSN) assigned to the item, which is used for requisitioning.

E.2.4 Column 4, Description

Column 4 indicates the Federal item name and, if required, a description to identify the item. The last line for each item indicates the part number followed by the Commercial and Government Entity (CAGE) in parenthesis, if applicable.

E.2.5 Column 5, Unit of Measure

Column 5 indicates the measure used in performing the actual maintenance function. this measure is expressed by a two-character alphabetic abbreviation (e.g., ea, in, pr). If the unit of measure differs from the unit of issue, requisition the lowest unit of issue that will satisfy the requirements.

Table E-1. Expendable Supplies and Materials

(1) Item No	(2) Level	(3) National Stock Number	(4) Description (Part No. and CAGE)	(5) Unit of Measure
1	F	N/A	Loctite	AR
2	O	8020-00-246-8806	Brush, soft	AR
3	O	8305-00-267-3015	Cloth, lint-free	AR
4	O	NA	Sandpaper, No. 000	AR
5	F	6810-01-310-8303	Alcohol, isopropyl	AR

APPENDIX F

WIRE LISTS

F.1 SCOPE

This appendix provides a list of power signal connections of Digital Processor Test Set TS-4204/TSQ105(V) (digital processor T/S C5A4). Power Module Junction Box (power junction box C5A6) wiring is shown in figure FO-2. Wiring information for internal and external unit under test (UUT) cables included as part of the Fast Direction Finding Test Set Group OQ-493/USD (FDF T/S group) are provided in the operation and maintenance manual for the ARF maintenance van.

F.2 DIGITAL PROCESSOR T/S POWER AND SIGNAL CONNECTIONS

Table F-1 lists the power and signal connections of digital processor T/S C5A4.

Table F-1. Digital Processor T/S C5A4 Power and Signal Connections

Connector	Pin	Function/Remarks
J1	2	SWOM input (grounded in cable W13, P/N 10-165117-1)
J1	3	SWIM input (grounded in cable W13, P/N 10-165117-1)
J1	4	SW2M input*
J1	5	SW0S input*
J1	6	SW1S input*
J1	7	SW2S input*
J1	8	SW0S2
J1	8	SW1S2
J1	10	SW2S2
J1	11-15	Spare
J1	16	IRQI3L0 input*
J1	17	IRQI3L1 input*
J1	18	IRQI3L2 input*
J1	20	ACIA INT1 output*
J1	21	ACIA INTO output*
J1	22	BHALTL input/output*
J1	23	BHALTL RTN input*
J1	24	FC2M output*
J1	25	PHALT1L input*
J1	26	FC2S1 output*
J1	27	PHALT2L input/output*
J1	28	FC2S2 output*
J1	29	PHALT3L input/output*
J1	30	CTS 1 input*
J1	31	CTS1 RTN*
J1	32	CTSO input*
J1	33	CTSO RTN*
J1	34	GND 01-34
J1	35	EXT RESET input*
J1	36	IRQ7M input*
J1	37	IRQ7M RTN*
J1	38	IRQ7S1 input*
J1	39	IRQ7S 1 RTN*
J1	40	IRQ7S2 input*
J1	41	IRQ7S2 RTN*
J1	42	INPUT A POS input/data from ARF and IPF digital processors under test
J1	43	INPUT A NEG input*
J1	44	OUTPUT A output/test data from digital processor T/S to ARF or IPF digital processor under test
J1	45	OUTPUT B output*
J1	46	INPUT B POS input/data input from alphanumeric display terminal

*Not connected externally

Table F-1. Digital Processor T/S C5A4 Power and Signal Connections - Continued

Connector	Pin	Function/Remarks
J1	47	INPUT B NEG input*
J1	48	OUTPUT C output*
J1	49	OUTPUT D output/data from digital processor T/S to alphanumeric display terminal for display
J1	50	MODE input*
J1	51	VEE input*
J1	52	RS ENABLE input (active low RS-422 mode)*
J1	53	GND 01-53
J1	54	EXT RESET input*
J1	55	GND 01-55 (connected to chassis)
J2	1	GND 02-1, 13 (connected to SCAR processor level 0 under test)
J2	2	SCR DAT IN POS input connected to SCAR processor level 0 under test
J2	3	SCR DAT IN NEG input connected to SCAR processor level 0 under test
J2	4	SCR DAT CLK POS input connected to SCAR processor level 0 under test
J2	5	SCR DAT CLK NEG input connected to SCAR processor level 0 under test
J2	6	SCR DAT LD POS input connected to SCAR processor level 0 under test
J2	7	SCR DAT LD NEG input connected to SCAR processor level 0 under test
J2	8	SCR CMD RDY POS input connected to SCAR processor level 0 under test
J2	9	SCR CMD RDY NEG input connected to SCAR processor level 0 under test
J2	10	AGC DUMP output*
J2	11	AGC DUMP RTN*
J2	12	Spare
J2	13	GND 02-1, 13 (connected to SCAR processor level 0 under test)
J2	14	RX RDY IN (not connected to SCAR interface CCA C5A4A6)
J2	15	RX RDY IN RTN (not connected to SCAR interface CCA C5A4A6)
J2	16-17	Spare
J2	18	DATA OUT BO (not connected to SCAR interface CCA C5A4A6)
J2	19	DATA OUT B0 RTN (not connected to SCAR interface CCA C5A4A6)

*Not connected externally

Table F-1. Digital Processor T/S C5A4 Power and Signal Connections - Continued

Connector	Pin	Function/Remarks
J2	20	TX RDY BO (not connected to SCAR interface CCA C5A4A6)
J2	21	TX RDY BO RTN (not connected to SCAR interface CCA C5A4A6)
J2	22	BT CK OUT0 (not connected to SCAR interface CCA C5A4A6)
J2	23	BT CK OUT0 RTN (not connected to SCAR interface CCA C5A4A6)
J2	24, 25	Spare
J2	26	DAT IN CO (not connected to SCAR interface CCA C5A4A6)
J2	27	DAT IN CO RTN (not connected to SCAR interface CCA C5A4A6)
J2	28	TX RDY CO (not connected to SCAR interface CCA C5A4A6)
J2	29	TX RDY CO RTN (not connected to SCAR interface CCA C5A4A6)
J2	30	SCR DATDY POS output (connected to SCAR processor level 0 under test)
J2	31	SCR DATDY NEG output (connected to SCAR processor level 0 under test)
J2	32	RX CMD LD POS output*
J2	33	RX CMD LD NEG output*
J2	34	GND 02-34, 53*
J2	35	Spare
J2	36	RX CMD CLK POS output*
J2	37	RX CMD CLK NEG output*
J2	38	RX CMD POS output*
J2	39	RX CMD NEG output*
J2	40	SCR CMD LD POS output (connected to SCAR processor level 0 under test)
J2	41	SCR CMD LD NEG output (connected to SCAR processor level 0 under test)
J2	42	SCR CMD CLK POS output (connected to SCAR processor level 0 under test)
J2	43	SCR CMD CLK NEG output (connected to SCAR processor level 0 under test)
J2	44	SCR CMD POS output (connected to SCAR processor level 0 under test)
J2	45	SCR CMD NEG output (connected to SCAR processor level 0 under test)
J2	46 - 52	Spare
J2	53	GND 02-34, 53 (connected to SCAR processor level 0 under test)
J2	54	Spare
J2	55	GND 02-55 (connected to chassis)

*Not connected externally

Table F-1. Digital Processor T/S C5A4 Power and Signal Connections - Continued

Connector	Pin	Function/Remarks
J3	1	GND 03-1, 13 (jumpered to connector J3, pin 13)*
J3	2	DAT OUT Al output**
J3	3	DAT OUT Al RTN output**
J3	4	TX RDY Al output**
J3	5	TX RDY Al RTN output**
J3	6	BT CK OUT A1 output**
J3	7	BT CK OUT Al RTN output**
J3	8	RX RDY Al input*
J3	9	RX RDY Al RTN input*
J3	10-12	Spare
J3	13	GND 03-1, 13 (jumpered to connector J3, pin 13)*
J3	14	RX RDY B1 input**
J3	15	RX RDY B1 RTN input**
J3	16,17	Spare
J3	18	DAT OUT B output**
J3	19	DAT OUT B1 RTN output**
J3	20	TX RDY B1 output**
J3	21	TX RDY B1 RTN output**
J3	22	BT CK OUT B1 output**
J3	23	BT CK OUT B1 RTN output**
J2	24,25	Spare
J3	26	DAT IN C1 input**
J3	27	DAT IN C1 RTN input**
J3	28	TX RDY C1 input**
J3	29	TX RDY C1 RTN input**
J3	30	BT CK IN C1 input**
J3	31	BT CK IN C1 RTN input**
J3	33	RX RDY C1 output**
J3	34	GND 03-34, 53 (jumpered to connector J3, pin 53)*
J3	35-52	Spare
J3	53	GND 03-34, 53 (jumpered to connector J3, pin 34)*
J3	54	Spare
J3	55	GND 03-55 (connected to chassis)
J4	-	CH B 446 kHz IF input/RF connector (not connected internally or externally)
J5	-	AGC input/RF connector (not connected internally or externally)

*Not connected externally
**Connected to LRU under test

Table F-1. Digital Processor T/S C5A4 Power and Signal Connections - Continued

Connector	Pin	Function/Remarks
J6	1	GND 06-1*
J6	2	BRQ1L input*
J6	3	BRQ1L RTN input*
J6	4	BHALTL input*
J6	5	BHALTL RTN input*
J6	6-9	Spare
J6	10	BSACKL input*
J6	11	BSACKL RTN input*
J6	12	BEVENTL output*
J6	13	BEVENTL RTN output*
J6	14	BDOUTL input*
J6	15	BDOUTL RTN input*
J6	16	BRPLYL output*
J6	17	BRPLYL RTN output*
J6	18	BDINL input*
J6	19	BDINL RTN input*
J6	20	BSYNCL input*
J6	21	BSYNCL RTN input*
J6	22	BWTBTL output*
J6	23	BWTBTL RTN output*
J6	24	BIRQL output*
J6	25	BIRQL RTN output*
J6	26	BIAKOL output*
J6	27	BIAKOL RTN output*
J6	28	BBS7L output*
J6	29	BBS7L RTN output*
J6	30	BDMGOL input*
J6	31	BDMGOL RTN input*
J6	32	BINITL input*
J6	33	BINITL RTN input*
J6	34	RTN
J6	35	RTN
J6	36	+5 VDC
J6	37	+5 VDC
J6	38	+5 VDC
J6	39	+5 VDC
J6	40	PROM SEL input/grounded*
J6	41	Spare
J6	42	Spare
J6	43	Spare
J6	44	PGML output (connected to VCC)*
J6	45	Spare
J6	46	BDAL0L/common bus*
J6	47	BDAL0L RTNmon bus*
J6	48	BDAL1L/common bus*
J6	49	BDAL1L RTNmon bus*

*To DPU terminator

Table F-1. Digital Processor T/S C5A4 Power and Signal Connections - Continued

Connector	Pin	Function/Remarks
J6	50	BDAL2L/common bus*
J6	51	BDAL2L RTN/common bus*
J6	52	BDAL3L/common bus*
J6	53	BDAL3L RTN/common bus*
J6	54	BDAL4L/common bus*
J6	55	BDAL4L RTN/common bus*
J6	56	BDAL5L/common bus*
J6	57	BDAL5L RTN/common bus*
J6	58	BDAL6L/common bus*
J6	59	BDAL6L RTN/common bus*
J6	60	BDAL7L/common bus*
J6	61	BDAL7L RTN/common bus*
J6	62	BDAL8L/common bus*
J6	63	BDAL8L RTN/common bus*
J6	64	BDAL9L/common bus*
J6	65	BDAL9L RTN/common bus*
J6	66	BDAL10L/common bus*
J6	67	BDAL10L RTN/common bus*
J6	68	BDAL11L/common bus*
J6	69	BDAL11 L RTN/common bus*
J6	70	BDAL12L/common bus*
J6	71	BDAL12L RTN/common bus*
J6	72	BDAL13L/common bus*
J6	73	BDAL13L RTN/common bus*
J6	74	BDAL14L/common bus*
J6	75	BDAL14L RTN/common bus*
J6	76	BDAL15L/common bus*
J6	77	BDAL15L RTN/common bus*
J6	78	GND 06-78*
J6	79	VCC*
J6	80	PBL (connected to VCC)*
J6	81	PGM 0 input*
J6	82	PGM 1 input*
J6	83	PGM 2 input*
J6	84	PGM 3 input*
J6	85	PGM 4 input*
J6	86	PGM 5 input*
J6	87	PGM 6 input*
J6	88	PGM 7 input*
J6	89	PGM 8 input*
J6	90	PGM 9 input*
J6	91	CSE (connected to VCC)*
J6	92	PGM 10 input*
J6	93	PGM 11 input*
J6	94	PGM 12 input*

*To DPU terminator

Table F-1. Digital Processor T/S C5A4 Power and Signal Connections - Continued

Connector	Pin	Function/Remarks
J6	95	PGM 13 input*
J6	96	PGM 14 input*
J6	97	PGM 15 input*
J6	98	PBWE input (connected to VCC)*
J6	99	GND 06-99*
J6	100	GND 06-100 (connected to chassis)
J7	-	CH A 446 kHz IF input/RF connector (not connected internally or externally)
J8	-	Not installed
J9	1-23	Spare
J9	24	1 MHz 1 POS output**
J9	25	1 MHz 1 NEG output**
J9	26	1 MHz 1 DISABLE input/grounded to pin 53, connector P2, in cable W2, P/N 10-164856-1, and grounded to pin 53, connector P1, in cable W12, P/N 10-165116-1 (not connected to LRU under test)
J9	27-33	Spare
J9	34	GND 09-34, 53 (jumpered to connector J9, pin 53)**
J9	35-37	Spare
J9	38	DATA TX1 output*
J9	39	DATA TX1 RTN input*
J9	40	CLOCK TX1 input*
J9	41	CLOCK TX1 RTN input*
J9	42	DATA RX1 input*
J9	43	DATA RX1 RTN input*
J9	44	CLOCK RX1 input*
J9	45	CLOCK RX1 RTN output*
J9	46-52	Spare
J9	53	GND 09-34, 53 (jumpered to connector J9, pin 34)
J9	54	Spare
J9	55	GND 09-55 (connected to chassis)
J10	1	GND 10-1, 13 (jumpered to connector J10, pin 13)
J10	2	INS DAT POS input**
J10	3	INS DAT NEG input**
J10	4	INS CLK POS input***

*To DPU terminator
**Connected to LRU under test
***Not connected externally

Table F-1. Digital Processor T/S C5A4 Power and Signal Connections - Continued

Connector	Pin	Function/Remarks
J10	5	INS CLK NEG input*
J10	6	INS SYNC POS input*
J10	7	INS SYNC NEG input*
J10	8	TEST SYNC POS input*
J10	9	TEST SYNC NEG input*
J10	10	TEST CLK POS output*
J10	11	TEST CLK NEG output*
J10	12	NES SYNC IN POS input*
J10	13	GND 10-1, 13 (jumpered to connector J10, pin 1)*
J10	14	AEP DAT POS output*
J10	15	AEP DAT NEG output*
J10	16	AEP CLK POS input*
J10	17	AEP CLK NEG input*
J10	18	TEST SET input*
J10	19	TEST SET RTN input*
J10	20	OUT 0 POS output*
J10	21	OUT 0 NEG output*
J10	22	OUT 1 POS output*
J10	23	OUT 1 NEG output*
J10	24	OUT 2 POS output*
J10	25	OUT 2 NEG output*
J10	26	1 MHz 2 DISABLE output*
J10	27-33	Spare
J10	34	GND 10-34, 53 (jumpered to connector J10, pin 53)*
J10	35	NES SYNC IN NEG input*
J10	36,37	Spare
J10	38	DATA TX2 input*
J10	39	DATA TX2 RTN input*
J10	40	CLOCK TX2 input*
J10	41	CLOCK TX2 RTN input*
J10	42	DATA RX2 input*
J10	43	DATA RX2 RTN input*
J10	44	CLOCK RX2 input*
J10	45	CLOCK RX2 RTN input*
J10	46-52	Spare
J10	53	GND 10-34, 53 (jumpered to connector J10, pin 34)*
J10	54	Spare
J10	55	GND 10-55 (connected to chassis)
J11	1	GND 11-1, 13 (jumpered to connector J11, pin 13)*

*Not connected externally

Table F-1. Digital Processor T/S C5A4 Power and Signal Connections - Continued

Connector	Pin	Function/Remarks
J11	2	DIO1 POS bidirectional line (connected to signal generator C4A2 and function generator C4A1)
J11	3	DIO1 NEG*
J11	4	DIO2 POS bidirectional line (connected to signal generator C4A2 and function generator C4A1)
J11	5	DIO2 NEG*
J11	6	DIO3 POS bidirectional line (connected to signal generator C4A2 and function generator C4A1)
J11	7	DIO3 NEG*
J11	8	DIO4 POS bidirectional line (connected to signal generator C4A2 and function generator C4A1)
J11	9	DIO4 NEG*
J11	10	DIO5 POS bidirectional line (connected to signal generator C4A2 and function generator C4A1)
J11	11	DIO5 NEG*
J11	12-13	Spare
J11	14	DIO6 POS bidirectional line (connected to signal generator C4A2 and function generator C4A1)
J11	15	DIO6 NEG*
J11	16	DIO7 POS bidirectional line (connected to signal generator C4A2 and function generator C4A1)
J11	17	DIO7 NEG*
J11	18	DIO8 POS bidirectional line (connected to signal generator C4A2 and function generator C4A1)
J11	19	DIO8 NEG*
J11	20	TX RDY B2 (not implemented on GPIB interface CCA C5A4A11)
J11	21	TX RDY B2 RTN (not implemented on GPIB interface CCA C5A4A11)
J11	22	ATN POS bidirectional line (connected to signal generator C4A2 and function generator C4A1)
J11	23	ATN NEG bidirectional line (connected to signal generator C4A2 and function generator C4A1)
J11	24	IFC POS bidirectional line (connected to signal generator C4A2 and function generator C4A1)

*Not connected externally

Table F-1. Digital Processor T/S C5A4 Power and Signal Connections - Continued

Connector	Pin	Function/Remarks
J11	25	IFC NEG bidirectional line (connected to signal generator C4A2 and function generator C4A1)
J11	26	EOI POS bidirectional line (connected to signal generator C4A2 and function generator C4A1)
J11	27	EOI NEG bidirectional line (connected to signal generator C4A2 and function generator C4A1)
J11	28	SRQ POS bidirectional line (connected to signal generator C4A2 and function generator C4A1)
J11	29	SRQ NEG bidirectional line (connected to signal generator C4A2 and function generator C4A1)
J11	30	REN POS bidirectional line (connected to signal generator C4A2 and function generator C4A1)
J11	31	REN NEG bidirectional line*
J11	32	NRFD POS bidirectional line (connected to signal generator C4A2 and function generator C4A1)
J11	33	NRFD NEG bidirectional line (connected to signal generator C4A2 and function generator C4A1)
J11	34,35	Spare
J11	36	NDAC POS bidirectional line (connected to signal generator C4A2 and function generator C4A1)
J11	37	NDAC NEG bidirectional line (connected to signal generator C4A2 and function generator C4A1)
J11	38	DAV POS bidirectional line (connected to signal generator C4A2 and function generator C4A1)
J11	39	DAV NEG bidirectional line (connected to signal generator C4A2 and function generator C4A1)
J11	40-54	Spare
J11	55	GND 11-55 (connected to chassis)
J12	1	GND 12-1, 13 (jumpered to connector J12, pin 13)*
J12	2	DAT A output*
J12	3	DAT B output*
J12	4	STB A output*

*Not connected externally

Table F-1. Digital Processor T/S C5A4 Power and Signal Connections - Continued

Connector	Pin	Function/Remarks
J12	5	STB B output*
J12	6	CLK A output*
J12	7	CLK B output*
J12	8-17	Spare
J12	18	DAT C output*
J12	19	DAT D output*
J12	20	STB C output*
J12	21	STB D output*
J12	22	CLK C output*
J12	23	CLK D output*
J12	24-54	Spare
J12	55	GND 12-55 (connected to chassis)
J13	-	Not implemented
J14	A	115 V ac, 400 Hz, phase 1 input (not used by digital processor T/S - connected to connector J19, pin 1)
J14	B	115 V ac, 400 Hz, phase 2 input (not used by digital processor T/S - connected to connector J19, pin 2)
J14	C	115 V ac; 400 Hz, phase 3 input (not used by digital processor T/S - connected to connector J19, pin 3)
J14	D	120 V ac neutral input (used by digital processor T/S blower - connected to connector J19, pin 4)
J14	E	Sensor input (used by digital processor T/S heat sensor)
J14	F	Heat input (used by digital processor T/S heat sensor)
J14	G	120 V ac, 60 Hz input (used by digital processor T/S blower - connected to connector J19, pin 5)
J14	H	GND (connected to chassis)
J15	A	+5 V dc input (from connector J4 of power junction box C5A6)
J15	B	GND input (from connector J4 of power junction box C5A6)
J15	C	+5 V dc input (from connector J4 of power junction box C5A6)
J15	D	GND input (from connector J4 of power junction box C5A6)
J15	C	+5 V dc input (from connector J4 of power junction box C5A6)

*Not connected externally

Table F-1. Digital Processor T/S C5A4 Power and Signal Connections - Continued

Connector	Pin	Function/Remarks
J15	D	GND input (from connector J4 of power junction box C5A6)
J15	E	+5 V dc input (from connector J4 of power junction box C5A6)
J15	F	GND input (from connector J4 of power junction box C5A6)
J15	G	+5 V dc input (from connector J4 of power junction box C5A6)
J15	H	GND input (from connector J4 of power junction box C5A6)
J15	J	+15 V dc input (from connector J4 of power junction box C5A6)
J15	K	GND input (from connectorJ4 of power junction box C5A6)
J15	L	-15 V dc input (from connector J4 of power junction box C5A6)
J15	M	GND input (from connector J4 of power junction box C5A6)
J15	N	+5 V dc input (from connector J4 of power junction box C5A6)
J15	P	GND input (from connector J4 of power junction box C5A6)
J15	R	+5 V dc input (from connector J4 of power junction box C5A6)
J15	S	GND input (from connector J4 of power junction box C5A6)
J16	1	GND 16-1, 13 (jumpered to connector JI6, pin 13)*
J16	2	DAT OUT A3 output*
J16	3	DAT OUT A3 RTN output*
J16	4	TX RDY A3 output*
J16	5	TX RDY A3 RTN output*
J16	6	BT CK OUT A3 output*
J16	7	BT CK OUT A3 RTN output*
J16	8	RX IN A3 input*
J16	9	RX IN A3 RTN input*
J16	10	EXT CK IN A3 input*
J16	11	EXT CK IN A3 RTN input*
J16	12	Spare
J16	13	GND
J16	14	RX IN B3 input*
J16	15	RX IN B3 RTN input*
J16	16, 17	Spare
J16	18	DAT OUT B3 output*
J16	19	DAT OUT B3 RTN output*

*Not connected externally

Table F-1. Digital Processor T/S C5A4 Power and Signal Connections - Continued

Connector	Pin	Function/Remarks
J16	20	TX LD B3 output*
J16	21	TX LD B3 RTN output*
J16	22	BT CK OUT B3 output*
J16	23	BT CK OUT B3 RTN output*
J16	24,25	Spare
J16	26	DAN IN C3 input*
J16	27	DAT IN C3 RTN input*
J16	28	TX LD C3 input*
J16	29	TX LD C3 RTN input*
J16	30	BT CK IN C3 input*
J16	31	BT CK IN C3 RTN input*
J16	32	RX OUT C3 output*
J16	33	RX OUT CE RTN output*
J16	34	GND 16-34*
J16	35 - 54	Spare
J16	55	GND 16-55 (connected to chassis)
J17	-	Not implemented
J18	1	Spare
J18	2	IO1 POS output**
J18	3	IO1 NEG output**
J18	4	IO2 POS output**
J18	5	IO2 NEG output**
J18	6	IO3 POS output**
J18	7	IO3 NEG output**
J18	8	IO4 POS output**
J18	9	IO4 NEG output**
J18	10	IO5 POS output**
J18	11	IO5 NEG output**
J18	12	Spare
J18	13	GND 18-13*
J18	14	IO6 POS output**
J18	15	IO6 NEG output**
J18	16	IO7 POS output**
J18	17	IO7 NEG output*
J18	18	IO8 POS output**
J18	19	IO8 NEG output*
J18	20	IO9 POS output**
J18	21	IO9 NEG output*
J18	22	IO10 POS output**
J18	23	IO10 NEG output*
J18	24	IO11 POS output*
J18	25	IO11 NEG output*
J18	26	IO12 POS output*

*Not connected externally
**Connected to LRU under test

Table F-1. Digital Processor T/S C5A4 Power and Signal Connections - Continued

Connector	Pin	Function/Remarks
J18	25	IO11 NEG output*
J18	26	IO12 POS output*
J18	27	IO12 NEG output*
J18	28, 29	Spare
J18	30	DATA HIGH output*
J18	31	DATA LOW output*
J18	32	CLK HIGH output*
J18	33	CLK LOW output*
J18	34	GND 18-34, 53 (jumpered to connector J18, pin 53)
J18	35 - 37	Spare
J18	38	TX DAT output*
J18	39	TX TAD RTN output*
J18	40	TX CLK output*
J18	41	TX CLK RTN output*
J18	42	RX DAT output*
J18	43	RX DAT RTN output*
J18	44	RX CLK output*
J18	45	RX CLK RTN output*
J18	46 - 52	Spare
J18	53	GND 18-34, 53 (jumpered to connector J18, pin 34)*
J18	54	Spare
J18	55	GND 18-55 (connected to chassis)
J19	1	115 V ac, 400 Hz, phase 1 input (from connector J14, pin A - not used by digital processor T/S)
J19	2	115 V ac, 400 Hz, phase 2 input (from connector J14, pin B - not used by digital processor T/S)
J19	3	115 V ac, 400 Hz, phase 3 input (from connector J14, pin C - not used by digital processor T/S)
J19	4	120 V ac neutral input (from connector J14, pin D - used by digital processor T/S blower)
J19	5	120 V ac, 60 Hz input (from connector J14, pin G - used by digital processor T/S blower)
J19	6 - 9	Spare

*Not connected externally

GLOSSARY

The following is a glossary of acronyms and abbreviations used in the Fast Direction Finding Test Set OQ-493/USD (FDF T/S group):

Acrornym/Abbrev.	Definition
A	Ampere
AC	Alternating current
ACCUM	Accumulation
ACIAINTO and ACIAINTI	Asynchronous communications interface adapter, interrupt 0 and 1
ACULOAD	Accumulator load
ADOVRFLO	Address overflow
AD1 - ADO1	Address bits 1 thru 10
AD1 -AD11	Address bits 1 thru 11
ADEN	Address enable
ADERR	Address error (DMA status bit)
ADL1 - ADL12	Latched address bits 1 thru 12
AEP	Airborne executive processor
AER	Address error (rollover)
AGC	Automatic gain control
AM	Amplitude modulation
AMP	Amplitude
ARF	Airborne relay facility
ARO	Address rollover
ATN	Attention
BCT	Byte counter (clock)
BCZ	Byte count zero
BDALOL - BDAL15L	Bus data/address lines 0 thru 15 low (common bus data/address lines)
BDAL16L - BDAL22L	Bus data/address lines 16 thru 22 low (common bus extended address lines)
BDINL	Bus data in low
BDMGIL	Bus direct memory grant in low (DMA)
BDMGOL	Bus direct memory grant out low (DMA)
BDMRL	Bus direct memory request low (DMA)
BDOUTL	Bus data out low
BEVENTL	Bus event low
BGRANTL	Bus grant low
BHALT	Bus halt
BIAKIL	Bus interrupt acknowledge in low
BIAKOL	Bus interrupt acknowledge out low
BINITL	Bus initialize low (system reset)
BIRQL	Bus interrupt request low
BREPLYL	Bus reply low
BREQL	Bus request low
BSACKL	Bus acknowledge low

Acronym/Abbrev.	Definition
BSYNCL	Bus synchronize (address) low
BTCK	Byte clock
BWTBTL	Bus write byte low
C	Celsius
CCA	Circuit card assembly
CER	Clock enable R register
CES	Clock enable S register
CH	A/CH BChannel A/channel B
CK	Clock (MS byte of DMA address register)
CKM	Clock (interrupt) mask (register)
CLK	Clock
CLRDST	Clear DMA status (register)
CLRR	Clear R (register)
CMD	Command
CNTRL	Control bit
COEFFO - COEFF11	Coefficient bits 0 thru 11
CORREL	Correlation
CPU	Central processing unit
CS	Chip select
CSE	Chip select enable
CTS	Clear to send
CW	Continuous wave
DALI - DAL22	Data/address low (bits) 1 thru 22
DAT	Data
DATIN	Data in
DAV	Data available
DB	Decibel
DBM	Decibel power measurement referred to 1 milliwatt
DC	Direct current
DCAD	(Decoded) DAM control (register) address
DF	Direction finding
DIO1 - DIO8	Data input/output bits 1 thru 8 (IEEE Standard-488 Interface Bus)
DIV	Division
DMA	Direct memory access
DMAD	(Decoded) DMA address (register address)
DMAEN	Direct memory access enable
DMAG	Direct memory access grant
DMAIN	Direct memory access in
DMAP	Direct memory access pending
DMAR	Direct memory access request (by GPIA)
DPU	Digital processor unit
DTEN	Data enable
EMI	Electromagnetic interference
ENB	Enable
ENDC	End (message) conditioned (by DMA cycle end)
ENDM	End message
ENS	Enable (DMA) status
EOI	End or identify

Acrorym/Abbrev.	Definition
EPROM	Erasable programmable read-only memory
EXT	External
FDF	Fast direction finding
FIF00 - FIFO15	First-in/first-out bits 0 thru 15
FM	Frequency modulation
GND	Ground
GPAD	(Decoded) general purpose interface adapter address
GPIA	General purpose interface adapter
GPIB	General purpose interface bus
GT/R	Generate transmit/receive
HORZ	Horizontal
IACKL	Interrupt acknowledge low
IATN	Interrupt attention
IENA	(Attention) interrupt enable
IENE	Interrupt enable EOI
IENF	Interrupt enable interface clear
IENS	Interrupt enable SRQ
I/F	Interface
IF	Intermediate frequency
IFC	Interface clear
INS	Inertial navigation system
INT	Interrupt
INTA	Interrupt attention (pending)
INTAL	Interrupt attention (pending) latched
INTD	Interrupt DMA (pending)
INTDL	Interrupt DMA (bit) latched
INTDS	Interrupt DMA strobe
INTE	Interrupt EOI (pending)
INTEL	Interrupt EOI (pending) latched
INTEN	Interrupt enable (GPIB CCA)
INTF	Interrupt IFC (pending)
INTS	Interrupt SRQ (pending)
INTSL	Interrupt SRQ (pending) latched
IPF	Integrated processing facility
IRCLK	Interrupt (acknowledge) clock (strobe)
IREQ	Interrupt request (GPIA)
IREQL	Interrupt request (GPIA) latched
IREQP	Interrupt request (GPIA) pending
IRQ1L thru 1RQ6L	Interrupt request priority level 1 low thru Interrupt request priority level 6 low
ISRQ	Interrupt SRQ (buffered)
KYBD	Keyboard
LBYT	Lower byte (write from C-bus)
LD	Load
LDS	Lower data strobe
LED	Light emitting diode
LOADC	Load counter (DMA byte)

Acronym/Abbrev.	Definition
LOADL	Load least (significant byte DMA address register)
LOADU	Load (middle byte DMA address register)
LRU	Line-replaceable unit
LS	Least significant
MAG	Magnitude
MOD	Modulation
MS	Most significant
NDAC	No data accepted
NEG	Negative
NRFD	Not ready for data
NVM	Nonvolatile memory
OEC	Output enable counter (DMA byte)
OEH	Output enable high (MS) (byte DMA address to internal GPIB bus)
OEM	Output enable middle (and least significant bytes of DMA address to internal GPIB bus)
OES	Output enable strobe (data to GPIA)
PAL	Programmable array logic
PGM	Program
PIO	Parallel input/output
PM	Pulse modulation
P10/O	Part of
POS	Positive
PROM	Programmable read-only memory
PS	Power supply
RAM	Random access memory (read/write)
RCVR	Receiver
REF	Reference
REN	Remote enable
RF	Radio frequency
RMS	Root mean square
RP9	Reply 9 (for data input from GPIA)
RPGN	Reply generate (decoded address FFF830 to FFF83A)
RPLC	Reply clock (strobe from data output to GPIA)
RPLG	Reply generate (for interrupt)
RS	Reset
RTN	Return
RWB	Read/write (not) (GPIA to be conditioned)
R/W (NOT)	Read/write (not) (68488 GPIA)
RX	Receiver
RXRDY	Receiver ready
SCAR	Signal classification, acquisition, and recognition
SCRCMDCLK	SCAR command clock
SCRCMDLD	SCAR command load
SCRCMDRDY	SCAR command ready
SCRDATCLK	SCAR data clock

Acrornym/Abbrev.	Definition
SCRDATIN	SCAR data in
SCRDATLD	SCAR data load
SEC	Second
SEL	Select
SOE	Strobe enable (DMA termination on end message)
SRQ	Service request
SWOM - SW2M	Switch bits 0 thru 2 M
SYNTH	Synthesizer
TCAD	Byte counter address (decoded)
T/S	Test set
TB	Terminal block
TO	Time out
TOERR	Time out error (DMA status bit)
TX	Transmitter
TXRDY	Transmitter ready
UDS	Upper data strobe (byte address)
UHF	Ultrahigh frequency
VA	Voltampere
VDT	Video display terminal
VERT	Vertical
VHF	Very high frequency
V/S-NOT	Vector or status (not) for PAL-A
VSWR	Voltage standing wave ratio
WRT	Write

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NOTES (UNLESS OTHERWISE SPECIFIED):
1. * LOWBAND

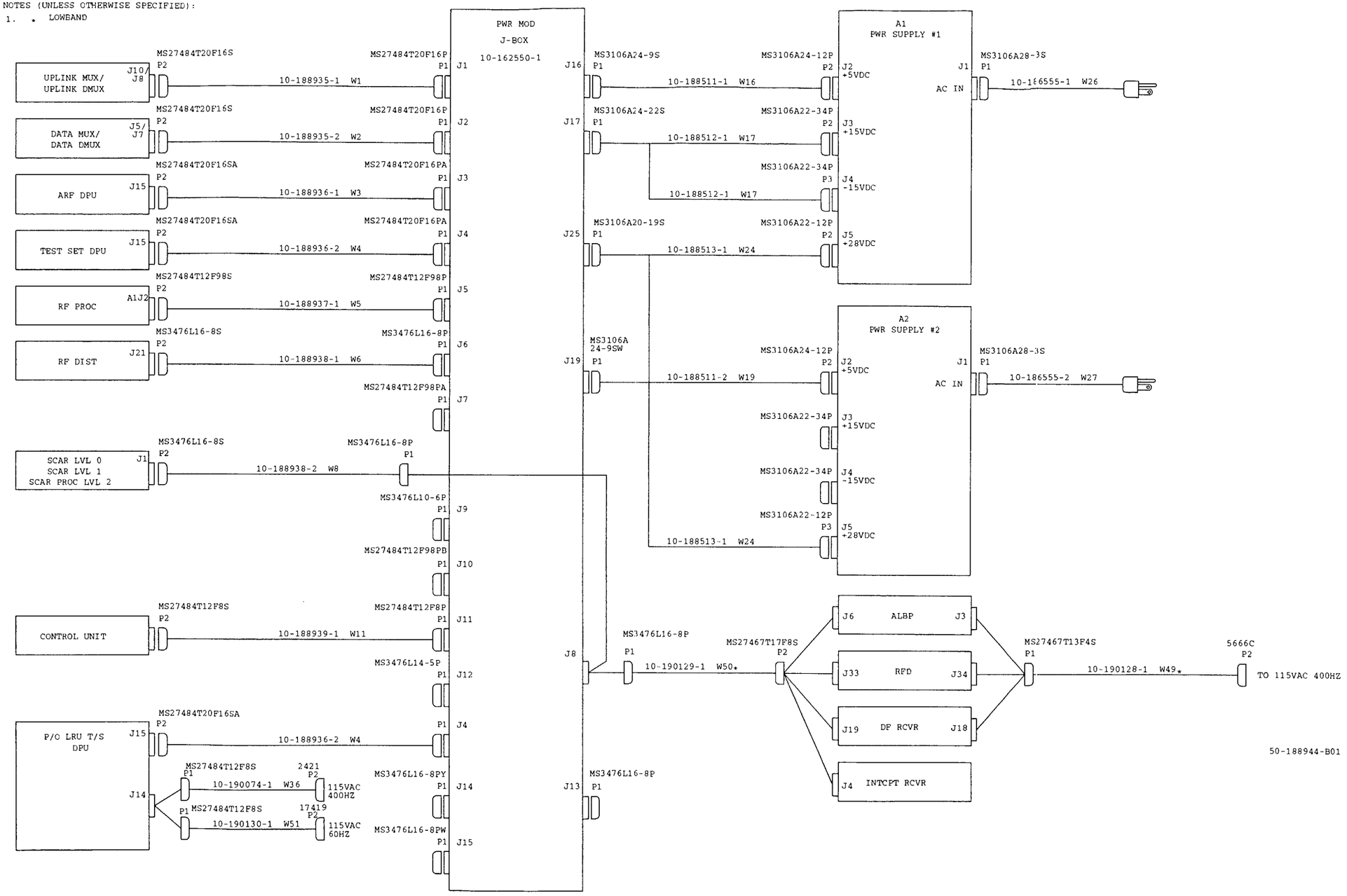

Figure FO-1. FDFT/S GROUP CABLING DIAGRAM (Sheet 1 of 3)

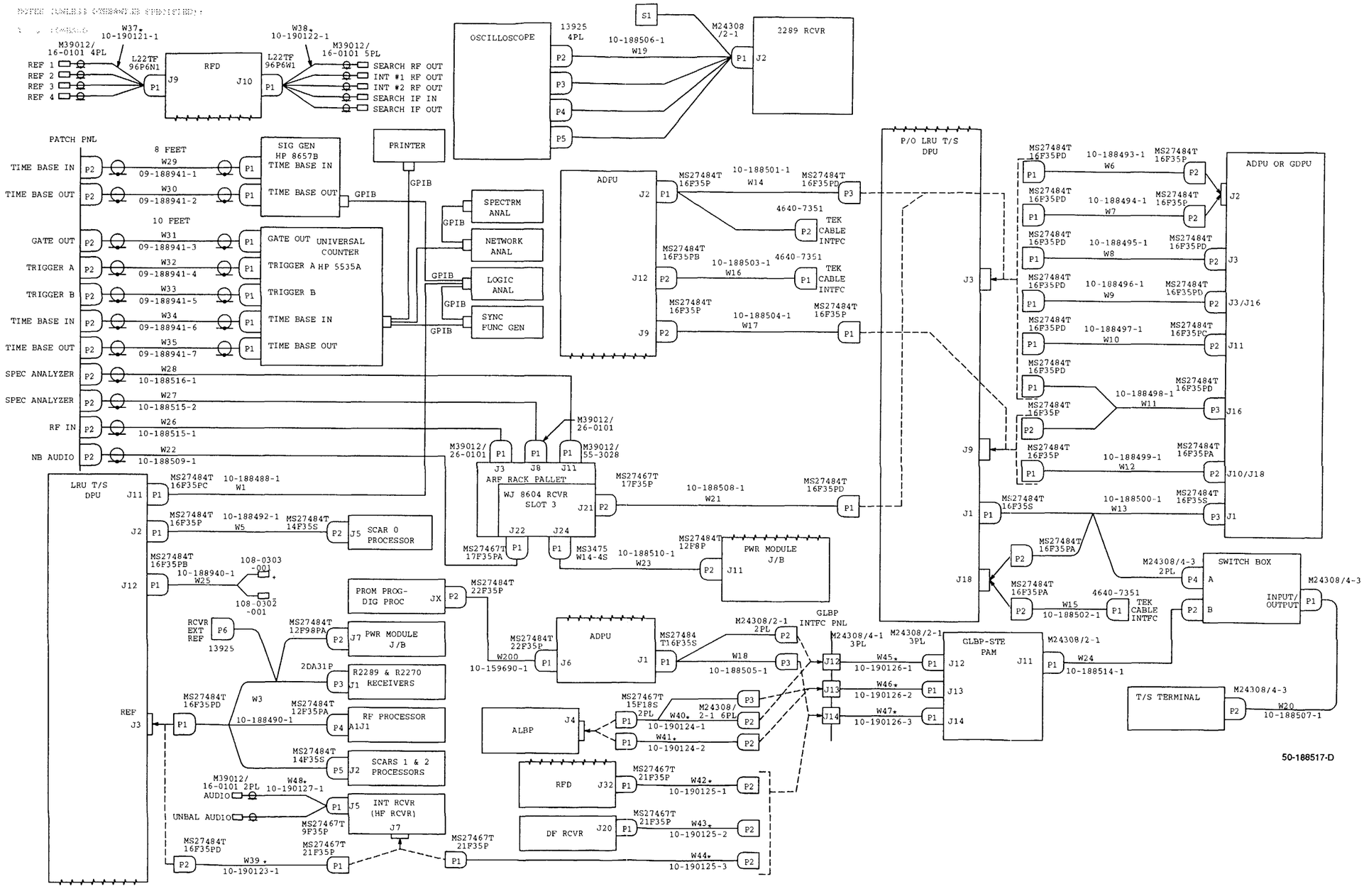

Figure FO-1. FDFT/S Group Cabling Diagram (Sheet 2 of 3)

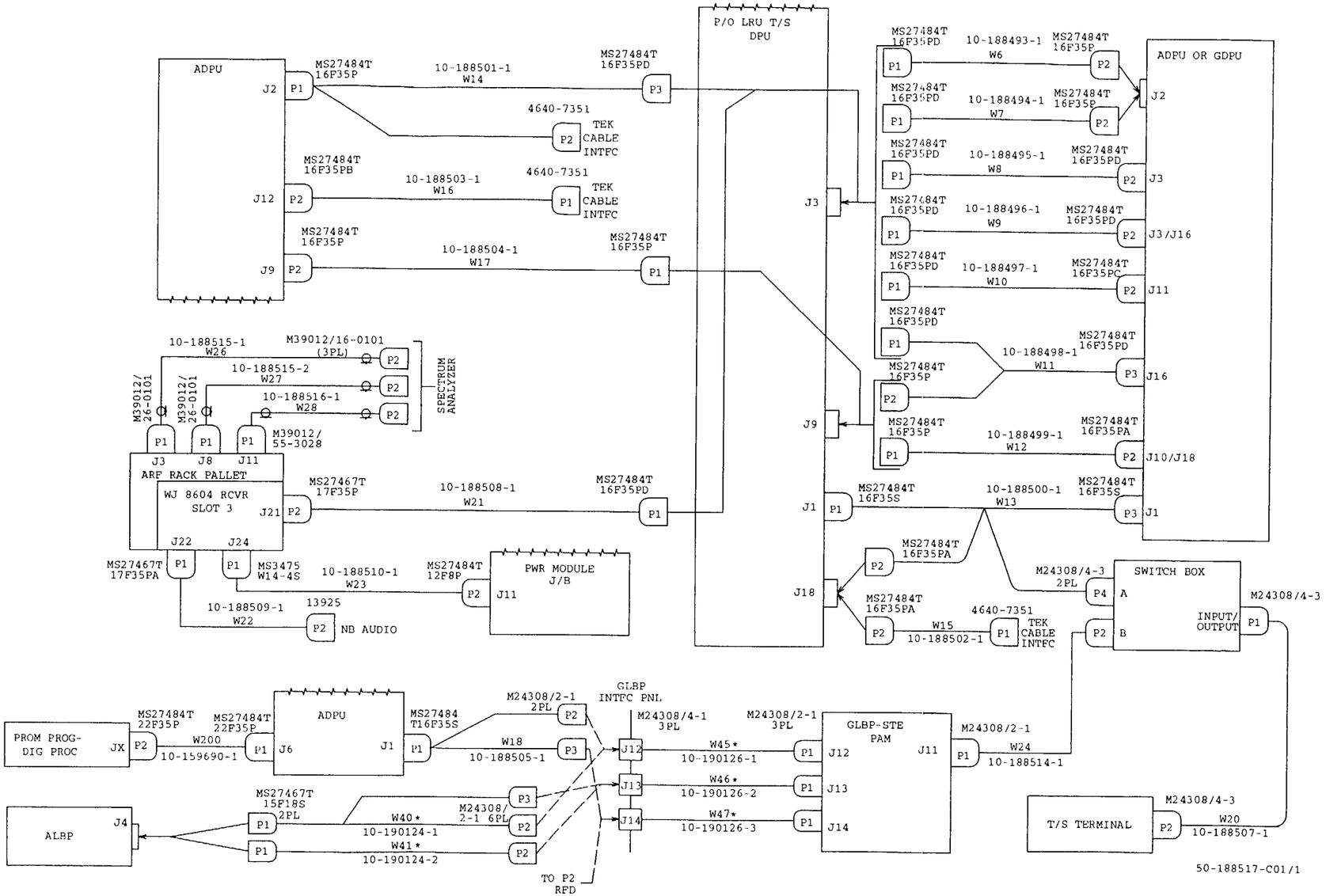

Figure FO-1. FDFT/S Group Cabling Diagram (Sheet 3 of 3)

NOTES (UNLESS OTHERWISE SPECIFIED):

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE REFERENCE DESIGNATION PREFIX WITH APPLICABLE UNIT AND ASSEMBLY DESIGNATIONS.

2. ALL WIRES ARE STRANDED 16 AWG RED.

3. FOR WIRE, TERMINAL LUGS, RESISTORS AND JUMPERS SEE PL10-162550.

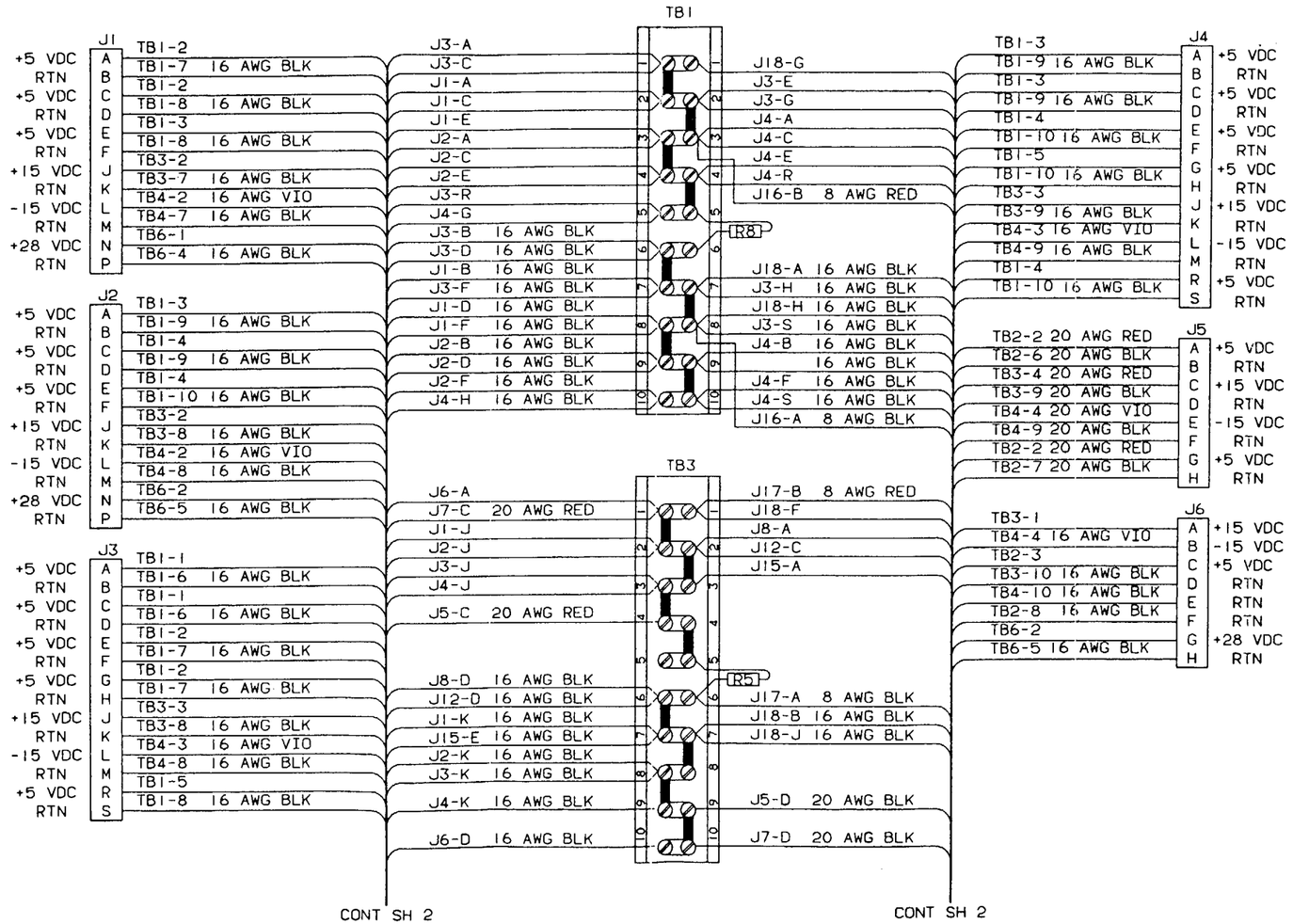

Figure FO-2. Power Junction Box C5A6 Wiring Diagram (Sheet 1 of 3)

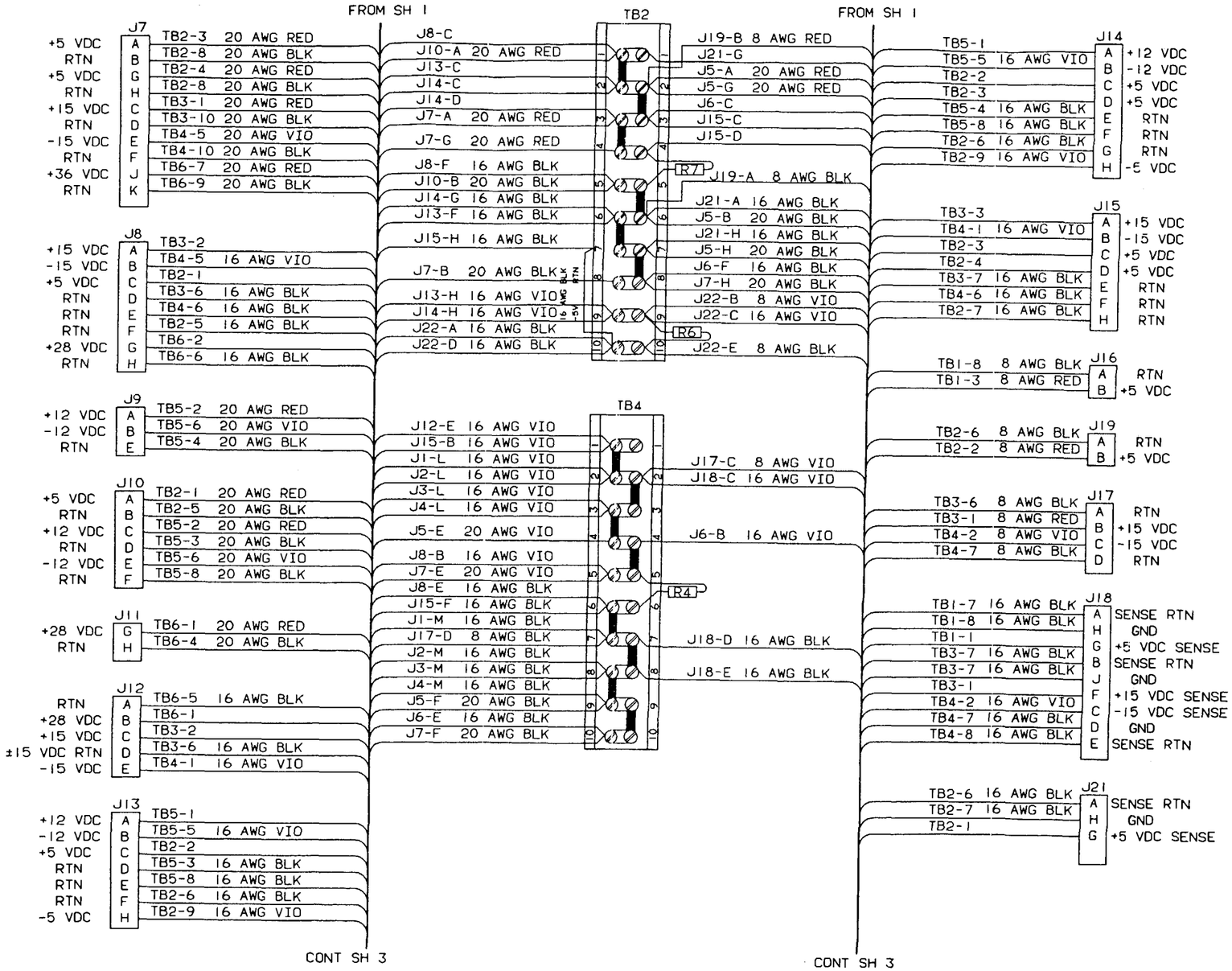

Figure FO-2. Power Junction Box C5A6 Wiring Diagram (Sheet 2 of 3)

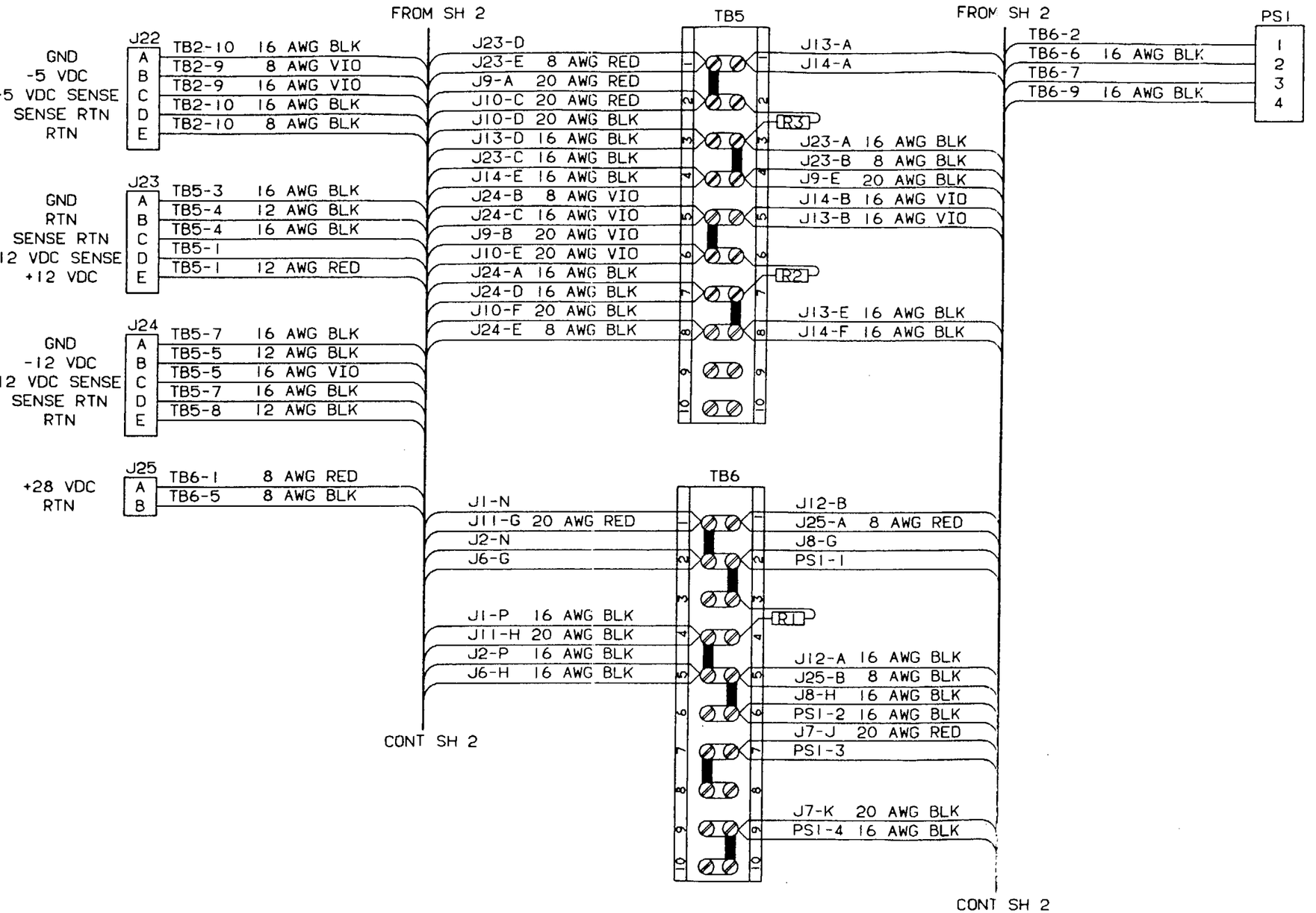

Figure FO-2. Power Junction Box C5A6 Wiring Diagram (Sheet 3 of 3)

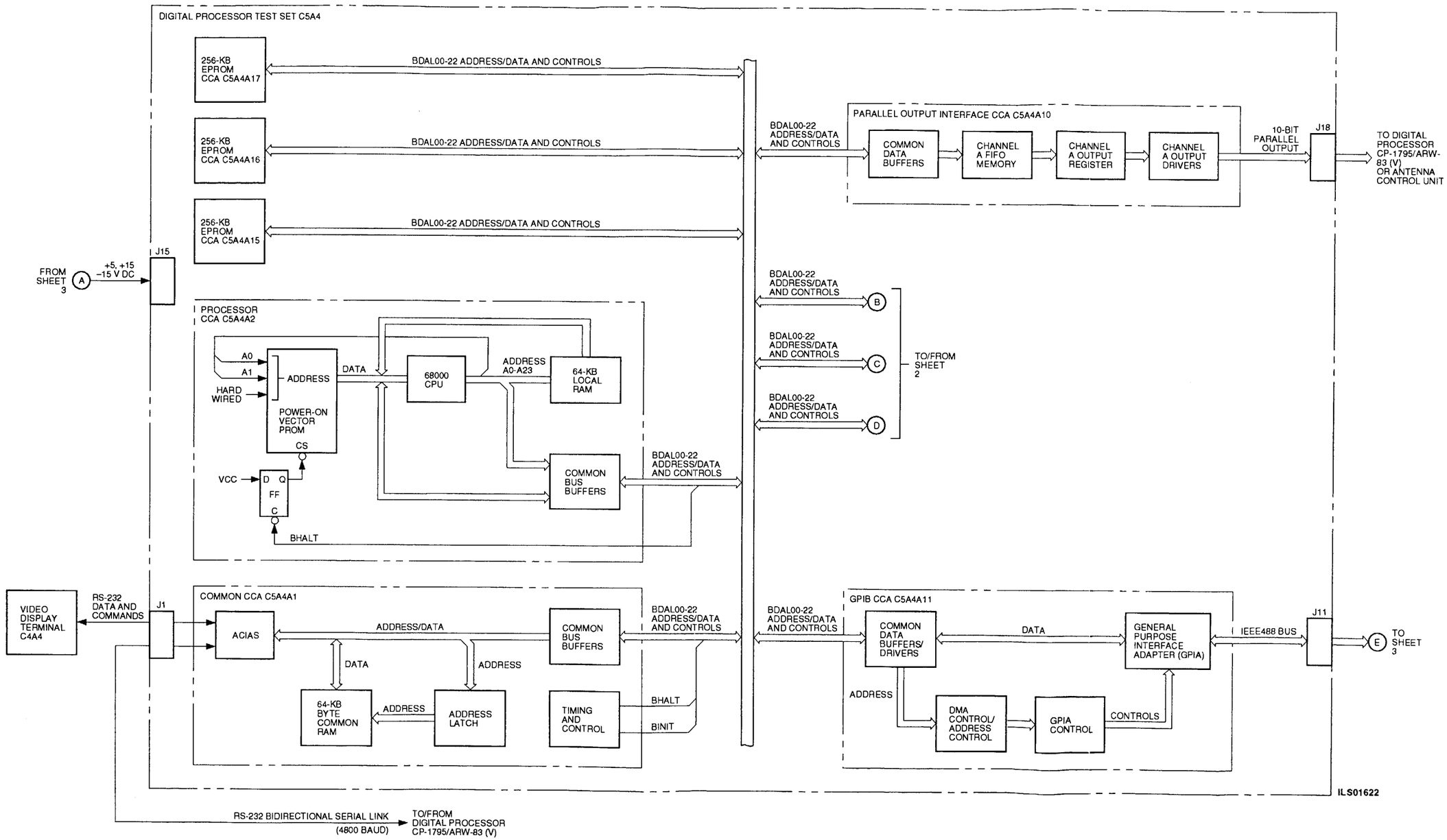

Figure FO-3. FDF T/S Group Functional Block Diagram (Sheet 1 of 3)

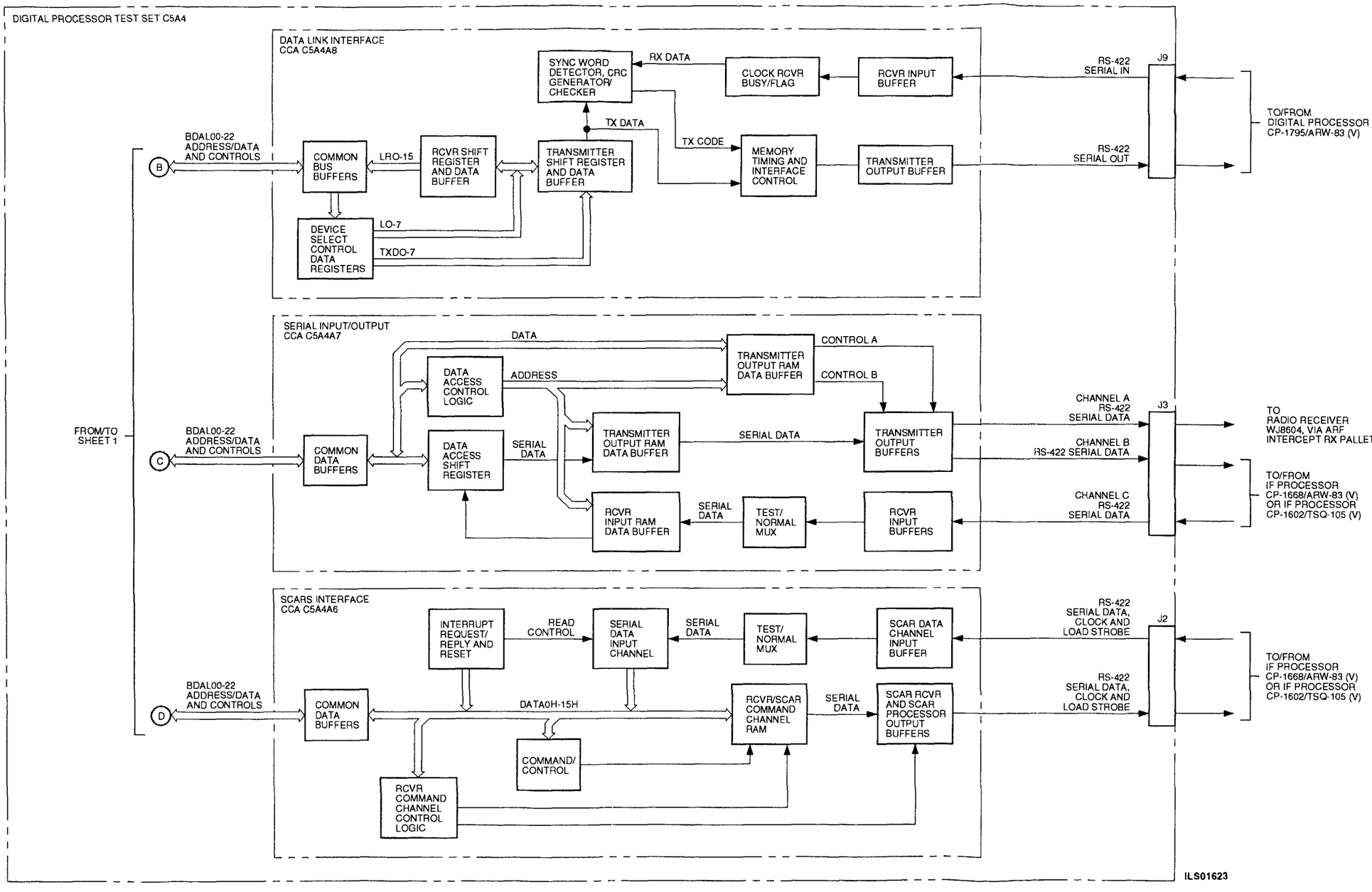

Figure FO-3. FDF T/S Group Functional Block Diagram (Sheet 2 of 3)

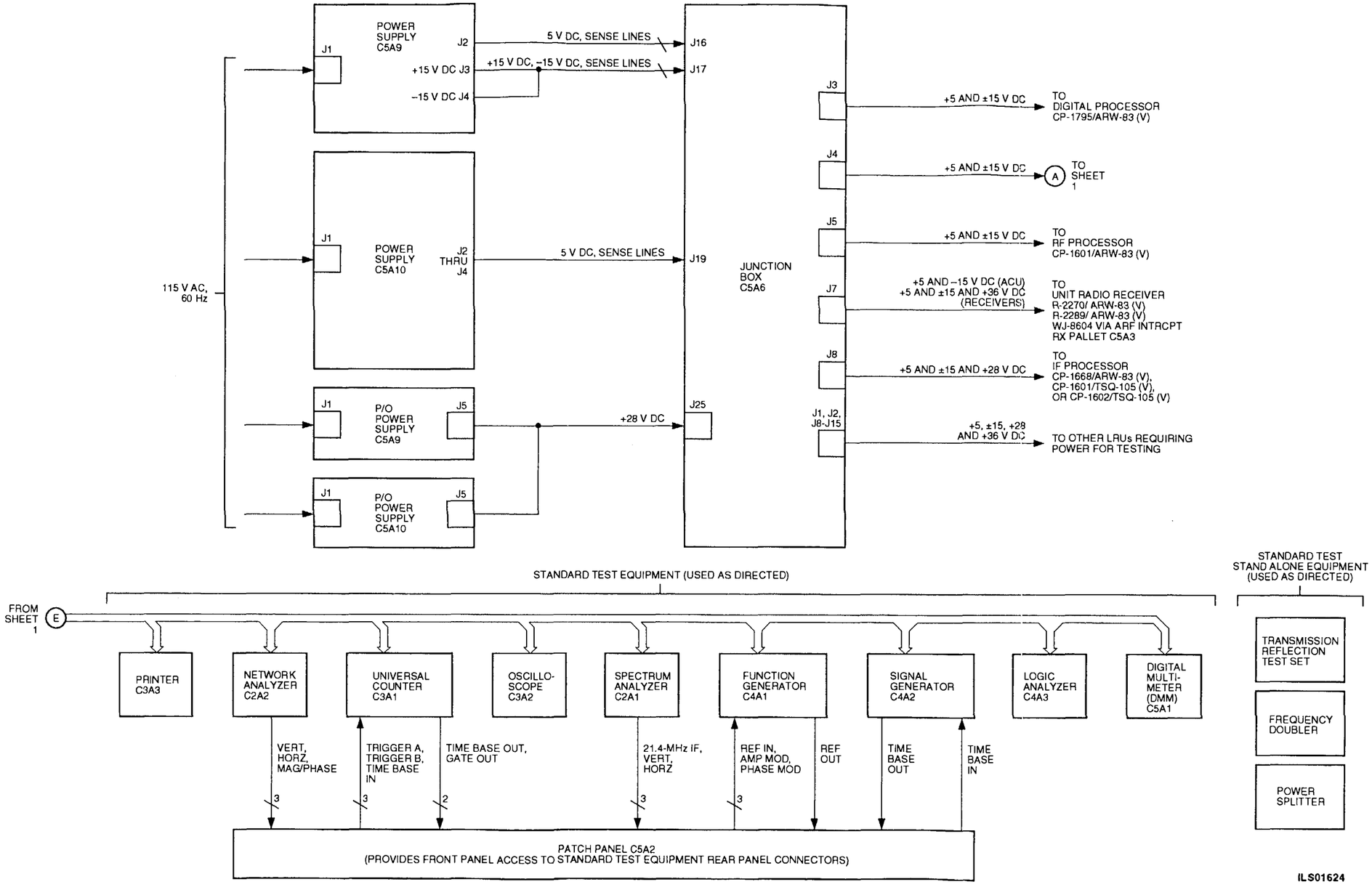

Figure FO-3. FDF T/S Group Functional Block Diagram (Sheet 3 of 3)

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