TM 11-5840-339-34

DEPARTMENT OF THE ARMY TECHNICAL MANUAL

DS AND GS MAINTENANCE MANUAL

RADIO FREQUENCY MONITOR SET AN/USQ-42

(LIMITED COVERAGE)

HEADQUARTERS, DEPARTMENT OF THE ARMY
MAY 1968

TECHNICAL MANUAL
No. 11-5840-339-34

HEADQUARTERS
DEPARTMENT OF THE ARMY
WASHINGTON, D.C., *28 May 1968*

DS and GS Maintenance Manual

RADIO FREQUENCY MONITOR SET AN/USQ-42

CHAPTER 1

INTRODUCTION

1-1. Scope

a. This is a first edition manual containing preliminary information. The manual covers direct and general support maintenance for Radio Frequency Monitor Set AN/USQ-42. It includes a description of the functioning of the set in the analysis section. It also includes instructions appropriate to the direct and general support categories for troubleshooting and repairing the equipment, replacing maintenance parts, and repairing maintenance parts. It also lists tools, materials, and test equipment for direct and general support maintenance.

b. The complete technical manual for this equipment includes TM 11-5840-339-12.

Note. For other applicable forms and records, refer to TM 11-5840-339-12.

1-2. Indexes of Publications

a. DA Pam 310-4. Refer to the latest issue of DA Pam 310-4 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

b. DA Pam 310-7. Refer to DA Pam 310-7 to determine whether there are modification work orders (MWO's) pertaining to the equipment.

1-3. Report of Equipment Manual Improvements

Report of errors, omissions, and recommendations for improving this publication by the individual user is encouraged. Reports should be submitted on DA Form 2028 (Recommended Changes to DA Publications) and forwarded direct to Commanding General, U.S. Army Electronics Command, ATTN: AMSEL-ME-NMP-AD, Fort Monmouth, N.J. 07703.

CHAPTER 2

FUNCTIONING OF EQUIPMENT

Section I. BLOCK DIAGRAM

2-1. Introduction

a. This section presents the general analysis of operation of Radio Frequency Monitor Set AN/USQ-42 on a block diagram level. The AN/USQ-42 is divided into two major funtional sections: the receiver section and the digital section. Paragraph 2-2 describes the block diagram of the receiver section, illustrated in the top portion of figure 2-1. Paragraph 2-3 describes the digital section shown in the bottom portion of figure 2-1. Power regulator circuits contained in the auxiliary mounting adapter are described in paragraphs 2-18 and 4-4.

b. Radio Frequency Monitor Set AN/USQ-42 consists of four replaceable unitized electronic assemblies: a power supply assembly, a front housing assembly onto which are mounted the electronic assemblies, a rear housing assembly, and a removable digital indicator assembly. Also described in this manual is an auxiliary mounting adapter. The reference designators assigned to these components are as follows:

Designator	*Component*
1A1	Front housing assembly.
1A2	Digital indicator assembly.
1A3	Data converter power supply assembly.
1A4	Command signal decoder assembly.
1A5	Amplifier-filter assembly.
1A6	Preselector-synthesizer assembly.
1A7	Power supply assembly.
1A8	Rear housing assembly.
----------	Mounting adapter.

c. Parts located on or within each module have their reference designations prefixed by the assigned module reference designation. For example, the reference designation 1A6A1R1 denotes resistor number one within subassembly A1 in the preselector-synthesizer module 1A6.

d. Figure 2-1 is an overall block diagram of Radio Frequency Monitor Set AN/USQ-42, which shows the relationships which exist between the various functional circuit groups. The dashed lines define the modules, and the main signal path is shown in heavy lines. The top portion of this figure shows the receiver section; the bottom portion shows the digital section.

2-2. Description of Receiver Section (fig. 2-1)

a. The receiver section is made up of the circuits in the preselector-synthesizer assembly 1A6, the amplifier filter assembly 1A5, and the TB1 assembly 1A1A1. The receiver section receives signals from the antenna, tunes to the channel selected by the CHANNEL switch, amplifies the signal on the selected frequency channel, and provides two outputs:

(1) A tone pattern output to the digital section. This tone pattern is transmitted from the signal source.

(2) An audio output of the transmitted information to the headset.

b. The channel selection logic converts the setting of the front-panel CHANNEL switches to control signals to the preselector and the frequency synthesizer. For each setting of the CHANNEL switches, the following output signals are provided from the channel selection logic:

(1) Three direct current (dc) enabling signals which each select one oscillator in the frequency synthesizer.

(2) A 1.3 to 5.4 dc voltage level is used for fine tuning in the preselector and the frequency synthesizer. The preselector is an electrically tuned radio frequency (RF) amplifier, which amplifies the signals in the frequency band of the selected channel.

c. The frequency synthesizer generates the three frequencies enabled by the channel selection logic, and mixes them to provide one of 31 selectable output frequencies. The first mixer circuit mixes the preselected RF signal and the frequency synthesizer output, and provides an output signal at the first intermediate frequency.

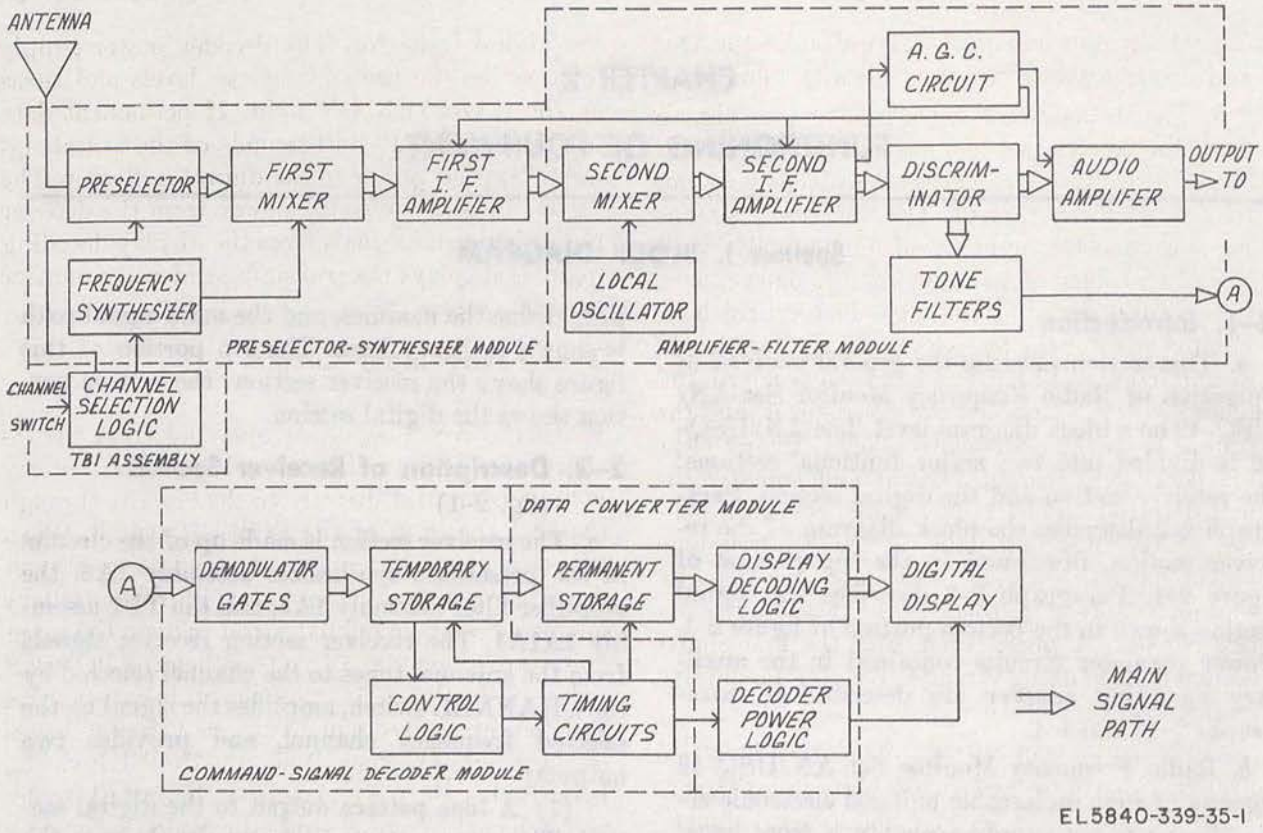


Figure 2–1. Radio Frequency Monitor Set AN/USQ–42, block diagram.

d. The intermediate frequency (IF) mixer output is amplified in the first intermediate frequency amplifier. This amplifier is sharply tuned to a narrow band about the first IF frequency, and rejects all other input signals. The local oscillator generates a fixed 26.5-megacycle (MHz) frequency which is used by the second mixer. The second mixer mixes the incoming signals from the first IF amplifier and the 26.5-MHz signal from the local oscillator. Its output frequency is the second IF frequency which is the difference between the two inputs. The second IF amplifier amplifies those signals which lie in a narrow band about the mixer output frequency, and rejects all other frequencies.

e. The discriminator separates the IF carrier frequency from the audio and ultrasonic intelligence information. Its output is an audio frequency band between 100 and 3,000 Hertz (Hz). The audio amplifier amplifies the discriminator output signals which lie below 3 kilohertz (kHz). These are the transmitted audio signals. The output connects directly to the operators' headset. The automatic gain control (agc) circuit detects the voltage level of the output of the second IF amplifier, rectifies the signal, and uses it to control the gain of the IF amplifiers. This circuit maintains an approximately even audio output level as the IF signal strength varies. The tone filters pass three ultrasonic tone signals corresponding to the frequencies at which the sensor identity signals are transmitted. They reject all other signals. The outputs of the tone filters are sent to the digital section.

2–3. Description of Digital Section
(fig. 2–1)

a. The digital section is made up of the circuits in the command signal decoder assembly 1A4, the data converter-power supply assembly 1A3 and the digital indicator assembly 1A2. The digital section receives tone signals, corresponding to transmitted identity numbers, from the receiver section. It examines the incoming tone signals for proper sequence and timing, and counts the number received. If the signals fulfill all requirements, the

digital section turns on the digital indicator 1A2, and displays the transmitted identity number.

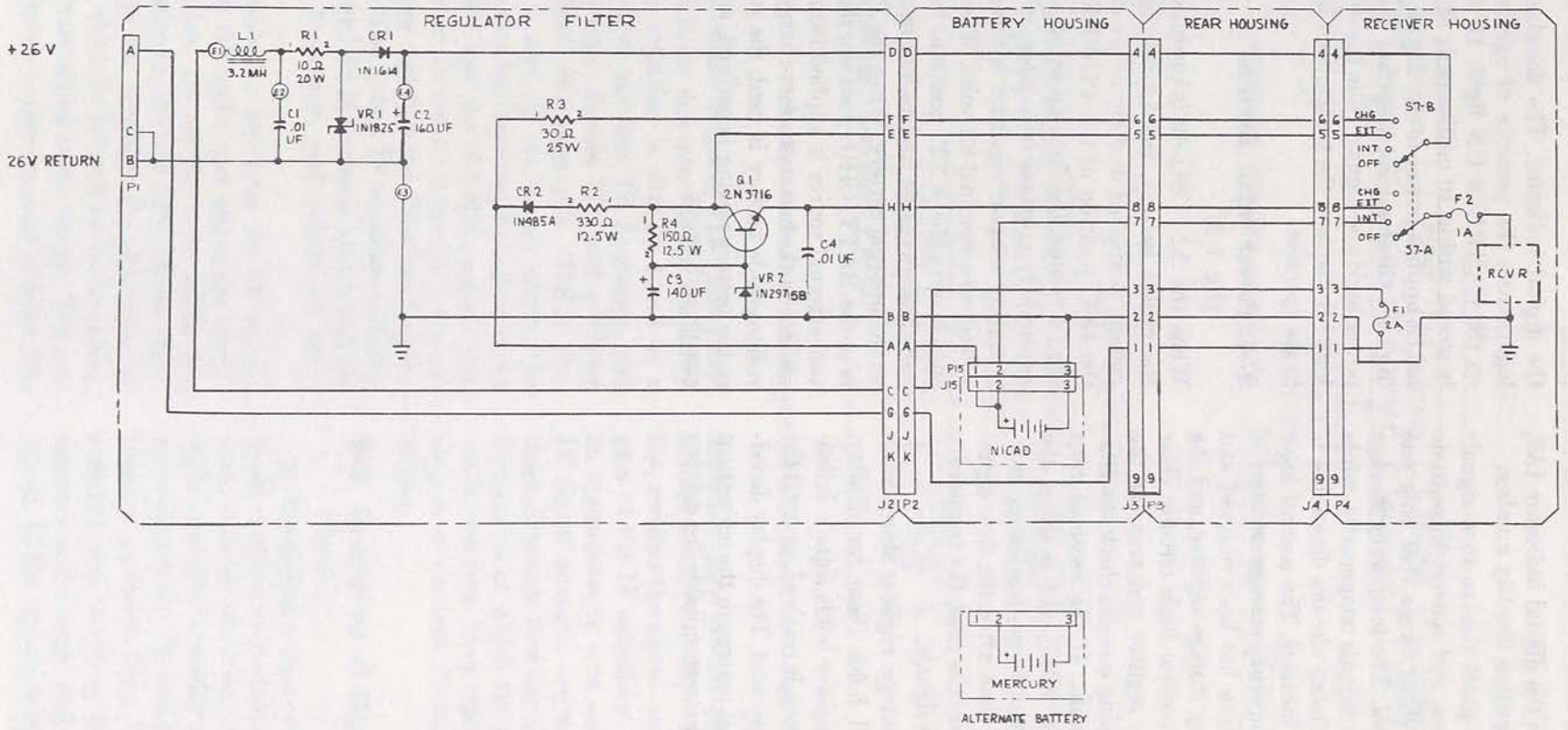
b. The demodulator gates receive tone signals from the receiver section, and convert them to dc levels. The gates also check to see that only one tone at a time is present. The temporary storage register holds the input signals temporarily, while the control logic and timing circuits determine if it is a valid incoming message. The control logic circuits monitor the temporary storage register. If a completed valid pattern has been received and placed in the temporary storage register, and the timing is correct, the control logic circuits clear the permanent storage register and transfer the new data to it. The timing circuits check the timing of the incoming data. If the received tone bursts have the proper width and spacing, the timing circuits store them in the temporary storage register. A preset time after the first signal occurred, the timing circuits reset the temporary storage register for new signals.

c. The permanent storage register stores valid incoming patterns and holds them for display. The permanent data register holds signals indefinitely, until a new pattern is received, or until the MAN. CLR switch is operated. The display decoding logic converts the bit pattern in the permanent storage register into a pattern suitable for driving the digital indicator. The decoder power supply logic senses the presence of agc levels and turns on the CARRIER ON light. If permanent data is stored within 10 milliseconds of the initial signal, it applies power to the digital indicator. The digital indicator receives power from the decoder power logic and signals from the display decoding logic. It displays the transmitted identity number to the operator.

2–4. Power Input Circuits

(fig. 2–2)

When the AN/USQ–42 is operated from the rechargeable battery, the 8.4-volt nominal battery voltage is applied directly to the circuits through the INT. position of the POWER switch. When the set is operated from an external 24- to 32-volt dc supply, a power regulator in the auxiliary mounting adapter regulates and reduces the input voltage to a nominal 8.4 volts. When the POWER switch is in the EXT. position, this external 8.4 volts powers the set, and maintains a trickle charge on the internal battery. When the POWER switch is in the BATT. CHG. position, the full 24- to 32-volt external source is applied through a limiting resistor to the battery to fast-charge it. If the nonrechargeable battery is used, the recharging path in the battery wiring is omitted, and no charging circuit path exists.



EL5840-399-35-45

Figure 2-2. Power supply circuits, schematic diagram.

Section II. ANALYSIS OF OPERATION OF RECEIVER SECTION

2-5. Channel Selection Logic
(fig. 2-3)

a. The channel selection logic is contained on terminal board 1A1A1, and converts the positions of the CHANNEL switches to dc levels which control the preselector amplifier and the frequency synthesizer. For each valid position of the CHANNEL switches the outputs from the logic are—

(1) A dc tuning voltage to the preselector and synthesizer.

(2) A dc level which selects one of the five oscillators, 1A6A1A1 through 1A6A1A5.

(3) A dc level which selects one of the four oscillators, 1A6A1A6 through 1A6A1A9 in the synthesizer.

(4) A dc level which selects oscillator 1A6A1A10 or 1A6A1A11 in the synthesizer.

(5) A second dc tuning voltage to the synthesizer.

b. When the CHANNEL switch is in the 01 position, power supply voltage is applied through regulator transistor 1A1Q69, 1A1CR10, TB1-12 to the wiper of 1A1S1A. Zener diode CR17 sets the output voltage level to 7.5 volts. In the 0-tens position it is connected through 1A1S1A-1 and TB1-40 to P6-20, where it selects oscillator 1A6A1A10 on the preselector-synthesizer assembly. A second path connects dc voltage through 1A1S2A-2, TB1-3, and J6-12, selecting oscillator 1A6A1A2. Voltage divider 1A1A1 R4 and 1A1A1 R5 establishes a tuning voltage which is coupled through diode 1A1A1 CR1 to P6-4 of the frequency synthesizer. The third path connects dc voltage through 1A1S2B-2 to TB1-19, through 1A1A1CR15 to the wiper of 1A1S1-F. In the 0-tens position 1A1S1F connects TB1-9 to P6-16, selecting oscillator 1A6A1A9. Voltage divider 1A1A1R16 and 1A1A1R17 establishes a second tuning voltage which is coupled through 1A1A1CR9 to P6-5, and is used in tuning both the preselector and the frequency synthesizer. Resistors 1A1A1R1 and 1A1A1R20 establish ground references on the diode cathodes.

c. For each of the 31 available channels, three oscillators and two tuning voltages are selected by the CHANNEL switches 1A1S1 and 1A1S2 in a similar manner. The selected oscillators, and tuning voltage outputs for each channel are shown in table 2-1.

2-6. Preselector
(fig. 2-4)

a. The signal from the antenna is applied to the parallel tuned circuit consisting of 1A6A2L1, 1A6A2C1, 1A6A2C2, and varactor diode 1A6A2CR1. Tuning voltage from the channel selection logic is applied to 1A6A2CR1 through isolation resistor 1A6A2R1. The output of the tuned circuit is T-coupled by 1A6A2C3 to a second voltage-tuned circuit consisting of 1A6A2L2, 1A6A2C4, 1A6A2C5, and varactor diode 1A6A2CR2. These two tuned circuits form a bandpass filter which may be preset to the selected channel frequency.

b. The output of the second tuned circuit is applied to the gate (base) input of field effect transistor 1A6A2Q1. Resistor 1A6A2R3 is for biasing; 1A6A2C9 is a bypass capacitor. The collector signal from 1A6A2Q1 is developed across transformer 1A6A2T1. The voltage from the secondary 1A6A2T1 is inverted and fed back through 1A6A2C8 to neutralize any oscillations.

c. The primary of transformer 1A6A2T1, together with 1A6A2C13, 1A6A2C14, and varactor diode 1A6A2CR3, form a third parallel-tuned circuit. The output signal from this tuned circuit is applied to a fourth tuned circuit consisting of 1A6A2L3, 1A6A2C16, 1A6A2C17 and 1A6A2CR4. These two tuned circuits form an output bandpass filter which is tuned by the input voltage on 1A6A2CR3 and 1A6A2CR4.

2-7. Frequency Synthesizer
(fig. 4-5)

a. The frequency synthesizer accepts three input signals and two tuning voltages from the channel select logic. Using these command signals, it generates three crystal-controlled frequencies, and mixes them to form a variable crystal-controlled local oscillator frequency.

b. When one of the input signals on J6-11 through J6-15 is placed at +7.5 volts by CHANNEL switch 1A1A1S2A, the corresponding oscillator begins to operate. For example, a positive signal on J6-11 will cause oscillator 1A6A1A1 to

Table 2-1. Channel Selection Logic Outputs

Channel	Selected oscillators in frequency synthesizer 1A6A1			Tuning voltage outputs	
				At J6-4	At J6-5
01	A-2(J6-12)	A-6(J6-16)	A-10(J6-20)	2. 0v	1. 3v
02	A-3(J6-13)	A-6	A-10	3. 0v	1. 3v
03	A-4(J6-14)	A-6	A-10	4. 0v	1. 3v
04	A-5(J6-15)	A-6	A-10	5. 0v	1. 3v
05	A-1(J6-11)	A-7(J6-17)	A-10	1. 0v	2. 7v
06	A-2(J6-12)	A-7	A-10	2. 0v	2. 7v
07	A-3(J6-13)	A-7	A-10	3. 0v	2. 7v
08	A-4(J6-14)	A-7	A-10	4. 0v	2. 7v
09	A-5(J6-15)	A-7	A-10	5. 0v	2. 7v
10	A-1(J6-11)	A-8(J6-18)	A-10	1. 0v	4. 2v
11	A-2(J6-12)	A-8	A-10	2. 0v	4. 2v
12	A-3(J6-13)	A-8	A-10	3. 0v	4. 2v
13	A-4(J6-14)	A-8	A-10	4. 0v	4. 2v
14	A-5(J6-15)	A-8	A-10	5. 0v	4. 2v
15	A-1(J6-11)	A-9(J6-19)	A-10	1. 0v	5. 4v
16	A-2(J6-12)	A-9	A-10	2. 0v	5. 4v
17	A-3(J6-13)	A-6(J6-16)	A-11(J6-21)	3. 0v	1. 3v
18	A-4(J6-14)	A-6	A-11	4. 0v	1. 3v
19	A-5(J6-15)	A-6	A-11	5. 0v	1. 3v
20	A-1(J6-11)	A-7(J6-17)	A-11	1. 0v	2. 7v
21	A-2(J6-12)	A-7	A-11	2. 0v	2. 7v
22	A-3(J6-13)	A-7	A-11	3. 0v	2. 7v
23	A-4(J6-14)	A-7	A-11	4. 0v	2. 7v
24	A-5(J6-15)	A-7	A-11	5. 0v	2. 7v
25	A-1(J6-11)	A-8(J6-18)	A-11	1. 0v	4. 2v
26	A-2(J6-12)	A-8	A-11	2. 0v	4. 2v
27	A-3(J6-13)	A-8	A-11	3. 0v	4. 2v
28	A-4(J6-14)	A-8	A-11	4. 0v	4. 2v
29	A-5(J6-15)	A-8	A-11	5. 0v	4. 2v
30	A-1(J6-11)	A-9(J6-19)	A-11	1. 0v	5. 4v
31	A-2(J6-12)	A-9	A-11	2. 0v	5. 4v

operate at the frequency determined by crystal 1A1A6Y1. 1A6A1L6 and 1A6A1C17 form a filter to remove switching transients, and resistor 1A6A1R5 decouples the oscillator from the remaining four nonoperating oscillators. Similarly, a positive level at 1A6A1 J6-20 or 1A6A1 J6-21 will cause oscillators 1A6A1A10 or 1A6A1A11 to operate at the frequency of 1A6A1Y10 or 1A6A1Y11. The two oscillator outputs are fed into the balanced mixer transistors 1A6A1Q1 and 1A6A1Q2. One frequency is placed on one base of Q1 and emitter of Q2 and the second frequency output is coupled to the corresponding emitter and base. 1A6A1C28 and 1A6A1C32 are coupling capacitors, and resistor pairs 1A6A1R19–R21 and 1A6A1R20–R22 establish the operating bias on the mixer transistors. Four frequencies are present at the common collectors of the mixer: the two original frequencies, the sum of the two frequencies, and the difference between the two frequencies. The mixer outputs are applied to a voltage-tuned, four-pole filter consisting of 1A6A1L18, 1A6A1L19, 1A6A1L20, and 1A6A1L21, and their associated tuning capacitors. The filter is tuned to pass only the sum frequency by a tuning voltage from the channel selection logic. This tuning voltage is applied to varactor diodes 1A6A1CR1, 1A6A1CR2, 1A6A1CR3 and 1A6A1CR4 through isolation resistors 1A6A1R26, 1A6A1R27, 1A6A1R28 and 1A6A1R29. The sum frequency is coupled through 1A6A1C39 to the base of the second synthesizer mixer 1A6A1Q3.

c. A third crystal-controlled frequency is selected by the channel selection logic from oscillators 1A6A1A6, 1A6A1A7, 1A6A1A8 or 1A6A1A9. The selected oscillator output is

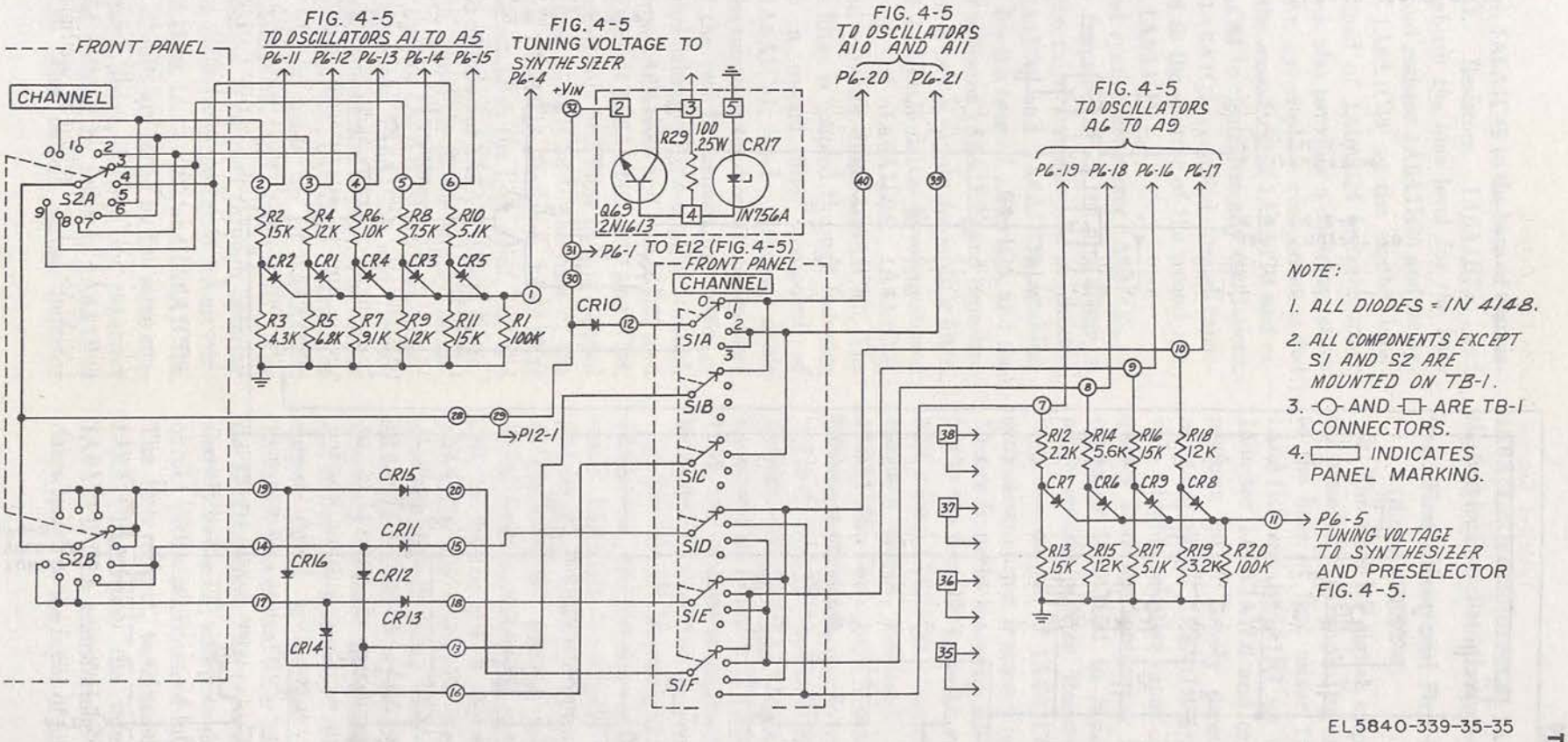


Figure 2-3. CHANNEL switches and channel selection logic, schematic diagram.

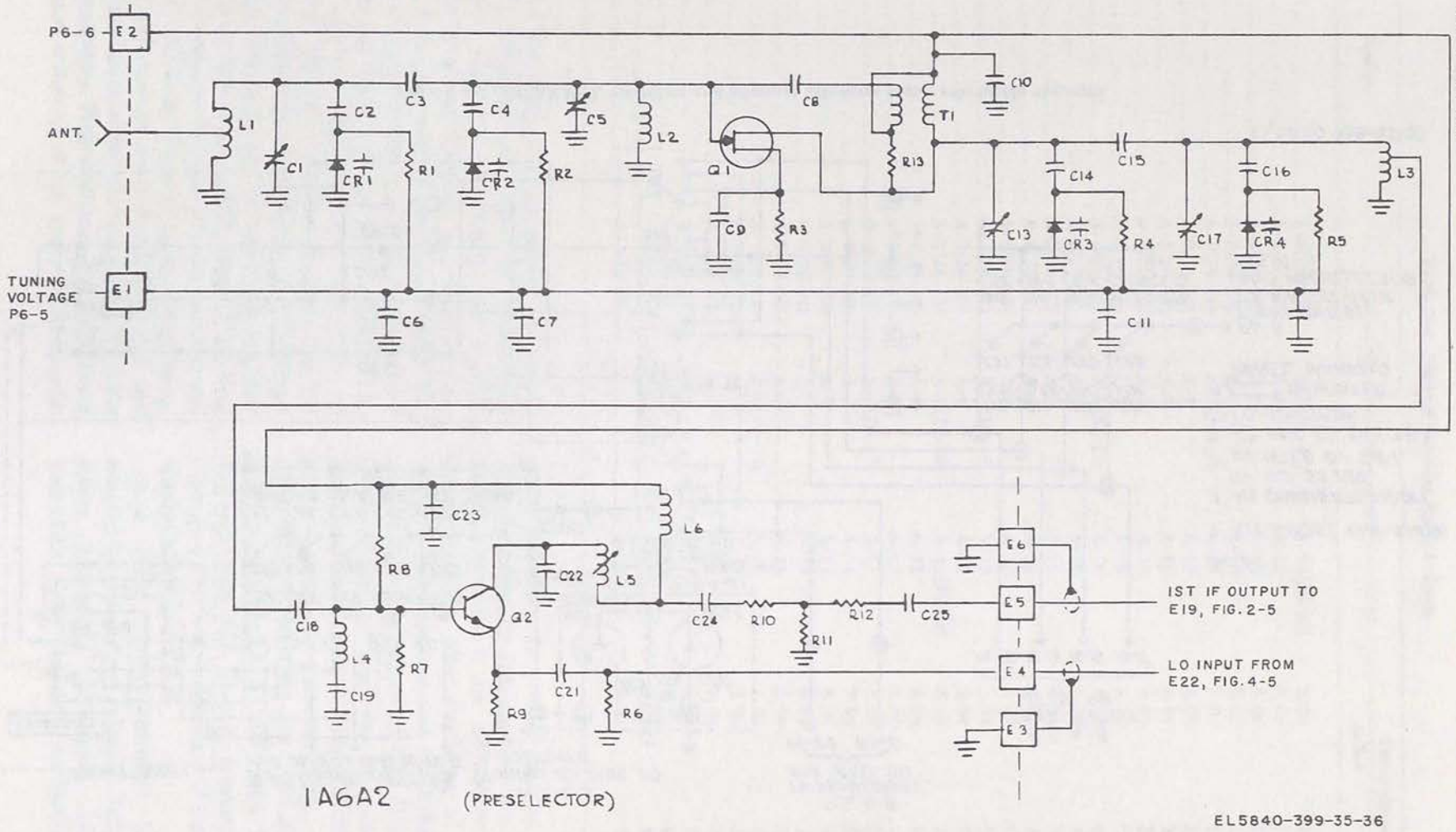


Figure 2-4. Preselector-synthesizer assembly 1A6, preselector, and first mixer, schematic diagram.

coupled through 1A6A1C42 to the base of transistor 1A6A1Q4. Resistors 1A6A1R32 and 1A6A1R31 establish the bias level for the base of 1A6A1Q4, and resistor 1A6A1R33 and its bypass capacitor 1A6A1C45 set the emitter level. The collector load of 1A6A1Q4 is transformer 1A6A1T3, which also provides a collector return to +8 volts. An out-of-phase component is fed back through the secondary of 1A6A1T3 and capacitor 1A6A1C44 to neutralize any oscillations. The output of 1A6A1Q4 is coupled through capacitor 1A6A1C46 to the emitter of the second synthesizer mixer, 1A6A1Q3.

d. The second synthesizer mixer 1A6A1Q3, receives the sum frequency from the first mixer on its base, and the third frequency on its emitter. Resistors 1A6A1R34 and 1A6A1R30 establish the bias point for the base of 1A6A1Q3, and the combination of inductor 1A6A1L22 and capacitor 1A6A1C41 form a power supply decoupling filter. The output of 1A6A1Q3 drives a voltage-tuned filter made up of 1A6A1L24, 1A6A1C48, 1A6A1C49, and varactor diode 1A6A1CR5. The output of this filter is coupled through inductor 1A6A1L26 to a second filter composed of 1A6A1L26, 1A6A1C51, and varactor diode 1A6A1CR6. The two varactor diodes tune the filter to the sum of the two frequencies by a voltage from the channel selection logic applied through isolation resistors 1A6A1R36 and 1A6A1R37 and the decoupling circuit 1A6A1R42 and 1A6A1C58.

e. The output of this first filter pair is coupled through capacitor 1A6A1C52 to the base of the buffer amplifier 1A6A1Q5. Resistors 1A6A1R34 and 1A6A1R38 establish the bias point, and the filter, composed of inductor 1A6A1L23 and capacitor 1A6A1C55, provides power supply decoupling. Emitter resistor 1A6A1R39 provides degeneration, and capacitor 1A6A1C54 and resistor 1A6A1R40 bypass the emitter resistor. The output of the buffer amplifier 1A6A1Q5 drives the voltage-tuned circuit made up of 1A6A1L27, 1A6A1C56, 1A6A1C57, and 1A6A1CR7. The tuned circuit output is coupled through inductor 1A6A1L28 to a second voltage-tuned circuit consisting of 1A6A1L29, 1A6A1C60, and 1A6A1CR8. Both of these circuits are tuned by the same control voltage used above, filtered by capacitor 1A6A1C59, and isolated by resistors 1A6A1R43 and 1A6A1R44. The output across inductor 1A6A1L29 is coupled out by 1A6A1C61, and forms the first local oscillator frequency.

2–8. First Mixer and First IF Amplifier

(figs. 2–4 and 2–5)

a. The input RF signal, amplified and tuned by the preselector, is coupled by capacitor 1A6A1C18 to the base of first mixer 1A6A1Q2. Resistors 1A6A1R8 and 1A6A1R7 set the base bias level. Inductor 1A6A1A1L6 and capacitor 1A6A1C28 perform power supply decoupling. The series resonant circuit 1A6A1L4 and 1A6A1C19 provide a highly selective input circut. The sum frequency from the synthesizer is coupled through capacitor 1A6A1C21 to resistor 1A6A1R9, the mixer emitter resistor. Resistor 1A6A1R6 references the output of 1A6A1C61 to ground. The synthesizer output frequency is always a fixed difference from the incoming RF signal, corresponding to the first IF frequency. The output of the first mixer 1A6A1Q2 is applied to the parallel resonant circuit composed of 1A6A1L5 and 1A6A1C22. This circuit is tuned to the difference between the two incoming frequencies, corresponding to the first IF frequency. The output is coupled through capacitor 1A6A1C24, attenuated by the tee circuit of 1A6A1R10, 1A6A1R11, and 1A6A1R12, and coupled through capacitor 1A6A1C25 to the first IF amplifier.

b. The first IF frequency is applied to amplifier 1A6A1AR1, the first stage of the IF amplifier. Resistor 1A6A1R1 terminates the coaxial cable, and capacitor 1A6A1C1 bypasses the cable shield to the amplifier ground. A dc gain-adjusting signal from the automatic gain control (agc) circuit is fed in pin 5 through filter elements 1A6A1L1 and 1A6A1C5. Amplifier 1A6A1AR1 provides signal gain, and drives the circuit 1A6A1L2–1A6A1C6, which is tuned to the first IF frequency. Resistor 1A6A1R2 broadens the band and flattens the response of this tuned circuit. The output signal is coupled through capacitor 1A6A1C7 to a crystal filter 1A6A1FL–1, tuned to the IF frequency. This crystal filter is tuned very sharply to the IF, and provides a highly selective output with a minimum of interchannel crosstalk. The filter output, terminated in 1A6A1R4 and 1A6A1C16, drives the interstage transformer 1A6A1T1. The transformer provides an impedance match to the input of amplifier 1A6A1AR2.

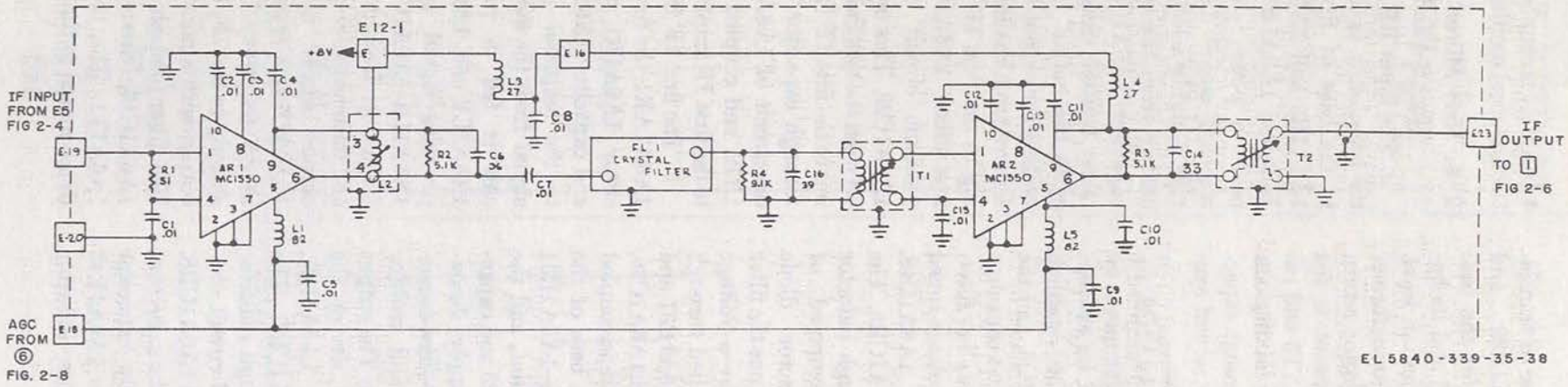


Figure 2–5. Preselector-synthesizer assembly 1A6, first IF amplifier, schematic diagram.

Amplifier 1A6A1AR2, controlled by the agc signal through 1A6A1L5, drives the circuit consisting of 1A6A1T2, 1A6A1C14, and 1A6A1R3. This circuit is also tuned to the IF frequency. Filter elements 1A6A1L4, 1A6A1C8, and 1A6A1L3 provides power supply decoupling. The secondary of transformer 1A6A1T2 drives the second mixer circuit.

2-9. Local Oscillator, Second Mixer, and Second IF Amplifier

(fig. 2-6)

a. The local oscillator is an encapsulated circuit which oscillates at 26.500 MHz, as determined by crystal 1A5A1Y1. L1 decouples the power supply. The 26.500-MHz signal is coupled by 1A5A1C1 to the emitter of the second mixed stage, 1A5A1Q1.

b. The first IF output signal is attenuated by the pi network 1A5A1R2, 1A5A1R32, and 1A5A1R33, and is coupled through capacitor 1A5A1C29 to the base of the second mixer 1A5A1Q1. Resistors 1A5A1R1 and 1A5A1R18 set the base bias point. The local oscillator signal is coupled to the emitter resistor, 1A5A1R4. Resistor 1A5A1R5 is a power supply decoupling resistor. The two frequencies are mixed in 1A5A1Q1 and the difference frequency (26.5 MHz−first IF) passes through the circuit consisting of 1A5A1T1, 1A5A1C2, and 1A5A1R3, which is tuned to the second IF frequency. The secondary of transformer 1A5A1T1 couples the signal to the second IF amplifier.

c. The second IF amplifier consists of four integrated-circuit amplifiers 1A5A1AR1, 1A5A1AR2, 1A5A1AR3, and 1A5A1AR4. Successive amplifiers are coupled by transformers 1A5A1T2, 1A5A1T3, 1A5A1T4, and 1A5A1T5, which are tuned to the second IF frequency by capacitors 1A5A1C7, 1A5A1C13, 1A5A1C18, and 1A5A1C23. The gain of each amplifier is controlled by an automatic gain control dc level applied through decoupling coils 1A5A1L2, 1A5A1L4, and 1A5A1L6. Eight-volt power is applied through decoupling coils 1A5A1L3, 1A5A1L5, 1A5A1L7, and 1A5A1L8.

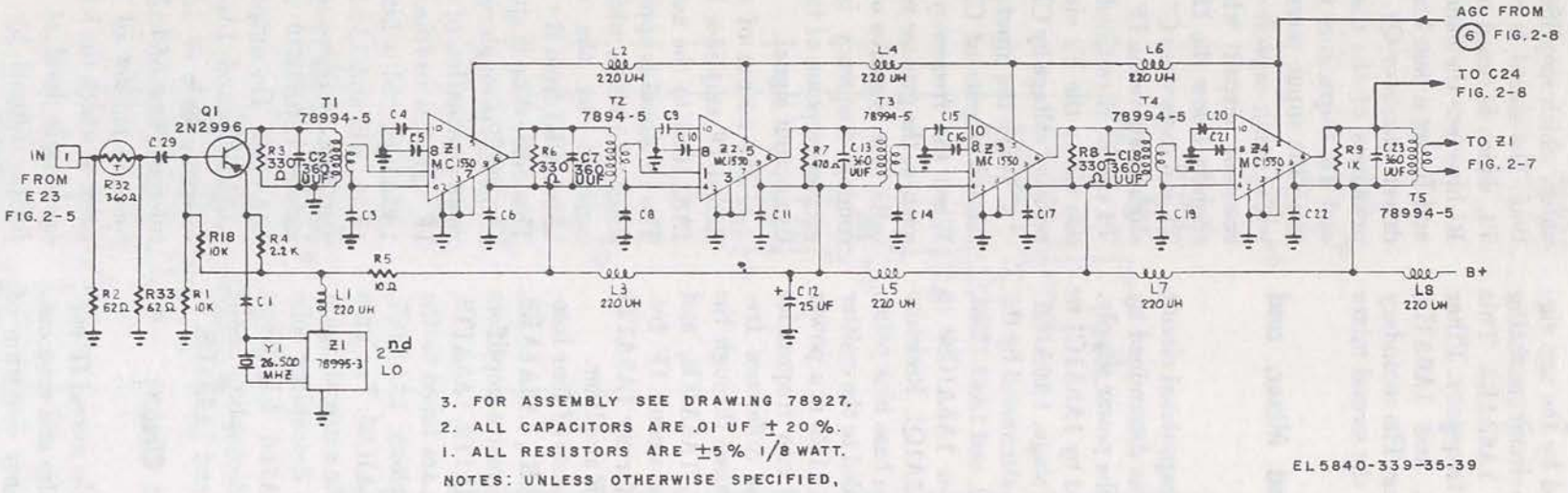
2-10. Discriminator and Agc Circuits

(figs. 2-7 and 2-8)

a. The discriminator removes the second IF carrier frequency, and provides audio and tone outputs proportional to the frequency deviation of the received RF carrier. The second IF amplifier output is applied to amplifier Z1 in the discriminator, which amplifies the input signal to saturation. The signal is coupled through transformer T1, which is tuned to the IF frequency. Resistor R1 broadens the bandpass of T1, and resistors R2 and R3 set a base bias of +4 volts on the base of driver transistor Q1. The output of Q1 drives the primaries of the discriminator transformers T2 and T3. Capacitors C1 and C5, and inductor L1 filter the input power voltage. Transformer T2, with tuning capacitors C6 and 8, form a parallel resonant circuit whose resonant frequency is slightly below the IF carrier input; transformer T3 and capacitors C7 and C9 are tuned to resonate slightly above the IF frequency. The output of the T2 circuit is rectified to a negative voltage by diode CR1; the T2 circuit output is rectified to a positive voltage by CR2.

b. When the input signal is at the IF frequency, the dc outputs of CR1 and CR2 cancel to zero. When the frequency is lower than the IF frequency, the greater response of the T2 circuits results in a negative output voltage. When the incoming frequency is higher than the IF, the greater response of the T3 circuit results in a positive output signal.

c. The output of amplifier 1A5A1AR4 in the second IF amplifier is coupled through capacitor 1A5A1C24 to the automatic gain control circuit. The IF signal is applied to the input base of transistor 1A5A1Q2, which is biased to a slightly on condition by the voltage drop across diode 1A5A1CR1 from B+ through resistor 1A5A1R10. This diode drop is applied to the base of transistor 1A5A1Q2 through resistor 1A5A1R11, which prevents attenuation of the incoming IF signal. The IF signal is rectified by the half-wave action of 1A5A1Q2, and is filtered by the time constant of 1A5A1R12 and 1A5A1C25. This filtered signal is amplified by transistor 1A5A1Q3, whose collector resisor 1A5A1R19 drives the emitter follower 1A5A1Q4. The output of 1A5A1Q4 is filtered by 1A5A1R16 and 1A5A1C27, and applied to the reference base of 1A5A1Q2. The signal on the reference base of 1A5A1Q2 varies the level of the common emitter of 1A5A1Q2, which varies the point at which the left side begins to conduct. The agc output level at the emitter of 1A5A1Q4 is further filtered by 1A5A1R21 and 1A4A1C28. The filtered output is then used to adjust the gains of the first IF amplifier, and the second IF ampli-



3. FOR ASSEMBLY SEE DRAWING 78927.
2. ALL CAPACITORS ARE .01 UF ± 20 %.
1. ALL RESISTORS ARE ±5% 1/8 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED,

EL 5840-339-35-39

Figure 2-6. Amplifier-filter assembly 1A5, local oscillator, second mixer, and second IF amplifier, schematic diagram.

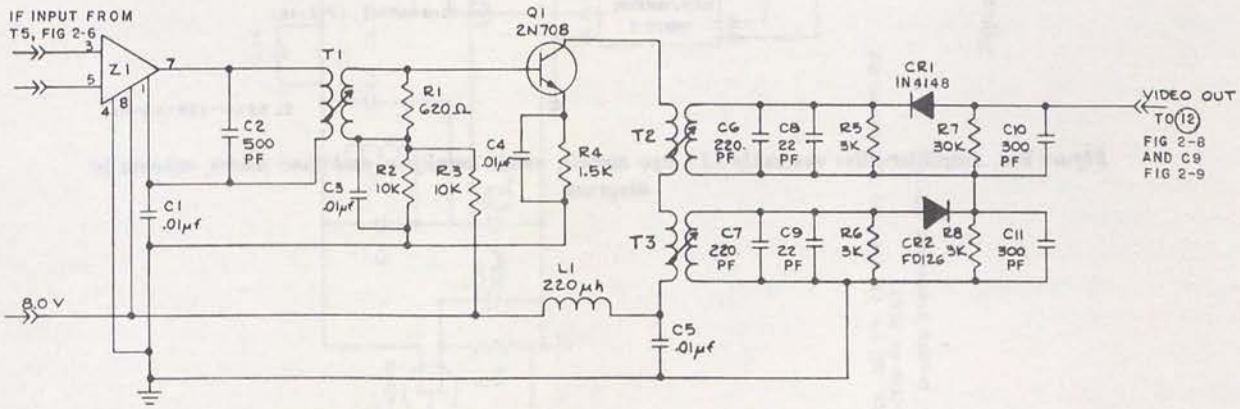
fier, to maintain a constant output with a varying input signal level. The agc output also drives the front panel signal-strength meter. The agc output drives the voltage divider, 1A5A1R21 and 1A5A1R22. Resistor 1A5A1R22 is a potentiometer which adjusts the sensitivity of the front panel signal-strength meter. The agc output is also applied to the SQUELCH potentiometer through a series resistor. The arm of the SQUELCH control is connected to the Schmidt trigger circuit 1A5A1Q5 and 1A5A1Q6. When the agc level at the Schmidt trigger input exceeds 2.5 volts, the circuit switches and transistor 1A5A1Q6 turn off. If the Schmidt trigger output is connected to the audio amplifier through the SQUELCH switch, this removes the shunt across the audio amplifier, enabling an audio output. When the agc level is below the Schmidt firing point, the audio amplifier is disabled, and no audio output occurs.

2–11. Audio Amplifier and Tone Filters

(fig. 2–8)

a. Audio Amplifier. The audio output of the discriminator is applied to the top of the front panel VOLUME potentiometer. The signal from the arm of the potentiometer, coupled through 1A5A1C30 is applied to the input of the audio amplifier, 1A5A1AZ5. Resistors 1A5A1R27 and 1A5AR28, and capacitors 1A5A1C32, and 1A5A1C33 stabilize the amplifier, and attenuate the input frequencies above 3KHZ. Resistor 1A5A1R29 adjusts the zero output point. The squelch signal input on pin 11 shunts the amplifier with the low on-resistance of 1A5A1Q6 and 1A5A1R24, with a low input, but enables the amplifier when a high input occurs. The audio amplifier provides power gain. Its output drives the output transformer, 1A5A1T6, which provides an impedance match to the headset earphone.

b. Tone Filters (figs. 2–8 and 2–9). The three tone filters, 1A5A1FL1, 1A5A1FL2, and 1A5A1FL3, are driven from the discriminator output through isolating resistor 1A5A1R22. These filters are highly selective. The three tone filter outputs are connected to the inputs of the digital section. Input signals to each tone filter demodulator are applied to the gate of the field effect transistor Q1. The output of Q1 drives a three-stage tuned circuit, consisting of L1 in parallel with C1 and C4, L2 in parallel with C2 and C5, and L3 in parallel with C3 and C6. Capacitors C7, C14, C8, and C15 couple the signal between filter stages. This three-stage filter passes only the selected tone frequency and rejects all others. The filter output drives emitter follower Q2, whose emitter output is coupled through capacitor C13 to the digital section.



3. ALL CAPACITOR VALUES IN MICROFARADS.
2. ALL RESISTOR VALUES IN OHMS, ±5%, 1/4 W.
1. FOR ASSEMBLY SEE DRAWING 79084-1.
NOTE: UNLESS OTHERWISE SPECIFIED.

EL 5840-339-35-40

Figure 2–7. Amplifier-filter assembly 1A5, discriminator, schematic diagram.

308-129 O - 68 - 2

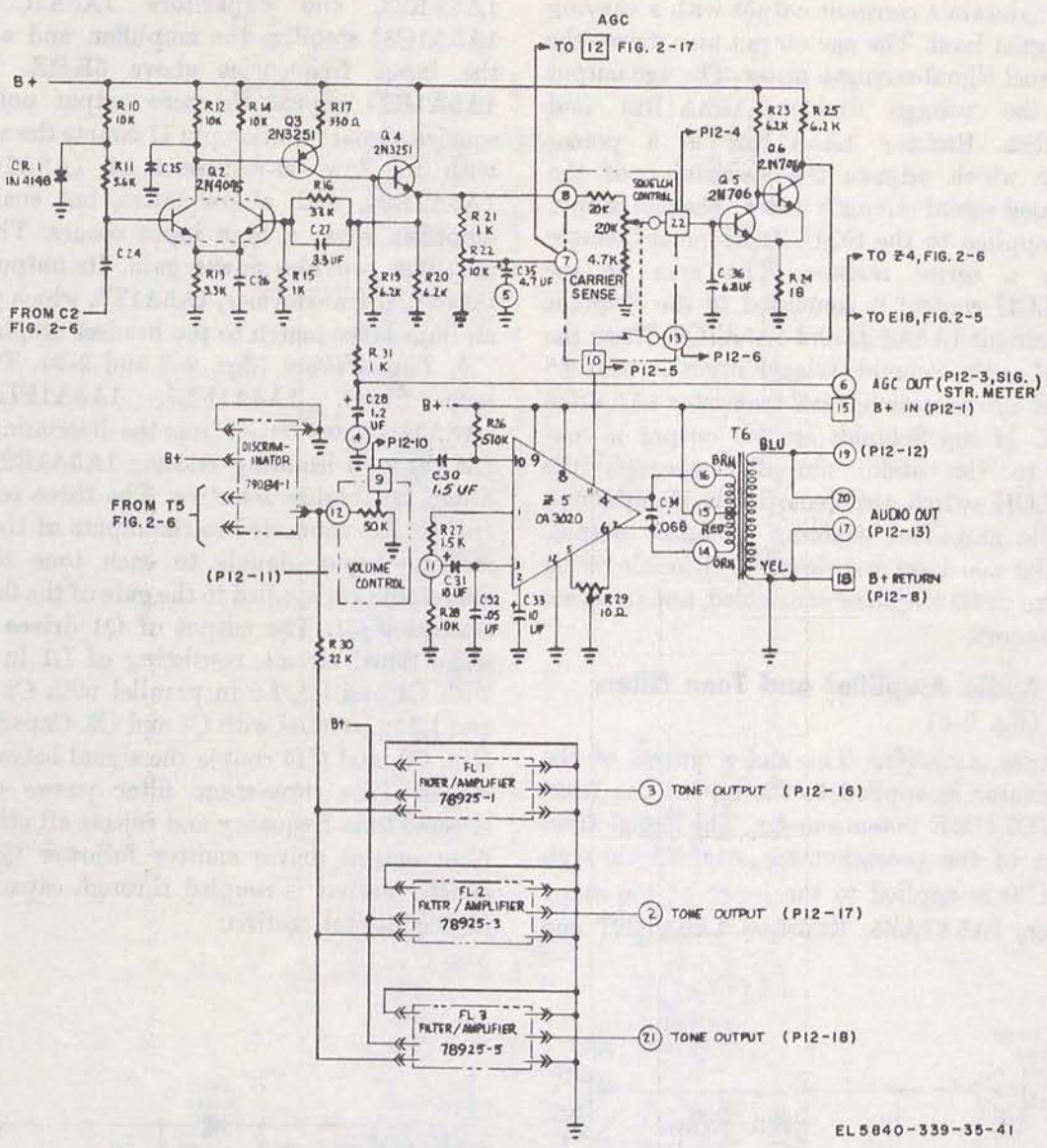
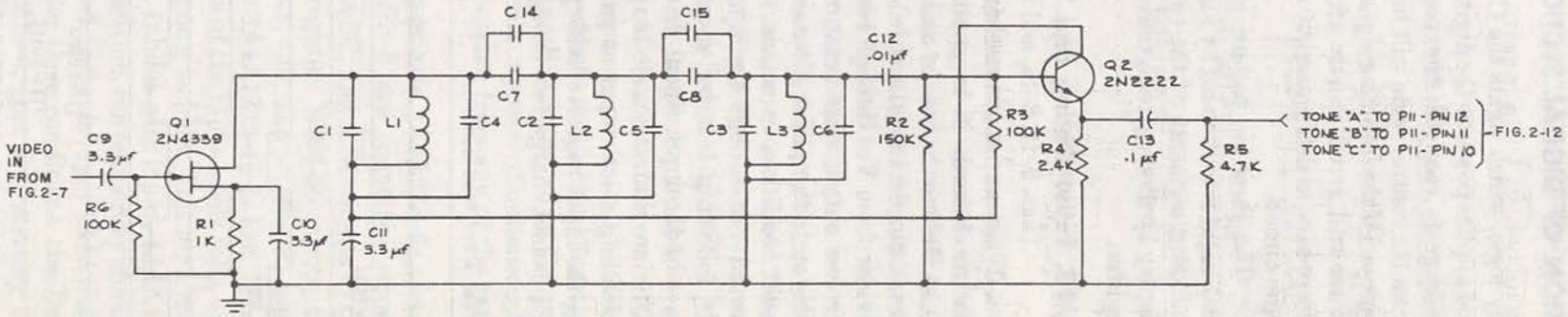


Figure 2-8. Amplifier-filter assembly 1A5, agc circuit, audio amplifier, and tone filters, schematic diagram.



1. C4, C5, C6, C7, C8, C14 & C15 VALUES TO BE SELECTED AT TEST.

NOTES: UNLESS OTHERWISE SPECIFIED

EL5840-339-35-42

Figure 2-9. Tone filter demodulator, schematic diagram.

Section III. ANALYSIS OF OPERATION OF DIGITAL SECTION

2–12. Overall Operation and Timing

(figs. 2–1 and 2–10)

a. Incoming tone bursts, one at a time, are demodulated and applied to the temporary storage register. The first incoming signal sets the data inhibit line down, which starts the timing circuits. The timing circuit removes the clear signal from the temporary storage register and, 1.5 millisecond later, generates a clock pulse, which stores the first bit in the temporary register. When the two following signals are received and demodulated, two additional clock pulses are generated 1.5 millisecond after their leading edges. These clock pulses cause the data to be shifted down the temporary storage shift register, and the new data to be stored.

b. As soon as a bit is present in each of the three temporary storage time slots, the control logic circuits detect this state and issue a reset command, which clears the permanent data register. When this register is reset, it returns a permanent data signal, which enables a load command. The load command transfers the contents of the temporary storage register to the permanent storage register.

c. Twelve milliseconds after the leading edge of the first input pulse, the timing circuits clear the contents of the temporary register, and the circuits become quiescent again.

d. When a message comes in, the rise of the receiver agc level triggers the display power supply logic, which lights the CARRIER ON lamp, and applies power to the digital indicator. If a true message is received, the permanent data signal from the control logic will hold the power supply logic on; if the incoming signal is noise, the display power will go off shortly after the carrier signal disappears, as determined by a time constant in the logic circuit.

e. The three-bit pattern stored in the permanent register is decoded by logic gates to the corresponding segments of the two-digit IDENTITY display by diode gates connected to the permanent register.

2–13. Input Gating and Timing Circuits

(figs. 2–11, 2–12, and 2–13)

a. When an input tone burst signal appears in the A channel, it is applied through resistor 1A4A2R20 to the base of demodulator 1A4A2Q12. Transistor 1A4A2Q12 is held near cutoff by the divider from Vcc through resistor 1A4A2R19 and the low output impedance of the 1A5A1Z1 tone filter on the amplifier-filter assembly. In this near-cutoff condition, capacitor 1A4A2C4 is charged toward Vcc through the input pull-up resistor of the following inverter stage. The positive half wave of the input signal drives transistor 1A4A-2Q12 into saturation, discharging 1A41A2C4, and providing a low input at gate 1A4A2Z7–1. During the input negative half-cycle capacitor 1A4A-2C4 cannot charge fast enough to change the low

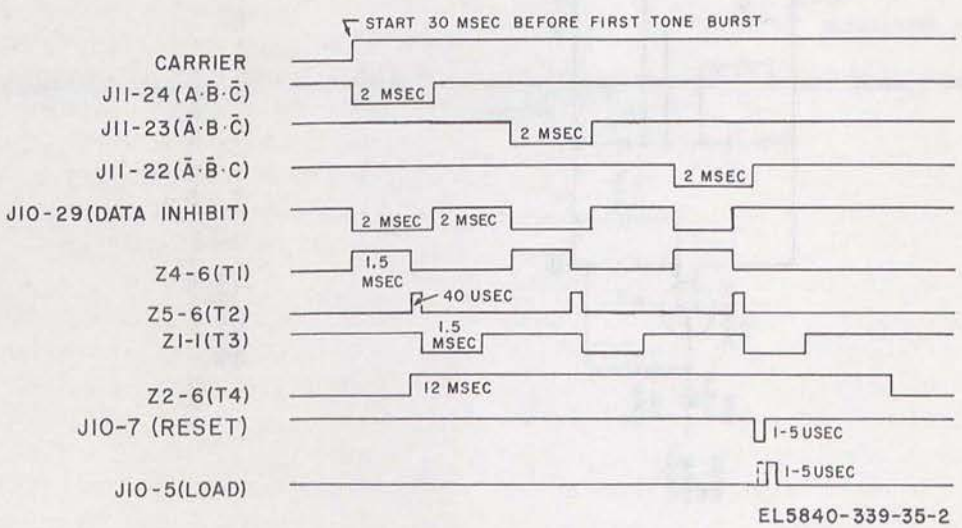


Figure 2–10. Overall digital section, timing diagram.

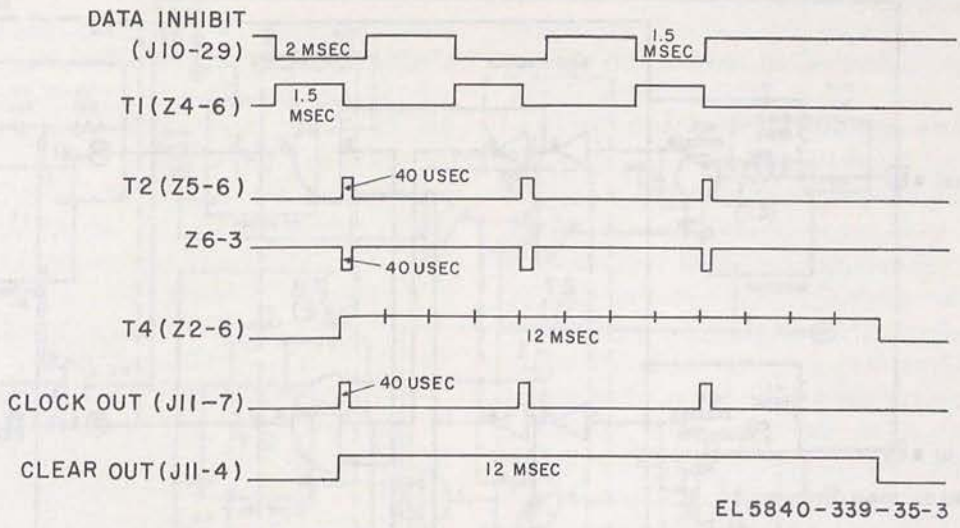


Figure 2-11. Timing circuits, timing diagram.

(0 to 0.5 volt) level before the next positive-half cycle arrives. The tone signal is thus demodulated to a dc level signal. Demodulation of the B input and C input signals is done identically by transistors 1A4A2Q13 and 1A4A2Q14.

b. The low level at gate 1A4A2Z7-1 is inverted at 1A4A2Z7-2 to a high (2.5 to 5.0 volt) level, and is applied to the exclusive-or gate at 1A4A2Z8-5. High inputs corresponding to the absence of B and C input signals are applied at 1A4A2Z8-4 and 1A4A2Z8-3. With all three inputs high, the NAND gate output 1A4A2Z8-6 falls to a low state. Identical exclusive-or circuits at 1A4A2Z8-12 and 1A4A2Z8-8 perform an identical function in examining for only a B input or only a C input. If two input signals appear simultaneously, caused by noise, no outputs from any of the gates occur.

c. The outputs from gate 1A4A2Z8-6, 1A4A-2Z2-12, and 1A4A2Z8-8 are connected respectively to the $A\overline{BC}$, $\overline{A}B\overline{C}$, and $\overline{AB}C$ inputs to the temporary storage register. With no inputs, the levels at 1A4A1Z12-1, -13, and -2 are all high, and the gate output 1A4A1Z12-12 is low. When any input occurs, one of the input levels falls, and the NAND gate output goes high. This high level appears at the Data Inhibit gate input, 1A4A1Z-12-11. In normal operation, the temporary storage register is held cleared, and gate input 1A4A1Z12-10 is also high. Under these conditions, the Data Inhibit line, 1A4A1Z12-8, goes low, starting the timing circuits. Alternately, if a bit is contained in each of the three positions of the register, it can accept no new information, 1A4A1Z12-10 will be low, and the incoming bit will not be stored.

d. The fall of the Data Inhibit line triggers the pulse width measuring one-shot at 1A4A2Z4-3, and is also applied at gate input 1A4A2Z6-4. Under normal conditions, the input pulse is 2 milliseconds long, and holds 1A4A2Z6-4 false during the 1.5-millisecond pulse output from 1A4A2Z4-6.

e. At the end of the first one-shot period, the fall of the pulse width one-shot, 1A4AZ4-6 triggers the clock one-shot at 1A4A2Z5-3, which generates a positive 40-microsecond clock pulse at 1A4A2Z5-6, and a resulting negative pulse at gate output 1A4A2Z6-3. This 40-microsecond pulse, reinverted at 1A4A2Z3-8 forms the positive clock pulse to the temporary storage register.

f. The fall of gate output 1A4A2Z6-3 also triggers the clear one-shot at 1A4A2Z2-3. The positive output at 1A4A2Z2-6 is a 12-millisecond pulse which is double inverted through 1A4A2Z6-11 and 1A4A2Z3-6, removes the reset on the temporary storage register, and permits data to be stored.

g. At the end of the 40-microsecond clock pulse, the rise of 1A4A2Z6-3 is inverted by 1A4A2Z6-8 and triggers the pulse separation one-shot at 1A4A2Z1-3. The output is a negative 1.5-millisecond pulse which inhibits the clock output gate 1A4A2Z6-1, rejecting any pulses which do not have a 1.5-millisecond time separation. The cycle

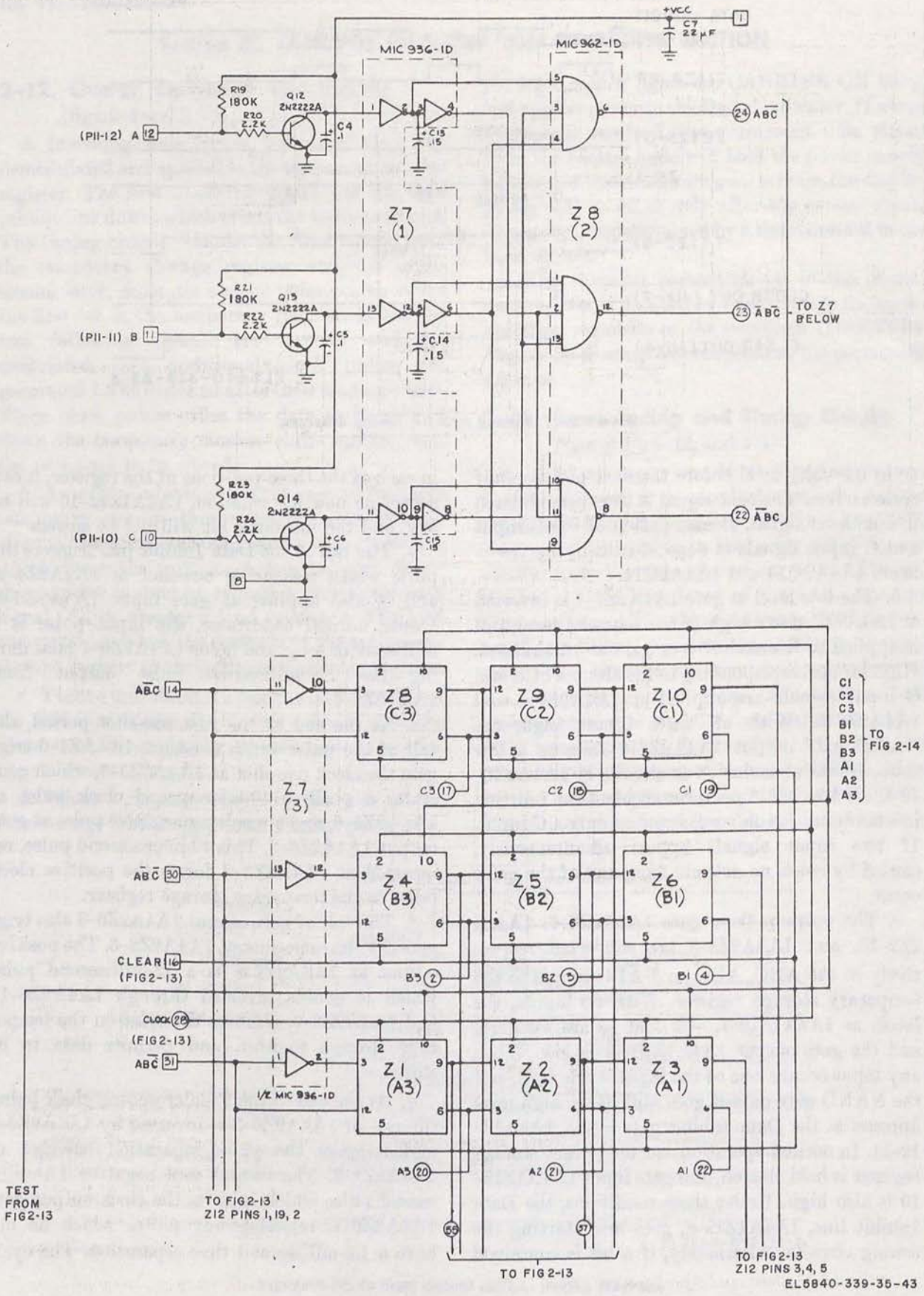


Figure 2-12. Command signal decoder assembly 1A4, input circuits and temporary storage register, schematic diagram.

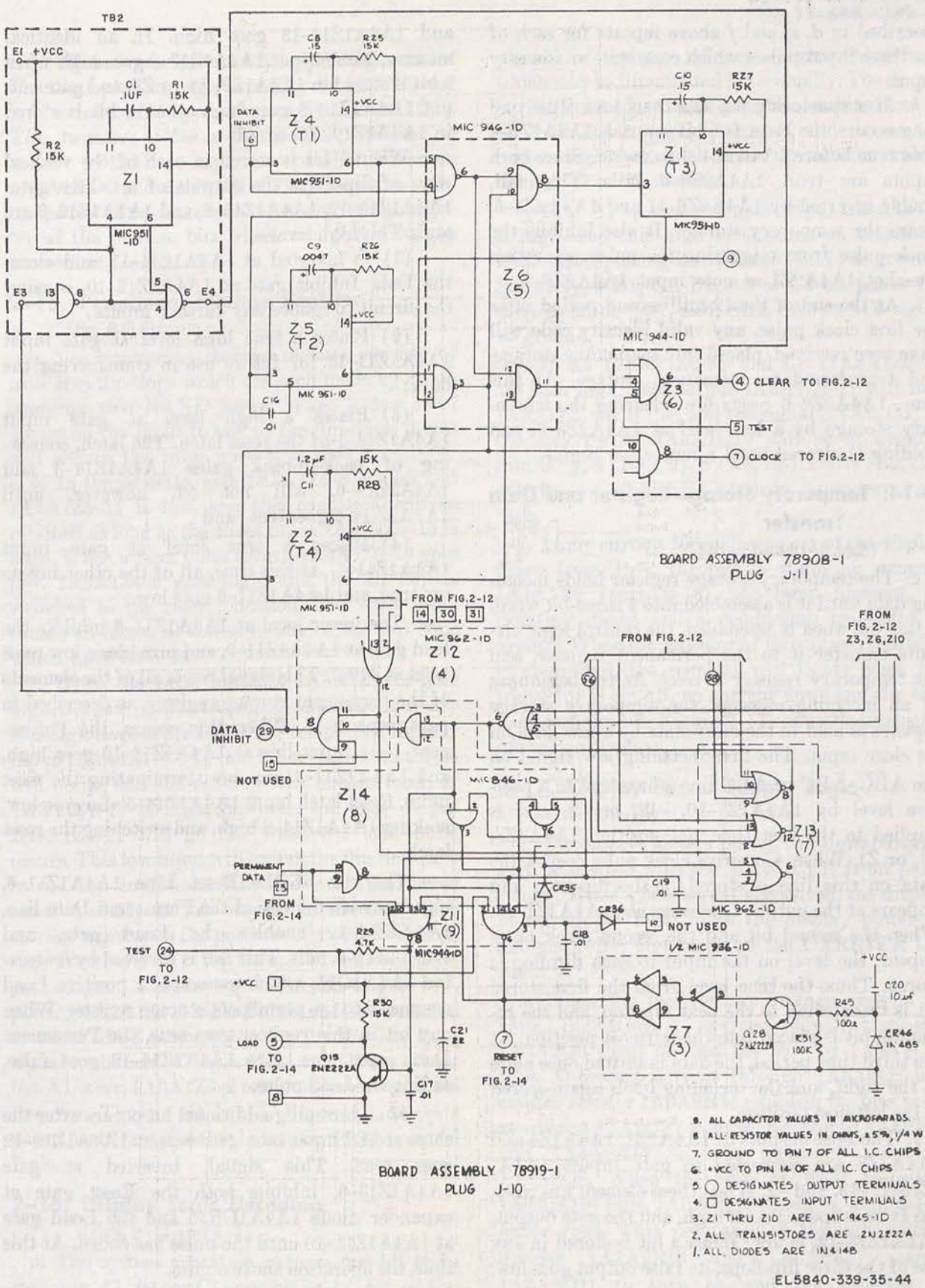


Figure 2-13. Command signal decoder assembly 1A4, control logic and timing circuits, schematic diagram.

described in *d*, *e*, and *f* above repeats for each of the three input pulses which constitute an identity input.

h. If a spurious pulse less than 1.5 millisecond long occurs, the Data Inhibit input at 1A4A2Z6–4 goes true before 1A4A2Z4–6 has reset. Since both inputs are true, 1A4A2Z6–6 falls. This fall, double-inverted by 1A4A2Z6–11 and 1A4A2Z3–6, clears the temporary storage. It also inhibits the clock pulse from triggering the pulse separation one-shot 1A4A2Z1 at gate input 1A4A2Z6–9.

i. At the end of the 12-millisecond period after the first clock pulse, any valid identity code will have been received, placed into temporary storage, and transferred to permanent storage. At this time, 1A4A2Z2–6 resets low, clearing the temporary storage by a low level at 1A4A2Z3–6, and holding it cleared until a new cycle begins.

2–14. Temporary Storage Register and Data Transfer

(figs. 2–12 and 2–13)

a. The temporary storage register holds incoming data until it is assembled into a three-bit word. After the word is assembled, the control logic circuits transfer it to the permanent register, and the temporary register is reset. At the beginning of an incoming message, the temporary storage register is held in the clear state by a low level on its clear input. The first incoming low signal on the $A\overline{BC}$, $\overline{A}B\overline{C}$ or $\overline{AB}C$ line is inverted to a positive level by 1A4A1Z7–10, –12, or –2, and is applied to the first time slot position 1A4A1Z8, Z4, or Z1. When a positive clock pulse occurs, the data on this line is stored in the flip-flop, and appears at the output (*for example*, 1A4A1Z1–6). When the second bit and the second clock pulse appear, the level on the input to each flip-flop is stored. Thus, the true level from the first stored bit is transferred to the next flip-flop, and the incoming bit is placed into the leftmost position. At the third time period, the data is shifted once more to the right, and the incoming bit is again stored in the leftmost position.

b. The false outputs of 1A4A1Z1, 1A4A1Z4 and 1A4A1Z8 are connected to gate inputs 1A4A1Z13–1, –13, and –2. When these element are reset, the false outputs are all high, and the gate output, 1A4A1Z13–12, is low. When a bit is stored in any one of the three flip-flops, its false output goes low, and 1A4A1Z13–13 goes high. In an identical manner, gate output 1A4A1Z13–8 goes high when a bit is stored in 1A4A1Z9, Z5, or Z2, and gate output 1A4A1Z12–6 goes high when a bit is stored in 1A4A1Z10, Z6, or Z3.

c. When a bit is stored in each of the vertical rows of flip-flops, the outputs of all three gates 1A4A1Z13–12, 1A4A1Z13–8, and 1A4A1Z12–6 are high. This high level—

(1) Is inverted at 1A4A1Z14–11, and closes the Data Inhibit gate at 1A4A1Z12–10, causing the circuit to ignore any further inputs;

(2) Places a true high level at gate input 1A4A1Z11–13 for future use in transferring the data;

(3) Places a high level at gate input 1A4A1Z14–1 of the reset latch. The latch, consisting of back-to-back gates 1A4A1Z14–3 and 1A4A1Z14–6, will not set, however, until 1A4A1Z 14–2 goes true; and

(4) Places a true level at gate input 1A4A1Z11–1. At this time, all of the other inputs are true, and 1A4A1Z11–6 goes low.

d. The lower level at 1A4A1Z11–6 inhibits the load gate at 1A4A1Z11–9, and provides a low reset level at J10–7. This signal resets all of the elements of the permanent storage register, as described in paragraph 2–15. When this occurs, the Permanent Data input line at 1A4A1Z14–10 goes high, and 1A4A1Z11–4 goes low, terminating the reset pulse. Reset latch input 1A4A1Z14–5 also goes low, making 1A4A1Z14–2 high, and switching the reset latch.

e. The rise of the Reset Line 1A4A1Z11–6, together with the rise of the Permanent Data line, 1A4A1Z11–12 enables the Load gate, and 1A4A1Z11–8 falls. This fall is inverted by transistor 1A4A1Q15, which generates a positive Load command to the permanent storage register. When any bit in this register goes true, the Permanent Data input line, gate 1A4A1Z14–12 goes false, ending the Load pulse.

f. If an incoming additional bit occurs after the three stored input bits, gate output 1A4A1Z12–12 goes true. This signal, inverted at gate 1A4A1Z13–6, inhibits both the Reset gate at expander diode 1A4A1CR35 and the Load gate at 1A4A1Z11–10 until the pulse has ended. At this time, the operation above occurs.

g. When power is initially applied, the rise of Vcc is coupled through capacitor 1A4A1C20, and is inverted and steepened by amplifier 1A4A1Q28. This negative pulse is further steepened by inverter 1A4A1Z–4, and the parallel inverters 1A4A1Z7–6 and 1A4A1Z7–8. This negative pulse on the reset line clears the permanent storage register of the random bits which occurred when the power first came on.

2–15. Permanent Storage Register

(fig. 2–14)

a. The permanent storage register consists of nine R-S flip-flops which are each made by cross-coupling two NAND gates. When a low level occurs on the input to any of the flip-flops, it sets and retains the value until it is reset.

b. In the set state, gate 1A3A1Z4–8 is high and 1A3A1Z5–11 is low, and this condition will be retained as long as the Reset input 1A3A1Z5–13 is high. When a reset pulse occurs, 1A3A1Z5–13 goes low, 1A3A1Z4–9 goes high, and the flip-flop is switched to the reset condition. The reset pulse causes an identical action in any of the flip-flops which have been set.

c. When the Load input at 1A3A1Z4–12 goes high, the gate output 1A3A1Z4–11 will go low only if a high level is present at the temporary register input 1A3A1Z4–13. If this input is low, no action will occur, and the flip-flop will remain reset. If 1A3A1Z4–13 is high, however, the gate output 1A3A1Z4–11 will go low when the load pulse occurs. This low input will switch the flip-flop back to its set condition. All bits are transferred simultaneously in this way from the temporary storage register to the permanent storage register.

d. If either a bit in the B1 or C1 position occurs, gate output 1A3A1Z2–3 or 1A3A1Z2–11 goes low, placing 1A3A1Z2–6 high. This high level, inverted at 1A3A1Z3–4 becomes the low Permanent Data signal to the control logic. If B1 and C1 are not set but A1 is set, 1A3A1Z3–2 sets the Permanent Data line low. Thus, a bit in A1, B1, or C1 causes a permanent Data signal to be returned to the control logic.

2–16. Display Logic Decoding

(figs. 2–14 and 4–7)

a. The system operation permits one bit to be stored in A1, B1, or C1; one bit in A2, B2, or C2; and one bit in A3, B3, or C3. The digital indicator consists of two sets of seven segments, each of which may be illuminated individually. The decoding logic decodes the 27 possible combinations in the permanent storage register, and drives the proper segments which make up the numerals 1 through 27 on the display.

b. If an A1 bit is stored, gate output 1A3A1Z4–8 is high, and this high level turns on transistor 1A3A1Q16, placing its collector (SA1) at ground. Similarly, a B1, C1, B2, A3 or C3 bit places the corresponding SB1, SC1, SB2, SA3 or SC3 signal at ground.

c. If A2 (1A3A1Z6–3) and C3 (1A3A1Z9–3) are both high, gate output 1A3A1Z6–11 will fall, 1A3A1Z3–8 will rise, and the signal S (A2, C3) at the collector of 1A3A1Q19 will be at ground. Similarly, S (B3, C2), S (A2, B3), and S (B2, C3) will be low when both of their input terms are high.

d. Lamp current for each segment of the display flows from B+, through a dimming control, 1A1A1R2 (para 2–16), the lamp filament, an isolating diode, and a conducting transistor to ground. When the collector of its control transistor is at ground, the segment will light; when the transistor is cut off, no current flows and the segment remains off. Figure 2–17 shows the segments of the two displays.

2–17. Display Power Supply Logic

(fig. 2–16)

a. To conserve battery power, the digital display may be cleared with the MAN. CLR front panel switch. When a new signal is received, the display power supply logic turns the display power on automatically, and turns on the CARRIER ON light.

b. When the receiver agc voltage exceeds 2.5 volts, indicating a received signal, transistor 1A3A2Q9 turns on and the base of 1A3A2Q10 falls. Quiescent current through 1A3A2Q8 and emitter resistor 1A3A2R14 establish the bias point at which 1A3A2Q9 conducts. Resistors 1A3A2R12 and 1A3A2R13 set the quiescent point of 1A3A2Q8. When the base of PNP transistor 1A3A2Q10 falls, 1A3A3Q10 conducts, and its collector rises. This rise, applied through voltage divider 1A3A2R16 and 1A3A2R17, causes 1A3A2Q11 to turn on and the collector of 1A3A2Q11 is placed at ground. Current flows

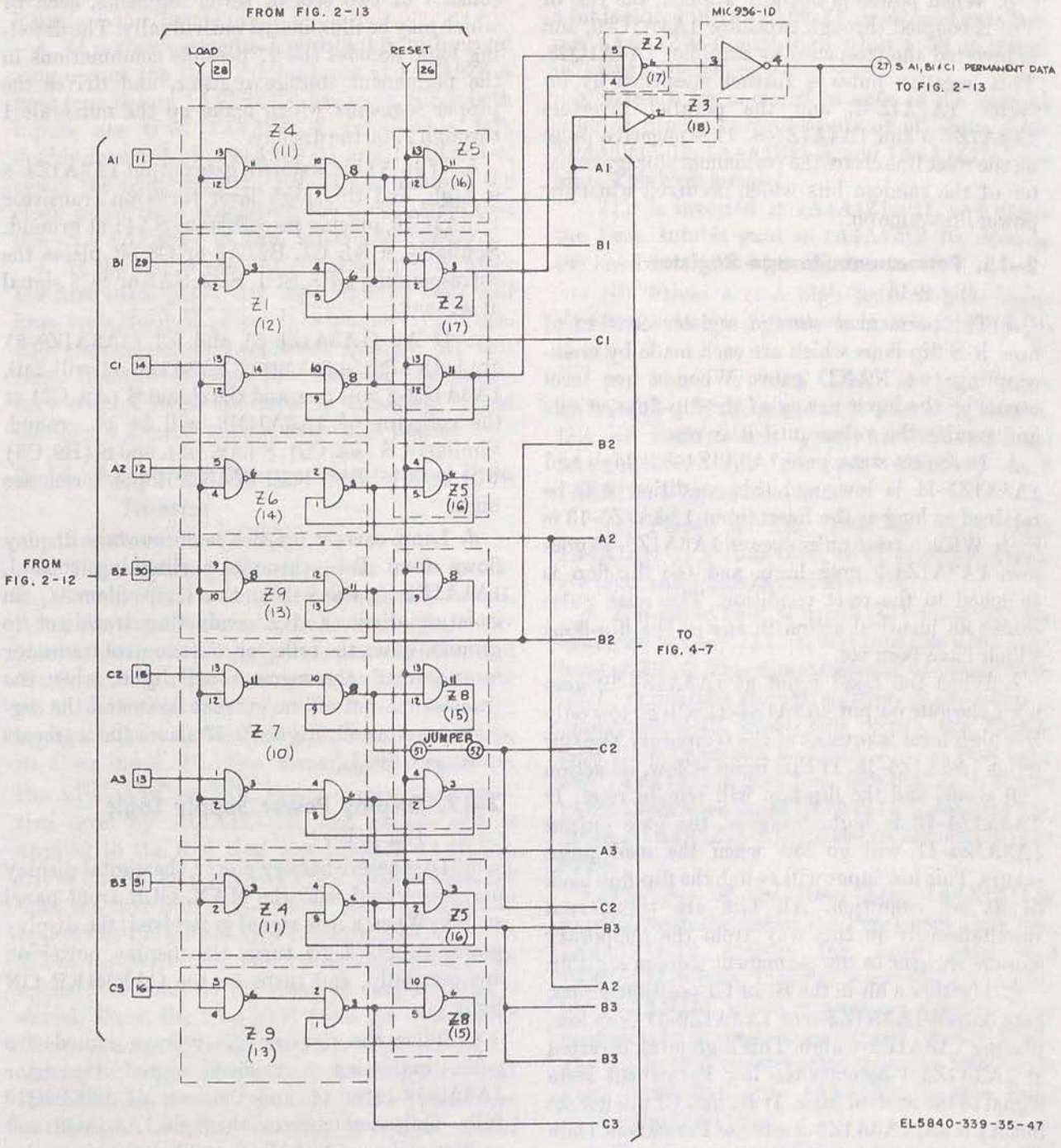


Figure 2-14. Data converter-power supply assembly 1A3, permanent storage register, schematic diagram.

through the CARRIER ON lamp, 1A1A11, isolating diode 1A3A2CR1, and through 1A3A2Q11, and the CARRIER ON light comes on. Feedback resistor 1A3A2R44, is now effectively between the base of 1A3A2Q8 and ground, shunting resistor 1A3A2R13. This reduces the current flow through 1A3A2Q8 and 1A3A2R14, lowering the emitter of 1A3A2Q9, and eliminating fluctuations caused by a marginal agc input level.

c. When transistor 1A3A2Q11 conducts, current also flows through 1A3A2R2, 1A3A2CR4, 1A3A2Q11, and the junction of 1A3A2CR4 and 1A3A2CR5 is close to ground. Capacitor 1A3A-2C22, which had charged to +.6 volt through 1A3A2R2, discharges through 1A3A2R3. This time constant lessens the response of the circuit to transient noise spikes. When 1A3A2C22 has discharged, transistor 1A3A2Q1 cuts off, 1A3A2Q2 conducts, and 1A3A2Q3 cuts off. The voltage rise at the base of emitter follower 1A3A2Q5 causes its emitter to rise, turning on the pass transistor, 1A1A1Q6 on the front panel. The output voltage from the emitter of 1A1A1Q6 is applied through voltage divider 1A3A2R9 and 1A3A2R10 to regulator amplifier 1A3A2Q4, which controls 1A3A-2Q5 as a conventional power supply regulator.

d. Battery voltage is applied through 1A3A-2R11 to Zener diode 1A3A2CR7, which provides a constant output voltage to the DIM potentiometer 1A1A1R2. The arm of this potentiometer controls the current through dimming transistor 1A1A1Q7 to the digital indicator filaments.

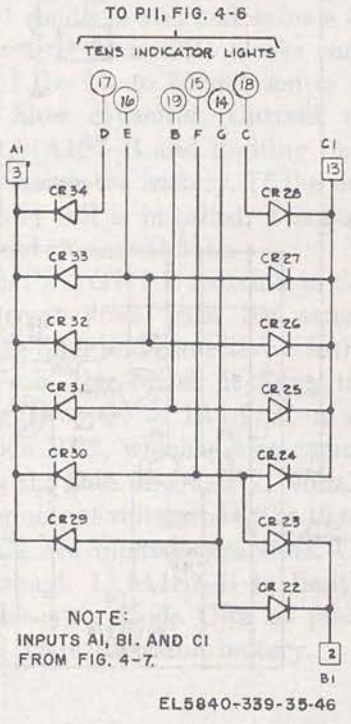


Figure 2-15. Command signal decoder assembly 1A4, tens display decoding logic, schematic diagram.

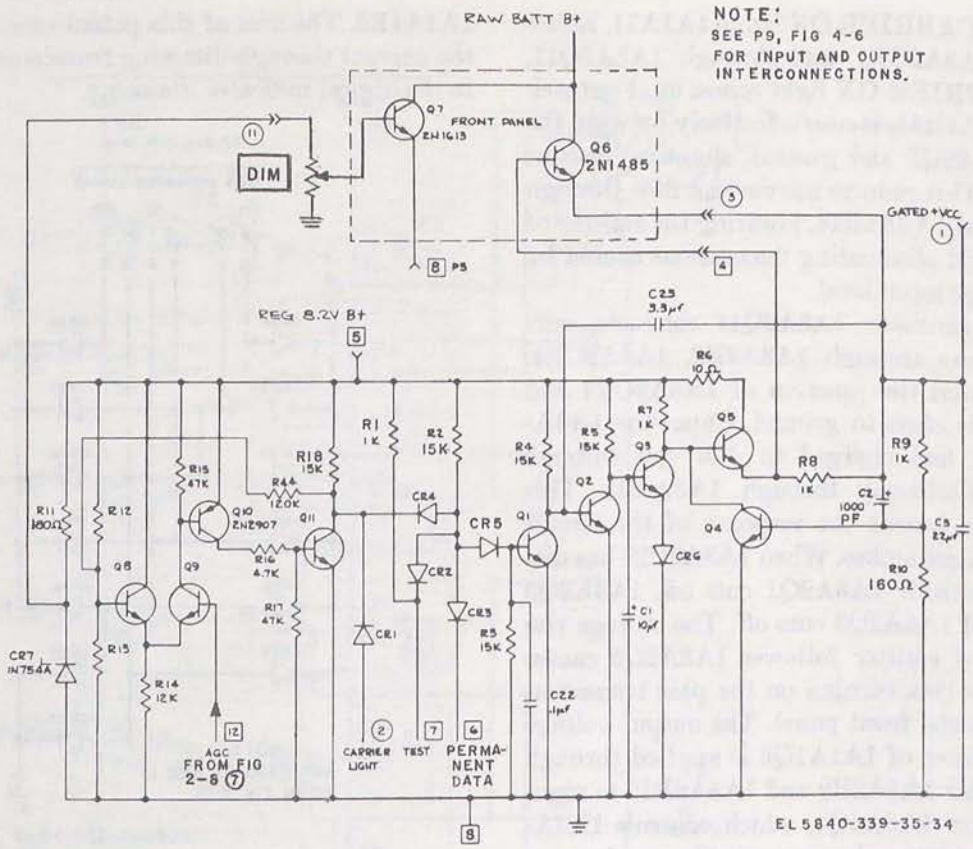


Figure 2-16. Data converter-power supply assembly 1A3, display power supply logic, schematic diagram.

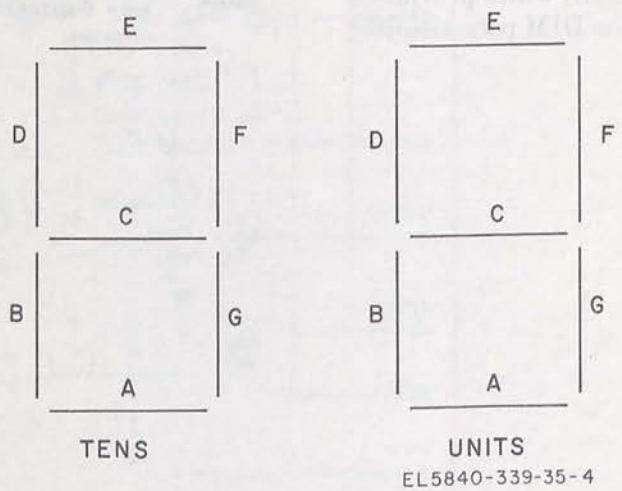


Figure 2-17. Digital indicator assembly 1A2, display segments, pictorial diagram.

Section IV. ANALYSIS OF OPERATION OF POWER CIRCUITS

2-18. Power Distribution

(fig. 2-2)

a. The AN/USQ-42 may be operated from three sources of power: a nonrechargeable mercury cell battery, a rechargeable Nicad battery, or an external 24- to 32-volt dc source. The Nicad battery may be recharged by connecting the set to a source of 24 to 32 volts dc, and placing the POWER switch to CHG. When the set is operated from external power, a regulator in the mounting adapter drops the source voltage to 10 volts, which powers the set, and trickle-charges the Nicad battery.

b. When the POWER switch is in the INT position, current flows from the battery anode through switch 1A1A1S7-A and fuse 1A1A1F2 to the set. It returns through chassis ground to the battery cathode. Inductor L1 and capacitor C1 form a smoothing filter to remove spikes and noise on the incoming line. Resistor R1 and Zener diode VR1 form a protective circuit to eliminate the effects of high voltage surges which may occur on the power line. If the input voltage exceeds 33 volts, VR1 conducts and maintains a 33-volt output. Protective diode CR1 blocks current if the polarity of the 24- to 32-volt source is reversed. C2 is a filter capacitor. Current then passes through 1A1A1S7-B and limiting resistor R3 to P15-1 to charge the battery. If the nonrechargeable mercury cell is installed, it is not connected to P15-1 and no current flows.

c. When the POWER switch is in the EXT position, current flows from the external source through the filter and protective circuits to 1A1A1S7-B. From the switch it flows through the power regulator Q1 to 1A1A1S7-A and the set. Zener diode VR2, which draws current through R4, keeps the base of Q2 at 11 volts, which sets the emitter output voltage of Q2 at 10 to 10.4 volts. C3 and C4 are filtered capacitors. Current also passes through 1A1A1S7-B to limiting resistor R2 and blocking diode CR2 to place a trickle charge on the rechargeable battery.

CHAPTER 3

DIRECT SUPPORT MAINTENANCE

Section I. GENERAL

3–1. Scope of Direct Support Maintenance

Direct Support Maintenance of the AN/USQ–42 includes troubleshooting the defective set to the replaceable assembly level, replacement of defective assemblies, and verification that the assembly replacement has restored the set to satisfactory service. This chapter includes procedures for localizing faults, repair instructions, and test sequences to verify proper operation of the set after repair.

3–2. Test Equipment Required

The following chart lists the test equipment required for troubleshooting the AN/USQ–42 at the direct support maintenance category:

Test equipment	*Type*
Test set, rf monitor set (test set).	
Oscilloscope	Tektronix 535 or equivalent.
Multimeter	Simpson 250 or equivalent.
24- to 32-volt dc power source, 1 ampere.	
Power input cable	
Mounting adapter	
Power connection cable	

Section II. TROUBLESHOOTING

3–3. General

The direct support maintenance category troubleshooting instructions are contained in this section of the manual. Complete troubleshooting procedures for the Monitor Set begin with the organizational maintenance tests (TM 11–5840–339–12). The procedures in this chapter enable the maintenance technician to isolate the trouble to a specific unitized electronic assembly, to the circuits within the mounting adapter, or to the circuits wired in the front housing assembly.

3–4. Troubleshooting Procedure

a. General. Follow the general procedures listed in the *Symptom* column of the troubleshooting chart (para 3–5). These procedures are operational checks which are performed under bench test conditions using the test set (use external 24 v at 1 amp supply). Proceed with the operational checks until the trouble symptoms are known. If the symptom is as described, proceed in sequence through the tests, and take the corrective action outlined. If the symptoms are not as described, go to the item referenced in the *Next step* column.

Caution: **Do not adjust any control on the unitized electronic assemblies. All of these control settings require specialized test equipment, and are aligned only at the depot category of maintenance.**

b. Test Setup (fig. 3–1).

(1) Remove the battery pack cover and the rear housing assembly from the AN/USQ–42.

(2) Mount the battery pack in the mounting adapter.

(3) Connect the power input cable between the mounting adapter rear connector and the 24- to 32-volt power supply.

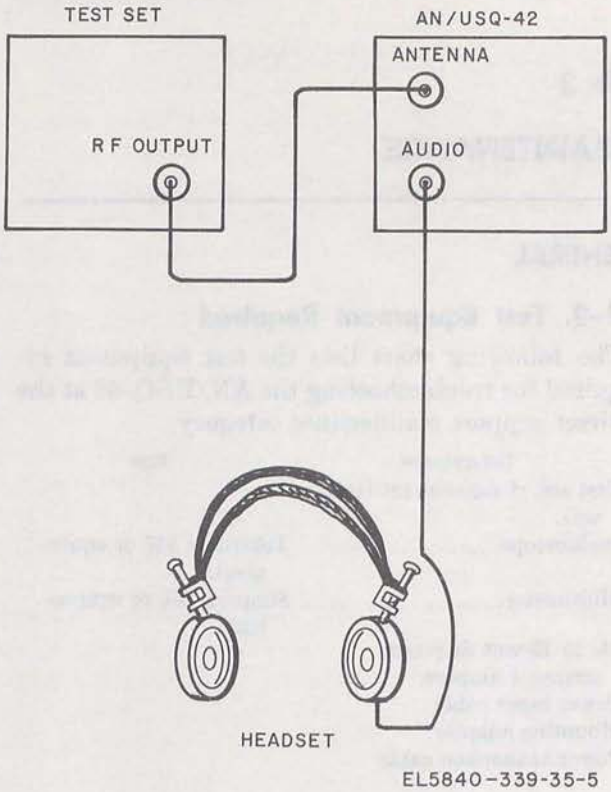


Figure 3-1. Direct support maintenance test setup.

(4) Connect the power connection cable between the battery pack connector and the connector on the front housing assembly.

(5) Connect the test set RF—OUTPUT jack to the AN/USQ-42 ANTENNA jack.

(6) Connect the headset to the AN/USQ-42 AUDIO connector.

(7) Set the test set controls as follows:

(*a*) POWER to INT. or EXT.
(*b*) RF CHANNEL to 01.
(*c*) DB ATTENUATOR to 100 DB.
(*d*) AUDIO TONE to 1KC.
(*e*) RF LEVEL SET to midrange.
(*f*) AUDIO LEVEL SET to midrange.
(*g*) TONE LEVEL SET to midrange.
(*h*) TONE CHANNEL to 01.
(*i*) FREE RUN-SINGLE CODE to FREE-RUN.
(*j*) DEV CW-XTAL-CODE to DEV CW.

(8) Set the AN/USQ-42 controls as follows:

(*a*) POWER to INT.
(*b*) SQUELCH to OFF.
(*c*) CHANNEL to 01.
(*d*) SIG STR to LOW.

3-5. Troubleshooting Chart

Item No.	Symptom	Probable trouble	Corrective action	Next step
1	IDENTITY display remains blank when TEST switch is operated.	*a.* Power circuit fault	*a.* Measure battery voltage by setting SIG STR switch to BAT. VOLTAGE.	3
			b. Check fuse F1.	
2	Voltage at fuse F1 is less than 8.0 volts.	*a.* Discharged battery	*a.* Check the rechargeable battery is installed in battery pack cover. Set POWER witch to CHG. Replace fuse and change battery.	
		b. Defective POWER switch 1A1A1S7.	*b.* Measure voltage at battery terminals during charging cycle. If voltage is less than 10.5 volts, return AN/USQ-42 for general support maintenance.	
3	Number 01 does not appear on IDENTIFY display, and no 1-KHz tone in headset when test set POWER switch is set to INT.	Defective receiver circuit	Remove preselector-synthesizer assembly 1A6.	9

Item No.	Symptom	Probable trouble	Corrective action	Next step
4	Voltage at J6–1 is less than 8.0 volts.	Defective internal power wiring	Return AN/USQ–42 for general support maintenance.	5
5	Voltage at pins of J6 corresponding to channel 01 oscillator (table 2–1) is less than 8.0 volts.	Defective channel selection logic	Return AN/USQ–42 for general support maintenance.	6
6	Voltages at J6–4 and J6–5 do not correspond to values for channel 01 (table 2–1). Reinstall preselector-synthesizer assembly 1A6. Remove filter assembly 1A5.	Defective tuning voltage circuit	Return AN/USQ–42 for general support maintenance.	7
7	Low voltage at J13	Defective preselector-synthesizer assembly (A6).	Replace preselector-synthesizer assembly 1A6. Reinstall amplifier filter assembly 1A5, and retest.	8
8	Reinstall amplifier-filter assembly 1A5. Remove command signal decoder assembly 1A4. Remove headset.			
9	IDENTITY display indicates 01, but no 1-KHz tone in headset.	*a.* Defective headset *b.* Defective audio amplifier in amplifier filter assembly 1A5. *c.* Defective squelch circuit	*a.* Check headset by substitution *b.* Replace amplifier-filter assembly 1A5, and retest. *c.* Return AN/USQ–42 for general support maintenance.	10
10	One-KHz tone in headset, but no IDENTITY display.	Defective digital section curcuit	Remove command signal decoder assembly 1A4.	15
11	No tone burst oscilloscope patterns at J11–10, J11–11 and J11–12.	Defective filter in amplifier-filter assembly 1A5.	Replace amplifier-filter assembly 1A5. Reinstall command signal decoder assembly 1A4, and retest.	
12	Remove data converter power supply assembly 1A3. Bit patterns on pins J10–2 to J10–4 and J10–17 to J10–23 do not agree with patterns for channel 01 (table 5–3).	Defective command signal decoder assembly 1A4.	Replace command signal decoder assembly 1A4. Reinstall data converter-power supply assembly 1A3, and retest.	
13	Remove digital indicator assembly 1A2. DC levels on indicator connector J3 are not correct.	Defective data converter-power supply assembly 1A3.	Replace data converter-power supply assembly 1A3. Reinstall digital indicator assembly 1A2, and retest.	
14	No reading on digital indicator	Defective digital indicator assembly 1A2.	Check digital indicator assembly by substitution.	
15	Missing segments on IDENTITY display.	Defective digital indicator assembly 1A2.	Check digital indicator assembly by substitution.	16
16	Missing segments in units column of IDENTITY display.	Defective data converter-power supply assembly 1A3.	Replace data converter-power supply assembly 1A3.	17
17	Missing segments in tens column of IDENTITY display.	Defective command signal decoder assembly 1A4.	Replace command signal decoder assembly 1A4.	18
18	AN/USQ–42 receives some, but not all channels.	*a.* Defective oscillator in preselector-synthesizer assembly 1A6. *b.* Defective component in channel selection logic.	*a.* Replace preselector-synthesizer assembly 1A6. *b.* Return AN/USQ–42 for general support maintenance.	19
19	Signal strength meter and audio signal fluctuate during transmission.	Defective agc circuit on amplifier-filter assembly 1A5.	Replace amplifier-filter assembly 1A5.	20

308-129 O - 68 - 3

Item No.	Symptom	Probable trouble	Corrective action	Next step
20	SQUELCH control does not vary squelch level.	*a.* Defective squelch circuit on amplifier-filter assembly 1A5.	*a.* Replace amplifier-assembly 1A5.	
		b. Defective SQUELCH control	*b.* Return AN/USQ-42 for general support maintenance.	

Section III. REMOVAL AND REPLACEMENT

3-6. Removal and Replacement of AN/USQ-42 Cover

(fig. 3-2)

a. Remove battery pack cover by releasing the four latches and pulling it off slowly to disengage connector.

b. Remove rear housing assembly by releasing the four latches and pulling it off slowly to disengage connector.

c. Replace unitized electronic assemblies as described in paragraph 3-7.

d. Replace rear housing assembly by aligning connector guide pins and pushing assemblies together. Secure latches.

e. Replace battery pack cover by aligning connector guide pins and pushing assemblies together. Secure latches.

3-7. Removal and Replacement of Unitized Electronic Assemblies

(fig. 3-3)

***Caution:* Do not adjust any control on any unitized electronic assembly.**

a. Loosen the three assembly holddown screws until the screws are completely disengaged from the mounting plate.

b. Remove the assembly from the mounting plate by pulling up at the sides.

c. Align the connectors of the new assembly with the mounting plate connectors.

d. Push the assembly down gently until the connectors are fully engaged. Do not use excessive force.

e. Tighten the three holddown screws.

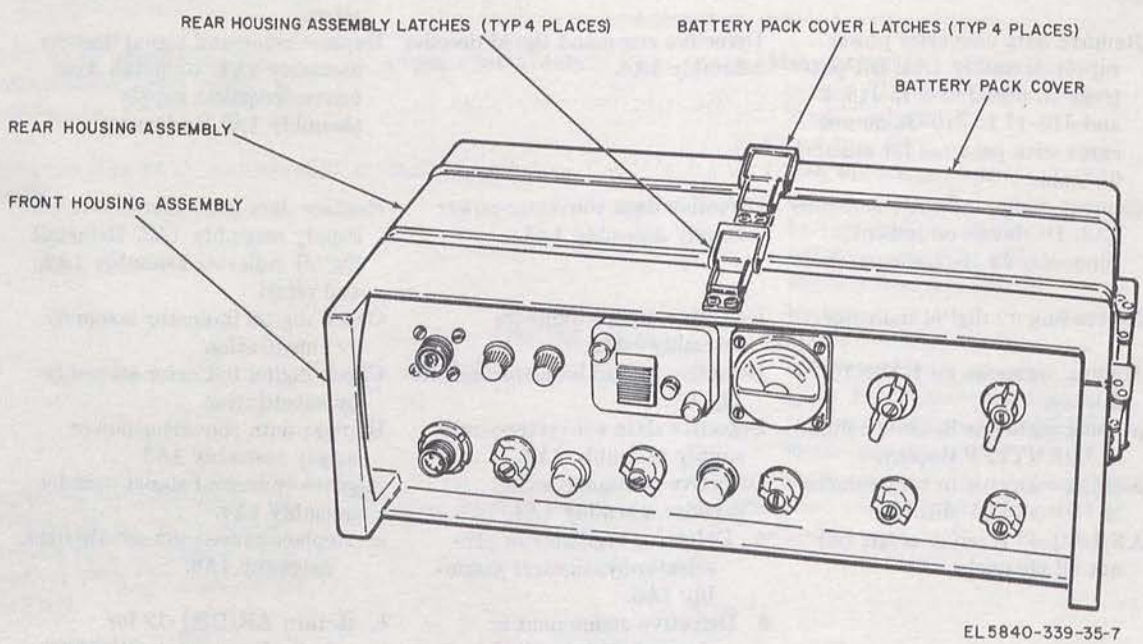


Figure 3-2. AN/USQ-42 front housing assembly 1A1, front view.

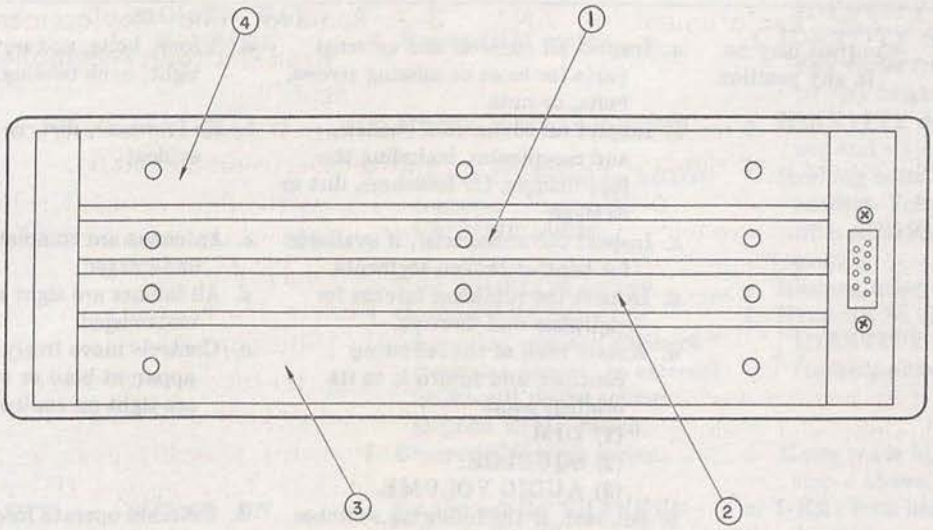
3-8. Removal and Replacement of Digital Indicator Assembly 1A2

a. Loosen the two thumbscrews until the screws are disengaged from the set.

b. Lift the digital indicator assembly out of the well.

c. Insert the new digital indicator assembly into the well and push down gently.

d. Tighten the two thumbscrews.



(1) IA3 78922-1 DATA CONVERTER-POWER SUPPLY ASSY
(2) IA4 78921-1 DECODER COMMAND SIGNAL
(3) IA5 78923-1 AMPLIFIER FILTER ASSY
(4) IA6 78928-1 PRESELECTOR-SYNTHESIZER

EL5840-339-35-8

Figure 3-3. AN/USQ-42 disassembled, rear view board location.

Section IV. DIRECT SUPPORT TESTING PROCEDURE

3-9. General

This section provides test procedures for use by the direct support technician to determine whether repaired equipment is performing satisfactorily before it is returned to the using organization. The procedure steps should be followed in the order given, and all controls must be set to the indicated positions.

3-10. Physical Testing Procedure

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	N/A	Controls may be in any position.	*a.* Inspect all controls and external parts for loose or missing screws, bolts, or nuts.	*a.* Screws, bolts, and nuts must be tight; none missing.
			b. Inspect all connectors, sockets, and receptacles, including the fuse holders, for looseness, dirt or damage.	*b.* No looseness, dirt, or damage evident.
			c. Inspect the antenna(s), if available for bent or broken segments.	*c.* Antennas are complete and undamaged.
			d. Inspect the retaining latches for tightness and damage.	*d.* All latches are tight and undamaged.
2	N/A		*a.* Rotate each of the following controls, and return it to its original point: (1) DIM. (2) SQUELCH. (3) AUDIO VOLUME.	*a.* Controls move freely with no apparent bind or sticking. Knobs are tight on control shaft.
			b. Set each of the following switches to each of its positions: (1) POWER. (2) SIG STR. (3) CHANNEL (2). (4) SQUELCH. (5) TEST. (6) MAN CLR.	*b.* Switches operate freely, without bind. Knobs are tight on control shafts.

3–11. Functional Testing Procedure

Connect the test set as shown in figure 3–1, and perform the following procedures.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	POWER to OFF	POWER: INT. SQUELCH: OFF. SQUELCH: ON. POWER: EXT. POWER: CHG. SIG STR: BAT VOLTAGE	*a.* Set SIG STR switch to BAT VOLTAGE.	*a.* SIG STR meter reads in green zone.
			b. Set SIG STR switch to LOW	*b.* No deflection on SIG STR meter.
			c. Depress TEST switch	*c.* Numerals 88 appear in IDENTITY window.
			d. Rotate DIM control	*d.* IDENTITY display brightness varies from very dim to very bright.
			e. Depress MAN CLR switch	*e.* IDENTITY display goes out and stays out.
			f. Connect H headset to AUDIO connector. Vary AUDIO VOLUME control.	*f.* Rushing noise heard in headset. Volume variable with AUDIO VOLUME control.
			g. Vary SQUELCH control	*g.* Rushing noise is reduced.
			h. Connect AN/USQ–42 to mounting adapter. Connect mounting adapter to external 24–32-volt power source. Depress TEST switch.	*h.* Numerals 88 appear in IDENTITY window. Rushing noise in headset.
			i. Observe SIG STR meter	*i.* Meter reads higher than in step *a* above.
2	POWER: INT. DB ATTENUATOR: 100DB. AUDIO TONE: 1KC. FREE–RUN–SINGLE CODE: FREE–RUN. DEV CW–XTAL–CODE: DEV CW. TONE CHANNEL: 01. RF CHANNEL: as indicated in procedure.	POWER: ON. SIG STR: LOW. CHANNEL: as indicated in procedure.	*a.* Set test set RF CHANNEL 1 switch to 01.	*a.* 1-KHz tone heard in headset.
			b. Set AN/USQ–42 CHANNEL switch to 01.	*b.* Numerals 01 displayed in IDENTITY window.
			c. Depress MAN CLR switch. *Note.* Repeat the steps in *a* above, each time changing the channel switches on the test set and the AN/USQ–42. Repeat for channels 02 through 31.	*c.* SIG STR meter deflects.
3	RF CHANNEL: 31. TONE CHANNEL: as indicated in procedure.	CHANNEL: 31	Set test set TONE CHANNEL switches successively at 01 through 27.	At each setting, the numeral displayed in the IDENTITY window is the same as that set in the test set TONE CHANNEL switches.

CHAPTER 4

GENERAL SUPPORT MAINTENANCE

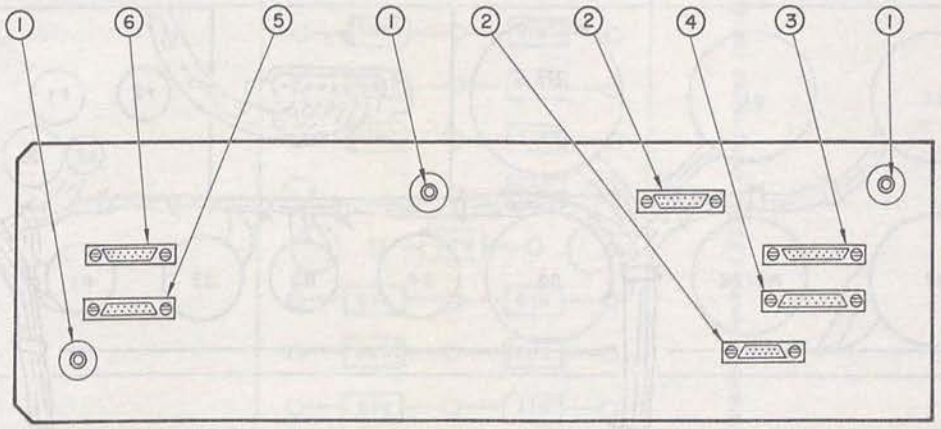
Section I. GENERAL

4-1. Scope of General Support Maintenance

General support maintenance of the AN/USQ-42 includes troubleshooting the defective set to the replaceable piece part (except unitized electronic assemblies). Removal and replacement instructions for components which are not part of a replaceable assembly are included. Maintenance of the power regulator circuits in the auxiliary mounting adapter is also included.

4-2. Test Equipment and Tools Required

In addition to the direct support maintenance test equipment specified in paragraph 3-2, Tool Kit, Radio Repairman TK100 is required for general support maintenance.



(1) CONNECTOR, RIGHT ANGLE
(2) CONNECTOR, 21 PIN
(3) CONNECTOR, 31 PIN
(4) CONNECTOR, 31 PIN
(5) CONNECTOR, 25 PIN
(6) CONNECTOR, 25PIN

EL5840-339-35-9

Figure 4-1. AN/USQ-42 disassembled, connector locations.

Section II. TROUBLESHOOTING

4-3. General

The general support maintenance category troubleshooting procedures contained in this section of the manual pertain to the isolation of piece part failures in the chassis of the AN/USQ-42 and its auxiliary mounting adapter. The circuit areas which are considered in this section are primarily—

a. Channel selection logic circuits.
b. Power supply circuits.
c. Front panel components and circuits.

4-4. Troubleshooting Procedures

a. General. The troubleshooting procedures which follow form a sequential pattern to isolate problems in each of the areas of general support

maintenance. Proceed with the operational checks until the defective component is isolated. If the symptom is as described, proceed in sequence through the tests.

Caution: **Do not adjust any control on the unitized electronic assemblies. All of these control settings require specialized test equipment, and are aligned only at the depot category of maintenance.**

b. Channel Selection Logic Troubleshooting (figs. 4–1, 4–2, 4–3, and 2–3).

(1) *Disassembly for troubleshooting and repair.*

(*a*) Remove battery pack cover and rear housing assembly as described in paragraph 3–4*b*.

(*b*) Remove all unitized electronic assemblies as described in paragraph 3–7.

(*c*) Remove ten screws and fold the module mounting plate outward.

(*d*) Connect the power connection cable between the battery pack assembly and 1AP4 on the front housing assembly.

(*e*) Set the POWER switch to INT.

(2) *Troubleshooting procedures.* In troubleshooting the channel selection logic, an analysis of operative and inoperative channels often points

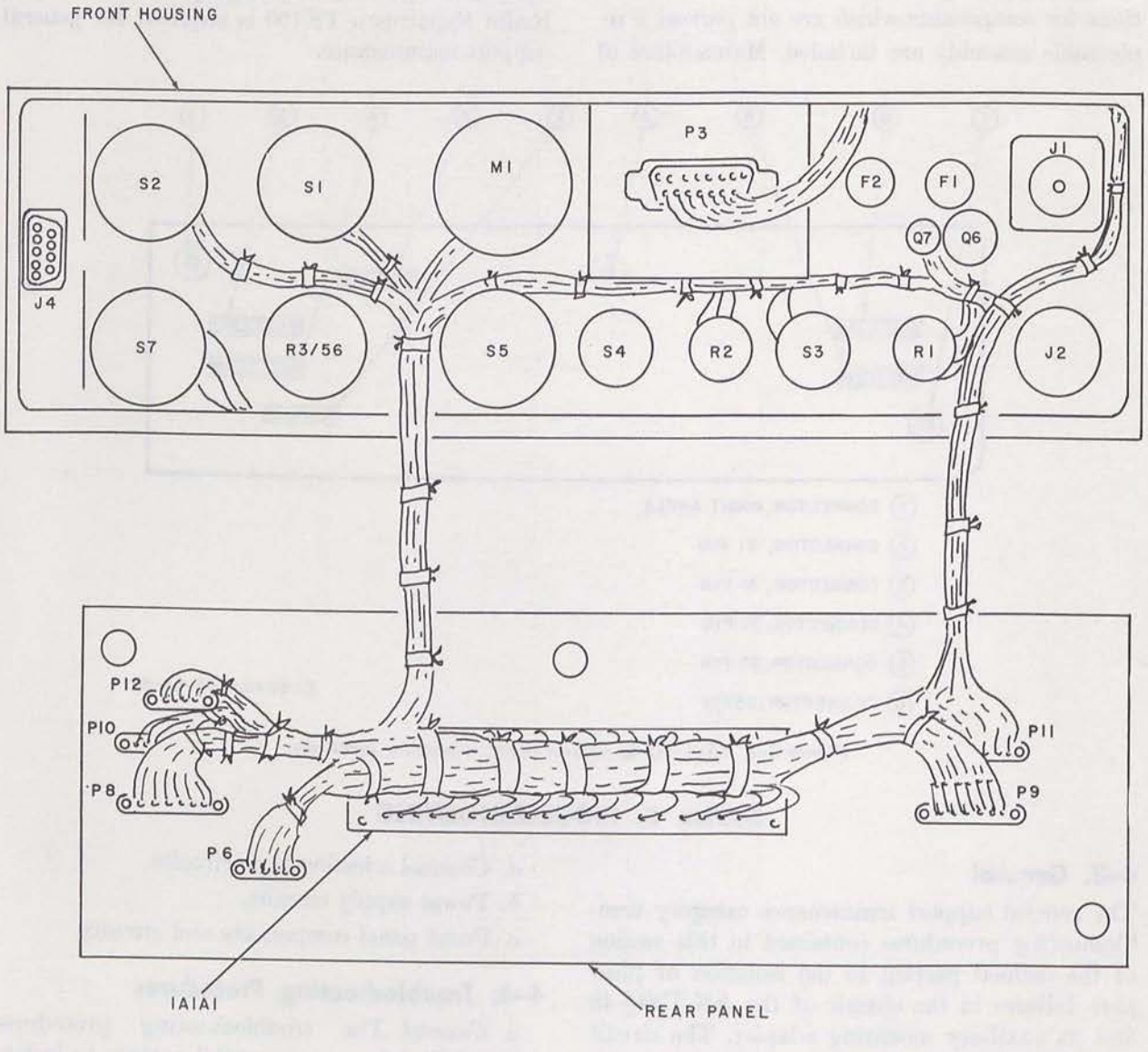
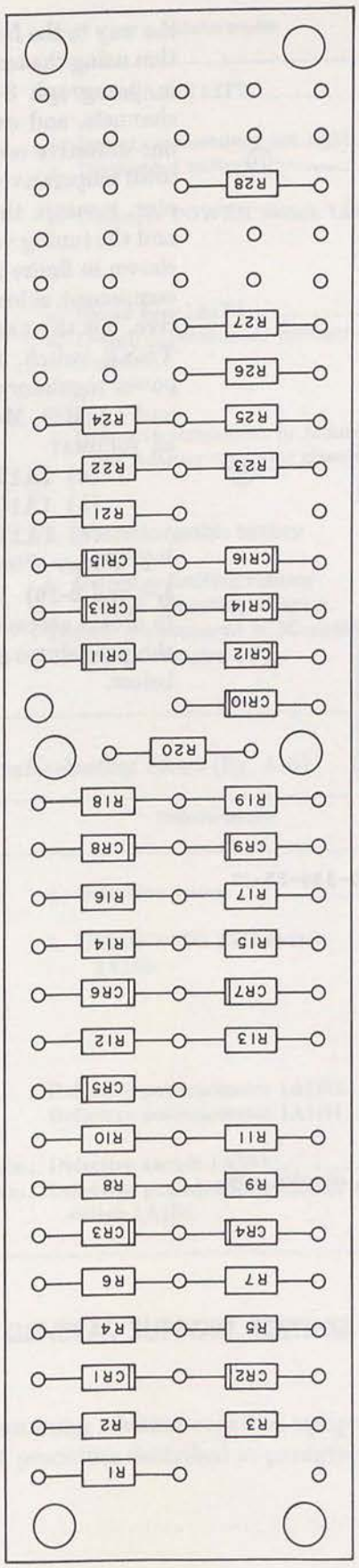


Figure 4–2. Front housing assembly 1A1, rear view.



EL5840-339-35-11

Figure 4-3. Terminal board 1A1A1, component location.

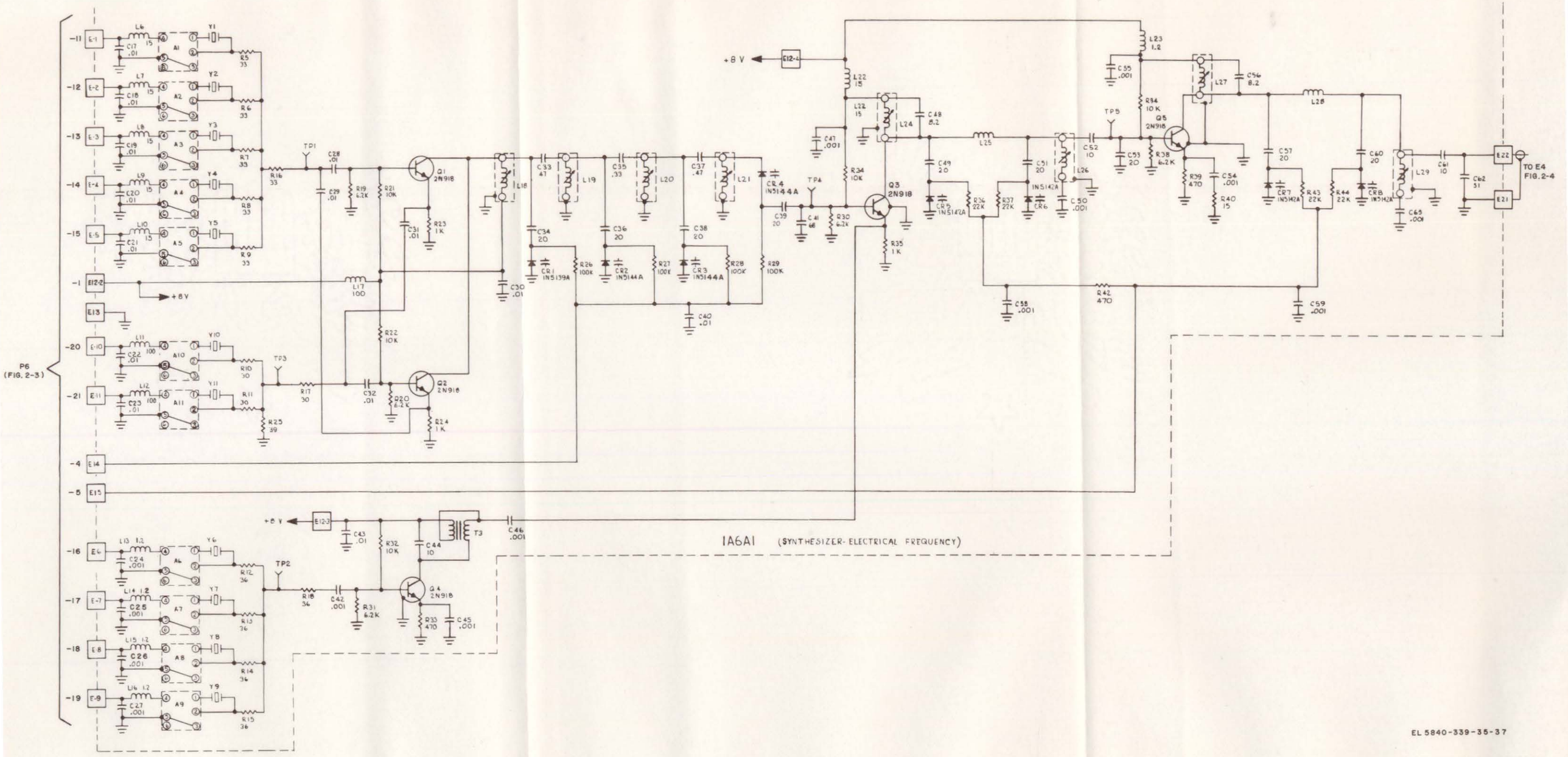


Figure 4-5. Preselector-synthesizer, schematic diagram.

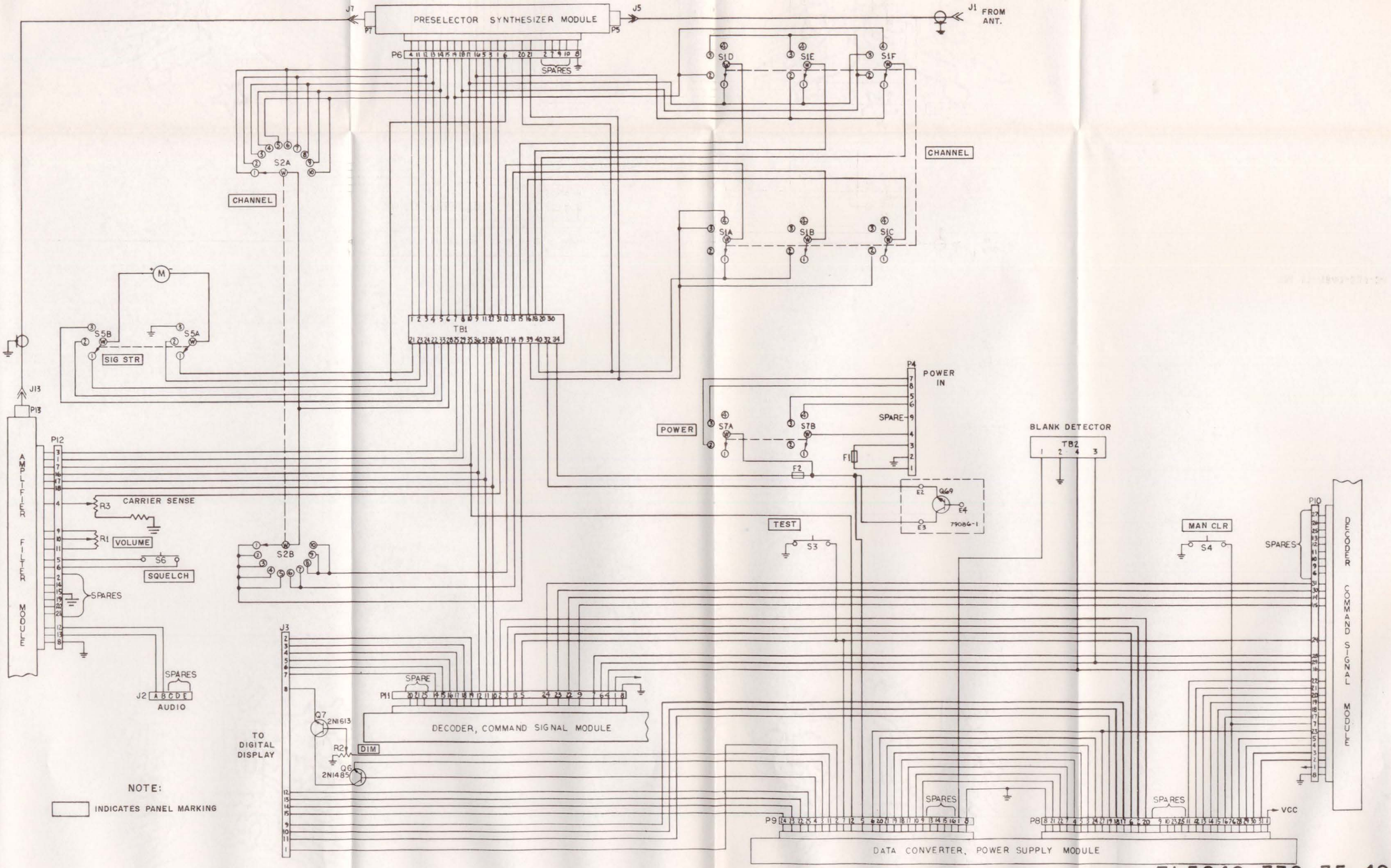


Figure 4-6. Front housing assembly 1A1, schematic diagram.

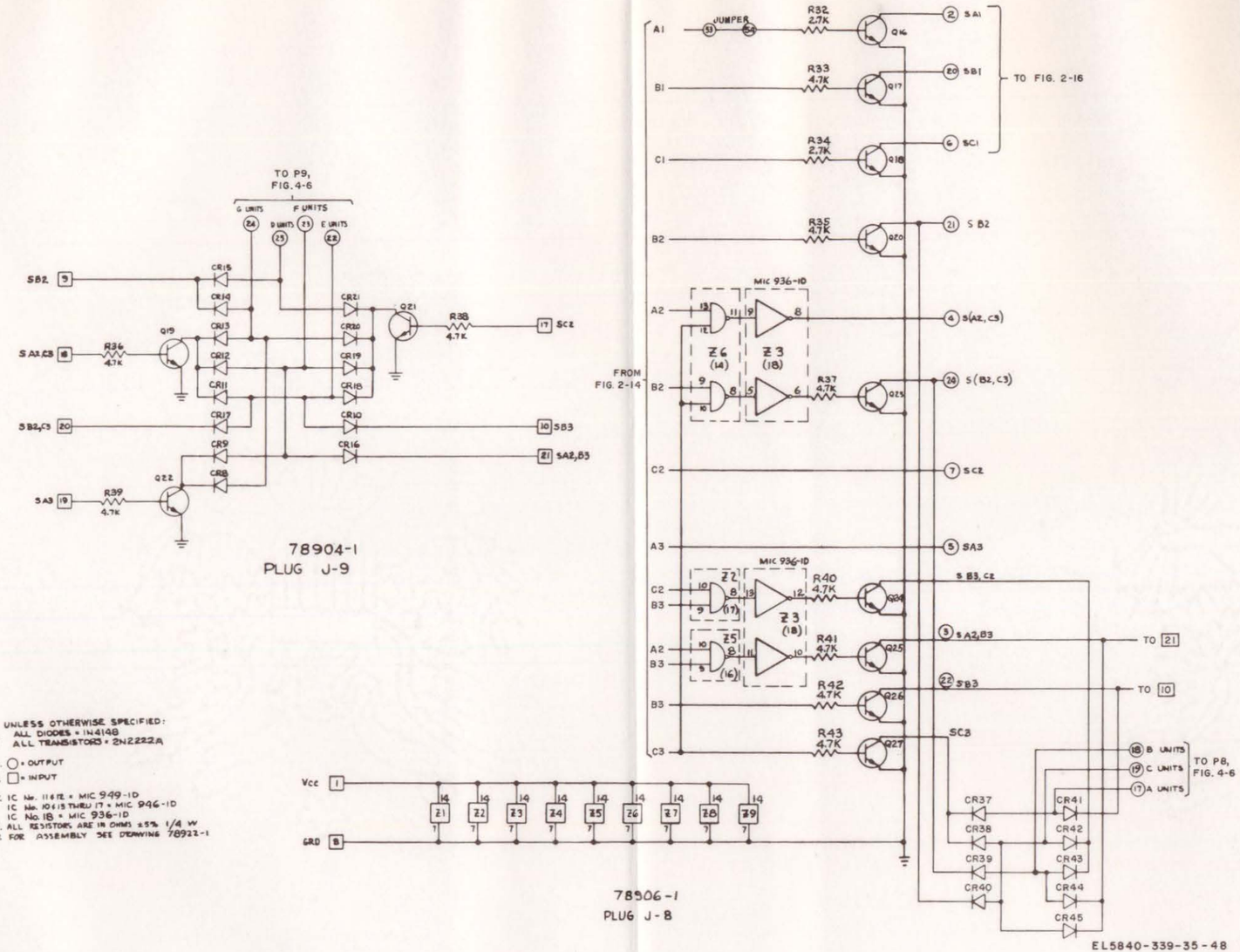


Figure 4-7. Data converter-power supply assembly 1A3, units display decoding logic, schematic diagram.

APPENDIX A

REFERENCES

DA Pam 310-4	Index of Technical Manuals, Technical Bulletins, Supply Manuals (types 7, 8, and 9), Supply Bulletins, and Lubrication Orders
DA PAM 310-7	U.S. Army Equipment Index of Modification Work Orders
TM 38-750	Army Equipment Record Procedures
TM 11-5840-339-12	Operator and Organizational Maintenance Manual, Radio Frequency Monitor Set AN/USQ-42