

TM 11-5805-367-35/2

DEPARTMENT OF THE ARMY TECHNICAL MANUAL

DS, GS, AND DEPOT MAINTENANCE MANUAL

MULTIPLEXER TD-204/U

**This copy is a reprint which includes current
pages from Changes 1 and 2.**

**HEADQUARTERS, DEPARTMENT OF THE ARMY
12 DECEMBER 1966**

WARNING

Serious injury or death may result if safety precautions are not observed.

DON'T TAKE CHANCES!

Up to 1,100 volts may be encountered when using Restorer, Pulse Form TD-206/G.

USE EXTREME CAUTION

DON'T TAKE CHANCES!

CAUTION

This equipment is transistorized. Do not make resistance measurements. Consult the maintenance section of this manual before making voltage or waveform measurements.

CHANGE

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, DC, 2 December 1983

No. 2

**DIRECT SUPPORT, GENERAL SUPPORT AND
DEPOT MAINTENANCE MANUAL
MULTIPLEXER TD-204/U
(NSN 5805-00-900-8200)**

TM 11-5805-367-35/2, 12 December 1966, is changed as follows:

1. The title is changed as shown above.
2. New or added material is indicated by a vertical bar in the margin.
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3-1 and 3-2	3-1 and 3-2
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Figure 6-11 (foldout).....	Figure 6-11 (foldout)
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5. File this change sheet in front of the publication for reference purposes.

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To be distributed in accordance with DA Form 12-51C, Direct and General Support Maintenance requirements for TD-204/U.

**DIRECT SUPPORT, GENERAL SUPPORT AND
 DEPOT MAINTENANCE MANUAL
 MULTIPLEXER TD-204/U
 (NSN 5805-00-900-8200)**

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in the back of this manual direct to: Commander, US Army Communications-Electronics Command and Fort-Monmouth, ATTN: DRSEL-ME-MP, Fort Monmouth, New Jersey 07703. A reply will be sent direct to you.

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CHAPTER 1

INTRODUCTION

1-1. Scope

a. This manual covers direct and general support and depot maintenance for Multiplexer TD-204/U. It includes instructions for direct and general support for troubleshooting, testing, and aligning the equipment. It also lists materials and test equipment required for this maintenance. Chapter 2 provides circuit analysis of the TD-204/U.

b. The complete technical manual for this equipment also includes TM 11-5805-367-12.

1-2. Reporting Errors and Recommending Improvements

Report of errors, omissions, and recommendations for improving this publication by the individual user is encouraged. Reports should be submitted on DA Form 2028 (Recommended Changes to DA Publications) and forwarded direct to: Commander, US Army Communications-Electronics Command and Fort Monmouth. ATTN: DRSEL-ME-MP. Fort Monmouth, New Jersey 07703.

1-3. Consolidated Index of Army Publications and Blank Forms

Refer to the latest issue of DA Pam 310-1 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

1-4. Maintenance Forms, Records, and Reports

a. *Reports of Maintenance and Unsatisfactory Equipment*. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by TM 38-750, The Army Maintenance Management System (TAMMS).

b. *Report of Packaging and Handling Deficiencies*. Fill out and forward SF 364 (Report of Discrepancy (ROD)) as prescribed in AR 735-1 1-2/DLAR 4140.55 /NAVMATINST 4355.73 A/AFR 400-54/MCO 4430.3F.

c. *Discrepancy in Shipment Report (DISREP) (SF 361)*. Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38 /NAVSUPINST 4610.33 C/AFR 75-18/MCO P4610.19D/DLAR 4500.15.

1-5. Reporting Equipment Improvement Recommendations (EIR)

If your Multiplexer TD-204/U needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design. Put it on an SF 368 (Quality Deficiency Report). Mail it to: Commander, US Army Communications-Electronics Command and Fort Monmouth. ATTN: DRSEL-ME-MP, Fort Monmouth. New Jersey 07703.

CHAPTER 2

FUNCTIONING

Section I. BLOCK DIAGRAM ANALYSIS

2-1. General

Multiplexer TD-204/U provides facilities to transmit and receive pulse-code modulation (pcm) signals over a cable system. The TD-204/U, accepts 12-, 24-, or 48-channel full-width pcm signals and changes them to half-width signals at a frequency of 2,304 kilocycles (kc). Correspondingly, the TD-204/U changes half-width pcm signals to 12-, 24-, or 48-channel full-width pcm signals for retransmission or demultiplexing by exterior equipment (refer to TM 11-5805-367-12). The TD-204/U supplies operating current for as many as 39 Restorers, Pulse Form TD-206/G, and also furnishes an independent order-wire circuit for the cable system. It includes a built-in test facility for measuring, testing, and monitoring.

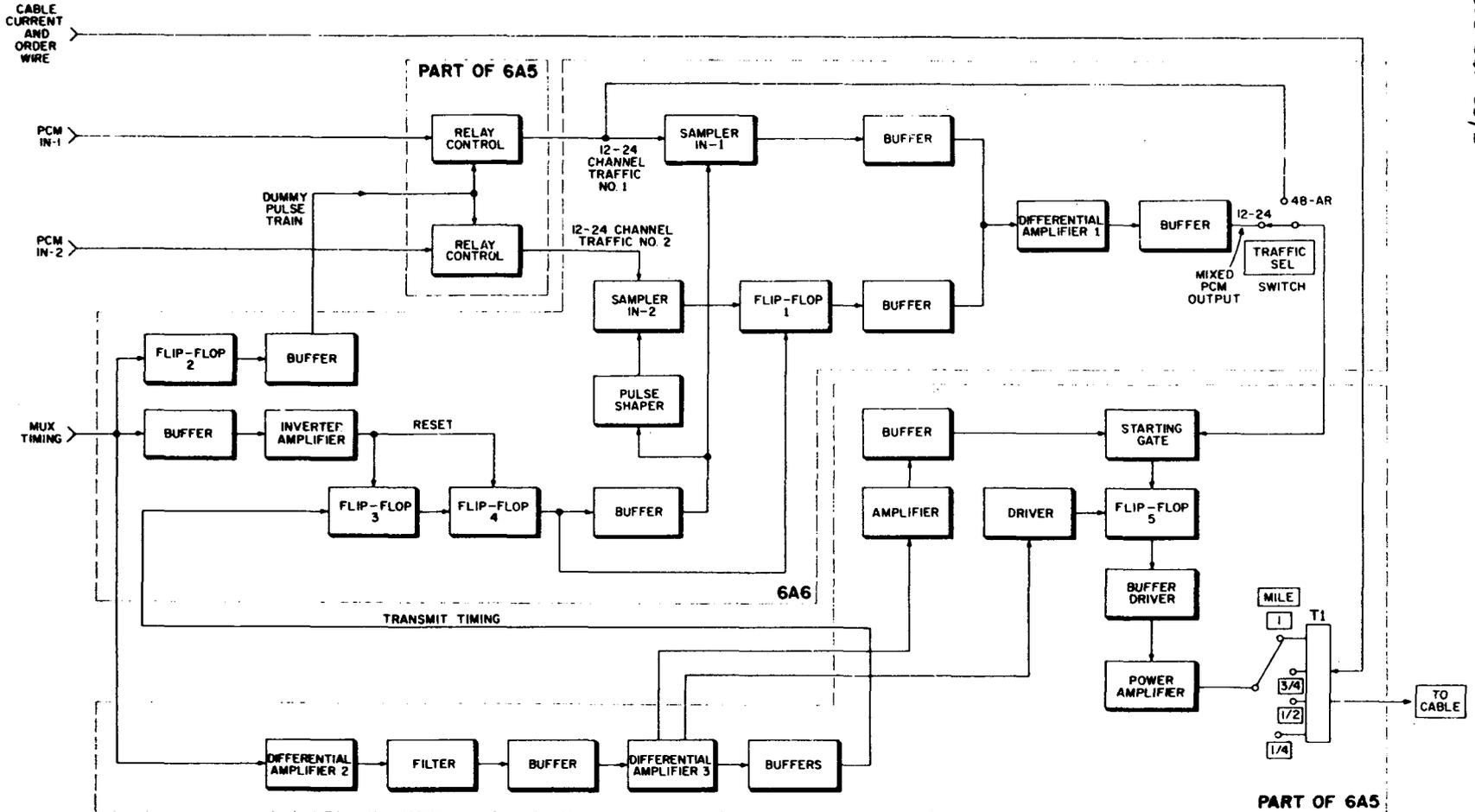
2-2. Transmit Circuits (fig. 2-1)

a. General. Components of the transmit circuits of the TD-204/U are mounted on panels 6A5 and 6A6. These panels receive either one or two full-width pcm signals containing 12, 24, or 48 channels. A multiplexer-timing signal from exterior equipment enters the transmit circuits at a frequency of 576 kc for 12- or 24-channel operation, or 2,304 kc for 48-channel or attended repeater (AR) operation. The transmit circuits convert the full-width pcm signals to half-width signals at a frequency of 2,304 kc (interleaving them if they are two different pcm trains) and the resulting signal is routed to the cable.

b. 12-Channel Operation.

- (1) In 12-channel operation, one pcm pulse train is applied to the PCM IN/1 input jack; for interleaving, a 288-kc dummy pulse train is derived by halving the 576-kc multiplexer-timing signal in flip-flop 2. This signal is then routed through a buffer stage, where it is available at the pcm in-2 relay control.
- (2) The multiplexer-timing signal is also routed to a buffer stage and an amplifier stage, where the signal is differentiated and the trailing edge amplified. The output of the amplifier stage is transmitted to flip-flops 3 and 4 as reset pulses.
- (3) A third portion of the multiplexer-timing signal is routed to differential amplifier 2 in panel 6A5. The 576-kc pulse output of the differential amplifier is transmitted to a filter that produces a 2,304-kc sine wave. The output of the filter is routed through a buffer stage to differential amplifier 3, which produces two 2,304-kc pulse trains 180° out-of-phase.
- (4) One pulse train is routed to an amplifier and buffer stage. The output of the buffer stage is applied to the input of the starting gate and is used to trigger the leading edge of the half-width pcm pulses to be developed. The mixed pcm output from the TRAFFIC SEL switch is also applied to the starting gate, which samples each pcm pulse twice. The output is applied to flip-flop 5.
- (5) The other pulse train from differential amplifier 3 is applied to a driver. The output of the driver, a series of positive-going pulses, resets flip-flop 5 to form the trailing edge of the half-width pcm pulses. The output of flip-flop 5 is a series of half-width pulses which are applied through a buffer driver to a power amplifier. The output of the power amplifier is applied across transformer T1 and an attenuation network to the cable. When the distance to the first restorer is 1 mile, the MILE switch is set to 1 MILE; when the distance is less than 1 mile, the switch is set to the position required (1A MILE, 1½ MILE, ¾ MILE). The cable current and order-wire input are added to the output to the cable.
- (6) Another output of differential amplifier 3

Figure 2-1. Transmit circuits, block diagram.



(transmit timing) is applied through buffer stages to the input of flip-flop 3, which divides the 2,304-kc pulse train to 1,152 kc. In turn, the 1,152kc pulse train is divided to 576-kc by flip-flop 4, one output of which is applied through a buffer stage and then divided, with one branch applied to a pulse shaper, and the other branch routed to sampler in-1.

- (7) In the pulse shaper, the 576-kc signal is differentiated, with the negative-going pulses passing to ground. The positive-going pulses cause a series of negative-going pulses to be transmitted to sampler in-2.
- (8) PCM IN-1 pulses are routed through a relay control to the input of sampler in-1. These pulses are designated 12-24 channel traffic No. 1. The 576-kc signals from flip-flop 4 sample these pulses and produce a square-pulse output which is routed through a buffer stage to differential amplifier 1.
- (9) The 268-kc dummy pulse train applied to the pcm in-2 relay control is routed to the input of sampler in-2. These pulses are designated 12-24 channel traffic No. 2. The negative-going pulses from the pulse shaper sample the dummy pulse train input and provide a spiked pulse output to flip-flop 1. Flip-flop 1 produces half-width traffic pulses which are sent to the input of differential amplifier 1 through a buffer stage. Flip-flop 1 is reset by pulses from flip-flop 4.
- (10) At the input to differential amplifier 1, the traffic 1 and traffic 2 pulses are interleaved. The mixed pcm output of the differential amplifier is applied through a buffer stage to the TRAFFIC SEL switch.

c. 24-Channel Operation. Operation of the transmit circuits for 24 channels is exactly the same as for 12 channels except that two separate 12-channel pcm inputs are applied (one to PCM IN-1 and one to PCM IN-2), thereby eliminating the need for the dummy pulse train. The exception occurs when either pcm input is lost; if this happens, the relay control automatically substitutes the dummy pulse train for the missing 12-channel binary train.

d. 48-Channel and Attended Repeater (AR)

Operation. During 48-channel and AR operation, panel 6A6 is not used, but operation of panel 6A5 is the same as for 12- and 24-operation, with the following exceptions. Each pulse is sampled only once, since the pcm input is at a 48-channel rate. The multiplexer-timing signal is applied at a frequency of 2,304 kc, and operation of the filter does not modify it. The pcm input is applied to the PCM IN-1 connector only.

2-3. Receive Circuits

(fig. 2-2)

a. General. Components of the receive circuits of the TD-204/U are mounted on panels 6A4 and 6A7. The receive circuits accept the half-width pcm signal, separate the order wire and direct current (dc) cable currents, and restore the shape of the pcm signal. A 2,304-kc timing pulse is originated for use in other panels, and an alarm signal is provided for traffic failures. The receive circuits deliver two parallel full-width pcm outputs and attendant timing pulses to exterior equipment.

b. Input Circuits. The input signal to the receive circuits consists of a composite pcm signal at 2,304 kc, dc cable current, and order wire. The dc cable current and order-wire signal are separated from the pcm signal in panel 6A4 and are applied to panel 6A2. The pcm signal is passed through an attenuator network if the nearest restorer is less than 1 mile from the TD-204/U; if the nearest restorer is 1 mile from the TD-204/U, the pcm signal is transformer coupled directly to amplifier 1. The amplified signal is transformer coupled to amplifier 2 where it is reamplified. The output of amplifier 2 is routed in two directions: one branch is transmitted to a buffer stage in the timing circuit; the other is applied to driver 1 in the pcm output circuit.

c. Pcm Output Circuit. The amplified pcm signal applied to driver 1 is also routed in two directions: one branch is transmitted to the pcm sampler in panel 6A7 and is designated *received pcm*; the other branch is routed to a switch.

d. Switch Operation. During normal operation, the switch is open, and a voltage is applied to the relay driver to cause the alarm relay to remain inoperative. The same voltage is applied to the oscillator in the timing circuit. When there is a failure in the pcm input, the switch closes, removing the voltage from both the relay driver and the

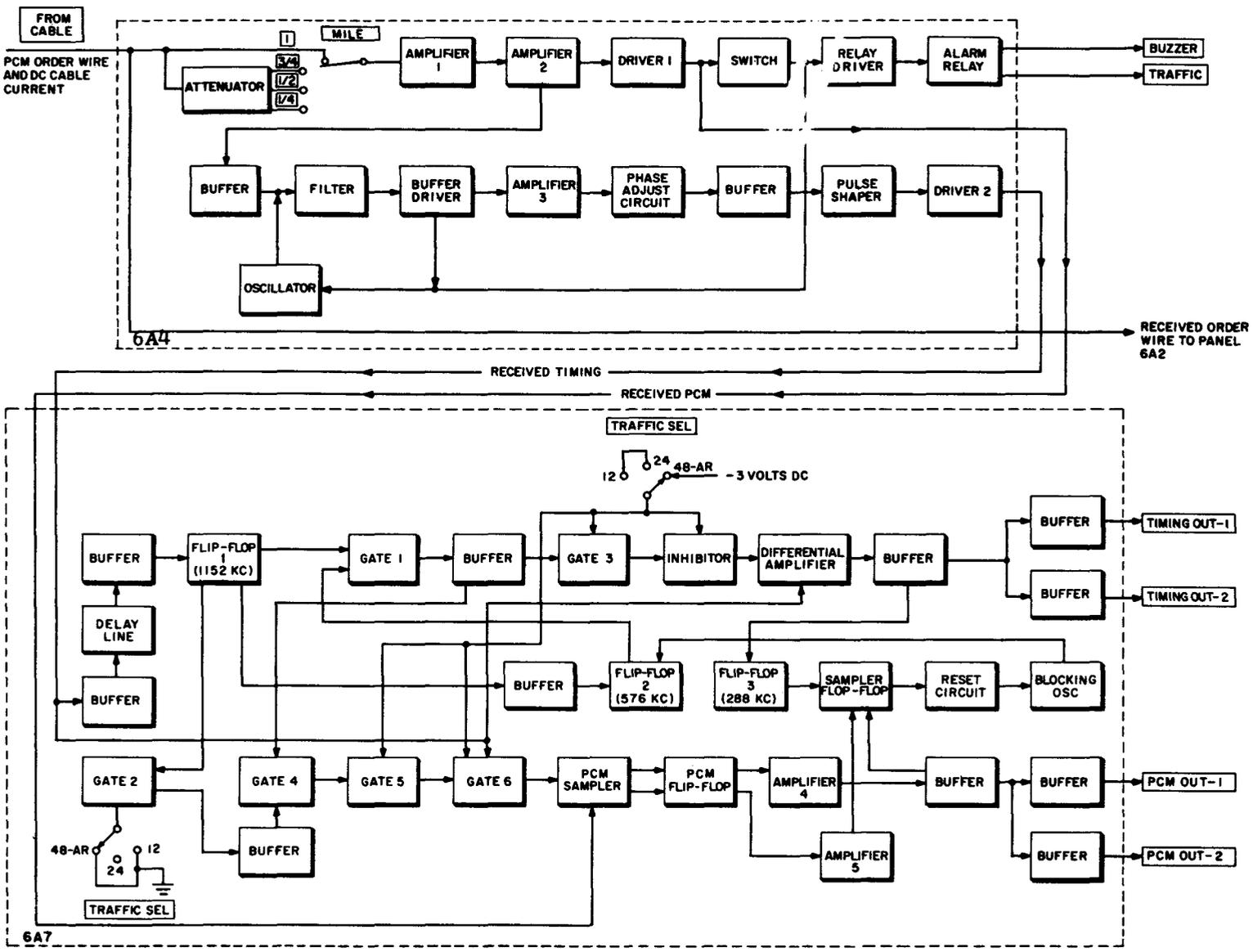


Figure 2-2. Receive circuits, block diagram.

oscillator. This causes alarm relays to operate, the buzzer to sound, and the TRAFFIC indicator lamp to light.

e. Timing Circuit. The signal from amplifier 2 passes through the buffer stage into the filter, where a 2,304-kc sine wave is produced. This sine wave signal is applied through a buffer driver to an amplifier and then to a phase-adjust circuit, where its phase is shifted so that the timing pulses produced will coincide with the center of the pcm pulses. The phase-shifted sine wave is then coupled through a buffer stage to a pulse shaper, and the output of the pulse shaper is applied through driver 2 to a buffer stage in panel 6A7 as a train of positive-going spike pulses. This pulse train is designated 48-channel timing.

f. Oscillator Operation. When traffic fails, the voltage applied to the oscillator from the switch is removed, causing the oscillator to apply a voltage to the filter, which produces a 2,304-kc sine wave. The sine wave is applied to the buffer driver, which transmits the signal in two directions: one branch is routed to the amplifier and phase-adjust circuit as in normal operation; the other branch is applied to the oscillator as feedback, thereby sustaining oscillation until normal operation resumes.

g. 12-Channel Operation.

(1) *Pcm output circuits.*

- (a) The received pcm signal is a half-width pcm signal consisting of a single binary pulse train interleaved with a train of 288-kc dummy pulses. It is routed to the pcm sampler from driver 1. The other inputs are applied to the pcm sampler: a 2,304-kc pulse train and a series of 576-Kc gating pulses.
- (b) The pcm is sampled whenever a 2,304-kc pulse and a 576-kc gating pulse arrive simultaneously at the pcm sampler. The pcm sampler separates the digital 1 pulses from the digital 0 pulses and applies them to the pcm flip-flop. The output of the pcm flip-flop operates two simplifiers to regenerate and reshape the pcm pulse levels. The output of one amplifier is transmitted to the sampler flop-flop, while the output of the other amplifier is applied to a buffer.
- (c) The output of the buffer is routed in three directions: one branch is routed

to the sampler flop-flop and the other two are transmitted to two output buffers, the outputs of which are designated *PCM OUT-1* and *PCM OUT-2*.

(2) *Frequency division circuits.*

- (a) A second path for the 2,304-kc timing pulse train is through a buffer, a delay line, and another buffer to flip-flop 1, Flip-flop 1 divides the input signal frequency to 1,152 kc and applies its output to gates 1 and 2, and through a buffer to flip-flop 2.
 - (b) Flip-flop 2 divides the 1,152-kc signal to 576 kc and applies its output to gate 1. Here the 576-kc output of flip-flop 2 is gated with the 1,152-kc output of flip-flop 1 to produce the 576-kc gating pulse. The 576-kc gating pulse is applied through a buffer to gates 4, 5, and 6 to pcm sampler; it is also applied through gate 3 and an inhibitor to the differential amplifier.
- (3) *Output timing circuits.* A third branch of the 48-channel timing is routed through the cliff differential amplifier. In 12-channel operation, the differential amplifier is gated by the 576-kc gating pulse. The output of the differential amplifier is a 576-kc positive-going pulse train which is routed to a buffer stage. The output of the buffer stage is applied three ways: one branch is applied to flip-flop 3; the other two branches are applied to twin output-buffer stages which provide dual output-timing pulse trains designated *TIMING OUT-1* and *TIMING OUT-2*.
- (4) *Phasing of timing pulses, normal operation.* The 288-kc square wave from flip-flop 3 is routed to the sampler flop-flop. The output of the sampler flop-flop is a random pulse train which inhibits the blocking oscillator through the reset circuit.
- (5) *Phasing of timing pulses, abnormal operation.*
- (a) In abnormal operation (when the gated timing pulse train is 180° out-of-phase with the pcm pulse train), the dummy pulse train is sampled instead of the pcm pulse train. The 288-kc square wave from flip-flop 3 is routed to the sampler

flop-flop, as in normal operation. The sampler flop-flop provides a constant output (when sampling the dummy pulse train) which causes the reset circuit to operate the blocking oscillator.

- (b) The blocking oscillator produces a pulse that is routed back to the input of flip-flop 2. This pulse affects the phase of the outputs of flip-flops 2 and 3. The blocking oscillator continues to operate until the gated timing pulse applied to the sampler flop-flop samples the pcm pulse train instead of the dummy pulse train.

h. 24-Channel Operation. The 24-channel operation is the same as the 12-channel operation, with the following exceptions;

- (1) The received pcm consists of two interleaved binary pulse trains.
- (2) The received pcm is sampled by an 1,152-kc sampling pulse obtained by gating the 2,304-kc received timing pulses with an 1,152-kc gating pulse in gate 6. This 1,152-kc gating pulse is an output of flip-flop 1 which passes through gate 2, a buffer, and gates 4 and 5 to gate 6.
- (3) The blocking oscillator is disabled since there is no dummy pulse train in the received pcm.

i. 48-Channel Operation. The 48-channel operation and AR operation are the same as the 12-channel operation, with the following exceptions:

- (1) The received pcm consists of one 48-channel binary pulse train.
- (2) The receive pcm is sampled by a 2,304-kc sampling pulse, which is identical to the received timing pulse train.
- (3) The blocking oscillator is disabled, since there is no dummy pulse train.
- (4) A -3-volt potential applied to gates 3, 5, and 6, and to the inhibitor prevents the gating pulses (from gates 1 and 2) from inhibiting differential amplifier 2. It also eliminates the gating pulse on the received timing input to the pcm sampler.

2-4. Order Wire Circuits

(fig. 2-3)

a. General. Components of the order-wire circuits of the TD-204/U are mounted on panels 6A2 and

6A3. These panels receive order-wire signals from exterior equipment (panel 6A4) and front panel terminals. These signals are amplified and coupled through a resistive hybrid to transmit amplifiers for use in exterior equipment or on the cable.

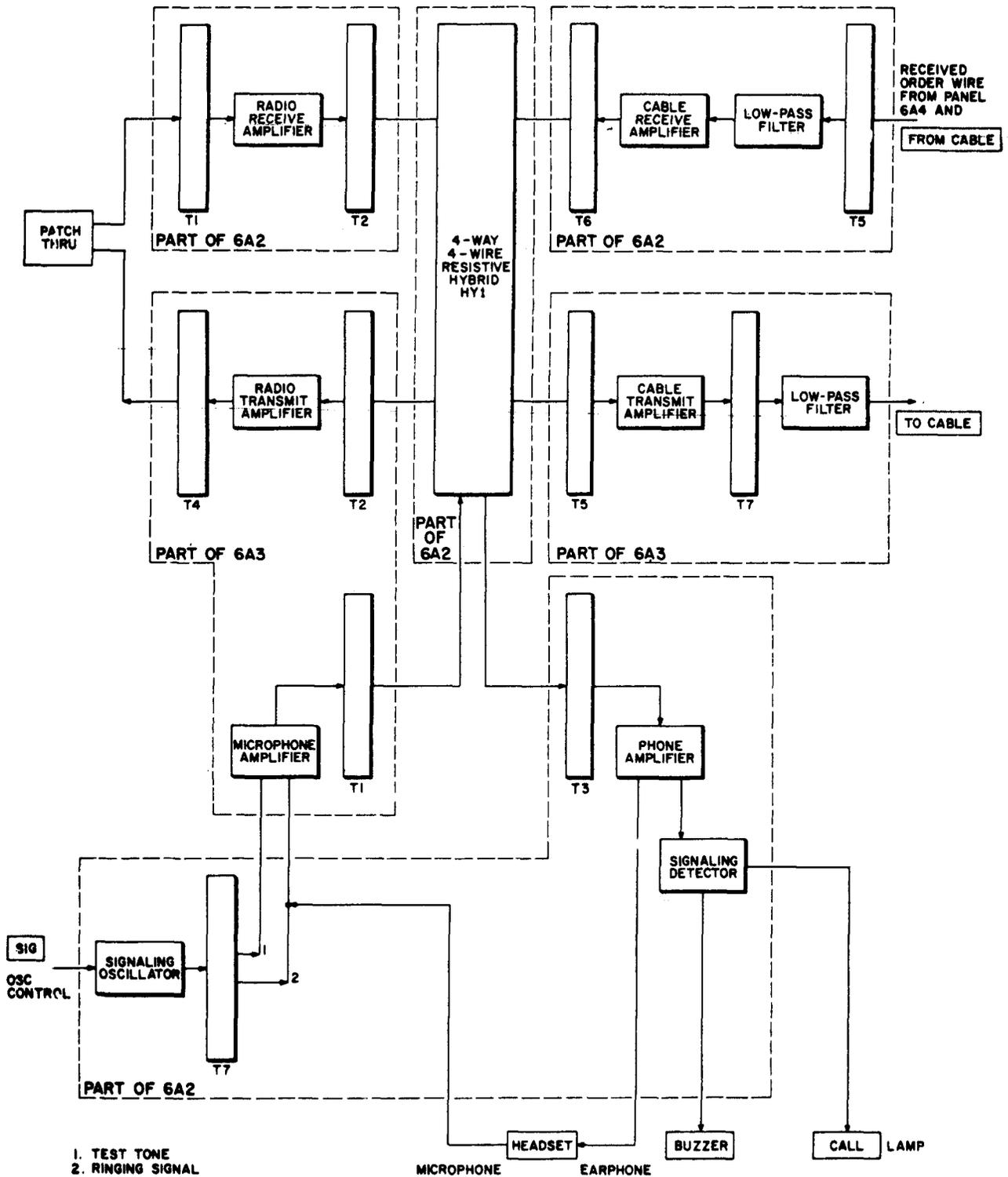
b. Radio Received Order Wire. Order-wire signals received by exterior equipment as part of a radio transmission are coupled through the PATCH THRU connector and transformer T1 to the radio receive amplifier, which amplifies the order-wire signal and couples it to the input of transformer T2. Transformer T2 couples the signal to the resistive hybrid which, in turn, couples the signal to the phone amplifier through transformer T3, and to the cable transmit amplifier through transformer T5.

c. Cable Received Order Wire. Order-wire signals from panel 6A4 are coupled through transformer T5 to the low-pass filter, where the high frequency components are attenuated. The output of the low-pass filter is applied to the cable receive amplifier, which increases the gain of the order-wire signal. The output of the cable receive amplifier is coupled to the input of T6, which provides an input to the resistive hybrid. The resistive hybrid couples the signal to the radio transmit amplifier through transformer T2, and to the phone amplifier through transformer T3.

d. Microphone Amplifier. Either an 1,100-cycle-per-second (cps) test tone or a 1,600-cps ringing signal (both generated by the signaling oscillator) is applied to the microphone amplifier through transformer T7. A signal from the microphone is also transmitted to the microphone amplifier. The output of the microphone amplifier is routed to transformer T1, which provides an input to the resistive hybrid. The resistive hybrid couples the signal to the radio transmit amplifier through transformer T2 and to the cable transmit amplifier through transformer T5.

e. Order-Wire Termination Facilities. Order-wire termination facilities are provided by the phone amplifier and the signaling detector. The phone amplifier amplifies the order-wire signals and couples them to the HEADSET connector and the signaling detector. The signaling detector sounds the buzzer and lights the CALL lamp whenever a ring signal arrives from a distant station.

f. Retransmission Facilities. The input signals to the radio transmit amplifier are amplified and applied to transformer T4 which supplies an output



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Figure 2-3. Order-wire circuits, block diagram.

to the PATCH THRU connector and external equipment. The input signals to the cable transmit amplifier are amplified and applied to transformer T7, which provides an output to the cable through the low-pass filter.

2-5. Power Supply Circuits

(fig. 2-4)

a. General. Components of the power supply circuits of the TD-204/U are mounted on panel 6A1. Dc potentials of ± 10 , ± 3 , -17 , and -28 volts are provided, as well as 28 volts alternating current (ac). These are described in *b* through *e* below.

b. +10 Volts Dc. The primary of transformer T1 receives 115 volts, 50 to 60 cycles, from the power source. One center-tapped secondary winding on transformer T1 supplies a full-wave rectifier circuit, the output of which is applied through a filter and a fuse to a series-regulator. The regulator output ground is the negative side of the +10-volt supply. The positive side (+10 VDC bus) is taken directly from the center tap of the secondary winding of transformer T1. The regulator is controlled by a differential amplifier that samples the supply output (through a variable tap on a voltage divider across the supply output) and compares the sample with a stable reference voltage. Any change in output voltage is detected by the amplifier and corrected by the series regulator.

c. -10 Volts Dc. The -10-volt supply is similar to the +10-volt supply, except that the positive side of the supply output is grounded instead of the negative side.

d. +3 Volts Dc and -3 Volts Dc.

- (1) The + and -3-volt dc power supply voltages are derived from a 6-volt floating supply centered at ground potential. The output from a center-tapped secondary winding on transformer T1 is rectified and filtered. The output from the filter is passed through a fuse to a series regulator, and its output is applied to the -3-volt output bus. Regulation is controlled by differential amplifier 1 and the driver. The output is sampled through voltage divider 1.
- (2) The center tap of the secondary winding of transformer T1 supplies the +3-volt output bus. Balance is maintained between

the positive and negative voltages by a subregulator composed of voltage divider 2, differential amplifier 2, the dc amplifier, and the regulator. The subregulator draws from the +3-volt supply, grounding an amount of current exactly equal to the excess current normally drawn from the -3-volt supply.

e. Remaining Power Supply Circuits.

- (1) Another output of transformer T1 is rectified, filtered, and passed through a fuse. From the fuse, the dc is routed through a voltage divider to the -17-volt bus. From the fuse, the dc is also routed to the -28-volt bus.
- (2) Another output of transformer T1 at 28 volts ac causes the CHANGE AIR FILTER indicator lamp to light whenever the temperature in the power supply rises above 160° F. The same transformer output is passed through a fuse from which the ac is routed in two directions. One branch is passed through a rectifier circuit whose output is applied to the cable power start control. The other is applied directly to the 28-volt ac bus.

2-6. Cable Power Supply Circuits

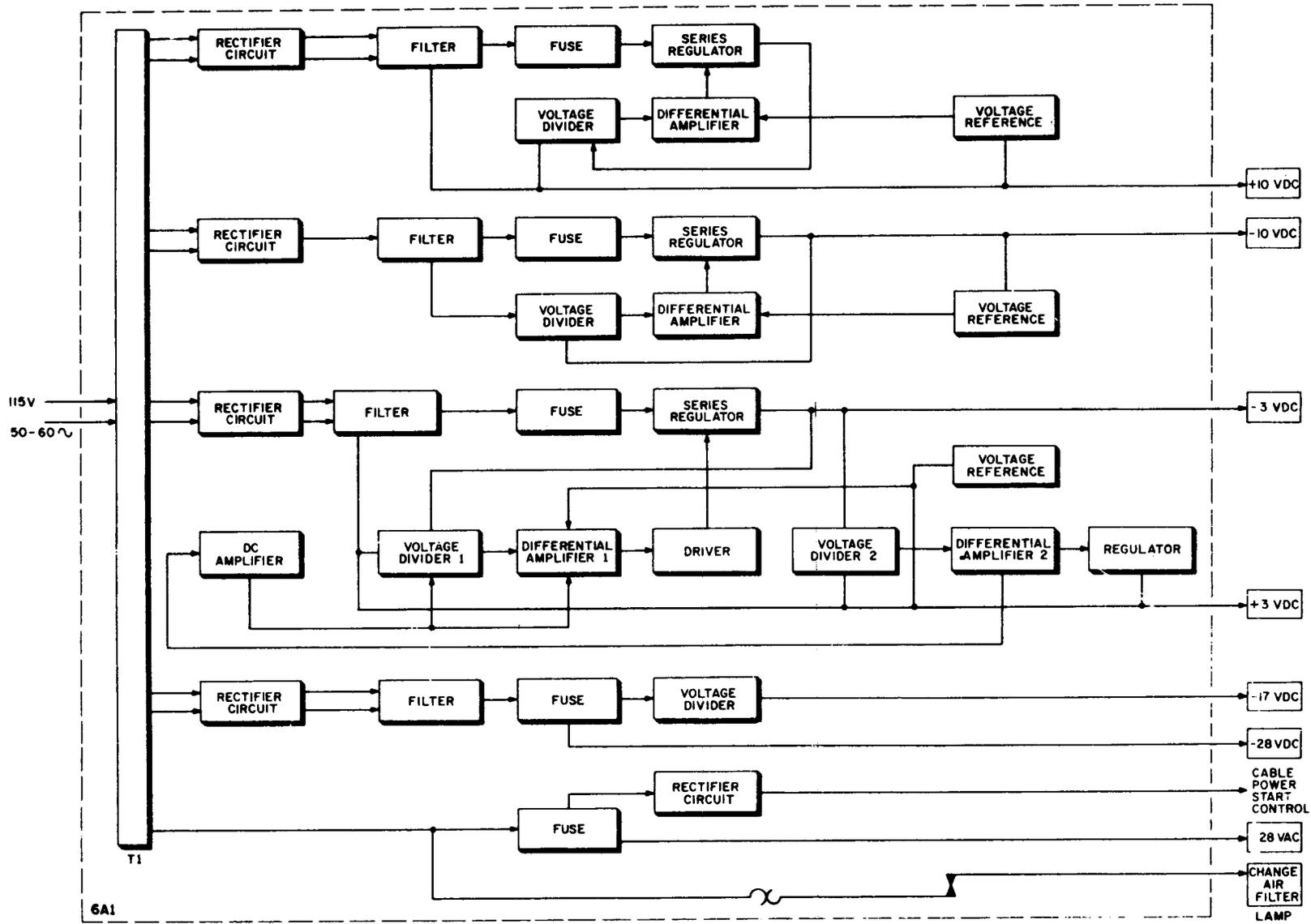
(fig. 2-5)

a. General. Cable power supply circuit components of the TD-204/U are mounted on panel 6A1. The cable power supply provides and regulates the current for the cable and restorers.

b. Cable Current Output Circuits.

- (1) The + and -3-volt outputs from the power supply are applied to the royer circuit, which converts them to a 3-kc square wave output at the secondary of transformer T3.
- (2) One output of transformer T3 is applied to an integrator which produces a sawtooth waveform. The sawtooth waveform is applied to the adding amplifier (dc and sawtooth) through the sawtooth amplifier, which performs the function of a buffer.
- (3) The adding amplifier, in addition to the sawtooth waveform, receives a dc level from the dc amplifier. The dc amplifier is routed to two inputs: one is from the differential amplifier in the form of a dc

Figure 2-4. Power supply circuits, block diagram.



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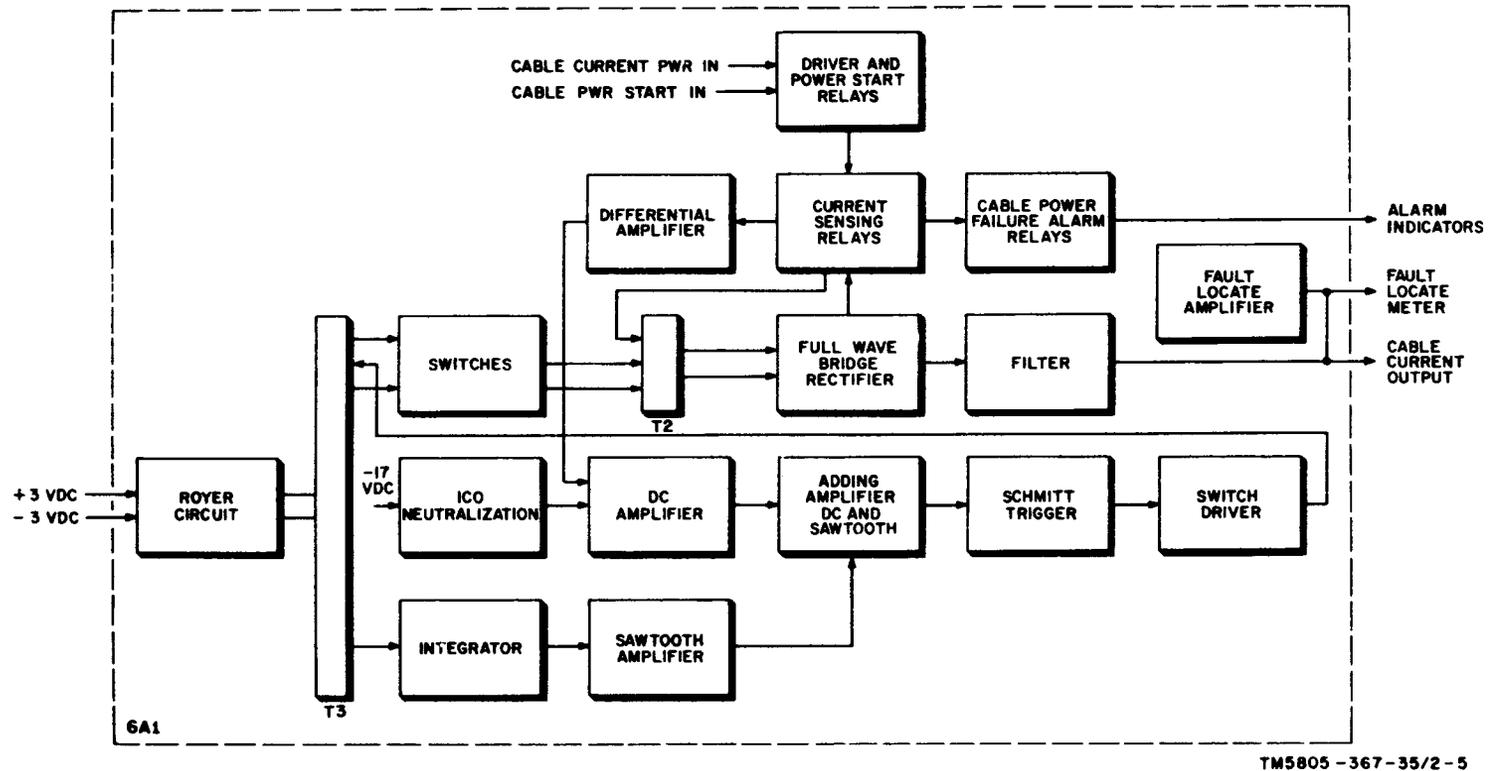


Figure 2-5. Cable power supply circuits, block diagram.

- level which is proportional to the output cable current; the other is compensating current from the ICO neutralization stage (see TM 11-690), which compensates for temperature variations in the dc amplifier. The adding amplifier combines the two inputs so that the sawtooth waveform rides on the dc level.
- (4) The output of the adding amplifier is applied to the Schmitt trigger which changes the sawtooth waveform to a pulse output, the width of the pulses being inversely proportional to the magnitude of the dc level. The output of the Schmitt trigger is transmitted to the switch driver which applies the inverted pulses to the secondary of transformer T3.
 - (5) Transformer T3 applies these inverted pulses to the switches, together with the 3-kc square wave output from the royer circuit. The resultant waveforms are rectangular, varying between a negative and a positive dc level. Whenever the waveform falls below 0 volt dc, the switches conduct, providing an output to transformer T2. The output from the secondary of transformer T2 is transmitted to the full-wave bridge rectifier which provides an output consisting of a series of positive pulses, the widths of which control the cable current.
 - (6) These pulses are filtered and applied to the cable current output terminal. A portion of this branch is routed to the fault-locate meter through the output of the fault-locate amplifier. The fault-locate meter and associated circuitry is used to determine the location of a faulty restorer.
 - (7) The ground return of the bridge rectifier is applied to the current-sensing relays and resistor. The current sensing relays shut down the power supply when the current exceeds or falls below a predetermined operating range. The driver and power-start relays provide power to the primary of transformer T2 through the current-sensing relays. In addition, it momentarily shorts out one of the current-sensing relays when power is applied, so that momentary surges of current will not shut down the power supply.
 - (8) The entire cable current passes to ground through the current-sensing resistor. The voltage developed across this resistor is transmitted to the differential amplifier to provide an indication of the cable current.
 - (9) When a power failure occurs that cuts off cable current, the cable power failure alarm relays no longer receive current through the current-sensing relays. This causes the cable power failure alarm relays to energize the alarm indicators.

Section II. MODULE SCHEMATIC ANALYSIS

2-7. General

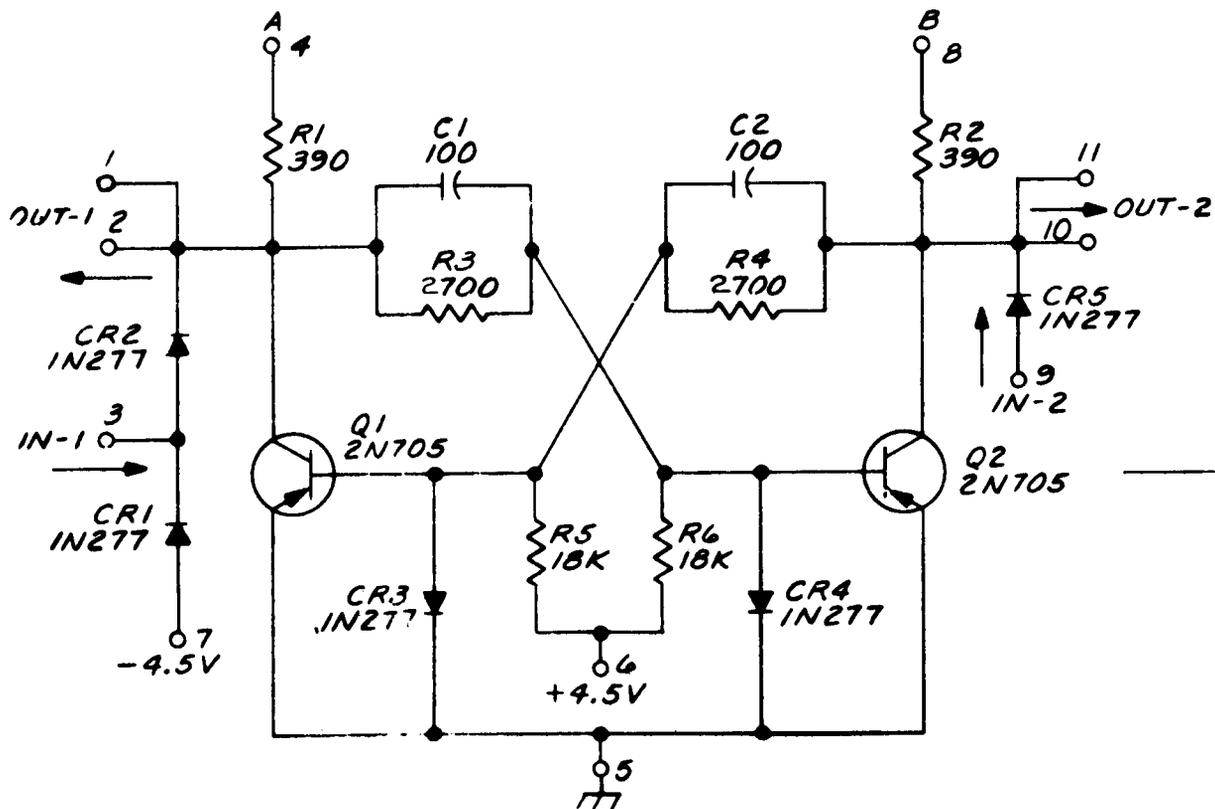
The TD-204/U contains two multivibrators (flip-flops) encased in sealed containers; the entire assembly is called a module. A circuit analysis of these flip-flop modules is given in paragraphs 2-8 and 2-9. Throughout the circuit analysis, unless otherwise specified, a positive-going pulse implies that the pulse is changing from a -3-volt reference level to zero, and a negative-going pulse implies that the pulse is changing from a zero reference level to -3 volts.

2-8. Flip-Flop Module 09

(fig. 2-6)

Flip-flop module 09 is a bistable multivibrator

capable of switching states at a 2.3-megacycle (mc) rate. Positive-going trigger pulses applied to terminals 3 (IN-1) and 9 (IN-2) enable switching, when the associated transistor (Q1 or Q2) is turned off. Either set-reset input triggering or complemented input triggering may be used for switching. Diodes CR2 and CR5 are steering diodes, and diode CR1 is a trigger-loading diode. Resistors R5 and R6 develop bias, and diodes CR3 and CR4 clamp the bases of transistors Q1 and Q2 slightly positive. Resistors R1 and R2 are collector load resistors. Resistors R3 and R4 and capacitors C1 and C2 make up the coupling circuits which determine the switching time.



NOTE.
RESISTANCES ARE IN OHMS, CAPACITANCES
ARE IN UF, UNLESS OTHERWISE INDICATED

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Figure 2-6. Flip-flop module 09, schematic diagram.

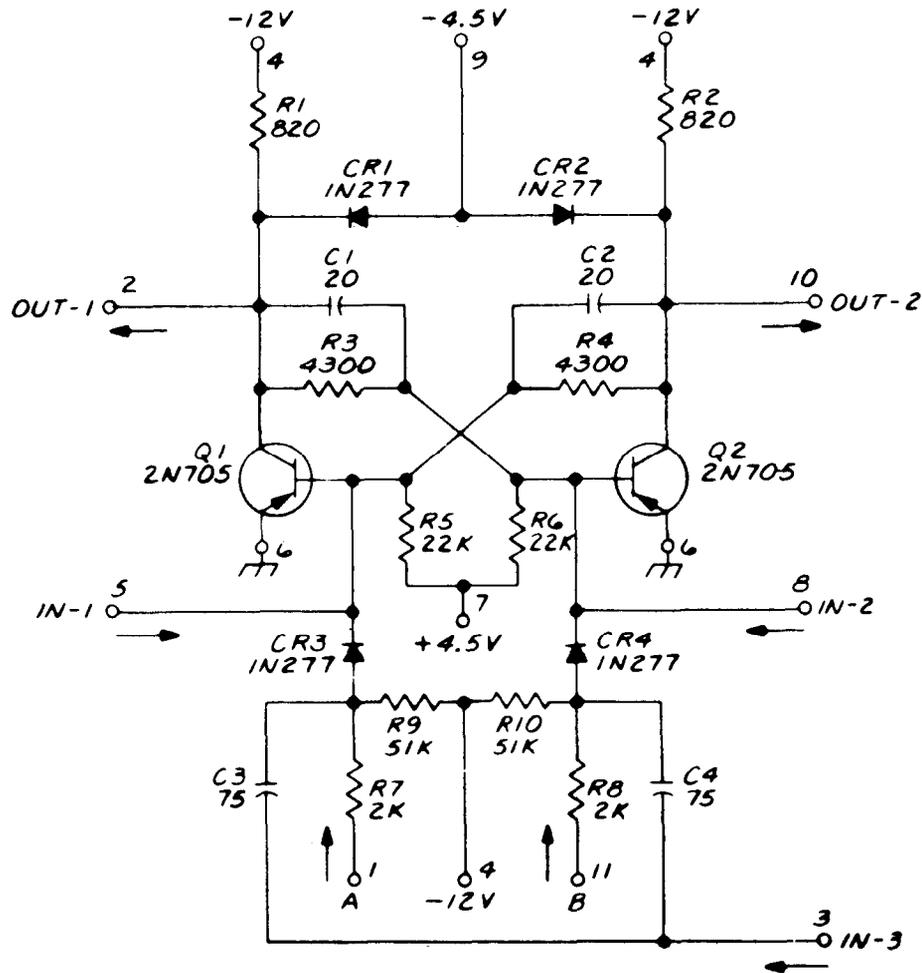
2-9. Flip-Flop Module 18

(fig. 2-7)

a. Flip-flop module 18 consists of multivibrator transistors Q1 and Q2 and a complementary input-triggering circuit consisting of two biased steering gates. The inputs to both steering gates are through pin 3. The collectors at transistors Q1 and Q2 are clamped at -3 volts by diodes CR1 and CR2, respectively.

b. Flip-flop module 18 switches states in response

to pulses varying between zero and 3 volts. These triggers are applied to the base of either transistor through external input-triggering circuits on pin 5 or 8. In addition, a 3-volt positive-going pulse applied to pin 3 will switch the flip-flop when pins 1 and 11 are tied to pins 2 and 10, respectively. Outputs are taken from either collector and are applied to external circuits through pins 2 and 10. The output from one of the pins is 0 volt when the output of the other pin is -3 volts.



NOTE:
RESISTANCES ARE IN OHMS, CAPACITANCES
ARE IN UF, UNLESS OTHERWISE INDICATED.
TM-5805-367-35/2-6

Figure 2-7. Flip-flop module 18, schematic diagram.

Section III. PANEL SCHEMATIC ANALYSIS

2-10. General

a. The TD-204/U accepts 12-, 24-, or 48-channel full-width pcm signals from exterior equipment and converts them into half-width signals at the 48-channel rate of 2,304 kc for transmission on the cable. In addition, the TD-204/U accepts the half-width band-limited video pulses from the cable and processes them by exterior equipment into the corresponding full-width pcm traffic for retransmission or demultiplexing.

b. The TD-204/U supplies the current required to operate cable restorers and supplies order-wire facilities for the cable system. The TD-204/U also provides warning and alarm signals whenever a failure occurs in the cable transmission system.

c. Circuitry for the TD-204/U is contained on seven plug-in panels. A circuit analysis of each panel, with individual schematic diagrams, is provided in paragraphs 2-11 through 2-17. A list of all plug-in panels used in the TD-204/U with a brief description of their functions is given below:

Quantity	Panel number	Nomenclature	Function
1	6A1	Power supply.	Receives 115-volts ac input; rectifies and produces regulated +10 and -10 volts dc, +3 and -3 volts dc, -17 volts dc, -28 volts dc, and 28 volts ac for use in panel circuits. Provides 38-ma constant current to restorers.
1	6A2	Order wire No. 1.	Provides amplification and hybrid interconnection for incoming radio, cable, and headset order-wire signals. Provides test tone level (TTL) and order-wire signaling. Adjusts receive cable level (RCL) order-wire signal.
1	6A3	Order wire No. 2.	Amplifies the outgoing cable and radio order-wire signals. In addition, it amplifies the microphone input signal.

Quantity	Panel number	Nomenclature	Function
	6A4	Receiver, signal, cable.	Amplifies incoming pcm signals from cable. Extracts 2.3-mc timing from pcm signals to drive timing circuits.
	6A5	Generator, signal, transmit No. 1.	Times and gates incoming pcm signals from exterior equipment. Combines 38-ma cable power and order-wire circuit with pcm signal.
	6A6	Generator, signal, transmit No. 2.	Combines and interleaves two 12-channel pcm signals from exterior equipment. Provides the dummy train.
	6A7	Generator, signal, receive.	Accepts pcm and timing signals from panel 6A4. Provides timing outputs for 12-, 24-, or 48-channel operation. Furnishes twin pcm output signals and twin timing output signals.

2-11. Power Supply, Panel 6A1
(fig. 6-11)

a. *General.* Circuitry on power supply panel 6A1 and auxiliary subpanel 6A1-A1 is divided into two functional sections: one section produces the required internal voltages for the TD-204/U; the other produces dc cable current for use by the cable restorers. The dc cable current is also used with a fault-locating system to identify a faulty restorer in the cable system. Internal power supply circuits are covered in *b* through *f* below, while the cable current supply circuits are covered in *g* through *n* below.

b. *Input to Transformer T1* (fig. 6-9). When AC POWER ON-OFF switch S5 is turned ON, line voltage at 115 volts ac, 50 to 60 cycles, is applied to panel 6A1 at terminals 1 and 2 of jack J1 through fuses F1 and F2, causing indicator lamp DS4 to light. This input voltage is then connected to terminals 1 and 2 of transformer T1 (fig. 6-11), whose secondary windings provide the several required voltages described in *c* through *f* below.

c. *+10-Volt Power Supply.*

- (1) The output at terminals 12 and 14 of transformer T1 (26.8 volts root mean square (rms)) is rectified by diodes CR1 and CR2 to produce an unregulated output of approximately +10 volts dc. This output is filtered by choke L1C and capacitors C1 and C2 and is routed to a series-regulator stage, through fuse F1. Capacitors C1 and C2 increase the average voltage across the outputs of the rectifiers. The output at terminal 13, the center tap of this winding of transformer T1, is brought out to terminal 13, jack J1 and test jack J2 and is designated + 10V. This output is regulated by the series regulator, differential amplifier, and voltage divider as described in (2) through (4) below.
- (2) **Transistors Q2 and Q3 form a differential amplifier.** The bias for the base of transistor Q2 is provided by +10V VOLTAGE ADJ potentiometer R1, which is connected across the power supply output and set to the stabilization point. The bias for the base of transistor Q3 is provided by the voltage divider consisting of resistors R5 and R-6 and breakdown diode VR1. Breakdown diode VR1 maintains a constant +6-volt potential across resistors R5 and R6 and the base of transistor Q3. Capacitors C4 and C5 bypass ac components to ground.
- (3) If the output voltage changes due to changes in ac supply or dc load current, the differential amplifier operates to stabilize the voltage. At best, the voltage on the bases of transistors Q2 and Q3 will be equal. If the output voltage tends to fall below 10 volts, the voltage drop across +10V VOLTAGE ADJ potentiometer R1 tends to fall also. This lower voltage drop will cause the base of transistor Q2 to be more positive than the base of transistor Q3; therefore transistor Q2 reduces its conductance. Transistor Q2 supplies a more negative voltage from its collector to the base of series-regulator transistor Q1, which increases conductance; this causes an increased voltage drop across

+10V VOLTAGE ADJ potentiometer R1, restoring the original conditions.

- (4) Similarly, if the voltage tends to increase to more than 10 volts, it will tend to increase the voltage drop across — 10V VOLTAGE ADJ potentiometer R1. This increased voltage drop will cause the base of transistor Q2 to become more negative than the base of transistor Q3; transistor Q2, in turn, increases conductance. The voltage on the base of series-regulator transistor Q1 will increase in a positive direction, thereby causing transistor Q1 to decrease its conductance and restore stabilization.

d. *-10-Volt Power Supply.*

- (1) The output at terminals 9 and 11 of transformer T1 (26.8 volts rms) is rectified by diodes CR3 and CR4 to produce an unregulated output of approximately — 10 volts. This output is filtered by choke LIB and capacitors C6 and C7 and applied to a series regulator through fuse F2.
- (2) The output of series-regulator transistor Q4 is applied to terminal 14 of jack J1 and to test jack J3, where it is designated -10V. This output is regulated by the series regulator, the differential amplifier, and the voltage divider in a similar manner to that described in c(2) through (4) above.

e. *+ and -3-Volt Power Supplies.*

- (1) The center-tapped outputs at terminals 6 and 8 of transformer T1 provide 22 volts rms to diodes CR5 and CR6, which full-wave rectify the alternating current and apply an unregulated output to a filter composed of choke L1A and capacitor C11. The output of the filter is applied to the collector of series-regulator transistor Q8 through fuse F3. Transistor Q8, operating as an emitter follower, presents its -3-volt output to terminal 20 of jack J1 and to test jack J4, where it is designated -3V. This output is regulated by the series regulator, the differential amplifier, and the voltage divider in a similar manner to that described in c(2) through (4), above.
- (2) The +3-volt supply is the opposite output of the 6-volt floating supply centered at

ground potential. In addition to the main regulator, a low-power subregulator aids in maintaining the balance between the two outputs. The subregulator draws from the +3-volt supply and grounds an amount of current exactly equal to the excess normally drawn from the -3-volt supply. Since the two loads are constant, balance is maintained.

- (3) The 6-volt output is adjusted by $\pm 3V$ VOLTAGE ADJ potentiometer R15. The subregulator consists of transistors Q11, Q12, Q13, and associated circuitry. Transistors Q11 and Q12 comprise a differential amplifier. The bias for the base of transistor Q11 is maintained at ground. The base bias for transistor Q12 is furnished by the voltage drop across $\pm 3V$ BAL VOLTAGE ADJ potentiometer R26. Potentiometer R26, connected across the 6-volt supply, is adjusted to pick off the midpoint voltage. If the voltage at the center of potentiometer R26 differs from ground potential, an output is produced at the collector of transistor Q12 and applied to the base of dc amplifier Q13. Transistor Q13 operates with resistor R30 as a bleeder circuit for the +3-voh supply; the signal applied to the base of transistor Q13 varies the amount of current drawn by the bleeder circuit. The output is available at terminal 15 of jack J1, and at test jack J5, where it is designated +3V.

f. *Remaining Internal Power Supply Circuits* (fig. 6-11).

- (1) The output at terminals 3 and 5 of transformer T1 is 55 volts rms. This voltage is full-wave rectified by diodes CR7 and CM and filtered by capacitors C16 and C17 and choke L2. The resulting dc output is passed through fuse F4 and then routed in two directions: one branch is applied to terminal 23 of jack J1, where the output is designated *cable current ckt dc pwr*, and to test jack J7, designated -28VDC; the other branch is applied to a voltage divider consisting of resistors R28, R29, R32, and R33. A breakdown diode (VR4) with a breakdown voltage of 17 volts is connected across resistor R32. The -17-volt dc output is applied to test jack J6.

- (2) The output at terminals 15 and 17 of transformer T1 is 28 volts ac. Terminal 17 is grounded, and the output of terminal 15 is split three ways. One branch goes to normally open thermostat switch S1; whenever the power supply temperature exceeds 160° F., the contacts close, and 28 volts ac is applied to terminal 3 of jack J1 (designated *change filter*), which causes CHANGE AIR FILTER indicator lamp DS2 on the front panel to light. Another branch of the 28-volt ac output is applied to terminal 7 of jack J1, which is designated 28-VAC. The third branch is applied to a peak-detecting circuit which develops a negative 30-volts dc output. This output, designated *cable power start control*, is applied to terminal 21 of jack J1.

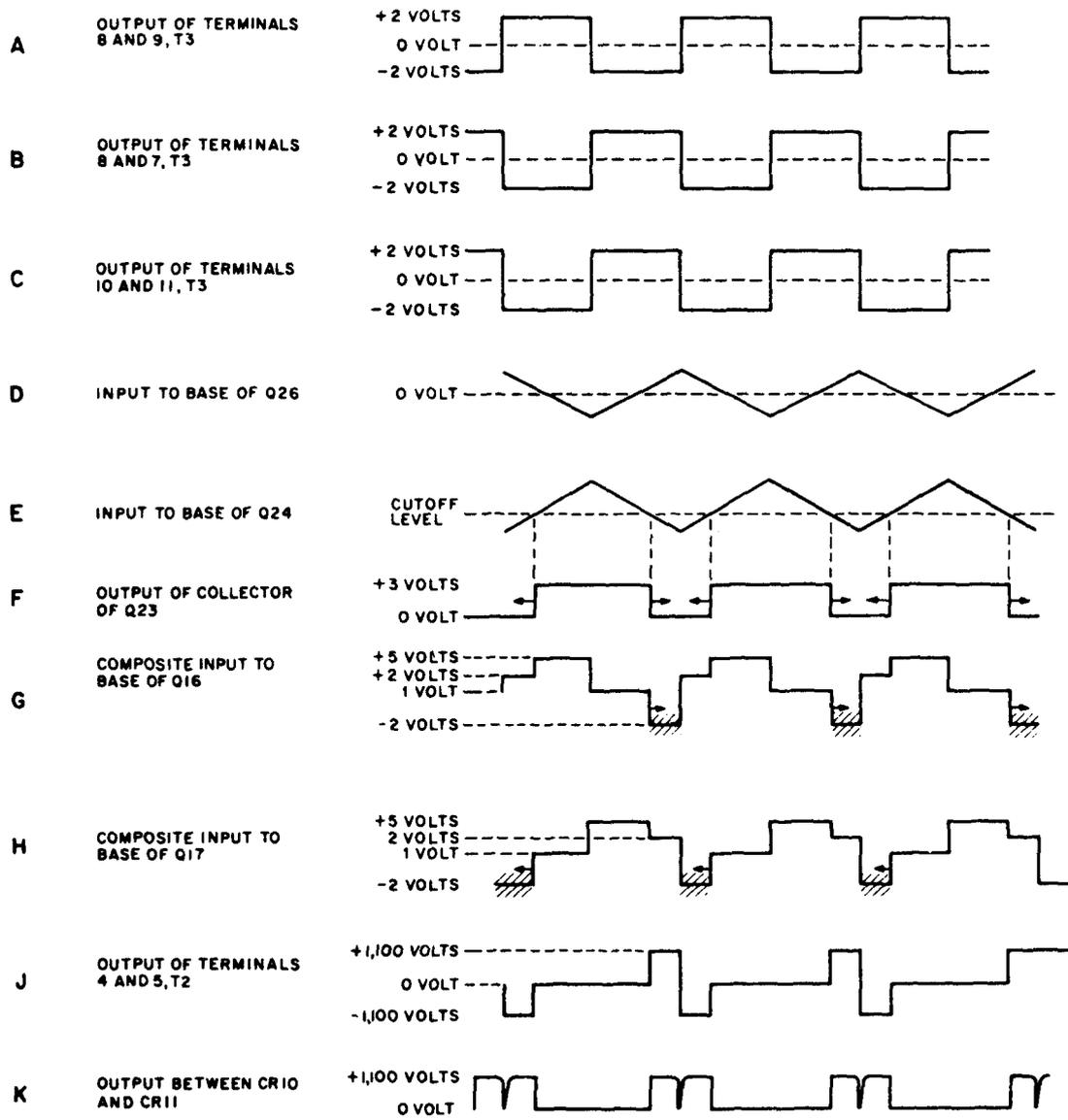
g. *Royer Circuit* (fig. 6-11). The + and -3-volt outputs from J1 are applied to the royer circuit, which is a form of saturable-core square wave oscillator. Operation of the royer circuit is described in TM 11-690. The outputs of transformer T3 at terminals 8 and 9 and 8 and 7, respectively, are shown in A and B, figure 2-8.

h. *Integrator Circuit* (fig. 6-11).

- (1) The output of the secondary of transformer T3 at terminals 10 and 11 is a train of square wave pulses with peaks of +2 and -2 volts. This output is applied to an integrator composed of resistor R61 and capacitor C29 (C, fig. 2-8).
- (2) The voltage drop across resistor R61 charges capacitor C29 exponentially to the positive voltage level. When the square wave pulse drops to -2 volts, capacitor C29 discharges through transistor Q26 and R61. As the square wave again turns positive, capacitor C29 recharges. The result is a sawtooth waveform (D, fig. 2-8).
- (3) The output of transistor Q26 is a sawtooth waveform applied through summing resistor R70. It is applied to the base of adding *ampl dc & sawtooth* transistor Q25, where it is combined with the output of *dc ampl* transistor Q27.

i. *Dc Amplifier Circuit* (fig. 6-11).

- (1) One input to the dc amplifier is from a differential amplifier stage composed of transistors Q28 and Q29 and attendant cir-



NOTES:
 1. ARROWS INDICATE DIRECTION OF PULSE EDGES FOR DECREASING OUTPUT CURRENT
 2. CROSSHATCHING INDICATES CONDUCTING CYCLES FOR TRANSISTORS

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Figure 2-8. Dc cable current power supply waveforms.

cuitry. The principal signal input is applied to the base of transistor Q29 from the junction of cable under current relay K4 and CABLE CURRENT ADJ potentiometer R47. A fixed -6-volt bias for the base of transistor Q28 is established by breakdown diode VR9. The voltage that represents the output current at the base of transistor Q29 is compared with the fixed -6-volt bias at the base of transistor Q28. If the two voltages are equal, the output at the collector of transistor Q29 is approximately -12 volts. Whenever the signal at the base of transistor Q29 becomes more negative than the fixed bias at the base of transistor Q28, transistor Q29 conducts. The output at the collector of transistor Q29 becomes more positive than -12 volts, and the output is applied through resistor R73 to the base of dc ampl transistor Q27.

- (2) The other input to transistor Q27 is from *Ico neut* transistor Q18, which compensates for the ICO changes in transistor Q27 caused by temperature variations. The ICO of transistor Q27 flows from collector to base, where the base bias could be changed by the voltage drop across resistor R73. However, the ICO of transistor Q18 operates in the same way as that in transistor Q27; it draws current from the base of transistor Q27 equal to the amount added by the ICO change of transistor Q27. Breakdown diodes VR7 and VR8 and diode CR17 maintain a constant voltage output, regardless of temperature, input voltage, and load current.
- (3) The output of transistor Q27 is applied through summing resistor R71 to the base of transistor Q25. Here the sawtooth waveform from the integrator circuit is combined with the dc level from the dc amplifier circuit.

j. Switch Input Circuit (fig. 6-11).

- (1) The composite signal formed by the addition of the sawtooth waveform from the integrator circuit and the dc level from the dc amplifier (E, fig. 2-8) is applied to the base of transistor Q25. This transistor acts as a preamplifier for the switch input circuit.

- (2) An inverted replica of the input at its base appears at the collector of transistor Q25; this signal is applied to the base of transistor Q24. Transistor Q24 operates with transistor Q23 as a conventional Schmitt trigger circuit.
 - (3) In this circuit, the sawtooth waveform is converted to a square wave. The width of the negative-going square wave (F, fig. 2-8) is dependent upon the dc level that supports the sawtooth waveform. If the level increases, the amplitude of the sawtooth waveform also increases, and the negative-going triangular points of the sawtooth waveform swing below the cutoff level for a short time, making the output pulses narrow. If the dc level is low, the triangular points of the sawtooth swing deeper into the cutoff region, the transistor conducts longer, and there is a wider output pulse. The output of the Schmitt trigger (F, fig. 2-8) is taken from the collector of transistor Q23 and applied to the bases of switch driver transistors Q21 and Q22.
 - (4) The switch driver operates as a conventional complementary-symmetry circuit which produces a push-pull output. The output of the switch driver is taken from the emitters of transistors Q21 and Q22 and applied through resistor R58 to terminal 8 of transformer T3. Thus, the negative-going square pulse output of the switch driver is added to the square wave output at terminals 7 and 9 of transformer T3 (G and H, fig. 2-8).
- k. Output Circuit** (fig. 6-11).

- (1) Transistors Q16 and Q17 comprise two switches that provide inputs to transformer T2. A dc level is transmitted to their bases (G and H, fig. 2-8). Proper collector voltage is supplied through a circuit composed of the cable current power input (28 volts dc), contact 1 of *cable under current relay K4*, and the center-tapped primary of transformer T2. Terminals 1 and 3 of transformer T2 supply the collector voltage for transistors Q16 and Q17.
- (2) The outputs of transistors Q16 and Q17 depend on the width of the Schmitt trigger pulses. If the negative-going portions

of the Schmitt trigger output pulses (F, fig. 2-8) are narrow, the negative-going portions of the outputs (G and H, fig. 2-8) are narrow, and vice versa. The negative-going portions of the pulses cause transistors Q16 and Q17 to conduct and provide a push-pull output for the primary of transformer T2 at terminals 1 and 3, respectively. The output of the secondary of transformer T2, across terminals 4 and 5, is shown in J, figure 2-8.

- (3) The output of transformer T2 is applied to a bridge rectifier consisting of diodes CR10, CR11, CR12, and CR13. The bridge rectifier produces an output (K, fig. 2-8) which is taken from the junction of diodes CR10 and CR11 and the junction of CR12 and CR13. At a peak positive voltage of 1,100 volts, the output of the bridge rectifier is applied through a filter network, consisting of chokes L3 and L4 and capacitor C25, to pin 9 of jack J 1, where the signal is designated *cable current output*.
 - (4) The cable current output must be regulated to provide a uniform amount of current to the cable and associated restorers, regardless of load. The ground return for the bridge rectifier is used to provide the initial signal for current regulations. The path to ground is from the junction of diodes CR12 and CR13, through the solenoid of relay K5, through the solenoid of relay K4 through CABLE CURRENT ADJ potentiometer R47, and then through resistor R54 to ground. A portion of the current passing through potentiometer R47 provides a voltage which is applied to terminal 10 of jack J1 through resistor R55; it is designated *cable current meter*.
- l. Dc Cable Current Control* (fig. 6-11).
- (1) The cable current output is adjusted by CABLE CURRENT ADJ potentiometer R47 which establishes the voltage value (proportional to the cable current) that is routed to the current-regulation system. Varying the voltage to the feedback loop (*diff ampl, dc ampl, adding ampl, de & sawtooth*, Schmitt trigger, and switch drivers), varies the width of the square wave pulses applied to the primary of transformer T2, and, therefore, the current output.
 - (2) The maximum permissible current output is 45 milliamperes (ma), adjusted by OVER CURRENT ADJ potentiometer R46. This potentiometer is connected in parallel with cable over current relay K5, which shuts down the power supply when the 45-ma limit is exceeded.
 - (3) Cable under current relay K4 drops out when the current falls below 6 ma, and, when this occurs, relay K4 deenergizes and shuts down the power supply. At shutdown, stored energy in the cable and in capacitor C25 is grounded out.
 - (4) The cable current supply is energized by CABLE POWER switch S4 located on the front panel. With switch S4 set to ON, -28 volts is applied from terminal 23 to terminal 24 of jack J1, through switch S4 and jack J12. From terminal 24 of jack J1, the voltage is applied to contact 1 of cable power start relay K3, which is energized momentarily during startup.
 - (5) Relay K3 is energized momentarily to perform three functions. The prime function is to provide power for switch transistors Q16 and Q17, the second function is to discharge the energy in the cable and in capacitor C25 at shutdown, and the third function is to momentarily short out cable over current relay K5.
 - (6) Current flow is in the main cable with the return through the cable shield to chassis ground. From ground, the current flow is through resistors R54 and R47, through the solenoid of relay K4, through momentarily closed contacts 7 and 8 of relay K3, to the junction of diodes CR12 and CR13. Current flow through the solenoid of relay K4 causes the relay to energize and close contacts land 2, thereby providing another path for the voltage at terminal 24 of jack J1 to reach terminal 2 of transformer T2. When this additional path is established, the initial path established by relay K3 is no longer required, and relay K3 is deenergized when the time constant of capacitor C20 and resistor R38 is terminated. To open a safety shunt, contacts 5 and 7 are opened by relay K4.

- (7) The relay network also contains features which temporarily defeat some of the protective measures. Relay K3 is connected in series with transistor Q15, which conducts when power is applied to energize relay K3. Transistor Q15 is normally held cut off by the output of a voltage divider consisting of resistors R40 and R41 and diode CR15. The bias voltage for driving transistor Q15 into conduction is developed by a resistance-capacitance (rc) circuit consisting of capacitor CM and resistor R38. The voltage for the rc circuit is furnished by CABLE POWER switch S4. When switch S4 is set to ON, -30 volts is applied from terminal 21 to terminal 22 of jack J1, and then to resistor R38. Current flow is from one plate of capacitor C20, through resistor R38, to ground, through the power supply, and through the emitter and base of transistor Q15 to the other plate of capacitor C20. The current flow clamps the transistor base slightly negative, and the transistor conducts to energize relay K3. Capacitor C20 charges in conformance with the rc time constant; the current decreases, and the voltage across the capacitor increases. When the voltage reaches approximately -15 volts, Zener diode VR6 breaks down, and the -30-volt input passes to ground through the diode. Thus, a constant -15-volt potential is maintained by breakdown diode VR6. Consequently, capacitor C20, having no changing voltage, loses its transferring capability. The base of transistor Q15 resumes its former cutoff bias from the voltage divider, and the transistor shuts off. Relay K3 deenergizes. Diode CR14 is connected across resistor R38 to provide a low impedance path for quickly discharging capacitor C20 at shutdown. Capacitor C20 must be discharged to enable the power supply to be started again after a temporary shutdown.
- (8) Before relay K3 deenergizes, relay K4 must energize to replace the functions initiated by relay K3 ((5) above). When the cable current power supply reaches an output of 20 ma, during initial startup, relay K4 energizes, closing contacts 1 and

2, and thereby providing the normal path for the power for switch transistors Q16 and Q17. In addition, relay K4 opens contacts 7 and 5 to provide another open in the safety shunt circuit. It closes at shutdown to discharge the energy in the cable and in capacitor C25. When relay K4 attains normal operation, relay K3 is ready to be deenergized. Relay K3, upon deenergizing, opens the short circuit across relay K5, so that it can energize if the current exceeds 45 ma. Relay K3 also closes contacts 5 and 7, closing the temporary opening in the safety shunt. If the current exceeds 45 ma, relay K5 energizes and shorts out relay K4. When relay K4 is shorted out, it is deenergized to shut down its circuit.

m. Cable Power Failure Alarms (fig. 6-11).

- (1) The dc cable current supply contains two cable power failure alarm relays, K1 and K2, which provide audible and visible alarms when one of the energizing input fails.
- (2) In normal operation, NO CABLE CURRENT indicator lamp DS3 is extinguished, and buzzer alarm indicator DS6 is silent. Relays K1 and K2 are wired in series and act as one relay. During normal operation, relay K1 of panel 6A4 (fig. 6-17) and relays K1 and K2 of panel 6A1 (fig. 6-11) are energized. This condition removes power from all the alarm components,
- (3) When cable power fails, relays K1 and K2 deenergize, allowing 28 volts ac to be applied through contacts 2 and 4 of relay K2 to terminal 4 of jack J1, and cause NO CABLE CURRENT indicator lamp DS3 to light. The 28 volts ac is also applied through contacts 7 and 5 of relay K2 to terminals 5 and 8 of jack J1, and then to the on terminal of BUZZER OFF switch S2. Then buzzer DS6 sounds. When the operator depresses the BUZZER OFF switch, buzzer DS6 is silenced.
- (4) After the fault is corrected, relays K1 and K2 are energized by operating CABLE POWER switch S4 on the front panel first to OFF and then to ON. Another method is to operate the AC POWER switch on the front panel first to OFF and then to

ON. A 28-volt ac signal is applied through closed contacts 2 and 8 of relay K1 on panel 6A4 (fig. 6-17) to terminal 11 of jack J7 of panel 6A2 (fig. 6-13). This voltage is then applied to terminal 16 of jack J1, and then

through closed contacts 2 and 1 of relay K1, to terminal 6 of jack J1 (fig. 6-11). Finally, the voltage reaches the off terminal of BUZZER OFF switch S2, passes through the switch arm, and energizes buzzer alarm indicator DS6.

Figure 2-9. (Deleted)

2-12. Order Wire No. 1, Panel 6A2 (fig. 6-13)

a. *General.* Order wire No. 1, panel 6A2, operates in conjunction with order wire No. 2, panel 6A3, to process the order wire. Panel 6A2 contains the receive circuits for processing the order wire. A signaling oscillator is provided to furnish an order-wire ring signal to signal operators at distant stations. A signaling detector is also included to separate a ring signal from the incoming order wire and to develop a signal to sound the buzzer. Panel 6A2 also contains a resistive hybrid that couples the input and output order-wire signals to their associated circuits. The resistive hybrid is designed to permit easy passage of signals in certain directions and to prevent their passage in other directions.

b. *Radio Receive Amplifier.*

- (1) When the order wire is applied directly from a radio receiver, a signal of approximately 45 millivolts (mv) is applied to terminals 14 and 15 of jack J10 through terminals G and H of the PATCH THRU connector mounted on the front panel. If the order wire arrives from another TD-204/U, a signal of approximately 225 mv is applied to terminals 12 and 13 of jack J10 through terminals A and B of the PATCH THRU connector. In this case, terminals 8 and 11 of jack J10 are tied together.
- (2) Because of the difference in signal levels between the alternative inputs, an attenuating pad (resistors R1 through R6) provides an identical input signal level to the primary of transformer T1. Without this attenuating pad, the radio receive amplifier would be overdriven by the larger signal level from the TD-204/U.
- (3) The signal is applied to the base of transistor Q1 from the secondary of transformer T1. The inverted output at the collector of transistor Q1 is applied to the base of transistor Q2, where it is reinserted and amplified further.
- (4) The output of transistor Q2 is applied to

the primary of transformer T2, the secondary of which supplies an output which is applied to terminals g and g' of 4-way 4-wire resistive hybrid HY1 (f below),

c. *Cable Receive Amplifier.*

- (1) A composite signal consisting of the order-wire signal and dc cable current is applied to terminal 3 of jack J10, and then across the primary winding of transformer T5 where the dc cable current is separated from the order-wire signal by passing the composite signal to ground through resistor R41. The potential across resistor R41 is applied through resistor R42 to terminal 5 of jack J10 where the output is designated *rcvd cable current [SF (RCC)]*.
- (2) The order-wire input to transformer T5 is induced in the secondary winding where the signal is applied to filter FL1. Here, the high frequency components of the signal are attenuated, and the signal is then applied across CRL (cable receive level) potentiometer R44 which supplies the desired signal level to the base of transistor Q9. An amplified and inverted replica of the signal appears at the collector and is applied to the primary of transformer T6, the output of which is applied to terminals c and c' of 4-way 4-wire resistive hybrid HY1.

d. *Microphone Amplifier Output.* The locally generated order wire is applied to terminals 25 and 26 of jack J10 and then directly to terminals a and a' of 4-way 4-wire resistive hybrid HY1.

e. *Signaling Oscillator.*

- (1) The signaling oscillator provides either a 1,600-cps ring signal or a 1,100-cps test tone. The ring signal alerts the operators at distant stations; the test tone provides a steady audiofrequency (af) signal for system alignment and troubleshooting.
- (2) When the front panel TALK-OFF-SIC switch is set to SIG, terminals 1 and 2 of jack J10 are connected together. The emitter of transistor Q10 is provided with a momentarily positive 10-volt potential through resistor R49 in series with resistors R51 and R52 which allows transistor Q10 to conduct.
- (3) The output of transistor Q10 is applied through the primary of transformer T7 to

the -10 -volt potential. The combination of the primary of transformer T7 and capacitor C24 comprises a tank circuit which resonates at 1,600 cps. This oscillation is induced in the secondary of transformer T7 and brought out to terminal 4 of jack J10 through resistor R55 as the ring signal.

- (4) To produce the 1,100-cps test tone, the resonant frequency of the signaling oscillator tank circuit is lowered by adding capacitance in parallel with capacitor C24. This is accomplished by setting TONE-OFF switch S1 to TONE. This places capacitor C23 in parallel with capacitor C24, and energizes transistor Q10 through resistors R51 and R52. The continuous 1,100-cps output is taken from TTL potentiometer R53 and applied through resistor R54 to terminal 6 of jack J10 where it is designated *test tone*.

f. Resistive Hybrid. The signal is branched in many directions in 4-way 4-wire resistive hybrid HY1. In undesired signal directions, the signal is attenuated over 80 decibels (db). In directions where the signal is desired, the signal is attenuated only 15 db.

g. Phone Amplifier.

- (1) The output of the resistive hybrid for the local headset is taken from terminals *h* and *h* of the hybrid and applied across the primary of transformer T3, the output of which is applied to the base of transistor Q3. The output of transistor Q3 is applied to the base of transistor Q4 through capacitor C5. The output of transistor Q4 is divided two ways.
- (2) One branch is routed back through capacitor C6 and resistor R21 to the emitter of transistor Q3. The other branch of the output of transistor Q4 is routed through capacitor C7 and then divided into two branches: one branch is applied directly to terminal 21 of jack J10 where the output is designated *HEADSET* ear-phone; the other branch is applied to the base of transistor Q5.
- (3) The output of transistor Q5 is applied to a monitoring circuit consisting of resistor R30, capacitor C10, and diode CR1. The dc output of the monitoring circuit is

applied to terminal 17 of jack J10, with the output designated *phone ampl mete [SF(Q)]*.

h. Signaling Detector,

- (1) The signaling detector allows the buzzer to be actuated whenever a 1,600-cps ring signal arrives from a distant station. A delay circuit present momentary frequencies of 1,600 cps from actuating the buzzer.
- (2) A reference level is applied to the base of transistor Q6 from the emitter of transistor Q5 (in the phone amplifier) through capacitor C11. The output of transistor Q6 is applied to the primary of transformer T4, the output of which is applied to a tuned circuit composed of coil L1 and capacitor C14. The inductor and capacitor resonate at 1,600 cps providing maximum voltage output in a narrow peak at 1,600 cps. This 1,600-cps signal is rectified by diode CR2 and filtered by capacitor C15
- (3) When the signal is above or below the 1,600-cps frequency, the timed circuit behaves like a short circuit. The signal provides a voltage drop across resistor R35 which is filtered by capacitor C16. The output of the tank circuit, composed of resistor R36 and capacitor C15, adds in series with the output of the tank circuit, composed of resistor R37 and capacitor C16. The time constants of capacitors C15 and C16 prevent intermittent false signaling clue to 1,600-cps speech and noise voltages present in the input. Transistor Q7 conducts only when there is no opposing voltage from the tank circuit composed of resistor R37 and capacitor C16.
- (4) With a continuous tone of approximately 1,600 cps, the dc voltage produced at the base of transistor Q7 maintains conduction of transistor Q7. This, in turn, provides base bias voltage for transistor Q8, which conducts and presents its output to terminal 7 of jack J10, where it is designated *sig det control*.

2-13. Order Wire No. 2, Panel 6A3 (fig. 6-15)

a. General. Order wire No. 2, panel 6A3, operates in conjunction with order wire No.1, panel 6A2,

to process the order wire. Three circuits accomplish this task. The first circuit provides amplification for the locally generated order-wire audio signal, the locally generated 1,600-cps ring signal, and the locally generated 1100-cps test tone. The second circuit amplifies the order wire and applies it to a radio or to another TD 204/U. The third circuit amplifies the order-wire signal for transmission over cable.

b. Microphone Amplifier. The input signal to the microphone amplifier enters panel 6A3 at terminals 26 or 27 of jack J7. Either the locally generated order-wire audio or the ringing signal is applied to the base of transistor Q1 and amplified in the cascade amplifier comprised of transistors Q1, Q2, and Q3. There are two outputs from transistor Q3: the output from the emitter provides negative feedback to the base of transistor Q1 for stabilizing the amplifier, while the output from the collector is applied to the primary of transformer T-1 through resistor R13. The output of transformer T1 is routed to terminals 28 and 29 of jack J7, designated *mike-ampl B* and *mike-ampl A*, respectively.

c. Radio Transmit Amplifier.

(1) The radio transmit signal enters panel 6A3 at terminals 30 and 31 of jack J7, and is applied across the primary of transformer T2. The output of T2 is applied to the base of transistor Q4. An amplified and inverted replica of the signal is produced at the collector of transistor Q-1 and applied to the primary of transformer T3.

(~) The secondary of transformer T3 produces two out-of-phase signals that are applied to a push-pull amplifier consisting of transistors Q5 and Q6. Whichever transistor receives a negative-going signal will conduct and apply its output to the primary of transformer T-4. One end of the primary is returned to the emitter of transistor Q4 for stabilization. The output of transformer T-4 is applied to terminals 18 and 21 of jack J7, designated *patch thru-E* and *patch thru-F*, respectively.

(3) Resistor R28, capacitor C12, and diode CR1 constitute a monitoring circuit, the output of which goes to terminals 20 and 17 of jack 7, designated *radio xmit O. W. meter-A [SF(P)]* and *radio xmit O. W. meter-B [SF(P)]*, respectively.

d. Cable Transmit Amplifier.

(1) The cable transmit signal enters panel 6A3 at terminals 6 and 7 of jack J7, and is applied across the primary of transformer T5. The output of T5 is applied to the base of transistor Q7.

(2) An amplified and inverted replica of the input signal appears at the collector of transistor Q7 and is applied to the base of transistor Q8, which reamplifies and inverts the signal and applies its output to the primary of transformer T6. The secondary of T6 provides out-of-phase inputs to the bases of transistors Q9 and Q10. The transistor that receives a negative-going signal will conduct, applying its output to the primary of transformer T7. One end of the primary is returned to the emitter of transistor Q8 for stabilization. The output of transformer T7 is applied through low-pass filter FL1 to terminal 2 of jack J7, and designated *cable xmit O. W.*

(3) Capacitor CM, resistor R48, and diode CR2 comprise a monitoring circuit, the output of which goes to terminal 1 of jack J7 and is designated *cable xmit O. W. meter [SF(O)]*:

2-14. Cable Signal Receiver, Panel 6A4

(fig. 6-17)

a. General. Cable signal receiver, panel 6A4, operates in conjunction with panel 6A7 as the receive section for the TD-204/U. Panel 6A4 restores the shape of the pcm after separating the dc cable current and order wire. In addition, it develops a 2,304-kc timing pulse for use in other panels and provides an alarm signal when traffic fails. Traffic failure causes an oscillator to generate a 2,304-kc timing signal to simulate the normal timing signal. Operation of the panel is the same for all modes of operation,

b. Input Signal. The input signal is a composite, consisting of pcm at a 2,304-kc random rate, dc cable current, and order-wire signal, if present. The signal is applied through FROM CABLE jack J10 directly to terminal 2 of jack J7.

c. Signal Distribution. The dc cable current and order-wire signal are separated from the pcm. The dc cable current and order wire are blocked by capacitor C19, and, therefore, follow a path through

coils L7, L8, and L9 to terminal 3 of jack J7, where the output is designated *recd order wire*.

d. *Attenuation Network.* The pcm passes through capacitor C19 and is applied to an attenuation network. Whenever the cable length from the nearest restorer to the receive circuitry of the TD-204/U is less than 1 mile, the signal must be attenuated to compensate for the shorter length of cable. This is done by an attenuation network consisting of coils L11 through L13, resistors R21 through R23, and capacitors C27 through C29. Operating switch S1 to the **1/4 MILE, 1/2 MILE, or 3/4 MILE** position adds the attenuation network to the circuit. Diodes CR5 and CR6 protect panel 6A4 against lightning damage.

e. *Amplifier.* The pcm signal is applied to the primary of transformer T2, the output of which is applied to the base of transistor Q10, which amplifies and inverts the signal and applies its output to the primary of transformer T3. The output of transformer T3 is applied to the base of transistor Q11, which divides its reamplified and reinserted signal into two branches. One branch goes to the base of transistor Q1 (*h* below). The other branch is applied to the base of driver transistor Q12, an emitter follower, which supplies the input to the switch circuit.

f. *Switch.* A portion of the output from transistor Q12 is applied to terminal 19 of jack J7, designated *recd pcm*. The remainder of the signal is applied to the base of switch transistor Q13 through capacitor C25 and diodes CR7 and CR8, which clamp and peak-detect the signal. Normally, capacitor C26 charges to a negative potential to prevent conduction of transistor Q13. The time constant of resistors R33 and R34 and capacitor C26 cuts off transistor Q13 when an extended series of digital zero pulses is received. With transistor Q13 cut off, the collector assumes a potential of +10 volts which is divided into three branches. One branch is applied to terminal 4 of jack J7 through resistor R37, where the output is designated *red pcm meter [SF(A)]*. Another branch is applied to the base of oscillator transistor Q2 to maintain this transistor cut off (*h* below). The third branch is applied through resistor R36 to the base of relay driver transistor Q14.

g. *Relay Driver.*

- (1) When the +10-volt potential is applied to its base, relay driver transistor Q14 con-

ducts, energizing relay K1 and supplying 28 volts ac to terminal 7 of jack J7. This output is designated *buzzer switch OFF power* and operates in conjunction with circuitry in power supply panel 6A1 (para 2-11 *m*).

- (2) If a failure occurs in reception of the pcm signal, capacitor C26 loses its charge, causing transistor Q13 to conduct. When transistor Q13 conducts, transistor Q14 stops conducting, thereby deenergizing relay K1. Relay K1 applies 28 volts ac to terminal 13 of jack J7, designated *traffic failure alarm*, and to terminal 11 of jack J7, designated *TRAFFIC failure indicator* (para 2-11 *m*).

h. *Input to Timing Circuit.*

- (1) The pcm output from the collector of transistor Q11 is applied to the base of buffer transistor Q1 (*e* above). The output is taken from the emitter and applied through capacitor C7 and resistor R3 to crystal filter FL1.
- (2) Normally, the input to the crystal filter produces a 2,304-kc sine wave at the output. However, when traffic fails, filter FL1 generates a 2,304-kc sine wave through oscillation of transistor Q2. This sine wave is applied to the base of buffer-driver transistor Q3.
- (3) The output of buffer-driver transistor Q3 is taken from its emitter and applied directly to the base of transistor Q4. Transistor Q4 amplifies and inverts the signal, and applies it to the base of transistor Q5. Transistor Q5 couples the signal to the primary of transformer T1.

i. *Timing Circuit.*

- (1) The secondary of transformer T1, capacitor C13, and potentiometer R12 constitute a phase-adjust circuit. Phase-adjust potentiometer R12 is adjusted until the timing pulses produced are properly aligned with the pcm pulses.
- (2) The output of the phase-adjust circuit is applied to the base of buffer transistor Q6, whose output is taken from its emitter and applied to the base of transistor Q7 through capacitor C14 and inductor L10. These components provide additional filtering for the signal applied to the base of Q7.

- (3) Transistors Q7 and Q8 and inductor L2 comprise a combination differential amplifier and pulse shaper circuit. When transistor Q8 conducts, inductor L2 starts to provide a ringing signal that begins in a positive direction and then reverses to a negative direction. Transistor Q9 operates as a diode to cut off negative-going excursions. The result is a train of positive pulses at the base of transistor Q9.
- (4) One output of driver transistor Q9 is taken from its emitter and applied to terminal 25 of jack J7, with the designation *reed* timing. The 2,304-kc signal consists of a wavetrain of positive-going pulses.
- (5) Another output of driver transistor Q9 is clamped to ground by diode CR3 and peak-detected by diode CR4 to store a negative charge on capacitor C18. This negative output is applied to terminal 31 of jack J7, designated *reed timing meter [SF(B)]*, and is used for monitoring.

2-15. Transmit Signal Generator No. 1, Panel 6A5

(fig. 6-19)

a. General. Transmit signal generator No. 1, panel 6A5, operates in conjunction with panel 6A6 as the transmit section for the pcm signal. Panel 6A5 contains a circuit to attenuate the pcm signal when the cable length to the first restorer is less than 1 mile. In 12/24-channel operation, panel 6A5 replaces each transmit pcm input pulse with two half-width pulses of positive-going polarity to adapt the pulse rate to that of the restorers. Automatic switch relays provide two full-width pcm signals, or one full-width pcm signal and one dummy pulse train, to panel 6A6. Panel 6A5 incorporates the order-wire signal and dc cable current into the line that carries the pcm to the main cable.

b. 12-Channel Rate Description. Since the TD-206/G is designed to handle pcm at a 48-channel rate (2,304 kc), it is necessary to increase the rate of the 12-channel wavetrain (A, fig. 2-10), the signal is first interleaved with a 288-kc dummy signal (D, fig. 2-10), in panel 6A6. The addition of the dummy signal increases the rate to 1,152 kc; this interleaved signal (E, fig. 2-10), is then returned to panel 6A5 where each full-width pulse is divided into two half-width pulses at a 48-channel rate.

c. Pcm Input (fig. 6-19).

- (1) In 12-channel operation, the *xmit pcm* input (E, fig. 2-10) is applied to terminal 15 of jack J10, and then to the bases of starting gate transistors Q1 and Q2. These act in conjunction with transistor Q3 as a differential amplifier (para 2-11c). A 2,304-kc timing signal (G, fig. 2-10) is applied to the base of transistor Q3. This timing signal (H, fig. 2-10), samples the pcm at the bases of transistors Q1 and Q2, causing transistor Q3 to conduct whenever a digital 1 pulse (J, fig. 2-10) appears. Each time transistor Q3 conducts, an amplified and inverted replica of the timing signal appears at the collector of transistor Q3 (K, fig. 2-10). Since the duration of a digital 1 pulse at the bases of transistors Q1 and Q2 is 0.87 microsecond (μsec), **two timing pulses appear at the base of transistor Q3** for this period. As a result, each pcm pulse is sampled twice.
- (2) The output of transistor Q3 is applied to the base of transistor Q7 through capacitor C1 and diode CR5. Transistors Q7 and Q8 constitute a flip-flop, which is set by random pairs of positive-going spike pulses. To reset the flip-flop, a periodic train of positive-going spike pulses (L, fig. 2-10) with a 2,304-kc rate is constantly applied through diode CR7 to the base of transistor Q8. These pulses are phased to reset the flip-flop 0.22 microsecond after it has been set. Each original digital 1 pulse is then represented by two negative-going pulses, each with a width of 0.22 psec (M, fig. 2-10) and 0.22 psec apart.

d. Pcm output (fig. 6-19).

- (1) The output from the flip-flop is applied to buffer and driver transistor Q9, whose output is applied to the base of power amplifier transistor Q19 through capacitor C9.
- (2) The output of transistor Q19 is applied to one end of the primary of transformer T1, which is in series with an attenuation network composed of inductors L5 through L7, resistors R51 through R53, and capacitors C41 through C43. When the cable length to the next restorer is less than 1 mile, switch S1 is operated to the $\frac{1}{4}$ MILE, $\frac{1}{2}$ MILE, or $\frac{3}{4}$ MILE position to

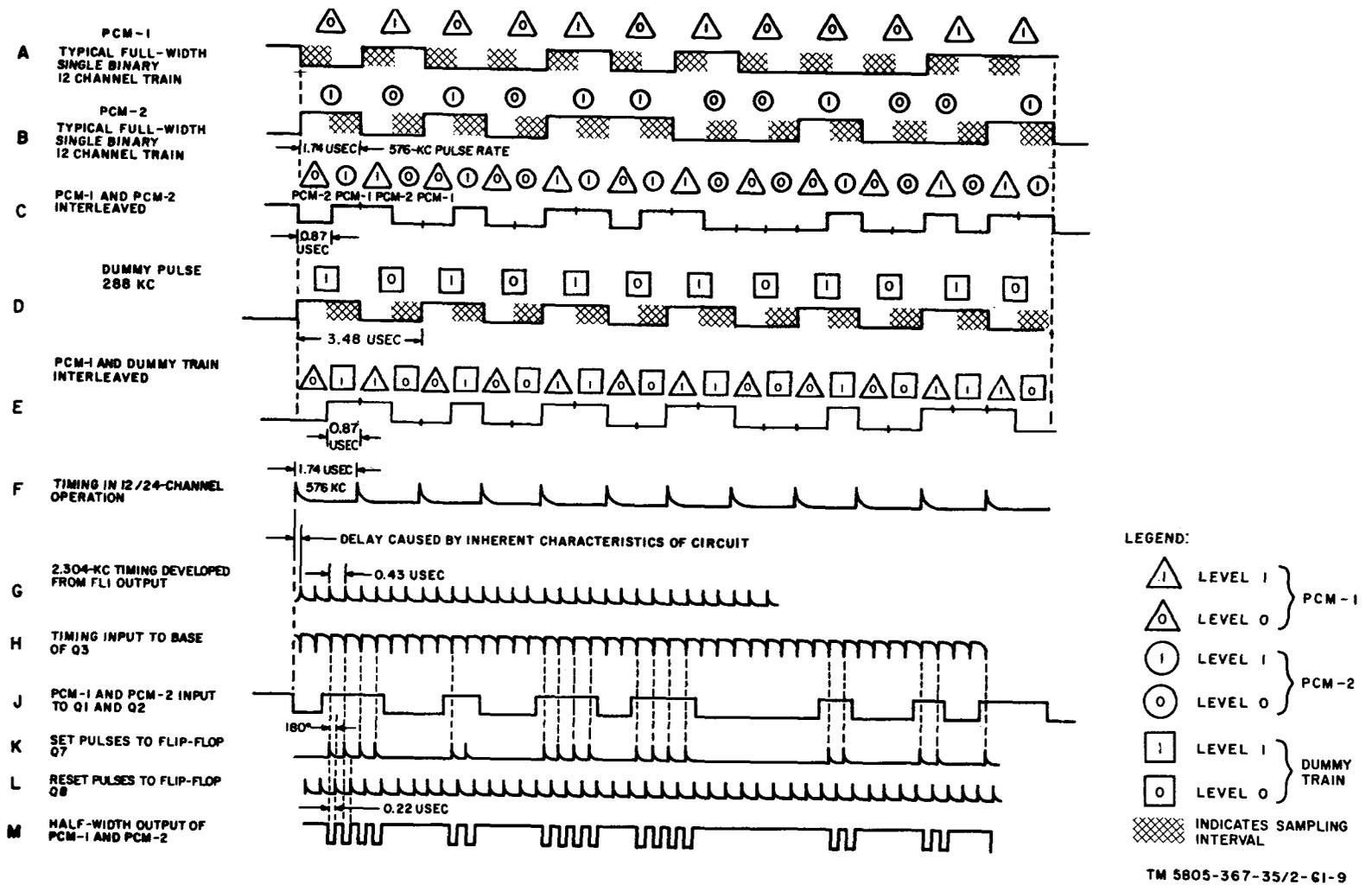


Figure 2-10. Panel 6A5, generation of half-width pulses.

add the required attenuation to the output pcm signal. The signal induced in the secondary of transformer T1 is applied to terminal 3 of jack J10, where the output is designated *TO CABLE*.

e. *Cable Current and Order Wire* (fig. 6-19). Cable current and order wire enter terminal 1 of jack J10, are applied to the secondary of transformer T1, and become a part of the signal applied to terminal 3 of jack J10.

f. *Pcm Monitor Circuit* (fig. 6-19). A portion of the output of transistor Q19 is applied to terminal 20 of jack J10 where it is designated *xmit pcm meter [SF(H)]*.

g. *Multiplex Timing* (fig. 6-19).

- (1) A train of positive-going spike pulses at a 576-kc rate is applied to terminal 31 of jack J10. From here, it goes to the base of transistor Q10 which forms a differential amplifier with transistor Q11.
- (2) The output from transistor Q11 is applied to filter FL1 through capacitor C13. The 576-kc timing pulses ring the filter to produce 2,304-kc sine wave signals which are applied to the base of buffer transistor Q12.
- (3) The output of buffer transistor Q12 is routed to the base of transistor Q13 through capacitor C16. Transistors Q13 and Q14 comprise a differential amplifier. The differential amplifier produces two timing pulses each with a frequency of 2,304 kc, phased 180° apart. The pulses trigger the leading and trailing edges of the half-width pcm pulses to be developed.
- (4) The pulses which trigger the leading edges are taken from the collector of transistor Q14 and applied through capacitor C4 to the base of amplifier transistor Q5. The output of transistor Q5 is applied to the base of buffer transistor Q4. The output is taken from the emitter of transistor Q4 and applied to the base of starting gate **transistor Q3 (c(1) above)**.
- (5) The pulses used to trigger the trailing edges are taken from the collector of transistor Q13 and applied to the base of driver transistor Q6. The output of transistor Q6, a series of positive-going spike pulses, is applied through capacitor C6 and diode

CR7 to the base of flip-flop transistor Q8. These pulses reset the flip-flop (c(2) above).

- (6) Another branch of the output of transistor Q13 is applied to the base of buffer transistor Q15. The output from the emitter of transistor Q15 is routed through capacitor C18 to terminal 24 of jack J10, where the output is designated *xmit timing*.

h. *Multiplex Timing Monitor Circuits* (fig. 6-19).

- (1) The output of the collector of transistor Q10 is applied through capacitor C12 and diode CR10 to terminal 27 of jack J10. The signal is designated *12/24 ch xmit timing meter (FP)*.
- (2) A branch of the emitter output of transistor Q15 is applied to the base of buffer transistor Q16. The output of transistor Q16 is taken from its emitter and applied to terminal 23 of jack J10 where the signal is designated *xmit timing meter [SF(J)]*.

i. *Automatic Switch Control* (fig. 6-19).

- (1) In 12-channel operation, the automatic **switch control automatically substitutes** a dummy signal for the additionally required 12-channel binary signal. The PCM IN-1 signal is taken from terminal 19 of jack J10 and divided into three branches.
- (2) One branch is applied through capacitor C29 to diodes CR17 and CR18. The signal is clamped to +3 volts by diode CR18 and peak-detected by diode CR17. A negative charge is stored on one plate of capacitor C30. When the charge is sufficient to overcome the bias at the base of automatic switch relay control transistor Q18, the transistor conducts and energizes relay K2.
- (3) With relay K2 energized, another branch of the PCM IN-1 signal is applied through K2, contacts 5 and 1, to terminal 12 of jack J10, where the signal is designated *12/24 channel traffic No. 1*.
- (4) In 12-channel operation, there is no signal applied to terminal 22 of jack J10 (PCM IN-2). Because of this, capacitor C24 does not charge, and relay K1 remains deenergized, thereby coupling the dummy pulse train signal to terminal 16 of jack J10, where it is designated *12/24 channel traffic No. 2*.

j. PCM IN-1 and PCM IN-2 Monitor Circuits (fig. 6-19).

- (1) The PCM IN-1 signal is applied to a monitoring circuit composed of diodes CR19 and CR20 and capacitor C27. The output of the monitoring circuit is applied to terminal 21 of jack J10, where the signal is designated *PCM IN-1 meter (FP)*.
- (2) The PCM IN-2 signal is also applied to a monitoring circuit composed of diodes CR15 and CR16 and capacitor C25. The output of the monitoring circuit is applied to jack J10 at terminal 10, where the signal is designated *PCM IN-2 meter (FP)*.

k. 24-Channel Rate Description (fig. 6-19). In 24-channel operation it is unnecessary to use a dummy pulse train because there is a pcm-2 signal input. To produce the necessary 48-channel rate, the two 12-channel pcm signals (A and B, fig. 2-10) are interleaved (C, fig. 2-10) in panel 6A6 and then returned to panel 6A5 where each pcm pulse of the interleaved pcm is divided into two half-width pulses. Panel 6A5 operates the same for 24-channel operation as for 12-channel operation, except that a pcm signal is applied to terminal 22 of jack J10 (PCM IN-2). This signal controls the automatic switch relay. If one pcm signal should fail, the automatic switch relay automatically provides a dummy pulse train to replace the missing pcm signal.

l. 48-AR Rate Description (fig. 6-19). During 48-AR operation, panel 6A5 operates the same as in 12/24 channel operation, with the following exceptions:

- (1) In addition to the monitoring circuits described in *h* above, an output from the collector of transistor Q10 is applied to terminal 25 of jack J10, where it is designated *48 ch xmit timing meter (FP)*. The signal from the PCM IN-1 terminal arrives at terminal 14 of jack J10 instead of terminal 19.
- (2) In addition to the 12/24-channel traffic No. 1 output (*i(3)* above), a branch of the same output is applied to terminal 11 of jack J10, where the signal is designated *48 channel traffic*. The signal on terminal 11 is then routed back to terminal 15 as the *xmit pcm signal*.
- (3) The pcm input for 48-channel operation is

sampled once instead of twice, because it is at the same rate. The timing signal at terminal 31 of jack J10 enters at the frequency of the 2,304-kc signal. Since the signal entering filter FL1 is at the desired frequency (2,304 kc), the filter supplies no multiplication of frequency.

2-16. Transmit Signal Generator No. 2, Panel 6A6
(fig. 6-21)

a. General. Transmit signal generator No. 2, panel 6A6, is used with panel 6A5 as the transmit section for the pcm signal. It contains the circuits in which traffic 1 and traffic 2 are interleaved. In addition, it develops a 288-kc dummy pulse train signal used for interleaving with the single pcm pulse train in 12-channel operation, or when either traffic 1 or traffic 2 fails. Panel 6A6 is not used for 48-channel operation except for fault-location procedures.

b. Dummy Pulse Train.

- (1) The dummy pulse train is derived from the *mux timing in pulse train* which is applied to terminal 3 of jack J11. During 12/24-channel operation, the *mux timing in* signal consists of a train of positive-going spike pulses, with a rate of 576 kc, which is divided to obtain the 288-kc dummy pulse train. During 48-channel AR operation, the *mux timing in* frequency is 2,304 kc, which is divided to obtain a 1,152-kc signal for a fault locating system.
- (2) From terminal 3 of jack J11, the signal is divided into two branches. One branch is applied to the base of flip-flop transistors Q7 and Q8 through capacitor C1. The flip-flop develops a square wave signal at a frequency of 288 kc which is applied to the base of buffer transistor Q9. The emitter output of transistor Q9 is applied to terminal 9 of jack J11, where the signal output is designated *dummy pulse train*.
- (3) The other branch from terminal 3 of jack J 11 is applied to the base of buffer transistor Q21. The emitter output of transistor Q21 is transmitted to the base of inverter transistor Q22 through a differentiating network composed of capacitor

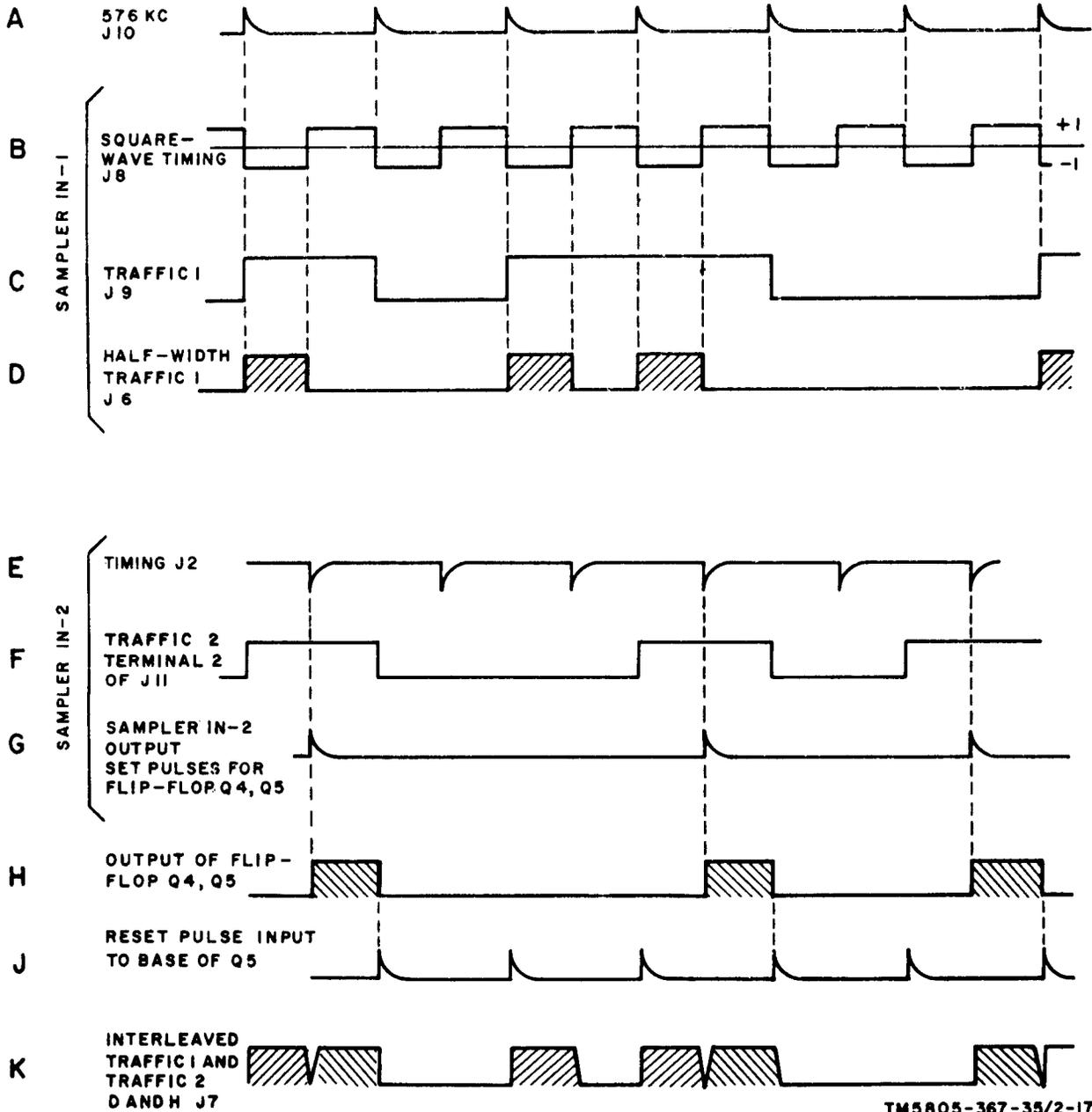
C35 and resistor R71. The negative-going pulses of the differentiated pulse train cause transistor Q22 to conduct. The output of transistor Q22 is a train of positive-going spike pulses (A, fig. 2-11).

- (4) The output of transistor Q22 is divided three ways. Two branches act as set pulses

and are routed through steering diodes CR15 and CR18 (fig. 6-21) to the bases of flip-flop transistors Q10 and Q12, respectively. The third branch goes to the base of Q23 (i below).

c. *Traffic 1 Input* (fig. 6-21).

- (1) One of the two pcm inputs is the 12-



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Figure 2-11. Panel 6A6, waveforr: relationship.

channel traffic 1 signal (C, fig. 2-11) which is applied to terminal 30 of jack J11. Normally, traffic 1 is identical to PCM IN-1. If PCM IN-1 fails, the traffic 1 signal is furnished by the dummy pulse train.

- (2) From terminal 30 of jack J11, the signal is routed to the base of transistor Q16, which, with transistor Q15, comprises the sampler in-1 differential amplifier. The output of the sampler in-1 differential amplifier is described in f(1) below.

d. *Traffic 2 Input* (fig. 6-21). The traffic 2 signal (F, fig. 2-11) is identical to the PCM IN-2 signal, except when the dummy pulse train replaces it in 12-channel operation or whenever PCM IN-2 fails. Traffic 2 enters at terminal 2 of jack J11 and then is routed to the base of transistor Q1, which, with transistor Q2, forms the sampler in-2 differential amplifier. The output of the sampler in-2 differential amplifier is described in g(1) below.

e. *Timing* (fig. 6-21).

- (1) The timing for the two sampling differential amplifiers is developed from the *xmit timing* signal that is applied to jack J11 at terminal 24. This train of positive-going spike pulses at a frequency of 2,304 kc is applied to the base of flip-flop transistor Q10 through diode CR11, and to the base of flip-flop transistor Q11 through diode CR12. Set pulses are applied through diode CR15 so that the output of the flip-flop is correctly phased with the *mux timing in* signal. This flip-flop halves the 2,304-kc signal to 1,152 kc.
- (2) The output from the collector of transistor Q11 is applied to the base of flip-flop transistor Q12 through diode CR16, and to the base of flip-flop transistor Q13 through diode CR17. Set pulses are applied through diode CR18 so that the output of the flip-flop is correctly phased with the *mux timing in* signal. This flip-flop divides the 1,152-kc signal to 576 kc.
- (3) The square wave output at the collector of transistor Q12 is fed to the base of buffer transistor Q14. The emitter output of transistor Q14 is divided into two branches.
- (4) One branch is routed through capacitor

C7, resistor R14, and diode CR3, differentiating the square wave signal and allowing only the positive-going spike pulses to be transmitted to the base of pulse shaper transistor Q3. Transistor Q8 provides a negative-going spike pulse (E, fig. 2-11) at its collector which is routed through capacitor C4 to the base of transistor Q2.

- (5) The other branch is routed through capacitor C28 to the base of transistor Q15. The signal at the base of transistor Q15 is a train of square wave pulses (B, fig. 2-11) used for sampling.

f. *Traffic 1 Output* (fig. 6-21).

- (1) A digital 1 pulse (or positive-going dummy train pulse) arriving at the base of transistor Q16 causes transistor Q15 to conduct when the signal at its base falls below zero. A positive-going pulse (D fig. 2-11) is produced at the collector of transistor Q15.
- (2) The output from transistor Q15 is routed to the base of buffer transistor Q17. The emitter output of transistor Q17 is applied through capacitor C29 to the anodes of diodes CR19 and CR21.

g. *Traffic 2 Output* (fig. 6-21).

- (1) A positive-going signal (F, fig. 2-11) at the base of transistor Q1 allows the negative-going spike pulses (E, fig. 2-11) at the base of transistor Q2 to appear at the collector of transistor Q2 (G, fig. 2-11). The output of transistor Q2 is applied through capacitor C3 and diode CR4 to the base of transistor Q4.
- (2) Transistors Q4 and Q5 comprise a flip-flop which produces a half-width traffic 2 signal (H, fig. 2-11) at the collector of transistor Q5. For reset pulses, the square wave output of transistor Q13 is differentiated by capacitor C27 and resistor R53, with the negative pulses blocked by diode CR5.
- (3) The regenerated half-width traffic 2 output from the collector of transistor Q5 is routed to the base of buffer transistor Q6. The emitter output of transistor Q6 is applied to the anodes of diodes CR8 and CR6.

h. Mixing Output (fig. 6-21). Diodes CR8, CR21, and CR22 comprise an OR gate. Here the traffic 2 pulses are interleaved between the pulses of the traffic 1 signal (K, fig. 2-11). This signal is applied to the base of transistor Q18. Transistors Q18 and Q19 form a differential amplifier. The output of the differential amplifier is taken from the collector of transistor Q19 and applied to the base of buffer transistor Q20. The output of transistor Q20 is taken from its emitter and applied to terminal 27 of jack J11, where the signal is designated mixed pcm traffic output.

i. Monitor Circuits (fig. 6-21). A portion of the mixed pcm traffic output is processed by a monitor circuit and brought out to terminal 26 of jack J11, where it is designated mixed pcm traffic out meter [SF(M)]. Part of the traffic 1 output is routed to terminal 28 of jack J11 through diode CR19 and resistor R60; its output is designated mixer traffic 1 meter [SF(K)]. Likewise, part of the traffic 2 output is applied to jack J11 at terminal 25 through diode CR6 and resistor R24; its output is designated mixer traffic-2 meter [SF(L)]. The third branch of the traffic 1 output of the collector of transistor Q22 is applied to the base of buffer transistor Q23. The output of transistor Q23 is taken from its emitter and applied through a monitor circuit to terminal 1 of jack J11 where the signal output is designated xmit reset timing meter [SF(N)].

2-17. Receive Signal Generator,

Panel 6A7

(fig. 6-24)

a. General. Receive signal generator, panel 6A7, operates with panel 6A4 as the receive section of the TD-204/U. Panel 6A7 receives a half-width pcm signal from panel 6A4 and converts it into two parallel full-width pcm signals. In addition, panel 6A7 receives and processes a timing train from panel 6A4.

b. Pcm Input.

- (1) In 12-channel operation, the pcm input is a binary train consisting of half-width pulses interleaved with dummy train pulses.
- (2) In 24-channel operation, the pcm input is the same as in 12-channel operation except that the input consists of two interleaved binary pulse trains. The second binary train occupies the space in the wavetrain occupied by the dummy pulses in 12-channel

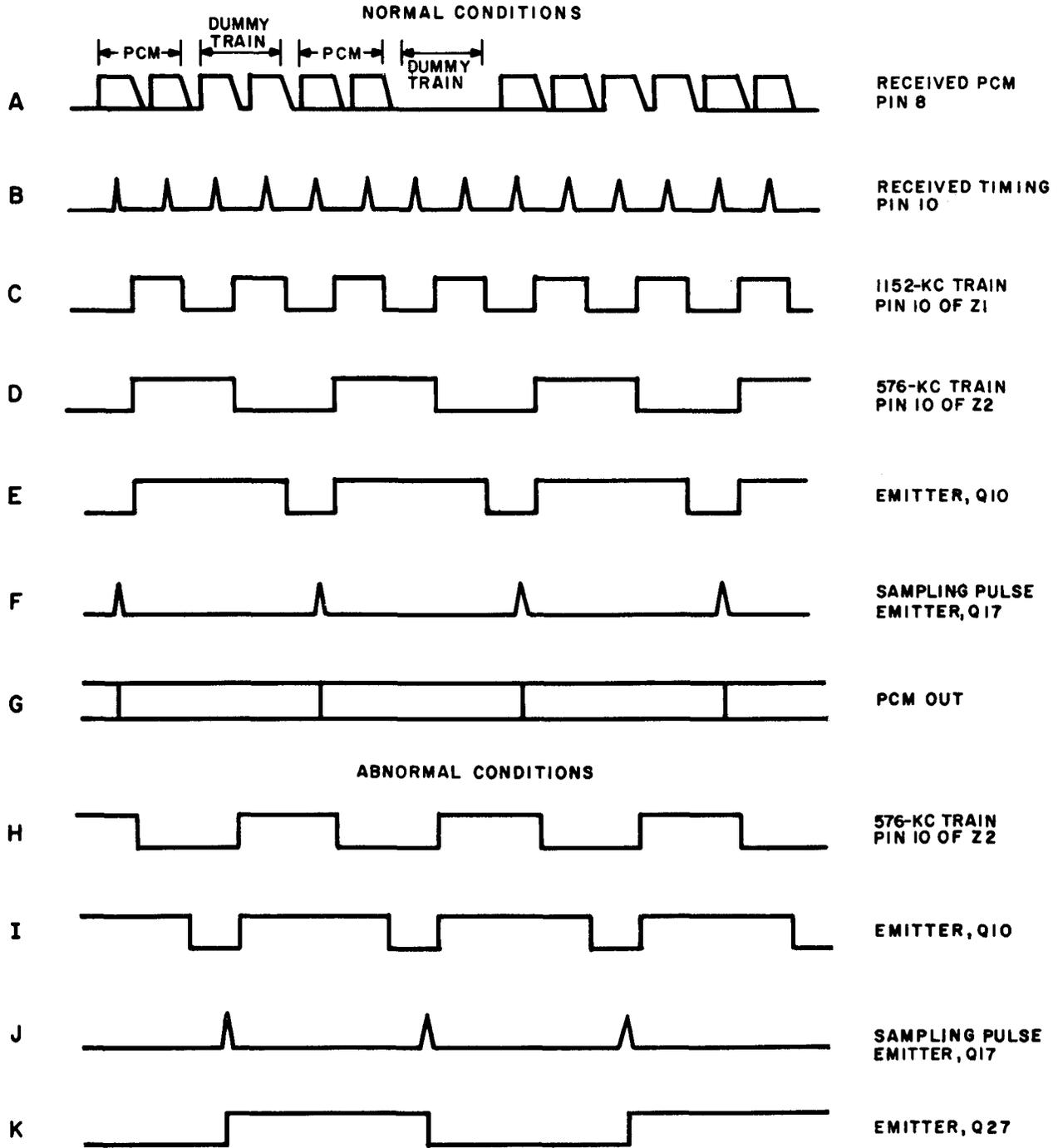
operation. If one of the binary pulse trains fails, however, the dummy train will automatically replace it.

- (3) In 48-channel AR operation, the pcm input may be either a single binary train with a dummy train, as in 12-channel operation, or two interleaved binary trains, as in 24-channel operation. The pcm input for all modes of operation is applied to terminal 8 of jack J11.

c. Sampling Pulse Generation. The received timing pulse train at a frequency of 2,304 kc is applied to terminal 10 of jack J11 from panel 6A4. From terminal 10 the pulse train is divided into three branches; one branch goes to the base of transistor Q9; another branch is applied to the base of transistor Q1 through capacitor C1; and the third goes to the base of transistor Q17 through capacitor C31.

d. Frequency Division Circuitry (fig. 6-24).

- (1) The received pcm at terminal 8 of jack J11 (A, fig. 2-12) and the received timing at terminal 10 of jack J11 (B, fig. 2-12) are adjusted in panel 6A4 so that the latter lags the former by 100 ± 10 nanoseconds. The 2,304-kc received timing is applied to the base of transistor Q9. The output of transistor Q9 passes through delay line DL1 to the base of buffer transistor Q11. The output of transistor Q11 is applied through capacitor C20 to terminals 3 and 9 of flip-flop module Z1, where the delayed received timing is divided to 1,152 kc (c, fig. 2-12).
- (2) An output of module Z1 at terminal 10 is applied to the base of buffer transistor Q13. The output of transistor Q13 is differentiated and applied to terminals 3 and 9 of flip-flop module Z2. Module Z2 operates exactly like module Z1, redividing the received timing to 576 kc (D, fig. 2-12).
- (3) The output at terminal 10 of module Z2 is applied to the anode of diode CR6. Another portion of the output of module Z1 is applied to the anode of diode CR7. Diodes CR6 and CR7 form an AND gate which gates the outputs of modules Z1 and Z2 to form the 576-kc gating pulse. The 576-kc gating pulse is formed whenever the 1,152-kc pulse train falls to a negative



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Figure 2-12. Panel 6A7, relationship between waveforms, 12-channel timing.

level while the 576-kc pulse train is at the negative level (E, fig. 2-12). This signal is applied to the base of buffer transistor Q12. The output of transistor Q12 is divided into two branches. One branch is applied through capacitor C8 to the base of transistor Q2. The other branch is applied through diode CR11 and capacitor C45 to the base of transistor Q20.

- (4) The third branch of the output of module Z1 is applied to the anode of diode CR9. Diodes CR8 and CR9 form an AND gate. The anode of diode CR8 is connected to ground through terminal 7 of jack J11 and the TRAFFIC SEL switch. This clamps the base of buffer transistor Q10 to ground, which prevents the output of module Z1 from appearing at the emitter of transistor Q10.

e. *Pcm Sampler* (fig. 6-24).

- (1) The pcm input is applied through capacitor C30 to the base of sampler transistor Q16. Transistors Q16 and Q18 form a differential amplifier.
- (2) Two other inputs are applied to the pcm sampler. One is the 2,304-kc timing pulse train applied to transistor Q17 from terminal 10 of jack J11. The other is a 576-kc gating pulse (in 12-channel operation) obtained from the collector of transistor Q20. Transistor Q20 normally conducts, inhibiting the 2,304-kc timing; it is cut off by the negative-going gating pulse which allows a sampling pulse from transistor Q17 (F, fig. 2-12) to sample the pcm.
- (3) The pcm sampler separates the digital 1 pulses from the digital 0 pulses. The timing signal for the emitters of transistors Q16 and Q18 is taken from the collector of transistor Q19.
- (4) Spike pulses representing the digital 1 pulses of the pcm appear at the collector of transistor Q18 and are applied through capacitor C33 and diode CR23 to the base of flip-flop transistor Q23. The digital 1 pulses are clamped to approximately 0 volt by diode CR20.
- (5) The digital 0 pulses appear at the collector of transistor Q16 and are applied through capacitor C34 and diode CR22 to the base

of flip-flop transistor Q21. The digital 0 pulses are also clamped to approximately 0 volt by diode CR21.

f. *Pcm Flip-Flop* (fig. 6-24).

- (1) The pcm signal is regenerated in the pcm flip-flop consisting of transistors Q21 and Q23. Dual differential amplifiers, composed of transistors Q21 and Q22, and Q23 and Q24, provide a binary output.
- (2) When a digital 1 pulse appears at the base of transistor Q23, Q23 conducts, shutting off transistor Q21. Transistor Q24 shuts off, and transistor Q22 conducts, providing a digital 1 pulse to terminal 1 of sampler flip-flop module Z4. Transistor Q24 provides a digital 0 pulse to buffer transistor Q27.
- (3) When a digital 0 pulse appears at the base of transistor Q21, it conducts and shuts off transistor Q23. Transistor Q22 shuts off and transistor Q24 conducts, furnishing a digital 1 pulse to buffer transistor Q27. Transistor Q22 provides a digital 0 pulse at terminal 1 of sampler module Z4.
- (4) The output of buffer transistor Q27 is divided into three branches. Two branches are applied to driver transistors Q25 and Q26. The third branch is applied to terminal 11 of sampler flip-flop module Z4.
- (5) The principal outputs of driver transistors Q25 and Q26 are applied to terminals 3 and 1 of jack J11. They are designated *PCM OUT-1* and *PCM OUT-2*.
- (6) A portion of each pcm output is passed through identical metering circuitry and applied to terminals 12 and 13 of jack J11. They are designated *pcm out-1 meter [SF(E)]* and *pcm out-2 meter [SF(F)]*.

g. *Phasing of 12-Channel Timing Pulses* (fig. 6-24).

- (1) In 12-channel operation, the 576-kc gating pulse at the base of transistor Q20 must be correctly phased with the received pcm signal so that the half-width pcm signals are sampled and not the interleaved dummy train. It is possible for the dummy train to be sampled if the gated timing pulses are 180° out-of-phase (H, fig. 2-12) with the 576-kc train at terminal 10 of module Z2 (D, fig. 2-12). Then the gating

- pulse (I, fig. 2-12) will form the sampling pulse which samples the dummy train instead of the pcm. Therefore, the signal at the emitter of Q27 (K, fig. 2-12) would be 180° out-of-phase with the normal pcm output.
- (2) To insure the proper phase relationship between the gating pulse and the received pcm signal, the 576-kc gating pulse is adjusted automatically to coincide with the binary pcm input. The circuits described ((3) through (7) below) shift the 576-kc gating pulse until it assumes the correct phase relationship.
 - (3) A timing pulse, gated by the 576-kc gating pulse, is applied to terminals 3 and 9 of module Z3 through capacitor C22. Module Z3 divides the pulse train to 288-kc which is applied to module Z4. Module Z4 has two other inputs: the pcm out signal from the emitter of transistor Q27 on terminal 11, and the complementary signal from the collector of transistor Q22 on terminal 1. Module Z4 produces a random output at terminal 10 as long as it continues to sample the pcm. This output is coupled through capacitor C26 to the base of transistor Q14, which conducts to inhibit blocking oscillator transistor Q15.
 - (4) However, if module Z4 samples the dummy train instead of the binary pcm, it produces a constant output at terminal 10. This constant output (dc) is blocked by capacitor C26. Transistor Q14 is biased to cut off without an input signal to its base. With transistor Q14 cut off, capacitor C29 charges in a negative direction and applies this potential through transformer T1 to the base of blocking oscillator transistor Q15. Operation of the free-running blocking oscillator is described in TM 11-690.
 - (5) Transistor Q15 conducts, applying a positive-going pulse from terminal 5 of transformer T1 through capacitor C24 to terminals 3 and 9 of module Z2. The positive pulse changes the state of module Z2, which causes a shift in the 576-kc output, and ultimately, in the 288-kc output. These positive-going pulses continue until the timing coincides with the pcm. In this condition, operation returns to that described in (3) above.
 - (6) The complement output of module Z4 is taken from terminal 4 and applied to a monitor circuit where a dc voltage is developed. This voltage is applied to terminal 9 of jack J11 where it is designated *timing activity meter [SF(S)]*.
 - (7) A branch of the collector output of transistor Q14 is applied to a monitoring circuit. A dc voltage is developed which is applied to terminal 6 of jack J11. The output is designated *osc bias meter [SF(G)]*.
- h. Output Timing* (fig. 6-24).
- (1) The third branch of the 2,304-kc timing pulse train from terminal 10 of jack J11 goes to the base of transistor Q1 through capacitor C1. Transistors Q1 and Q3 constitute a differential amplifier. Transistor Q2 normally conducts, grounding the emitters of transistors Q1 and Q3. This prevents the timing signal from appearing at the collector of transistor Q3. When the 576-kc gating pulse from the emitter of transistor Q12 is applied to the base of transistor Q2 through capacitor C8, transistor Q2 is cut off. With transistor Q2 cut off, the timing pulse appears at the collector of transistor Q3.
 - (2) The positive-going spikes of the differentiated signal are transmitted from the collector of transistor Q3 to the base of buffer transistor Q4. The output of transistor Q4 is taken from its emitter and divided into three branches. One branch is applied to driver transistor Q5 and another branch is applied to driver transistor Q6. The third branch is applied to terminals 3 and 9 of module Z3 through capacitor C22.
 - (3) The emitter output of transistor Q5 is divided into two branches. One branch is routed directly to terminal 2-3 of jack J11, where the output is designated *TIMING OUT-1*. The other branch is applied to the base of amplifier transistor Q7 through capacitor C11. The output of transistor Q7 is taken from its collector and applied through capacitor C13, clamped to ground

by diode CR1, peak-detected by diode CR2, with a positive charge stored in capacitor C14. The dc voltage stored in capacitor C14 is divided into two branches. One branch is applied to terminal 24 of jack J11 through resistor R13; its output is designated 48 chan *timing-1 meter [SF(C)]*. The other branch is applied to terminal 25 of jack J11 through resistor R14; its output is designated 12 & 24 chan *timing-1 meter [SF(C)]*.

- (4) The emitter output of transistor Q6 is also divided into two branches. One branch is fed to terminal 19 of jack J11, where its output is designated *TIMING OUT-2*. The other branch is processed by identical circuitry to that described in (3) above. Its outputs are designated 48 chan *timing-2 meter [SF(D)]* at terminal 14 of jack J11 and 12& 24 chan *timing-2 meter [SF(D)]* at terminal 15 of jack J11.

i. 24-Channel Operation (fig. 6-24).

- (1) Panel 6A7 operates in the same way in the 24-channel mode as it does in the 12-channel mode, except that the received pcm is sampled at a 1,152-kc rate. The received pcm consists of two interleaved 12-channel binary pulse trains.
- (2) With the TRAFFIC SEL switch at 24, the anode of diode CR8 is not grounded; this allows the 1,152-kc output of module Z1 to appear at the emitter of transistor Q10. The 576-kc gating pulse is in phase with the negative excursions of the 1,152-kc signal at the emitter of transistor Q10; therefore, it has no effect on the 1,152-kc signal.

- (3) The output of transistor Q10 is coupled through capacitor C45 to the base of transistor Q20 (*d(3)*, above). Transistor Q20 gates the received timing to the pcm sampler. Diode CR11 prevents the 1,152-kc signal at the emitter of transistor Q10 from appearing at the emitter of transistor Q12. Therefore, the 576-kc gating pulse is routed to the base of transistor Q2; the output timing is a 576-kc pulse train.
- (4) Since there is no dummy train, module Z4 constantly samples pcm, providing a continuing random signal at terminal 10. Transistor Q14 remains conducting, and transistor Q15 remains cut off.

j. 48-Channel Operation (fig. 6-24).

- (1) Panel 6A7 operates the same in the 48-channel mode as it does in the 12-channel mode, except that the received pcm is sampled at a frequency of 2,304 kc. The received pcm consists of 48-channel binary pcm. The timing output signal consists of a 2,304-kc pulse train.
- (2) With the TRAFFIC SEL switch at 48-AR, a — 3-volt potential is applied to the bases of transistors Q2 and Q20, through diodes CR30 and CR29. This potential cuts off transistors Q2 and Q20, allowing each pulse of the 2,304-kc pulse train to sample the pcm and to appear at the collector of transistor Q3. The —3-volt potential is also applied to the emitters of transistors Q10 and Q12, through diodes CR10 and CR5. This —3-volt signal inhibits output signals at the emitters of transistors Q10 and Q12 which might damage the transistors.

2-18. Circuit for Locating Faulty TD-206/G

a. General. The TD-204/G incorporates a circuit that permits locating a defective Restorer, Pulse Form TD-206/G in the transmission cable linking the local with the distant TD-204/U. Each TD-206/G contains a signal detector that *senses* whether a pulse train is available at the output of the TD-206/G and inserts a 105-ohm resistor in series with the transmission cable when no pulse train is detected. If a faulty signal-restoring circuit in a TD-206/G interrupts the pulse train, 105-ohm resistors are inserted in the transmission cable by the signal detector of that and all subsequent TD-206/G's, while no resistors are inserted in the TD-206/G's preceding the fault. The fault-locating circuit of the TD-204/U makes use of the action of the signal detectors to locate a defective TD-206/G. The fault-locating circuit first calibrates the total resistance to be expected if none of the TD-206/G's are working in the transmission cable link at a particular installation. This calibration, called zero setting, is accomplished by interrupting the pulse train at the TD-204/U, thereby forcing the signal detector circuit of all the TD-206/G's to insert a 105-ohm resistor in series with the transmission cable link, and by the ZERO SET control, calibrating the TEST ALIGN meter to indicate at the zero set mark inscribed on the meter face plate. The details of zero set circuit operation are described in *b* below. After calibration, the fault-locating circuit is switched to the read function, during which a test pulse train is applied to the transmission cable. The signal detector circuit of all TD-206/G's preceding the defective TD-206/G will remove the series 105-ohm resistor that was inserted in the transmission cable during calibration, causing the TEST ALIGN meter indication to move from the zero set mark. To locate the faulty TD-206/G, the TEST ALIGN meter indication is brought back to the zero mark by inserting precision resistors in series with the transmission cable at the TD-204/U. The total resistance required to return the meter indication to the mark provides a measurement of how far down the transmission cable the first defective TD-

206/G is located. The details of read circuit operation are given in *c* below.

b. Zero Set Circuit Operation.

- (1) *Cable current circuit.* For zero set circuit operation, switch S10 is set to the ZERO SET position. Dc cable current supplied by power supply panel 6A1 is applied through terminal 9 of jack J12, contacts 2 and 4 of switch S10, terminal 1 of jacks J17 and A5J10, terminal 3 of jacks A5J10 and J17, and TO CABLE jack J9, to the transmission cable. The cable current passes through the cable and the TD-206/G's inserted at 1-mile intervals in the cable, to FROM CABLE jack J10 of the distant TD-204/U. At the distant TD-204/U, the cable current flows through terminal 3 of jacks J14 and A2J10 and resistor A2R41 to ground. The current returns to the local TD-204/U through the transmission cable shield. With switch S10 set to ZERO SET, no *mux timing* pulse train is applied to the pcm transmit generating circuits on panel 6A5, and as a result, no *dummy pulse train* is available to be applied to the transmission cable from the output of the pcm transmit generating circuits through TO CABLE jack J9. With no *dummy pulse train* applied to the transmission cable, the signal detectors in all the TD-206/G's of the cable, failing to sense a pulse train, will switch their associated resistor R16 in series with the transmission cable. With a constant dc cable current supplied by power supply panel 6A1, the maximum IR (current times resistance) drop that can be developed at that installation by the transmission cable is established as the reference for zero setting the meter preparatory to the read function.
- (2) *Meter circuit.* The meter circuit, consisting of resistors R2, A1R34, A1R35, A1R36, A1R37, A8R3, break-

down diodes A8VR6 and A1VR5, transistor A1Q14, switches S1 and S7, and meter MI, is connected across the output of power supply panel 6A1. The current drawn from power supply panel 6A1 for a given transmission cable IR drop by the metering circuit is largely determined by series resistors A1R36 and A1R37, since these resistors are much larger than the resistance of the parallel combination of meter MI and transistor A1Q14. The current drawn by the meter circuit divides between constant current transistor A1Q14 and TEST ALIGN meter MI. Breakdown diode A8VR6 and resistor A8R3 provide a constant voltage for biasing transistor A1Q14, the actual bias being developed across resistor A1R34 and a portion of ZERO SET resistor R2. ZERO SET resistor R2 is adjusted so that transistor A1Q14 draws off a sufficient portion of the total current through resistors A1R36 and A1R37 to make 50 microampere flow through TEST ALIGN meter MI, causing the meter to indicate at the ZERO SET ' mark. Breakdown diode A1VR5 protects the meter and transistor A1Q14 by preventing excessive voltage from developing across them. The current drawn by transistor A1Q14 is determined primarily by the bias established when ZERO SET resistor R2 is adjusted, and this current is unaffected by any changes in the output voltage of power supply panel 6A1. As a result, the effective sensitivity of the meter to voltage changes is increased, since the entire change in current resulting from a voltage change flows through TEST ALIGN meter MI, not merely a fraction of the change in the same proportion as the ratio of the currents in the two parallel branches.

c. Read Circuit Operation.

- (1) The read circuit operation differs

from the zero set circuit operation (*b* above) in that the SYSTEM FAULT LOCATOR switches are in series with the dc cable current circuit and the 2,304-kc pulse train from terminal 19 of jack A7J11 is applied to the pcm transmit generating circuits. With switch S10 set to READ, contacts 1 and 4 open the short circuit placed across the SYSTEM FAULT LOCATOR switches in the NORM OPR and ZERO SET positions of S10. The 2,304-kc pulse train is applied through contacts 8 and 11 of switch S10 and terminal 31 of jacks J17 and A5J10 to provide the *mux timing in* signal required to enable the pcm transmit generating circuits on panel 6A5. When TRAFFIC SEL switch S8 is set to 48 AR, the *xmit pcm* signal input to the pcm transmit generating circuits (applied through terminal 15 of jacks J17 and A5J10) consists of a 1,152-kc square wave routed through contacts 6 and 7 of switch S8A. When TRAFFIC SEL switch S8 is set to either the 12 or 24 position, the *xmut pcm* signal input to the pcm transmit generating circuits consists of a 288-kc square wave routed through contacts 7 and 4 or 7 and 5 of switch S8A (shown inset in lower right portion of fig. 6-30). With both a *mux timing in* signal and an *xmit pcm* signal applied, the pcm transmit generating circuits superimpose a *dummy pulse train* on the dc transmission cable current.

- (2) The *dummy pulse train* is propagated down the transmission cable until the signal reaches an inoperative pulse form restorer (TD-206/G). A signal will be detected by the signal detector of all operative TD-206/G's passing the *dummy pulse train* in, with the result that 105-ohm resistor R16 will be short-circuited for these TD-206/G's. The corresponding resistor of the inoperative TD-206/G and of all subsequent TD-206/G's in the trans-

mission cable will not be short-circuited, since the signal detector of these units will fail to detect the *dummy pulse train*. With a constant dc current maintained through the cable by power supply panel 6A1, the IR drop is proportional to the total resistance of the transmission cable circuit. During read circuit operation, this resistance includes the resistors inserted by the SYSTEM FAULT LOCATOR switches. With the 105-ohm resistors of the operative TD-206/G's short-circuited, the resistance of the cable link will be less than it was during zero set circuit operation. The deficiency is made up by manually inserting an equal resistance using SYSTEM FAULT LOCATOR switches S3 and S9A. These switches are operated so that the TEST ALGIN meter indication

again falls on the zero set mark, at which point the total IR drop through the transmission cable circuit is equal to the IR drop during zero set operation.

- (3) With the TD-206/G's inserted in the cable at 1-mile intervals, switch S9A, marked in unit miles, inserts a 104-ohm resistor for each advance in the switch setting, while switch S3, marked in tens of miles, inserts a 1,040-ohm resistor for each advance. The 1-ohm difference between the resistor value inserted by the SYSTEM FAULT LOCATOR switches and the short-circuited 105-ohm series resistor in the TD-206/G for which it is substituted in the transmission cable circuit is caused by the allowance made for the 1-ohm resistance presented by turned-on signal detector transistor Q6 in the TD-206/G.

CHAPTER 3

DIRECT SUPPORT MAINTENANCE

Caution: Do not attempt resistance measurements of the panel transistorized circuits unless specifically directed in this manual.

3-1. General Instructions

a. Troubleshooting at the direct support maintenance category is limited to localizing trouble to the chassis or to the parts mounted on the front panel (for example, switches, fuseholders, and relays) and to repairing defective parts.

b. Voltage, resistance, or continuity measurements may be performed to localize the trouble to a component mounted on either the chassis or the front panel. If the defective part is inaccessible and cannot be repaired or replaced, the chassis should be tagged and sent to a higher maintenance category.

3-2. Test Equipment and Tools Required

All the test equipment and tools required for repair and for replacement of parts mounted on the chassis or front panels are listed in the maintenance allocation chart in appendix C, TM 11-5805-367-12.

3-3. Adjustments

Direct support adjustments are limited to PA potentiometer R12 on panel 6A4 and TTL potentiometer R53 on panel 6A2. Whenever instructions direct adjustment of either control, proceed to the applicable paragraph (*a* or *b* below).

a. *PA Potentiometer R12, Panel 6A4* (fig. 3-1). This adjustment sets the phase of the received timing signal relative to the associated pcm signal. Make the adjustment as follows:

- (1) Set the AC POWER switch to OFF.

- (1,1) Connect TD-352/U to TD-204/U.
- (2) Remove panel 6A4 from connector J16.
- (3) Remove the extender panel from its storage position, and plug it into connector J16.
- (4) Connect panel 6A4 to the extender panel.
- (5) Connect Oscilloscope AN/USM-140 to the extender panel as shown in figure 3-1.
- (5.1) Utilize SCOPE SYNC from TD-352/U. Connect to EXT. TRG INPUT.
- (6) Set the AC POWER switch to ON.
- (7) Adjust PA potentiometer R12 until pulses in the pcm waveform at pin 19 of panel 6A4 lead pulses in the timing waveform at pin 25 of panel 6A4 by 100 nanoseconds, as shown in the idealized waveform of figure 3-1.
- (8) Set the AC POWER switch to OFF.
- (9) Disconnect the AN/USM-140 from the extender panel and the TD-204/U front panel.
- (10) Remove panel 6A4 from the extender panel.
- (11) Remove the extender panel from connector J16, and replace it in its storage position.
- (12) Reconnect panel 6A4 to connector J16.
- (13) Set the AC POWER switch to ON.

b. *TTL Potentiometer R53, Panel 6A2.* This control is used to set the level of the test tone signal output. Make the adjustment as follows:

- (1) Set the AC POWER switch to OFF.

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- (2) Remove panel 6A2 from connector J14.
- (3) Remove the extender panel from its storage position, and plug it into connector J14.
- (4) Connect panel 6A2 to extender panel.
- (5) Set the panel 6A2 TONE-OFF switch to TONE.
- (6) On the TD-204/U front panel, disconnect the cables from the PATCH THRU and FROM CABLE jacks.
- (7) Connect the INPUT terminals of Voltmeter, Electronic ME-30B/U between pin jack J9 on panel 6A2 and ground.
- (8) Set the AC POWER switch to ON.
- (9) Adjust TTL potentiometer R53 for a 10-millivolt indication on the ME-30B/U.
- (10) Set the AC POWER switch to OFF.
- (11) Disconnect the ME-30B/U from panel 6A2 and ground.
- (12) Reconnect the cables to the TD-204/U PATCH THRU and FROM CABLE jacks.
- (13) Set the panel 6A2 TONE-OFF switch to OFF.
- (14) Remove panel 6A2 from the extender panel.
- (15) Remove the extender panel from connector J14, and replace it in its storage position.
- (16) Reconnect panel 6A2 to connector J14.
- (17) Set the AC POWER switch to ON.

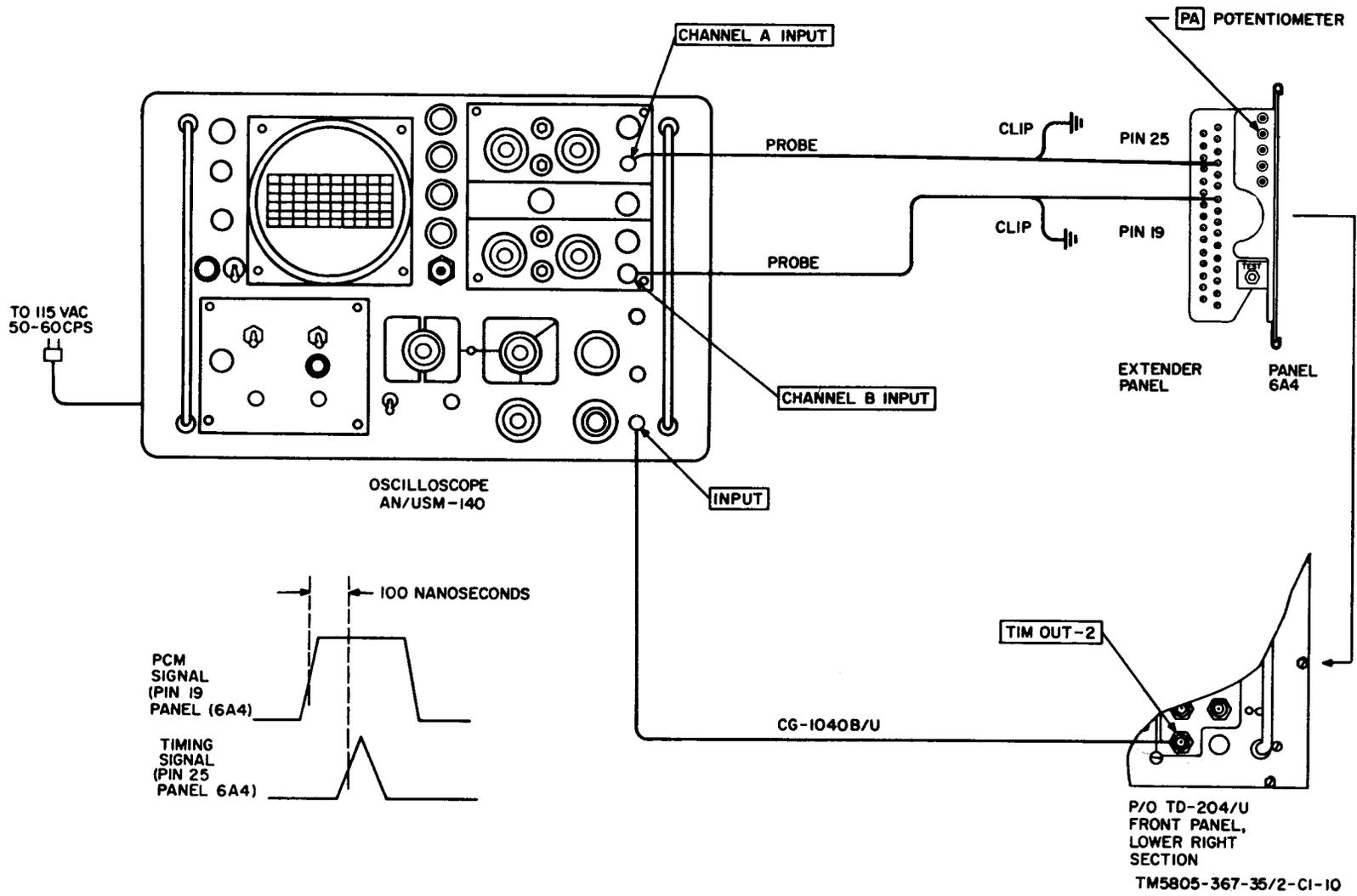


Figure 3-1. Panel 6A4 PA control, adjustment test setup.

CHAPTER 4

GENERAL SUPPORT MAINTENANCE

Warning: When troubleshooting or repairing this equipment, be careful not to come in contact with the 115-volt ac circuits. Use insulated test probes for voltage measurements. Always disconnect the power before touching any of the internal parts.

4-1. General Instructions

a. These general support maintenance procedures are not complete as outlined but supplement those described for organizational maintenance (TM 11-5805-367-12). Troubleshooting at this maintenance category includes all the techniques specified for organizational and direct support maintenance. The systematic troubleshooting procedures, which begin with the operational and sectionalization checks performed at organizational maintenance, must be completed by further localizing and isolating techniques performed at the general support maintenance category.

b. Some troubleshooting procedures may be done either while the equipment is operating as part of a system, or, if necessary, after the TD-204/U (or part of it) has been removed from system operation. When trouble occurs, certain observations and measurements can be made which may determine whether a plug-in panel or a chassis is at fault.

c. Usually, organizational troubleshooting is performed while the equipment is operating as part of a system (TM 11-5805-367-12). Troubleshooting at general support level is usually done with the defective equipment removed from the system. Paragraphs 4-2 through 4-6 contain general information for troubleshooting. Any trouble should be corrected as quickly as possible.

4-2. Organization of Troubleshooting Procedures

a. General. The first procedure in servicing a defective TD-204/U is to sectionalize the fault. Sectionalization means tracing the fault to plug-in panels or subassemblies responsible for the trouble. Refer to TM 11-5805-367-12 for sectionalization procedures in the TD-204/U. The second procedure is to localize the fault. Localization means tracing the fault to the defective stage. The third procedure, isolation, means tracing the fault to the defective part. Some faults, such as burned-out

resistors, can often be detected by sight, smell, or hearing. The majority of faults, however, will have to be located by checking waveforms and voltages.

b. Sectionalization. If the trouble has not been sectionalized, perform the operator's and organizational preventive maintenance checks given in chapter 5 of TM 11-5805-367-12.

c. Localization. Procedures are outlined in the troubleshooting charts (paras. 4-6 through 4-13) for localizing troubles to a defective stage or part located on a panel. Begin with item 1 of the troubleshooting chart, and proceed step-by-step until a symptom of trouble appears. When trouble has been localized to a particular stage, use waveform and voltage measurements to isolate the trouble to a particular part, and then replace the part.

Note. The corrective measures columns in the troubleshooting charts do not indicate the possibility of defective wiring. When the specified measures do not correct the trouble, the wiring should be checked, and any necessary repairs made.

d. Isolation.

- (1) Use resistor and capacitor color codes (figs. 6-7 and 6-8) to find component values. Compare the waveforms and voltages with the readings taken.
- (2) In all tests, do not overlook the possibility of intermittent troubles. This type of fault may often be located by tapping or jarring the equipment while in operation. Similarly, wiring and connections to the equipment should also be checked (figs. 6-26 and 6-27).

4-3. Troubleshooting Charts

To isolate a fault in a panel, first couple the panel to a panel extender, and insert it in an operable TD-204/U. Then proceed to isolate the fault to the specific component. Repair personnel should read and understand the theory of panel

operation before attempting repairs. The following troubleshooting charts may be used as a guide. Strict adherence to the procedures set forth in these charts is not mandatory except for sequence; correct sequence is essential, since each step implies that the circuits involved in previous steps are operating correctly. Where chart instructions recommend checking a component such as a transistor, it is assumed that the components or stages associated with the component are also to be checked. When a faulty component has been repaired or replaced, repeat the chart procedures to verify that no new faults have developed as a result of repairing the original fault. The troubleshooting procedures assume that all inputs required for a panel actually enter the panel. It is further assumed that all connections are in order and that solder joints are free of defects. It is uncommon for more than one fault to occur in a panel simultaneously. If, for example, it is suspected that more than one component (such as a flip-flop) of a panel is faulty, the dc voltage supplies should be checked before going further. This suggestion also applies where a series of stages fails. Avoid indiscriminate replacement of components in efforts to locate a fault. Such practice not only may impair the panel, but increases the risk of making incorrect connections. Despite the additional expenditure of time, repair personnel should exhaust all test methods available to verify that the suspected component actually is the faulty one. Only when repair personnel are reasonably convinced that the suspected component is defective should it be replaced. Remember, also, that component replacement (or making a repair) may necessitate one or more adjustments. Therefore, whenever replacements, repairs, or adjustments are made, operation of the entire unit should be checked.

4-4. Maintenance Illustrations

Illustrations are provided to help locate faults. Block diagrams present electrical interrelationships

of the stages in the TD-204/U. Individual panel schematic diagrams and complete unit interconnecting wiring diagrams, plus the module schematic diagrams, not only help locate faults, but also identify all component parts by reference designations and values. Locations of individual component parts on the panels are shown on top panel views (fig. 6-28 and 6-29) .

4-5. Test Equipment, Tools, and Materials Required

The following test equipment, tools, and materials should be provided for troubleshooting the TD-204/U:

a. Test Equipment.

- (1) Attenuator TS-402/U.
- (2) Frequency Meter AN/TSM-16.
- (3) Multimeter TS-352/U.
- (4) Multimeter ME-87/U.
- (5) Multiplexer TD-353/U.
- (6) Multiplexer TD-352/U.
- (7) Oscilloscope AN/USM-140 or equivalent.
- (8) Signal Generator SG-15/PCM.
- (9) Test Set TS-140/PCM.
- (10) Test Set, Transistor TS-1836/U.
- (11) Transmission Test Set TS-762/U.
- (12) Voltmeter, Meter ME-30/U or equivalent.

b. Tools.

- (1) Screwdriver (mounted in TD-204/U).
- (2) Tool Equipment TE-123.
- (3) Tool Kit, Electronic TK-105.

c. Materials.

- (1) Potentiometer, 1000 ohms, 5 watts.
- (2) Cable, Special Purpose, Electrical CX-4245/G, 1/4-mile reel.
- (3) Cable Assembly, Radio Frequency CG-2437/TCC.
- (4) Cable Assembly, Radio Frequency CG-2438/TCC.
- (5) Cable Assembly, Radio Frequency, CG-1040B/U.
- (6) Resistor, 1000 ohms, 5 watts.
- (7) Resistor, 270 ohms, 5 watts.

4-6. Panel 6A1, Troubleshooting
(figs. 6-10 through 6-12).

a. Troubleshooting Chart.

Item No.	Symptom	Probable trouble	Correction
<p>Warning: Up to 1100 volts are developed by panel 6A1. Before making dc resistance measurements, insure that primary power is removed.</p> <p><i>Note.</i> Prior to troubleshooting the panel, it is assumed that fuse replacement has been tried, with no corrective results.</p>			
1	Incorrect voltage at +10V jack J2; F1 keeps blowing.	Q1, Q2, Q3, or R1 defective	Check voltage at E3 (-18 ± 1.8 volts dc). If voltage is incorrect, proceed to item 2. If voltage correct, check Q1, Q2, Q3, and R1.
2	Incorrect voltage at E3	LIC defective	Check voltage at E7 (-18 ± 1.8 volts dc). If voltage is incorrect, proceed to item 3. If voltage correct, check LIC for resistance (<i>b</i> below).
3	Incorrect voltage at E7	CR1 or CR2 defective	Check voltage at E5 and E8 (12 ± 1.2 volts ac). If voltage is incorrect, proceed to item 4. If voltage correct, check CR1 and CR2.
4	Incorrect voltage at E5 and E8	Secondary of T1 defective	Check terminals 12, 13, and 14 of T1 for correct resistance (<i>b</i> below).
5	Incorrect voltage at all power supply outputs with all fuses intact.	Primary of T1 defective	Check terminals 1 and 2 of T1 for correct resistance (<i>b</i> below).
6	F1 fails to blow when terminals 13 and 19 are shorted together.	F1 or fuse holder defective	Check F1 for continuity and exact value, check its fuseholder for foreign material lodged on its contacts.
7	Improper voltage regulation at +10V jack J2 when input voltage varies from 109 to 121 volts ac.	VR1 defective	Check VR1 for breakdown voltage of 6.2 volts. If defective, replace; if not defective, proceed to item 8.
8	Improper voltage regulation at +10V jack J2 when input voltage varies from 109 to 121 volts ac; VR1 not defective.	Q2 or Q3 defective	Check base of Q1 for correct voltage (<i>c</i> below). If voltage incorrect, proceed to item 9. If voltage correct, check voltage at bases of Q2 and Q3. If voltage unequal, troubleshoot Q2 and Q3. If voltages equal (R1 adjusted), proceed to item 9.
9	Incorrect voltage at base of Q1; equal voltages at bases of Q2 and Q3 (R1 adjusted).	Q1 or R1 defective	Check Q1 and R1.
10	High output ripple at +10V jack J2.	C1, C2, LIC, CR1, CR2, C4 or C5 defective.	Check C1, C2, LIC, CR1, CR2, C4, and C5.
11	Incorrect voltage at -10V jack J3; F2 keeps blowing.	Q4, Q5, Q6, or R7 defective	Check voltage at E14 (-17.5 ± 1.8 volts dc). If voltage is incorrect, proceed to item 12. If voltage correct, check Q4, Q5, Q6, and R7.
12	Incorrect voltage at E14	L1B defective	Check voltage at E17 (-17.5 ± 1.8 volts dc). If voltage is incorrect, proceed to item 13. If voltage correct, check resistance of L1B (<i>b</i> below).

Item No.	Symptom	Probable trouble	Correction
13	Incorrect voltage at E17	CR3 or CR4 defective	Check voltage at E15 and E18 (12 ± 1.2 volts ac rms). If voltage is incorrect, proceed to item 14. If voltage correct, check CR3 and CR4.
14	Incorrect voltage at E15 and E18 ..	Secondary of T1 defective	Check terminals 9, 10, and 11 of T1 for correct resistance (<i>b</i> below).
15	F2 fails to blow when terminals 14 and 19 are shorted together.	F2 or fuse holder defective	Check F2 for continuity and exact value; check its fuse holder for foreign material lodged on its contacts.
16	Improper voltage regulation at -10V jack J3 when input voltage varies from 109 to 121 volts ac.	VR2 defective	Check VR2 for breakdown voltage of 6.2 volts. If defective, replace. If not defective, proceed to item 17.
17	Improper voltage regulation at -10V jack J3 when input voltage varies from 109 to 121 volts ac; VR2 not defective.	Q5 or Q6 defective	Check base of Q4 for correct voltage (<i>b</i> below). If voltage incorrect, proceed to item 18. If voltage correct, check voltage at bases of Q5 and Q6. If voltage unequal, troubleshoot Q5 and Q6. If voltages equal (R7 adjusted), proceed to item 18.
18	Incorrect voltage at base of Q4; equal voltage at bases of Q5 and Q6 (R7 adjusted).	Q4 or R7 defective	Check Q4 and R7.
19	High output ripple at -10V jack J3.	C6, C7, L1B, CR3, CR4, C9, or C10 defective.	Check C6, C7, L1B, CR3, CR4, C9, and C10.
20	Incorrect voltage across J4 and J5; fuse F3 keeps blowing.	Q8, Q7, Q9, Q10, Q11, Q12, Q13, R15, or R26 defective.	Check voltage at terminal 2 of L1A (-16 ± 1.6 volts dc). If correct, check Q8, Q7, Q9, Q10, Q11, Q12, Q13, R15 and R26. If incorrect, proceed to item 21.
21	Incorrect voltage at terminal 2 of L1A or E25.	L1A defective	Check voltage at terminal 1 of L1A (-16 ± 1.6 volts dc). If correct, check L1A. If incorrect, proceed to item 22.
22	Incorrect voltage at terminal 1 of L1A.	CR5, CR6, or T1 defective	Check voltage at terminals 6 and 8 of T1 (11 ± 1.1 volts ac rms). If correct, check CR5 and CR6. If incorrect, check resistance at terminals 6, 7, and 8 of T1.
23	F3 fails to blow when terminals 15 and 19 or 20 and 19 are shorted together.	F3 or its fuse holder defective	Check F3 for continuity and exact value; check its fuseholder for foreign material lodged on its contacts.
24	+6 volts measured between J4 and J5, but outputs not balanced.	R26 defective	Check voltage at E33 (0 ± 0.2 volts dc). If voltage not correct, check R26. If voltage is correct proceed to item 29.
25	Incorrect voltage regulation at -3V jack J4 when input voltage varies from 109 to 121 volts ac.	VR3 defective	Check VR3 for breakdown voltage of 6.2 volts. If defective, replace. If not defective, proceed to item 26.

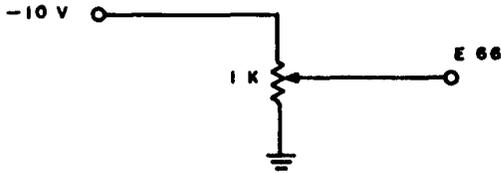
Item No.	Symptom	Probable trouble	Correction
26	Incorrect voltage regulation at -3V jack J4 when input voltage varies from 109 to 121 volts ac; VR3 not defective.	Q9 or Q10 defective	Check base of Q8 for correct voltage (<i>e</i> below). If voltage incorrect, proceed to item 27. If voltage correct, check voltage at bases of Q9 and Q10. If voltage unequal, troubleshoot Q9 and Q10. If voltages equal (R15 adjusted) proceed to item 27.
27	Incorrect voltage at base of Q8; equal voltage at bases of Q9 and Q10 (R15 adjusted).	Q7, Q8 or R15 defective	Check Q7, Q8, and R15.
28	Incorrect voltage regulation at +3V jack J5 when input voltage varies from 109 to 121 volts ac.	R26 defective	Check voltage at E33 (0 ± 0.2 volts dc). If voltage not correct, check R26. If voltage correct, proceed to item 29.
29	Correct voltage at E33 but incorrect voltage regulation or incorrect voltage balance.	Q13 defective	Check voltage at E40 ($+2 \pm 0.2$ volts dc). If voltage not correct, proceed to item 30. If voltage correct, check Q13.
30	Incorrect voltage at E40	Q11 or Q12 defective	Check Q11 and Q12.
31	High output ripple at -3V jack J4 and $\pm 3V$ jack J5.	L1A, CR5, CR6, T1, or C11 defective.	Check L1A, CR5, CR6, T1, and C11.
32	Incorrect voltage at -17VDC jack J6; fuse F4 keeps blowing.	VR4 defective	Check voltage at terminal 2 of L2 ($+20 \pm 4$ volts dc). If correct, check VR4. If incorrect proceed to item 33.
33	Incorrect voltage at terminal 2 of L2.	L2 defective	Check voltage at terminal 1 of L2 ($+20 \pm 4$ volts dc). If not correct, proceed to item 34. If voltage correct, check L2 (<i>b</i> below).
34	Incorrect voltage at terminal 1 of L2.	CR7, CR8, or T1 defective	Check voltage at terminals 3 and 4 of T1 (28 ± 3 volts ac rms). If voltage present, check CR7 and CR8. If voltage not present, check T1.
35	Incorrect voltage at -28VDC jack J7.	Same as items 33 and 34 above	Same as items 33 and 34 above.
36	High ripple at -28VDC jack J7	C16, C17, L2, CR7, CR8, or T1 defective.	Check C16 and C17. If not defective, repeat items 33 and 34 above.
37	Incorrect voltage at 28VAC jack J8.	T1 defective	Check terminals 15 and 17 of T1 (<i>b</i> below).
38	Incorrect negative dc voltage at terminal 21.	CR9 defective	Check CR9.
39	Incorrect output between terminals 9 and 19.	Dc cable current control circuits	Follow procedures in items 40 through 62 below.
<p><i>Note 1.</i> Check starting circuit and royer circuit prior to continuing into the regulator section.</p> <p><i>Note 2.</i> A single-sweep oscilloscope presentation is the most effective method for viewing the transient waveforms after operation of the CABLE POWER switch to ON.</p>			
40	No sawtooth waveform at emitter of Q26.	Q26 defective	Check for square wave signal at terminal 10 of T3. If signal present, check Q26. If absent, proceed to item 41.
41	No output at terminal 10 of T3	T3, Q19, or Q20 defective	Check for square wave at collectors of Q19 and Q20. If signal is present, check winding of terminals 10 and 11. If absent,

Item No.	Symptom	Probable trouble	Correction
42	No -28 volts applied to terminal 2 of T2 upon operation of CABLE POWER switch to ON.	K3 defective	check Q19, Q20 and pins 1 through 6 of T3. Check voltage at collector of Q15. Voltage should step from -10 volts dc to 0 volt dc, and, after approximately 1 second, return to -10 volts dc. If correct, check K3. If incorrect, proceed to item 43.
43	Collector voltage at Q15 incorrect ..	Q15 defective	Check voltage at base of Q15. Normally, it should be slightly positive ($\approx +0.5$ volts dc). When CABLE POWER switch is set to ON, it should go to ≈ -0.3 volt dc and hold there for approximately 1 second. After that time, it should return to positive voltage. If correct, check Q15. If incorrect, proceed to item 44.
44	Incorrect signal at base of Q15	CR15, CR14, or VR6 defective	Check signal at cathode of CR14. The signal should start at 0 volt dc and go to -17 volts dc with a 1-second time constant, when the switch is operated. If waveform is correct, check CR15. If incorrect, check CR14 and VR6.
<p><i>Note 3.</i> If there is no output current upon operation of CABLE POWER switch, proceed to item 45. All measurements are to be made within 1 second of operating CABLE POWER switch to ON.</p> <p><i>Note 4.</i> If cable current is generated with operation of CABLE POWER switch, but is removed after approximately 1 second, proceed to item 56.</p> <p><i>Note 5.</i> If cable current is generated with operation of CABLE POWER switch and remains, but is incorrect in value and cannot be adjusted to the correct value, proceed to item 58.</p> <p><i>Note 6.</i> For maximum safety, terminate the cable bnc connector with a 1,000-ohm (5 w) resistor to ground.</p>			
45	No cable current output at terminal 9 when CABLE POWER switch is set to ON.	L4, L3 defective	Check for voltage at E57 (+60 ± 6 volts dc). If present, check for continuity in L4 and L3 and associated wiring. If missing, proceed to item 46.
46	No voltage at E57 CABLE POWER switch is set to ON.	R54, R47, or coil of K4 defective ..	Check for voltage at E58 (-8 ± 0.8 volts dc). If present, check for continuity from this point to ground through R54, R47, and coil of K4. If no signal, proceed to item 47.
47	No signal at E58 or E57 when CABLE POWER switch is set to ON.	CR10, CR11, CR12, and CR13 defective.	Check for high voltage signal between E52 and E53 upon operation of CABLE POWER switch. If present, check CR10, CR11, CR12, and CR13. If missing, proceed to item 48.
48	No output at secondary of T2 when CABLE POWER switch is set to ON.	T2 defective	With CABLE POWER switch at ON, check for square wave at collector of Q16 and Q17. If correct, recheck T2. If incorrect, proceed to item 49.
<p><i>Note 7.</i> Items 49 through 54 are performed with CABLE POWER switch at OFF, unless otherwise indicated.</p>			

Item No.	Symptom	Probable trouble	Correction
49	No square wave signals at collectors of Q16 and Q17.	Q16 or Q17 defective	Check waveform at E74 with CABLE POWER switch at OFF and AC POWER switch at ON. Waveform should be approximately 0 volt dc. If 0 volt dc, check waveform at base of Q16 and Q17; it should be a square wave, with negative portions clamped to -0.5 volt dc. If not, check T3 secondary terminals 7, 8, and 9. If correct, check Q16 and Q17. If voltage at E74 is +3 volts dc, proceed to item 50.
50	Voltage at E74 is +3 volts	Q21 or Q22 defective	Check voltage at collector of Q23; it should be 0 volt dc. If correct, check Q21 and Q22. If incorrect, proceed to item 51.
51	Voltage at collector of Q23 is +3 volts.	Q23 or Q24 defective	Check voltage at base of Q24; it should be more negative than -6 volts dc. If correct, check Q23 and Q24. If incorrect, proceed to item 52.
52	Voltage at base of Q24 incorrect	Q25 defective	Check voltage at collector of Q27; it should be more positive than 0 volt dc (+4 volts dc). If correct, check Q25. If incorrect, proceed to item 53.
53	Voltage at collector of Q27 incorrect.	Q27 defective	Compare voltage at base of Q27 with that of the emitter. The base should be more negative. If correct, check Q27. If incorrect, proceed to item 54.
54	Voltage at emitter of Q27 incorrect.	Q18, VR7, VR8, or CR17 defective	Check signal at base of Q18; it should be more negative than the emitter. If correct, check VR7, VR8, and CR17. If incorrect, check Q18.
55	Voltage at base of Q27 incorrect	Q28, Q29, or VR9 defective	Check signal at collector of Q28; it should be -6 volts dc. If correct, check Q29 and continuity to ground through R53, R47, and R54. If incorrect, check Q28, Q29, VR9, and continuity to ground through R53, R47, and R54.
56	Cable power starts, but drops out after approximately 1 second.	K4 or CR16 defective	Check for operation of K4 by checking voltage at terminal 2 of K4 or cathode of CR16. It should be -28 volts dc upon closing contact (prior to release of starting relay). If incorrect, check K4. If correct, check CR16 with ohmmeter. If CR16 is not defective, proceed to item 57.
57	Cable power starts, but drops out after approximately 1 second.	K5 defective	Check for operation of K5. If terminal 2 is not shorted to terminal 1 at any time, check K5. If it shorts upon release of the

Item No.	Symptom	Probable trouble	Correction
58	Current is available, but is the wrong value.	L3, C25, or L4 defective	starting relay, check resistance of coil K5 and R46 in parallel. Check position of OVER CURRENT ADJ potentiometer R46 by setting it fully CW. If meter M1 indicates correct current, but actual current at front panel is incorrect, check for partial short to ground in L3, C25, and L4. If trouble remains, proceed to item 59.
59	Current is available, but is the wrong value.	VR9 defective	Measure voltage at VR9 anode; it should measure +6.2 volts dc. If it is within 10% to 20%, proceed to item 63. If incorrect, check VR9.
60	Current is available, but is the wrong value.	R53, R47, R54, or C26 defective ..	Check voltage at E66, it should be held equal to the breakdown voltage measured in item 59. If equal, check path from this point to ground through R53, R47, R54, and C26. If voltage is not held equal, the loop is defective. Proceed to item 61.
61	Correct current is available initially, but becomes incorrect after warmup.	Q18 or CR17 defective	Check Q18 and CR17.
62	Defective regulation loop	Complete loop	Using chart in <i>f</i> below, measure voltage, starting at Q29. The negative-positive condition refers to the relative voltage between the base of Q29 and the base of Q28. An alternate scheme for troubleshooting the loop is shown in item 63.
63	Defective regulation loop	Complete loop	
<p>Caution: The CABLE POWER switch should be set to OFF before proceeding further.</p>			
64	Incorrect voltage at pins 4, 5, and 8 when CABLE POWER switch is at OFF.	K2 or CR16 defective	Carefully remove leads to E75 and E66. Attach the test setup (fig. 4-1) to the circuit. Measure the voltage at anode of VR9. Set potentiometer to give approximately the voltage at E66. Proceed through the chart until an incorrect reading is obtained. Check that portion of the circuitry. After correction has been made, replace leads on E75 and E66. When power is removed, check K2 for continuity between pins 7 and 5 and 2 and 4. If good, check CR16.
65	Buzzer does not sound when TIMING IN connection is removed with the CABLE POWER switch at ON.	K1 defective	When power is removed, check K1.

Item No.	Symptom	Probable trouble	Correction
66	Fault-locate meter burned out	VR5 defective	Check VR5; the breakdown voltage should be +6.2 volts dc. If incorrect, check VR5.
67	Fault-locate meter inoperative	Q14 or VR5 defective	Check current between collector of Q14 at E51. It should be 1,000 microamperes. If correct, check breakdown voltage of VR5; it should be +6.2 volts dc. If correct, check Q14.



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Figure 4-1. Panel 6A1 test setup.

b. *Transformer and Coil Resistances.* The chart below indicates the resistance of the transformer and coils found in panel 6A1.

Item	Measure across terminals	Dc resistance (ohms)
T1	1 and 2.....	5.8
	3 and 5.....	3.0
	6 and 8.....	1.4
	9 and 11.....	18
	12 and 14.....	18
L1	15 and 17.....	7.5
	1 and 2.....	1.0
	3 and 4.....	20
L2	5 and 6.....	20
	1 and 2.....	1.0
L3	1 and 2.....	300
L4	1 and 2.....	150

c. *+10-Volt Regulator Voltages With Respect to +10-Volt Bus.* The chart below indicates the +10-volt regulator voltages with respect to the +10-volt bus.

Base Q29 with respect to base Q28	Collector Q29	Collector Q28	Base Q27	Collector Q27	Base Q25	Collector Q25	Collector Q23	Emitter Q21, Q22
Negative	-6	-17	+.4 ^a	+.4 ^a	-.5	-.5	+3	+3
Positive	-17	-6	-17	+4	+4	-10	0	0
Normal	-12	-12	+.3 ^a	-6	-.3	-6	0 and +3	0 and +3

^a Measured with respect to emitter Q27.

Base Q2 with respect to base Q3	Base Q1 and collector Q2	Collector Q3	Emitter Q1
Positive	-12 to -19	-6	-11.7 to -18.7
Negative	-6	-20	-5.7
Normal	-10.3	-14	-10.0

d. *-10-Volt Regulator Voltages With Respect to Ground.* The chart below indicates the -10-volt regulator voltages with respect to ground.

Base Q6 with respect to base Q5	Collector Q6	Base Q4 and collector Q5	Emitter Q4
Positive	-12 to -16.5	-9.5	-11.7 to -16.2
Negative	-6	-17	-5.7
Normal	-10.3	-14	-10.0

e. *+6-Volt Regulator Voltages With Respect to +3-Volt Bus.* The chart below indicates the +6-volt regulator voltages with respect to the +3-volt bus.

Base Q9 with respect to base Q10	Base Q7 and collector Q9	Base Q8 and emitter Q7	Emitter Q8
Positive	-7.5 to -12.5	-7.2 to -12.2	-6.9 to -11.9
Negative	-3	-2.7	-2.4
Normal	-6.6	-6.3	-6.0

f. *Dc Cable Current Supply Voltages With Respect to Ground.* The chart below indicates the dc cable current supply voltages with respect to ground.

g. Transistor Terminal Voltages. The transistor terminal voltage readings below were made with a 20,000-ohms-per-volt meter. A measurement that differs widely from those in the chart below can, when used with the schematic diagram, often localize the trouble to a specific part. The readings should not exceed the parameters listed.

Voltage to ground			
Transistor (all PNP)	Emitter	Collector	Base
Q1	0 ± 0.1	-5.0 ± 1	-0.22 ± 0.1
Q2 (measured with respect to +10 volt bus).	-6.0 ± 0.6	-11.6 ± 1.2	-6.2 ± 0.6
Q3 (measured with respect to +10 volt bus).	-6.0 ± 0.6	-11.6 ± 1.2	-6.2 ± 0.6
Q4 (measured with respect to -10 volt bus).	0 ± 0.1	-4.2 ± 1	-0.23 ± 0.1
Q5	-5.9 ± 0.6	-10.0 ± 1	-6.1 ± 0.6
Q6	-5.9 ± 0.6	-13.6 ± 1.4	-6.1 ± 0.6
Q7 (measured with respect to +3 volt bus).	-6.3 ± 0.6	-8.2 ± 0.8	-6.5 ± 0.6
Q8 (measured with respect to +3 volt bus).	-6.0 ± 0.6	-8.1 ± 0.8	-6.3 ± 0.6
Q9 (measured with respect to +3 volt bus).	-2.8 ± 0.3	-6.5 ± 0.6	-3.0 ± 0.3
Q10 (measured with respect to +3 volt bus).	-2.8 ± 0.3	-5.9 ± 0.6	-3.0 ± 0.3
Q11 (measured with respect to -3 volt bus).	+2.85 ± 0.3	+4.6 ± 0.5	+3.0 ± 0.3
Q12 (measured with respect to -3 volt bus).	+2.85 ± 0.3	+4.6 ± 0.5	+3.0 ± 0.3
Q13	+1.78 ± 0.2	0 ± 0.1	+1.66 ± 0.16
<i>Note.</i> Connect a jumper wire between TO CABLE and FROM CABLE connectors before measuring terminal voltages for transistors Q14 through Q29.			
Q14	-1.75 ± 0.2	+4.2 ± 0.4	-1.84 ± 0.2
Q15 (measured with CABLE POWER switch at ON).	0 ± 0.1	-.03 ± .02	-0.25 ± 0.1
Q16	0 ± 0.1	(fig. 6-12)	(fig. 6-12)

Voltage to ground			
Transistor (all PNP)	Emitter	Collector	Base
Q17	0 ± 0.1	(fig. 6-12)	(fig. 6-12)
Q18	-18.0 ± 1.8	-12.0 ± 1.2	-18.0 ± 1.8
Q19	+3.0 ± 0.09	(fig. 6-12)	(fig. 6-12)
Q20	+3.0 ± 0.09	(fig. 6-12)	(fig. 6-12)
Q21	(fig. 6-12)	+3.0 ± 0.09	(fig. 6-12)
Q22	(fig. 6-12)	0 ± 0.1	(fig. 6-12)
Q23	(fig. 6-12)	(fig. 6-12)	(fig. 6-12)
Q24	(fig. 6-12)	(fig. 6-12)	(fig. 6-12)
Q25	(fig. 6-12)	(fig. 6-12)	(fig. 6-12)
Q26	(fig. 6-12)	-3.0 ± 0.09	(fig. 6-12)
Q27	-12.0 ± 1.2	-10.0 ± 1.0	-12.0 ± 1.2
Q28	-6.0 ± 0.6	-11.8 ± 1.2	-6.2 ± 0.6
Q29	-6.0 ± 0.6	-11.8 ± 1.2	-6.2 ± 0.6

h. Diode Terminal Voltages. The chart below indicates the voltage at the cathode and anode of certain diodes in panel 6A1.

Diode	Cathode	Anode
CR1 (measured with respect to +10 volt bus).	+0.06 ± 0.1	-8.9 ± 0.9
CR2 (measured with respect to +10 volt bus).	+0.06 ± 0.1	-8.9 ± 0.9
CR3	+0.08 ± 0.1	-16.4 ± 1.6
CR4	+0.08 ± 0.1	-16.4 ± 1.6
CR5 (measured with respect to +3 volt bus).	0 ± 0.1	-9.6 ± 0.9
CR6 (measured with respect to +3 volt bus).	0 ± 0.1	-9.6 ± 0.9
CR7	+0.12 ± 0.1	-39.0 ± 4.0
CR8	+0.12 ± 0.1	-39.0 ± 4.0
CR10-CR13	Voltage at E52	
CR10-CR13	Voltage at E53	
CR10-CR13	Voltage at E57	+26.4 ± 3.0
CR10-CR13	Voltage at E58	-7.7 ± 0.7
VR1 (measured with respect to +10 volt bus).	0 ± 0.1	-6.0 ± 0.6
VR2	0 ± 0.1	-6.0 ± 0.6
VR3 (measured with respect to +3 volt bus).	0 ± 0.1	-6.0 ± 0.6
VR4	0 ± 0.1	+18.3 ± 1.8
VR5	+4.2 ± 0.4	0 ± 0.1
VR9	0 ± 0.1	-6.2 ± 0.6

4-7. Panel 6A2, Troubleshooting (figs. 6-1, 6-13, and 6-14)

a. General. If test tone and ring signal outputs are available at terminals 6 and 4 of panel 6A2,

loss of any outputs other than these can be caused by failure of hybrid HY1. Before performing further troubleshooting of the panel, verify that hybrid HY1 is functioning properly by performing the following checks:

Note. The inputs to panel 6A2 are as follows: (1) *Patch thru:* 224 mv rms at 1 kc, applied across terminals A and B of the PATCH THRU connector with terminals C and D shorted, and (2) *Reed order wire:* 150 mv rms at 1 kc applied to FROM CABLE connector.

- (1) Disconnect *patch thru* and *reed order wire* from front panel; operate TONE-OFF switch to TONE. Adjust TTL control for 10 mv rms at J9. The test tone output of approximately 60 mv rms should appear between terminals 27 and 28 and between terminals 29 and 31 of panel 6A2. If either output is not present, hybrid HY1 may be defective.
- (2) Operate the TONE-OFF switch to OFF, and connect *patch thru* input to front panel; leave *reed order wire* disconnected.

An output signal should appear between terminals 29 and 31 of panel 6A2, and a HEADSET terminal 21 (terminated with the 270-ohm resistor), indicating that hybrid HY1 is functioning properly. If the proper outputs are not present, check item: 1 through 11 in the troubleshooting chart (b below).

- (3) With the TONE-OFF switch at OFF, disconnect the *patch thru* input, and connect the order-wire signal to the FROM CABLE connector on the front panel. An output signal should appear between terminals 27 and 28 of panel 6A2 and at HEADSET terminal 21, indicating that hybrid HY1 is functioning properly. If the proper outputs are not present, check items 12 through 18 in the troubleshooting chart (b below).
- (4) After performing items 1 through 11, or 12 through 18, as necessary, proceed to item 19.

b. Troubleshooting Chart.

Item No.	Symptom	Probable trouble	Correction
1	Incorrect output at terminals 29 and 31; incorrect output at terminal 21.	Radio receive amplifier or HY1 defective.	Check signal at J2. If not present, proceed to item 3. If signal present, proceed to item 2.
2	Incorrect output at terminals 29 and 31; incorrect output at terminal 21; signal present at J2.	T2 or HY1 defective	Check signal at secondary of T2. If signal present, HY1 defective. If signal not present, T2 defective.
3	Incorrect signal at J2	Q2 defective	Check signal at collector of Q1. If not present, proceed to item 4. If signal present, check Q2.
4	Incorrect signal at collector of Q1	Q1 defective	Check waveform at base of Q1. If not present, proceed to item 5. If signal present, check Q1.
5	Incorrect signal at base of Q1	T1 defective	Check waveform at primary of T1. If not present, proceed to item 6. If signal present, check T1.
6	Incorrect signal at primary of T1...	Attenuator network defective (R1 through R6).	Check R1 through R6.
7	Incorrect output at terminals 29 and 31; correct output at terminal 21.	HY1 defective	Check HY1.
8	Correct output at terminals 29 and 31; incorrect output at terminal 21.	Phone amplifier or HY1 defective.	Check signal at collector of Q3. If not present, proceed to item 9. If signal present, check Q4.
9	Incorrect signal at collector of Q3.	Q3 defective	Check waveform at J3. If not present, proceed to item 10. If waveform present, check Q3.
10	Incorrect signal at J3	T3 or HY1 defective	Check signal at primary of T3. If signal not present, check HY1. If signal present, check T3.

Item No.	Symptom	Probable trouble	Correction
11	Correct output at terminal 21; incorrect output at terminal 17 (TEST ALIGN meter in green with SERV SEL switch at Q).	Q5 or CR1 defective	Check Q5 and CR1.
12	Incorrect output at terminals 27 and 28; no output at terminal 21.	Cable receive amplifier or HY1 defective.	Check signal at J1 with R44 fully clockwise. If not present, proceed to item 14. If signal present at J1, proceed to item 13.
13	Incorrect output at terminals 27 and 28; no output at terminal 21; signal available at J1.	T6 or HY1 defective	Check signal at secondary of T6. If signal present, HY1 is defective. If signal not present, T6 defective.
14	Incorrect output at J1	Q9 defective	Check signal at base of Q9. If not present, proceed to item 15. If signal present, check Q9.
15	Incorrect signal at base of Q9	R44 defective	Check signal at terminal 2 of FL1. If not present, proceed to item 16. If signal present, check R44.
16	Incorrect signal at pin 2 of FL1	FL1 or T5 defective	Check signal at secondary of T5. If not present, check T5. If signal present, check FL1.
17	Incorrect output at terminals 27 and 28; correct output at terminal 21.	HY1 defective	Check HY1.
18	Correct output at terminals 27 and 28; incorrect output at terminal 21.	HY1 defective	Check HY1.
19	Incorrect output at terminal 5. (TEST ALIGN meter in green with CABLE POWER switch at ON, SERV SEL switch at RCC, and TO CABLE connector shorted to FROM CABLE connector.)	T5, R41, R42, or C19 defective	Check primaries of T5, R41, R42, and C19.
20	Incorrect output at J7 (-8.9 ± 0.8 volts dc) with correct input to terminal 3.	<i>Note.</i> Prior to performing troubleshooting, remove jumper from FROM CABLE to TO CABLE and apply 150 mv at 1600 cps to FROM CABLE connector, and operate potentiometer R44 fully clockwise.	Check voltage at J5. If not correct, proceed to step 21. If correct, check Q7 and Q8.
21	Incorrect voltage at J5 (-6.3 ± 0.6 volts dc).	R35, R36, R37, R38, C14, C15, C16, CR2, CR3 or CR5 defective.	Check signal at terminal 6 of T4. If not present, proceed to item 22. If signal present, check R35 through R38, C14 through C16, and CR2 through CR4.
22	Incorrect signal at terminal 6 of T4.	Q6 or T4 defective	Check signal at base of Q6. If signal not present, check Q5. If signal present, check Q6 and T4.
23	CALL lamp lights and buzzer sounds with 150-mv input at 1 kc.	C15 and C16 defective	Check C15 and C16.
24	CALL lamp lights, and buzzer sounds with no input.	Q7 or Q8 defective	Check Q7 and Q8.
25	Incorrect output at terminal 4 with TALK-OFF-SIG switch at SIG and TONE-OFF switch at OFF.	Signaling oscillator defective	Check waveform at J8. If waveform present, check R49. If waveform not present, proceed to item 26.
26	Incorrect output at J8	Q10 or T7 defective	Check Q10 and T7.
27	Ring signal wrong frequency ($1,600 \pm 32$ cps).	T7, C24, or S1 defective	Check T7, C24, and S1.

Item No.	Symptom	Probable trouble	Correction
28	Incorrect output at terminal 6 with TALK-OFF-SIG switch at SIG and TONE-OFF switch at TONE.	S1, Q10, T7, or R53 defective	Check S1, Q10, T7, and R53.
29	Test tone wrong frequency (1,100 cps).	S1, T7, or C23 defective	Check S1, T7, and C23.

c. Transistor Terminal Voltages. The transistor terminal voltage readings below were made with a 20,000-ohms-per-volt meter. A measurement that differs widely from those in the chart below can, when used with the schematic diagram, often localize the trouble to a specific part. The readings should not exceed the parameters listed.

Voltage to ground			
Transistor (all PNP)	Emitter	Collector	Base
Q1 (No ac input).	+0.27 ± 0.1	-7.2 ± 0.7	0 ± 0.1
Q2 (No ac input).	-6.9 ± 0.7	+0.06 ± 0.04 ^a	-7.2 ± 0.7
Q3 (No ac input).	+0.27 ± 0.1	-6.1 ± 0.6	0 ± 0.1
Q4 (No ac input).	+0.92 ± 0.3	-6.6 ± 0.6	+0.61 ± 0.3

Voltage to ground			
Transistor (all PNP)	Emitter	Collector	Base
Q5 (Terminal 21 terminated with 270-ohm resistor).	+0.3 ± 0.1	-4.3 ± 0.5	0 ± 0.1
Q6	-2.65 ± 0.3	-7.6 ± 0.7	-2.95 ± 0.3
Q7 (TALK-OFF-SIG switch at SIG).	-7.8 ± 0.8	0 ± 0.1	-7.1 ± 0.7
Q8 (TALK-OFF-SIG switch at SIG).	-10.0 ± 0.3	-9.9 ± 0.2	-9.3 ± 1.0
Q9	+0.3 ± 0.1	+0.13 ± 0.1 ^a	0 ± 0.1
Q10 (TONE-OFF switch at TONE).	+1.75 ± 0.1	(fig. 6-14)	0 ± 0.1

^a Measured with respect to the -10-volt supply with an ungrounded meter.

4-8. Panel 6A3, Troubleshooting (figs. 6-2, 6-15, and 6-16)

a. Troubleshooting Chart.

Item No.	Symptom	Probable trouble	Correction
1	Incorrect output at terminal 28 (with 29 grounded) with 100 mv rms at 1 kc applied to terminals C and D of HEADSET connector and with TALK-OFF-SIG switch at TALK.	Defective microphone amplifier circuit.	Check waveform at J6. If not present, proceed to item 2. If present, check T1.
2	Incorrect output at J6	Q3 defective	Check base of Q3 for proper waveform. If not present, proceed to item 3. If present, check Q3.
3	Incorrect signal at base of Q3	Q2 defective	Check base of Q2 for proper waveform. If not present, proceed to item 4. If present, check Q2.
4	Incorrect signal at base of Q2	Q1 defective	Check Q1.
5	Incorrect output at terminals 18 and 21.	Defective radio transmit amplifier circuit.	Check waveform at collectors of Q5 and Q6. If not present, proceed to item 6. If present, check T4.
6	Incorrect waveform at collectors of Q5 and Q6.	Q5 or Q6 defective	Check waveform at base of Q5 and Q6. If not present, proceed to item 7. If present, check Q5 and Q6.

Item No.	Symptom	Probable trouble	Correction
7	Incorrect waveform at collector of Q4.	Q4 or T3 defective	Check waveform at J1. If not present, proceed to item 8. If present, check Q4 and T3.
8	Incorrect waveform at J1	T2 defective	Check T2.
9	Incorrect output at J2	Defective cable transmit amplifier.	Check waveform at secondary of T7. If not present, proceed to item 10. If waveform present, check FL1.
10	Incorrect waveform at secondary of T7 with 100 mv at 1 kc applied to terminals C and D (ground) of HEADSET connector and with TALK-OFF-SIG switch at TALK.	T7 defective	Check waveform at collectors of Q9 and Q10. If not present, proceed to item 11. If waveform present, check T7.
11	Incorrect waveform at collectors of Q9 and Q10.	Q9 or Q10 defective	Check waveform at base of Q9 and Q10. If not present, proceed to item 12. If waveform present, check Q9 and Q10.
12	Incorrect waveform at base of Q9 and Q10.	T6 defective	Check voltage at collector of Q8. If not present, proceed to item 13. If present, check T6.
13	Incorrect voltage at collector of Q8.	Q8 defective	Check voltage at collector of Q7. If not present, proceed to item 14. If voltage present, check Q8.
14	Incorrect voltage at collector of Q7.	Q7 defective	Check waveform at J5. If not present, proceed to item 15. If waveform present, check Q7.
15	Incorrect waveform at J5	T5 defective	Check T5.
16	Incorrect output at terminal 24	R1, R2, R3, or C1 defective	Check R1, R2, R3, and C1.
17	With SERV SEL switch at O, TEST ALIGN meter does not indicate in green region with correct signal at terminal 2.	CR2 defective	Check CR2.
18	With SERV SEL switch at P, TEST ALIGN meter does not indicate in green region with correct signal at J4A and J4B.	CR1 or C12 defective	Check CR1 and CR12.

b. Transistor Terminal Voltages. The transistor terminal voltage readings below were made with a 20,000-ohms-per-volt meter. A measurement that differs widely from those in the table can, when used with the schematic diagram, often localize the trouble to a specific part. All measurements were taken with no ac input. The readings should not exceed the parameters listed.

Transistor (all PNP)	Voltage to ground		
	Emitter	Collector	Base
Q1	+0.255 ± 0.1	-4.3 ± 0.4	0 ± 0.1
Q2	-4.0 ± 0.4	-10.0 ± 0.3	-4.3 ± 0.4
Q3	-4.8 ± 0.5	+0.17 ± 0.1 ^a	-5.1 ± 0.5
Q4	+0.13 ± 0.15	+6 ± 0.2 ^a	0 ± 0.1
Q5	-0.08 ± 0.04 ^b	+1.6 ± 0.5 ^a	-21 ± 0.1 ^b
Q6	-.06 ± 0.04 ^b	+1.54 ± 0.5 ^a	-.21 ± 0.1 ^b
Q7	+.26 ± 0.1	-3.5 ± 0.3	0 ± 0.1
Q8	-.7 ± 0.2	+0.45 ± 0.2 ^a	-.87 ± 0.1
Q9	0 to -0.1 ^b	+0.22 ± 0.2 ^a	-.05 ± .05 ^b
Q10	0 to -0.1 ^b	+0.22 ± 0.2 ^a	-.05 ± .05 ^b

^a Measure with respect to -10 volts dc (pin 22).
^b Measure with respect to +10 volts dc (pin 3).

4-9. Panel 6A4, Troubleshooting
(figs. 6-3, 6-17, and 6-18)

a. Troubleshooting Chart.

Item No.	Symptom	Probable trouble	Correction
1	Incorrect output at J3; correct output at terminal 19.	Stages Q1 through Q9 defective ...	Check signal at J2. If incorrect, proceed to item 2. If correct, Q7, Q8, and Q9 may be defective. Check signal at base of Q9. If present, Q9 is defective, if not present, check Q7 and Q8.
2	Signal at J2 incorrect	T1, R12, Q6, C14, or L10 defective.	Check signal at emitter of Q5. If incorrect, proceed to item 3. If correct, check the signal at base of Q6. If correct signal exists at base of Q6, check Q6, C14, and L10. If incorrect signal exists at base of Q6, check secondary of T1 and R12.
3	Signal at emitter of Q5 incorrect	Q4 and Q5 defective	Check signal at emitter of Q3. If incorrect, proceed to item 4. If correct, check the signal at the collector of Q4. If incorrect, Q4 is defective. If correct, Q5 is defective.
4	Signal at emitter of Q3 incorrect	Q3, Q2, or FL1 defective	Check signal at J1. If incorrect, proceed to item 5. If correct, check output of FL1. If signal is present, Q3 is defective. If it is not present, check FL1 and Q2.
5	Signal at J1 incorrect	Q1 or C7 defective	Check Q1 and C7.
6	Signal at base of Q3 is free-running, although pcm is received at terminal 2.	Q13, CR7, or CR8 defective	Check signal at terminal 19. If signal not present, proceed to item 7. If signal is present, proceed to check Q13, CR7, and CR8.
7	Incorrect output at terminal 19 and TRAFFIC lamp lighted.	Circuit of input stage defective	Check signal at J5. If signal not present, proceed to item 8. If signal present, check Q11 and Q12.
8	Incorrect signal at J5	T3 defective	Check signal at J4. If signal not present, proceed to item 9. If signal present, check T3.
9	Incorrect signal at J4	T2 or Q10 defective	Check T2 and Q10.
10	Incorrect phase between waveforms at terminals 25 and 19.	Incorrect adjustment of or defective R12.	Attempt adjustment of R12. If this fails, check R12.
11	No signal at terminal 25 with input to terminal 2 disconnected; TRAFFIC lamp is lighted.	Q2 defective	Check Q2.
12	TRAFFIC lamp lighted with signal at terminal 19.	K1 or Q14 defective	Check K1 and Q14.
13	No output at terminal 3 when audio input of 5 volts rms at 1 kc is received at terminal 2.	L3, L4, or L5 defective	Check L3, L4, and L5.
14	With SERV SEL switch at B, TEST ALIGN meter does not indicate in green region with correct output at terminal 25.	CR3 or CR4 defective	Check CR3 and CR4.

Item No.	Symptom	Probable trouble	Correction
15	With SERV SEL switch at A, TEST ALIGN meter does not indicate in green region with correct signal at collector of Q13.	R37 defective	Check R37.

b. Transistor Terminal Voltages. The transistor terminal voltage readings below were made with a 20,000-ohms-per-volt meter. A measurement that differs widely from those in the chart below can, when used with the schematic diagram, often localize the trouble to a specific part. The readings should not exceed the parameters listed.

Note. All measurements made with TRAFFIC SEL switch at position 24.

Voltage to ground			
Transistor (all PNP)	Emitter	Collector	Base
Q1	(fig. 6-18)	-3 ± 0.09	(fig. 6-18)
Q2 (Input removed from FROM CABLE connector).	+0.35 ± 0.3	(fig. 6-18)	+0.2 ± 0.2
Q2 (Input connected to FROM CABLE connector).	+4.0 ± 0.4	(fig. 6-18)	+8.2 ± 0.8

Voltage to ground			
Transistor (all PNP)	Emitter	Collector	Base
Q3	(fig. 6-18)	-3 ± 0.09	(fig. 6-18)
Q4	(fig. 6-18)	(fig. 6-18)	(fig. 6-18)
Q5	(fig. 6-18)	-3 ± 0.09	(fig. 6-18)
Q6	(fig. 6-18)	-3 ± 0.09	(fig. 6-18)
Q7	(fig. 6-18)	-3 ± 0.09	(fig. 6-18)
Q8	(fig. 6-18)	(fig. 6-18)	+0.1 ± 0.1
Q9	(fig. 6-18)	-3 ± 0.09	(fig. 6-18)
Q10	+0.3 ± 0.2	(fig. 6-18)	0 ± 0.1
Q11	0 ± 0.1	(fig. 6-18)	(fig. 6-18)
Q12	(fig. 6-18)	-3 ± 0.09	(fig. 6-18)
Q13 (Input removed from FROM CABLE connector).	0 ± 0.1	+0.1 ± 0.1	+0.2 ± 0.15
Q13 (Input connected to FROM CABLE connector).	0 ± 0.1	+8.2 ± 0.8	-1.1 ± 0.3
Q14	0 ± 0.1	+0.20 ± 0.15	+0.7 ± 0.2

4-10. Panel 6A5, Troubleshooting (figs. 6-4, 6-19, and 6-20)

Note. TRAFFIC SEL switch is set to position 24.

a. Troubleshooting Chart.

Item No.	Symptom	Probable trouble	Correction
1	With no power applied and no signal at terminals 22, 19, and 14, there is no continuity between terminal 16 and terminal 9 and between terminals 12 and 9.	K1 or K2 defective	Check K1 and K2.
2	Incorrect output at terminal 16 with no input at terminal 22 (PCM IN-2 disconnected).	K1 or Q17 defective	Check K1 and Q17.
3	Incorrect output at terminal 11, with no input at terminal 19 (PCM IN-1 disconnected).	K2 or Q18 defective	Check K2 and Q18.
4	Incorrect output at terminal 16 with correct input at terminal 22 (PCM IN-2 connected).	K1 or Q17 defective	Check signal at collector of Q17. If signal correct, check K1. If K2 not defective, check signal at base of Q17. If signal correct, check Q17. If incorrect, proceed to item 5.
5	Incorrect signal at base of Q17	CR13, CR14, CR23, and CR24 defective.	Check CR13, CR14, CR23, and CR24.

Item No.	Symptom	Probable trouble	Correction
6	Incorrect output at terminal 11 with correct input at terminal 19 (PCM IN-1 connected).	K2 or Q18 defective	Check signal at collector of Q12. If signal correct check K2. If K2 not defective, check signal at base of Q18. If signal correct, check Q18. If signal incorrect, proceed to item 7.
7	Incorrect signal at base of Q18	CR17, CR18, C29, or C30 defective.	Check CR17, CR18, C29, and C30.
8	Incorrect output at terminal 24 with input at terminal 31.	Q13, Q14, or Q15 defective	Check for signal at J1. If signal present, check Q13, Q14, and Q15. If signal not present, proceed to item 9.
9	Incorrect output at J1	FL1 or Q12 defective	Check for signal at collector of Q11. If signal absent, proceed to item 10. If signal present, check Q12 and FL1.
10	Incorrect output at collector of Q11.	Q10 or Q11 defective	Check Q10 and Q11.
11	Correct output at terminal 24, but SERV SEL switch in position J does not result in green indication on TEST ALIGN meter.	Q16, CR12, CR11 defective	Check signal at emitter of Q16. If present, check CR11 and CR12. If not present, check Q16.
12	Incorrect waveform at terminal 3 with inputs at terminals 31 and 15, and no input at terminal 1. (TRAFFIC SEL switch at 24.)	T1, CR24 and CR25 defective	Observe signal at collector of Q19. If present, check T1, CR24, and CR25. If not present, proceed to item 13.
13	Incorrect signal at collector of Q19.	Q19 defective	Check for signal at J8. If signal not present, proceed to item 14. If signal present, check Q19.
14	Incorrect signal at J8	Q7, Q8, or Q9 defective	Check for signals at J2 and J4. If signals present, check Q7, Q8, and Q9. If signals not present, proceed to items 15 and 16.
15	Incorrect signal at J2	Q1, Q2, or Q3 defective	Check for signal at J3. If signal present, check Q3, Q1, and Q2. If signal not present, proceed to item 17.
16	Incorrect signal at J4	Q6 defective	Check Q6.
17	Incorrect signal at J3	Q4 or Q5 defective	Check Q4 and Q5.
18	TEST ALIGN meter does not indicate in green region when METER SELECT switch is at PCM IN-2, but correct output is obtained at terminal 16.	CR15, CR16, C25, or C26 defective.	Check CR15, CR16, C25, and C26.
19	TEST ALIGN meter does not indicate in green region when METER SELECT switch is at PCM IN-2, but correct output is obtained at terminal 11.	CR19, CR20, C27, or C28 defective.	Check CR19, CR20, C27, and C28.
20	With a correct output at the collector of Q19, TEST ALIGN meter does not indicate in green region when METER SELECT switch is at SERV FAC and SERV SEL switch is at position H.	CR26, CR27, or C38 defective	Check CR26, CR27, and C38.
21	With a correct input at terminal 31, TEST ALIGN meter does not indicate in green region when METER SELECT switch is at TIMING IN.	Q10, CR9, CR10, C12, and C14 defective.	Check signal at collector of Q10. If signal absent, check Q10. If signal present, check CR9, CR10, C12, and C14.

b. *Transistor Terminal Voltages.* The transistor terminal voltage readings below were made with a 20,000-ohms-per-volt meter. A measurement that differs widely from those in the chart can, when used with the schematic diagram, often localize the trouble to a specific part. The readings should not exceed the parameters listed.

Voltage to ground			
Transistor (all PNP)	Emitter	Collector	Base
Q1	(Refer to fig. 6-20 for transistors Q1 through Q16.)	-3 ± 0.09 (fig. 6-20)	(fig. 6-20)
Q2		-3 ± 0.09 (fig. 6-20)	(fig. 6-20)
Q3		(fig. 6-20)	(fig. 6-20)
Q4		-3 ± 0.09 (fig. 6-20)	(fig. 6-20)
Q5		(fig. 6-20)	(fig. 6-20)

Voltage to ground			
Transistor (all PNP)	Emitter	Collector	Base
Q6		-3 ± 0.09 (fig. 6-20)	(fig. 6-20)
Q7		(fig. 6-20)	(fig. 6-20)
Q8		(fig. 6-20)	(fig. 6-20)
Q9		(fig. 6-20)	-0.3 ± 0.2
Q10		(fig. 6-20)	(fig. 6-20)
Q11		(fig. 6-20)	0 ± 0.1
Q12		(fig. 6-20)	(fig. 6-20)
Q13		(fig. 6-20)	(fig. 6-20)
Q14		(fig. 6-20)	0 ± 0.1
Q15		-3 ± 0.09 (fig. 6-20)	(fig. 6-20)
Q16		-3 ± 0.09 (fig. 6-20)	(fig. 6-20)
Q17	+3 ± 0.09	+2.8 ± 0.2	+2.65 ± 0.3
Q18	+3 ± 0.09	+2.8 ± 0.2	+2.65 ± 0.3
Q19	+3 ± 0.09	(fig. 6-20)	(fig. 6-20)

4-11. Panel 6A6, Troubleshooting
(figs. 6-5, 6-21, and 6-22)

Note. TRAFFIC SEL switch is set to position 24.

a. *Troubleshooting Chart.*

Item No.	Symptom	Probable trouble	Correction
1	Incorrect signal at terminal 9	Q7, Q8, or Q9 defective	Check Q7, Q8, and Q9.
2	Incorrect signal at terminal 27	Q18, Q19, or Q20 defective	Check for signal at J7. If correct signal present, check Q18, Q19, and Q20. If correct signal not present, proceed to item 3.
3	Incorrect signal at J7	CR7, CR20, CR8, CR21, or CR22 defective.	Check signal at J4. If signal not present, proceed to item 4. If signal present, check for signal at J6. If signal at J6 not present, proceed to item 10. If signal present, check CR7, CR8, CR21, CR20, and CR22.
4	Incorrect signal at J4	Q6 defective	Check for signal at base of Q6. If incorrect, proceed to item 5. If signal at base of Q6 correct, check Q6.
5	Incorrect signal at base of Q6	Flip-flop Q4 or Q5 defective	If signal at base of Q6 is 0 volt, check anode of CR5. If signal not present, proceed to item 8. If signal present, check Q4 and Q5. If signal at base of Q6 is -3 volts, check J1. If signal not present at J1, proceed to item 6. If signal present at J1, check Q4 and Q5.
6	Incorrect signal at J1	Q1 or Q2 defective	Check for signal at J2. If signal present, check Q1 and Q2. If signal not present, proceed to item 7.
7	Incorrect signal at J2	Q3 defective	Check for signal at J8. If signal present, check Q3. If signal not present, proceed to item 8.
8	Incorrect signal at J8 or at anode of CR5.	Q14 or flip-flop Q12 or Q13 defective.	Check for signal at J3. If signal present, check Q14, Q12, and

Item No.	Symptom	Probable trouble	Correction
9	Incorrect signal at J3	Flip-flop Q10 or Q11 defective Q15, Q16, or Q17 defective Q21, Q22, or Q23 defective CR24 or CR25 defective	Q13. If signal not present, proceed to item 9.
10	Incorrect signal at J6		Check Q10 and Q11.
11	Incorrect signal at J10		Check Q15, Q16, and Q17.
12	With SERV SEL switch at M, TEST ALIGN meter does not indicate in green region with correct signal at terminal 27.		Check Q21, Q22, and Q23.
12	With SERV SEL switch at M, TEST ALIGN meter does not indicate in green region with correct signal at terminal 27.		Check CR24 and CR25.
13	With SERV SEL switch at K, TEST ALIGN meter does not indicate in green region with correct signal at J6.	CR19 defective	Check CR19.
14	With SERV SEL switch at N, TEST ALIGN meter does not indicate in green region with correct signal at J10.	Q23, CR26, and CR27 defective	Check Q23, CR26, and CR27.
15	With SERV SEL switch at L, TEST ALIGN meter does not indicate in green region with correct signal at J4.	CR6 defective	Check CR6.

b. Transistor Terminal Voltages. The transistor terminal voltage readings below were made with a 20,000-ohms-per-volt meter. A measurement that differs widely from those in the chart can, when used with the schematic diagram, often localize the trouble to a specific part. The readings should not exceed the parameters listed.

Voltage to ground			
Transistor (all PNP)	Emitter	Collector	Base
Q1	(Refer to fig. 6-22 for transistors Q1 through Q21.)	-3 ± 0.09	Refer to fig. 6-22 for transistors Q1 through Q18.
Q2	(fig. 6-22)
Q3	(fig. 6-22)
Q4	(fig. 6-22)
Q5	(fig. 6-22)
Q6	-3 ± 0.09

Voltage to ground			
Transistor (all PNP)	Emitter	Collector	Base
Q7	(fig. 6-22)
Q8	(fig. 6-22)
Q9	-3 ± 0.09
Q10	(fig. 6-22)
Q11	(fig. 6-22)
Q12	(fig. 6-22)
Q13	(fig. 6-22)
Q14	-3 ± 0.09
Q15	(fig. 6-22)
Q16	-3 ± 0.09
Q17	-3 ± 0.09
Q18	-1.75 ± 0.2
Q19	(fig. 6-22)	+0.25 ± 0.1
Q20	-3 ± 0.09	(fig. 6-22)
Q21	-3 ± 0.09	(fig. 6-22)
Q22	-0.14 ± 0.1	(fig. 6-22)	(fig. 6-22)
Q23	(fig. 6-22)	-3 ± 0.09	(fig. 6-22)

4-12. Panel 6A7, Troubleshooting
(figs. 6-23 through 6-25)

Note. TRAFFIC SEL switch is set to position 24 for items 1 through 10.

a. Troubleshooting Chart.

Item No.	Symptom	Probable trouble	Correction
1	Incorrect output at terminal 1 with correct input at terminal 10.	Q26 defective	Check waveform at J7. If waveform present, check Q26. If waveform incorrect, proceed to item 3.
2	Incorrect output at terminal 3 with correct input at terminal 10.	Q25 defective	Check waveform at J7. If waveform present, check Q25. If waveform incorrect, proceed to item 3.

Item No.	Symptom	Probable trouble	Correction
3	Incorrect output at J7	Q27 defective	Check waveform at base of Q27. If waveform missing, proceed to item 4. If waveform present, check Q27.
4	Incorrect waveform at base of Q27.	Q21, Q22, Q23, or Q24 defective.	Check waveforms at J5 and J6. If proper waveforms present, check Q21, Q22, Q23, and Q24. If waveforms at J5 and J6 are incorrect, proceed to item 5.
5	Incorrect outputs at J5 and J6	Q16, Q18, or Q19 defective	Check emitter of Q19. If correct waveform present, check Q19, Q16, and Q18. If waveform incorrect at emitter of Q19, proceed to item 6.
6	Incorrect waveform at emitter of Q19.	Q17, Q20, CR30, or CR10 defective.	Check potential at base of Q20. If the potential is between -2 and -3 volts dc, check Q20 and Q17. Otherwise, check CR30 and CR10.
7	Incorrect output at terminal 19 with correct input at terminal 10 and terminal 26.	Q6 defective	Check signal at emitter of Q4. If signal incorrect, proceed to item 9; if signal correct, check Q6.
8	Incorrect output at terminal 23 with correct input at terminal 10 and terminal 26 (-3.0 volts dc).	Q5 defective	Check signal at emitter of Q4. If signal incorrect, proceed to item 9. If signal correct, check Q5.
9	Incorrect signal at emitter of Q4	Q4 defective	Check J10. If signal at J10 incorrect, proceed to item 10. A correct signal at J10 indicates Q4 defective.
10	Incorrect signal at J10	Q1, Q2, Q3, CR5, or CR29 defective.	Check potential at base of Q2. If the potential is between -2 and -3 volts dc, check Q1, Q2, and Q3. Otherwise check CR5 and CR29.
<i>Note.</i> Items 11 through 30 are performed with the TRAFFIC SEL switch set to position 12.			
11	Incorrect output frequency at terminals 23 or 19 with correct signal at terminal 10 and terminal 7 (0 volt dc).	Q2 defective	Check signal at base of Q2. If incorrect, proceed to item 12. If correct, check Q2.
12	Incorrect signal at base of Q2	Q12 or CR11 defective	Check signal at base of Q12. If correct, check Q12 and CR11. If incorrect (1,152-kc square wave), proceed to item 13. If incorrect (576-kc square wave), proceed to item 16. If signal not present, proceed to item 17.
13	1,152-kc square wave at base of Q12.	CR6 or CR7 defective	Check signal at pin 10 of Z2. If correct, check CR6 and CR7. If incorrect, proceed to item 14.
14	Incorrect signal at pin 10 of Z2	Z2 defective	Check signal at emitter of Q13. If correct, check Z2. If incorrect, proceed to item 15.
15	Incorrect signal at emitter of Q13 ..	Q13 defective	Check signal at pin 10 of Z1. If correct, check Q13. If incorrect, proceed to item 19.
16	576-kc square wave at base of Q12.	CR6 or CR7 defective	Check signal at pin 10 of Z1. If correct, check CR6 and CR7. If incorrect, proceed to item 19.

Item No.	Symptom	Probable trouble	Correction
17	Signal not present at base of Q12 ..	Z2 defective	Check signal at pin 10 of Z2. If correct, proceed to item 18. If incorrect, return to item 14.
18	No signal at base of Q12 with correct signal at pin 10 of Z1.	CR6 or CR7 defective	Check signal at pin 10 of Z1. If correct, check CR6 and CR7. If incorrect, proceed to item 19.
19	Incorrect signal at pin 10 of Z1	Z1 defective	Check signal at emitter of Q11. If correct, check Z1. If incorrect, proceed to item 20.
20	Incorrect signal at emitter of Q11 ..	Q11, Q9, or DL1 defective	Check signal at emitter of Q9. If correct, check DL1 and Q11. If incorrect, check Q9.
21	Incorrect frequency output at terminals 1 and 3.	Q20 defective	Check signal at base of Q20. If correct, check Q20. If incorrect, proceed to item 22.
22	Incorrect signal at base of Q20	Q10 or CR11 defective	Check potential at base of Q10. If the potential is between 0 and -5 volts dc, check CR8. If correct, check CR11.
23	Incorrect pcm outputs	Phasing circuitry defective	If incorrect, and no correction signal at J4, proceed to item 24. If incorrect, and continuous output at J4, proceed to item 28.
24	Incorrect pcm outputs; no correction signal at J4.	Q28 or T1 defective	Check dc level at base of Q15. If positive, proceed to item 25. If negative, check Q15 and continuity in T1.
25	Dc level at base of Q15 positive	Q14 or CR16 defective	Check for random square wave signal at J3. If not present, proceed to item 26. If present, check Q14 and CR16.
26	Incorrect signal at J3	Z3 or Z4 defective	Check signals at pins 3 and 1 of Z4. If correct, check Z4. If signal on pin 1 incorrect, check Q22. If signal on pin 3 incorrect, check Z3.
27	Incorrect pcm output (continuous correction signal at J4).	Q15 defective	Check dc voltage at base of Q15. If positive, check Q15. If negative, proceed to item 28.
28	Voltage at base of Q15 negative	Q14 or CR16 defective	Check for random square wave signal at J3. If correct, check Q14 and CR14. If incorrect, return to item 26.
29	With SERV SEL switch at G, TEST ALIGN meter does not indicate in green region with correct signal at J4.	CR15 defective	Check CR15.
30	With SERV SEL switch at S, TEST ALIGN meter does not indicate in green region with correct signal at J3.	CR12 or CR13 defective	Check CR12 and CR13.
<i>Note.</i> Items 31 through 35 are performed with the TRAFFIC SEL switch at position 24.			
31	Incorrect frequency of pcm outputs at terminals 1 and 3.	CR9 defective	Check CR9.
32	With SERV SEL switch at C, TEST ALIGN meter does not indicate in green region with correct signal at terminal 23.	Q7, CR1, or CR2 defective	Check Q7, CR1, and CR2.

Item No.	Symptom	Probable trouble	Correction
33	With SERV SEL switch at D, TEST ALIGN meter does not indicate in green region with correct signal at terminal 19.	Q8, CR3, or CR4 defective	Check Q8, CR3, and CR4.
34	With SERV SEL switch at F, TEST ALIGN meter does not indicate in green region with correct signal at terminal 1.	CR24 or CR25 defective	Check CR24 and CR25.
35	With SERV SEL switch at E, TEST ALIGN meter does not indicate in green region with correct signal at terminal 3.	CR26 or CR27 defective	Check CR26 and CR27.
<i>Note.</i> Items 36 through 40 are performed with TRAFFIC SEL switch in 48-AR position.			
36	Voltage at base of Q2 incorrect (-2.8 ± 0.3 volts dc).	CR29 defective	Check CR29.
37	Voltage at emitter of Q10 incorrect (-2.8 ± 0.3 volts dc).	CR10 defective	Check CR10.
38	Voltage at emitter of Q12 incorrect (-2.8 ± 0.3 volts dc).	CR5 defective	Check CR5.
39	Voltage at base of Q20 incorrect (-2.8 ± 0.3 volts dc).	CR30 defective	Check CR30.
40	Voltage at base of Q1 incorrect (-0.2 ± 0.2 volts dc).	CR8 defective	Check CR8.

b. Transistor Terminal Voltages. The transistor terminal voltage readings below were made with a 20,000-ohms-per-volt meter. A measurement that differs widely from those in the chart below can, when used with the schematic diagram, often localize the trouble to a specific part. The readings should not exceed the parameters listed.

Voltage to ground			
Transistor (all PNP)	Emitter	Collector	Base
Q1	-1.8 ± 0.2	-3 ± 0.09	(fig. 6-25)
Q2	0 ± 0.1	-1.8 ± 0.2	(fig. 6-25)
Q3	-1.8 ± 0.2	(fig. 6-25)	+0.7 ± 0.2
Q4	(fig. 6-25)	+3 ± 0.09	(fig. 6-25)
Q5	(fig. 6-25)	-2.5 ± 0.2	(fig. 6-25)
Q6	(fig. 6-25)	-2.5 ± 0.2	(fig. 6-25)
Q7	+0.46 ± 0.05	(fig. 6-25)	(fig. 6-25)
Q8	+0.46 ± 0.05	(fig. 6-25)	(fig. 6-25)
Q9	(fig. 6-25)	-3 ± 0.09	(fig. 6-25)
Q10	(fig. 6-25)	-3 ± 0.09	(fig. 6-25)
Q11	(fig. 6-25)	-3 ± 0.09	(fig. 6-25)

Transistor (all PNP)	Voltage to ground		
	Emitter	Collector	Base
Q12	(fig. 6-25)	-3 ± 0.09	(fig. 6-25)
Q13	(fig. 6-25)	-3 ± 0.09	(fig. 6-25)
Q14	+2.74 ± 0.3	(fig. 6-25)	(fig. 6-25)
Q15	0 ± 0.1	(fig. 6-25)	(fig. 6-25)
Q15 (FROM CABLE removed).	0 ± 0.1	(fig. 6-25)	(fig. 6-25)
Q16 (FROM CABLE connected).	(fig. 6-25)	(fig. 6-25)	(fig. 6-25)
Q17	(fig. 6-25)	-3 ± 0.09	(fig. 6-25)
Q18	(fig. 6-25)	(fig. 6-25)	+0.43 ± 0.1
Q19	(fig. 6-25)	(fig. 6-25)	+3 ± 0.09
Q20	0 ± 0.1	(fig. 6-25)	(fig. 6-25)
Q21	(fig. 6-25)	(fig. 6-25)	(fig. 6-25)
Q22	(fig. 6-25)	(fig. 6-25)	+0.73 ± 0.1
Q23	(fig. 6-25)	(fig. 6-25)	(fig. 6-25)
Q24	(fig. 6-25)	(fig. 6-25)	+0.73 ± 0.1
Q25	(fig. 6-25)	-2.2 ± 0.2	(fig. 6-25)
Q26	(fig. 6-25)	-2.3 ± 0.2	(fig. 6-25)
Q27	(fig. 6-25)	+3 ± 0.09	(fig. 6-25)

c. *Module Terminal Voltages.* The chart below lists the voltages or waveforms available at the terminals of each module in panel 6A7.

Z or Q number	1	2	3	4	5	6	7	8	9	10
Z1	(fig. 6-25)	-3 ± 0.09	0 ± 0.01	$+3 \pm 0.09$	-3 ± 0.09	-3 ± 0.09	(fig. 6-25)	(fig. 6-25)
Z2	(fig. 6-25)	-3 ± 0.09	0 ± 0.01	$+3 \pm 0.09$	-3 ± 0.09	-3 ± 0.09	(fig. 6-25)	(fig. 6-25)
Z3	(fig. 6-25)	-3 ± 0.09	0 ± 0.01	$+3 \pm 0.09$	-3 ± 0.09	-3 ± 0.09	(fig. 6-25)	(fig. 6-25)
Z4	(fig. 6-25)	(fig. 6-25)	$+3 \pm 0.09$	-3 ± 0.09	0 ± 0.01	$+3 \pm 0.09$	-3 ± 0.09	(fig. 6-25)

4-13. Panel 6A8 and Miscellaneous Components, Troubleshooting Chart

Item No.	Symptom	Probable trouble	Correction
1	<i>Panel 6A1 troubles; panel 6A1 found not defective (para 4-6):</i> No voltage at terminals 1 and 2 of jack J12.	Fuses F1 and F2 blown; S5, R23, R24, or FL1 defective; or input power to J1 lost.	Check voltage at E30 and E32 (115 volts ac rms). If no voltage, check F1, F2, S5, R23, R24, and FL1. Check input power to J1. If voltage available at E30 and E31, check wiring between E30 and pin 2 of J12 and E32 and pin 1 of J12.
2	Blower does not operate	No power to blower; blower motor defective; 6A8C1 defective.	Check voltage at E30 and E32. If voltage available, check voltage at E31 (175 volts ac rms). If voltage unavailable at E31, check 6A8C1. If voltage available at E31, check blower motor.
3	Correct voltage at E29 (28 volts ac rms) and contacts 6 and 3 of K1 (28 volts ac rms); CALL lamp does not light.	DS5 or K1 defective	Check voltage at terminal 8 of K1 (28 volts ac rms). If voltage present, DS5 defective. If voltage not present, K1 defective.
4	Correct voltage at E29 and contacts 6 and 3 of K1; buzzer does not operate.	K1 or DS6 defective	Check voltage at E28 (28 volts ac rms). If voltage present, DS6 defective. If voltage not present, K1 defective.
5	Correct voltage at terminals 3 and 1 of S2 (28 volts ac rms) and E28; BUZZER OFF switch S2 does not operate to stop buzzer.	S2 defective	Check S2.
6	Correct voltage at E17 (0-600 volts dc); SYSTEM FAULT LOCATOR-MILES switch S3 and MILES switch S9 do not operate correctly.	S3 or S9, R11, R12, or R13 defective.	Check S3, R11, R12, and R13.
7	Correct voltage at E17 (+39 volts dc); TEST ALIGN meter does not operate properly in CABLE V position.	S1, FL7, FL8, M1, 6A8R5, or 6A8R4 defective.	Check voltage at E18 (nearly ground). If present, check FL7, FL8, M1, and S1. If voltage not present, check 6A8R5 and 6A8R4.
8	Correct voltage at terminals 17 and 18 of J12 (-2.4 volts dc); ZERO SET control R2 does not operate properly.	R2 or VR6 defective	Check breakdown voltage of 6A8VR6; it should be +6.2 volts. If correct, check R2.
9	<i>Panel 6A2 troubles; panel 6A2 found not defective (para 4-7):</i> Correct voltage at terminal 7 (-10 volts dc); BUZZER OFF switch S2, buzzer, and CALL lamp do not operate properly.	K1 defective	Check K1.
10	Correct voltage at terminal 24; SERV SEL switch does not operate properly in +10 position.	S7 or 6A8R9 defective	Check S7 and 6A8R9.
11	Correct voltage at terminal 23; SERV SEL switch does not operate properly in -10 position.	S7, 6A8R3, or 6A8R8 defective	Check S7, 6A8R3, and 6A8R8.
	<i>Panel 6A3 troubles; panel 6A3 found not defective (para 4-8):</i>		

Item No.	Symptom	Probable trouble	Correction
12	Correct output at terminal 2; no input at panel 6A5 J10 terminal 1. <i>Panel 6A4 troubles; panel 6A4 found not defective (para 4-9):</i>	C5 defective	Check C5.
13	Correct output at terminal 21; SERV SEL switch does not operate properly in SUM ± position.	6A8R6, S7, or 6A8R7 defective	Check S7, 6A8R7, and 6A8R6.
14	Correct output at terminal 23; SERV SEL switch does not operate properly in BAL position.	S7 or 6A8R6 defective	Check S7 and 6A8R6.
15	No output at terminal 2 <i>Panel 6A5 troubles; panel 6A5 found not defective (para 4-10):</i>	Lightning arrester E4 defective	Check E4 for continuity and correct value.
16	Correct output at terminal 1 no input at panel 6A3 J7 terminal 2.	Same as item 12 above	Same as item 12 above.
17	No output at terminal 3	Lightning arrester E5 defective	Check E5 for continuity and correct value.

CHAPTER 5

GENERAL SUPPORT TESTING PROCEDURES

5-1. General

a. These testing procedures are prepared for use by Electronics Field Maintenance Shops and Electronics Service Organizations responsible for general support maintenance of electronic equipment to determine the acceptability of repaired electronic equipment. These procedures set forth specific requirements that repaired electronic equipment must meet before it is returned to the using organization. The testing procedures may also be used as a guide for the testing of equipment that has been repaired at direct support if the proper tools and test equipment are available. Perform the physical test and inspection (para 5-4) on the TD-204/U. Refer to paragraph 5-5 to perform the unit performance test on the TD-204/U. A summary of performance standards is provided in paragraph 5-6.

b. Each test depends on the preceding test for certain operating procedures. Comply with the instructions preceding the body of each chart before proceeding to the chart. Perform each test in sequence. Do not vary the sequence. For each step, perform all the actions required in the *Control settings* columns, then perform each specific test procedure, and verify it against its performance standard.

5-2. Test Equipment, Materials, and Other Equipment

a. *General.* All test equipment, materials, and other equipment required to perform the testing procedures given in this section are listed in the following charts and are authorized under TA 11-17 and TA 11-100 (11-17).

b. *Test Equipment.*

Nomenclature	Federal stock No.	Technical manual
Multiplexer TD-352/U (2 req).	5905-900-8199	TM 11-5805-367-12

Nomenclature	Federal stock No.	Technical manual
Multiplexer TD-204/U.	5805-900-8200	TM 11-5805-367-12
Restorer, Pulse Form TD-206/G.	5895-868-8078	TM 11-5805-367-12
Headset H-91A/U (4 req).	5965-699-6871	TM 11-5805-367-12

c. *Materials.*

Materials	Federal stock No.
Cable, Special Purpose, Electrical CX-4245/G (¼-mile reel) (8 req).
Cable Assembly, Radio Frequency CG-1040 B/U (5 ft) (16 req).	5995-913-0509
Cable Assembly, Radio Frequency CG-2437/TCC, (10 ft) (4 req).	5995-916-2252
Cable Assembly, Radio Frequency CG-2438/TCC, (10 ft) (4 req).	

d. *Other Equipment.* Electric Light Assembly MX-1292/PAQ, FSN 0695-537--4470, TM 11-5540.

5-3. Modification Work Orders

The performance standards listed in the tests (paras 5-4 and 5-5) assume that no modification work orders have been performed. A listing of current modification work orders will be found in DA Pam 310-4.

5-4. Physical Tests and Inspections

a. *Test Equipment and Materials.* Electric Light Assembly MX-1292/PAQ.

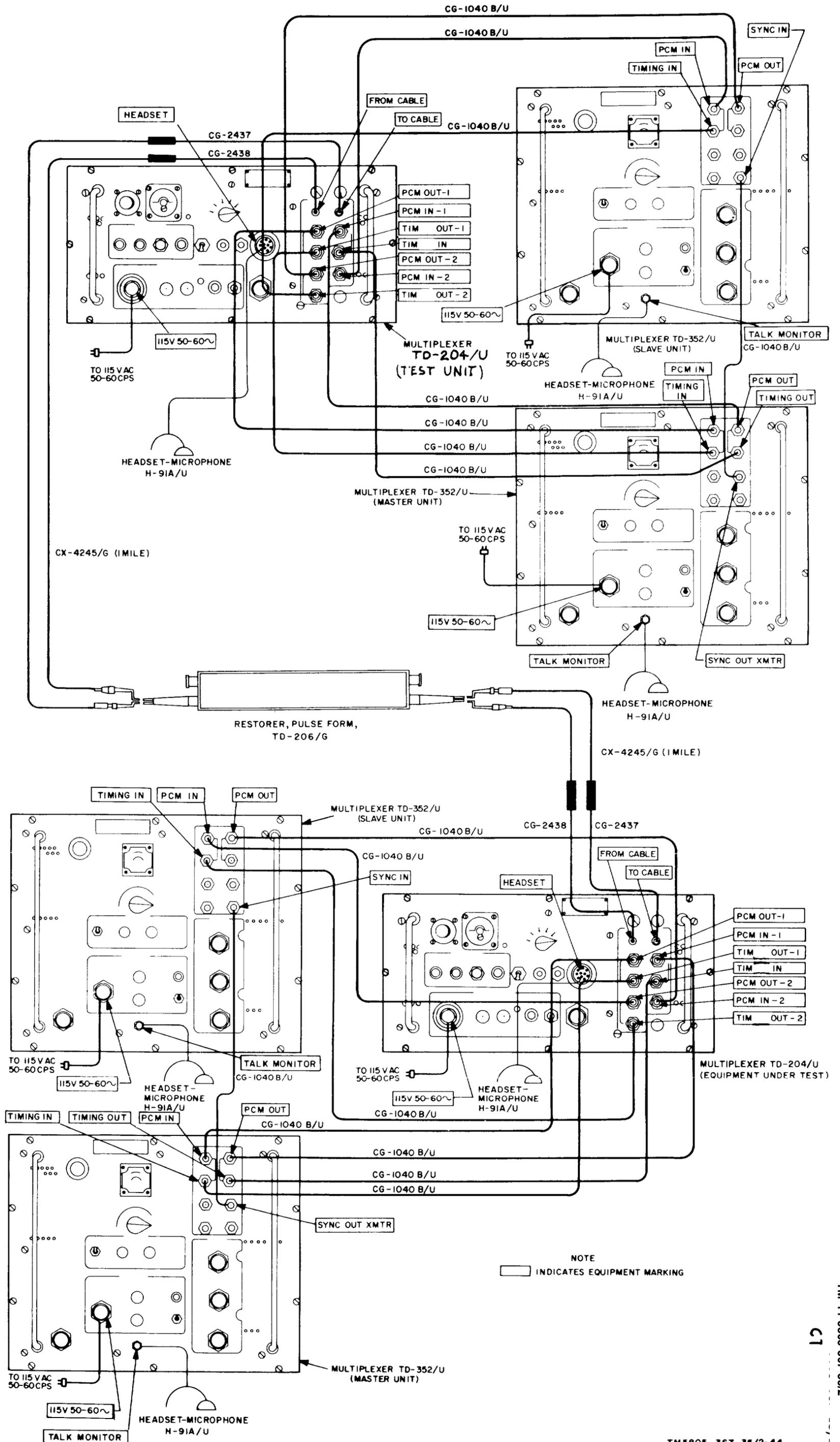
b. *Test Connections and Conditions.*

- (1) Do not make any connections to the equipment.
- (2) Perform the following checks when repairs are completed, before reassembly of the equipment.
- (3) Connect the MX-1292/PAQ to a 115-volt, 00-cps source, and install the wide band transmission filter.

c. Test Procedure.

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
1	N/A	Controls may be in any position.	<p>a. Inspect front panel for evidence of physical damage, loose or missing parts, screws, or panel fasteners.</p> <p>b. Inspect connectors and plugs for cleanliness and evidence of physical damage.</p> <p>c. Remove and check all fuses for proper size and amperage rating.</p> <p>d. Check all filter capacitors for evidence of overheating.</p> <p>e. Check all resistors for evidence of overheating.</p> <p>f. Inspect all wiring and cabling for worn or frayed insulation.</p> <p>g. Inspect all metal surfaces for conditions of finish.</p> <p><i>Note.</i> Touchup paint is recommended in lieu of refinishing whenever practical (TB SIG 364).</p>	<p>a. Front panel is complete and not damaged.</p> <p>b. Connectors and plugs are clean and not damaged.</p> <p>c. Fuses are proper size and rated as indicated on panel markings.</p> <p>d. Capacitors show no evidence of leakage.</p> <p>e. Resistors show no signs of discoloration due to overheating.</p> <p>f. Wiring and cabling are free of cuts and frays.</p> <p>g. All metal surfaces intended to be painted do not show bare metal. Panel lettering is legible.</p>
2	N/A	Controls may be in any position.	<p>Check the equipment for applicable modification work orders (refer to DA Pam 310-4 for a list of MWO's).</p>	<p>If MWO is performed, MWO number appears on equipment.</p>
3	MX 1292/PAQ 245V FOR M. V. LAMP: ON.	Controls may be in any position.	<p>a. Expose equipment to direct rays of MX-1292/PAQ, and inspect condition of moisture-fungiproofing epoxy.</p> <p><i>Note.</i> Moisture-fungiproofing appears blue-green under rays of MX-1292/PAQ. Epoxy appears milky-white, but blue-gray if defective.</p> <p>b. Operate 245V for M.V. LAMP switch of MX-1292/PAQ to OFF.</p>	<p>a. All components, wiring, and chassis surfaces are completely covered with moisture-fungiproofing epoxy with no evidence of it on connectors or switch contacts.</p> <p><i>Note.</i> Do not apply moisture-fungiproofing epoxy to parts not originally treated with it.</p> <p>b. None.</p>

Figure 5-1. Multiplexer TD-204/U, performance test setup.



5-5. TD-204/U Unit Performance Test (fig. 5-1)

a. Test Equipment and Materials.

- (1) Multiplexer TD-352/U (2 req).
- (2) Multiplexer TD-204/U.
- (3) Cable, Special Purpose, Electrical CX-4245/G (1/4-mile reel) (8 req).
- (4) Cable Assembly, Radio Frequency CG-1040B/U (5 ft) (16 req).

- (5) Cable Assembly, Radio Frequency CG-2437/TCC (10 ft) (4 req).
- (6) Cable Assembly, Radio Frequency CG-2438/TCC (10 ft) (4 req).
- (7) Restorer, Pulse Form TD-206/G.
- (8) Headset H-91A/U (4 req).

b. Test Connections and Conditions. Connect the equipment under test initially as shown in figure 5-1.

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
1	<p>TD-352/U (master units) AC POWER switch: ON. MASTER-SLAVE switch: MASTER.</p> <p>TD-352/U (slave units) AC POWER switch: ON. MASTER-SLAVE switch: SLAVE.</p> <p>TD-204/U (at B) AC POWER switch: ON. CABLE POWER switch: ON.</p> <p>TALK-OFF-SIG switch: TALK.</p> <p>MILE switches (panels 6A4 & 6A5): 1.</p> <p>TRAFFIC SEL: 24.</p>	<p>TD-204/U: AC POWER switch: ON. CABLE POWER switch: ON. TALK-OFF-SIG switch: OFF.</p> <p>MILE switches (panels 6A4 & 6A5): 1. TRAFFIC SEL: 24.</p>	<p><i>Order-wire tests:</i></p> <p><i>a.</i> Operate TALK-OFF-SIG switch on equipment under test to SIG.</p> <p><i>b.</i> Release TALK-OFF-SIG switch on equipment under test to TALK. Operator at equipment under test talks to operator at TD-204/U at B.</p> <p><i>c.</i> Operate TALK-OFF-SIG switch on TD-204/U at B to SIG.</p> <p><i>d.</i> Release TALK-OFF-SIG switch on TD-204/U at B to OFF.</p> <p><i>Communications tests:</i></p> <p><i>a.</i> Operator at TD-352/U (master unit) at A talks with operator at TD-352/U (master unit) at B.</p> <p><i>b.</i> Operator at TD-352/U (slave unit) at A talks with operator at TD-352/U (slave unit) at B.</p> <p><i>c.</i> Operate TRAFFIC SEL switch on equipment under test and TD-204/U at B to 12. Operate AC POWER switch on TD-352/U (slave unit) at A and B to OFF.</p> <p><i>d.</i> Repeat <i>a</i> above</p> <p><i>e.</i> Operate CABLE POWER switch on equipment under test and TD-204/U at B to OFF. Operate AC POWER switch on equipment under test to OFF. Remove equipment under test from test setup.</p>	<p><i>a.</i> Buzzer sounds and CALL lamp lights at equipment under test and at TD-204/U at B.</p> <p><i>b.</i> A conversation at an audible level and free of distortion should take place. <i>Note.</i> Excessive audio level and distortion indicates misalignment of the CRL potentiometer on panel 6A2.</p> <p><i>c.</i> Same as <i>a</i> above.</p> <p><i>d.</i> None.</p> <p><i>a.</i> A conversation at an audible level and free of clicks should take place.</p> <p><i>b.</i> Same as <i>a</i> above.</p> <p><i>c.</i> None.</p> <p><i>d.</i> Same as <i>a</i> above.</p> <p><i>e.</i> None.</p>
2	<p>Same as step 1.</p>	<p>Same as step 1</p>		

5-6. Multiplexer TD-204/U, Summary of Performance Standards

Test No.	Description	Performance standard	Test data
1	<i>Order-wire tests:</i>		
a	TALK-OFF-SIG switch on equipment under test at SIG.	Buzzer sounds and CALL lamp lights at equipment under test and at the TD-204/U at B.	
b	TALK-OFF-SIG switch on equipment under test at TALK; conversation held between equipment under test and the TD-204/U at B.	A conversation at an audible level and free of distortion should take place.	
c	TALK-OFF-SIG switch on the TD-204/U at B at SIG.	Same as a above.	
2	<i>Communications test:</i>		
a	Conversation held between TD-352/U master units at A and B.	A conversation at an audible level and free of clicks should take place.	
b	Conversation held between TD-352/U slave units at A and B.	Same as a above.	
c	Repeat step a above with TRAFFIC SEL switches on equipment under test and the TD-204/U at B set to 12, and with AC POWER switches on TD-352/U slave units at A and B at OFF.	Same as a above.	

CHAPTER 6

DEPOT OVERHAUL STANDARDS

6-1. Applicability of Depot Overhaul Standards

The depot overhaul standards are designed to measure the performance capability of a repaired equipment. Equipment that meets the minimum standards will have performance capabilities equivalent to that of new equipment.

6-2. Applicable References

a. Repair Standards. Applicable procedures of the depot performing these tests and the general standards for repaired electronic equipment given

in TB SIG 355-1, TB SIG 355-2, and TB SIG 355-3 form a part of the requirements for testing this equipment,

b. Modification Work Orders. Perform all modification work orders applicable to this equipment before making the tests specified. DA Pam 3104 lists all available MWO'S.

6-3. Depot Overhaul Standard

When depot repair and overhaul has been completed, perform the procedures in chapter 5. When the equipment has been tested, repackage it for stockage.

Figure 6-1. Panel 6A2, top view.

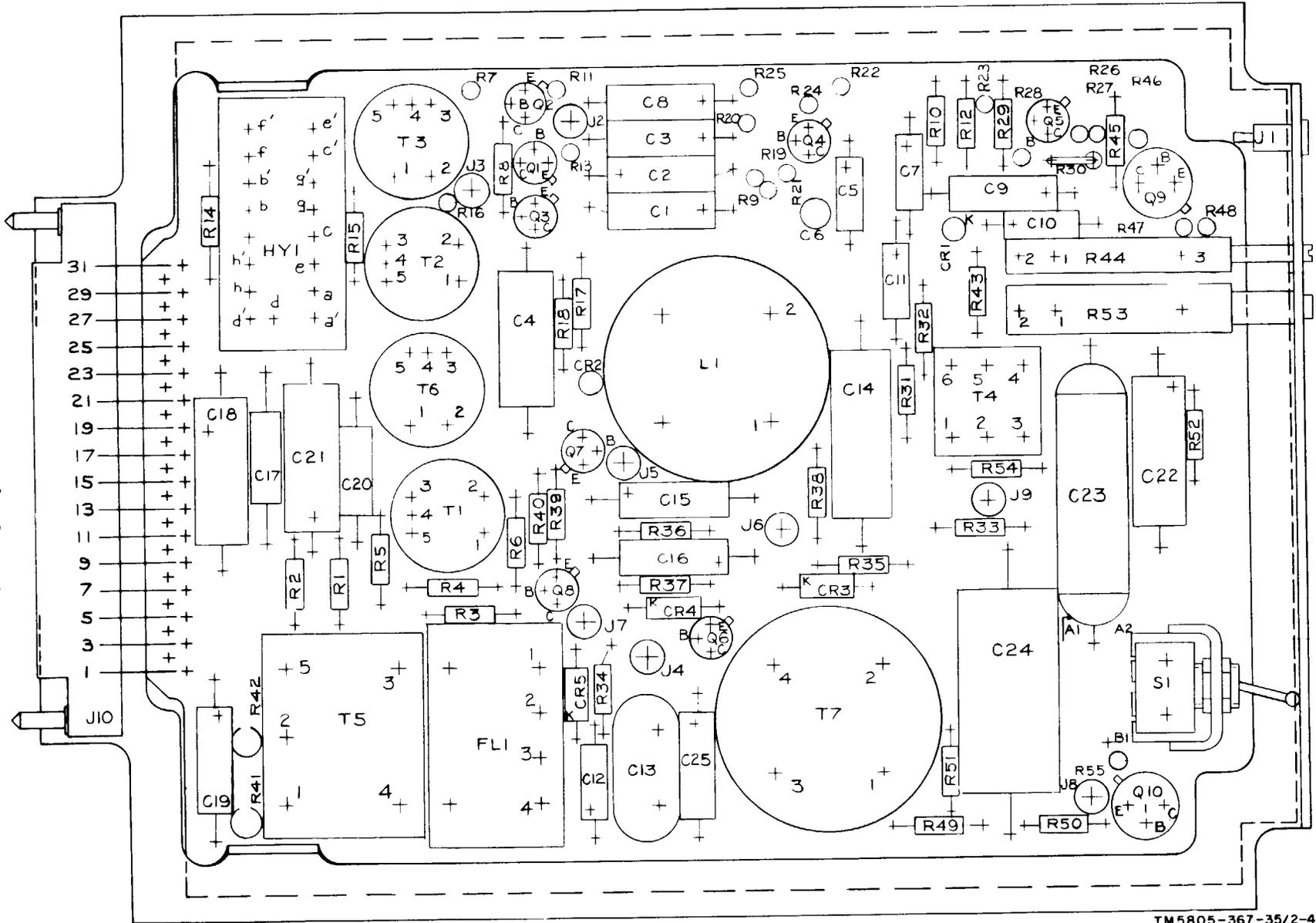
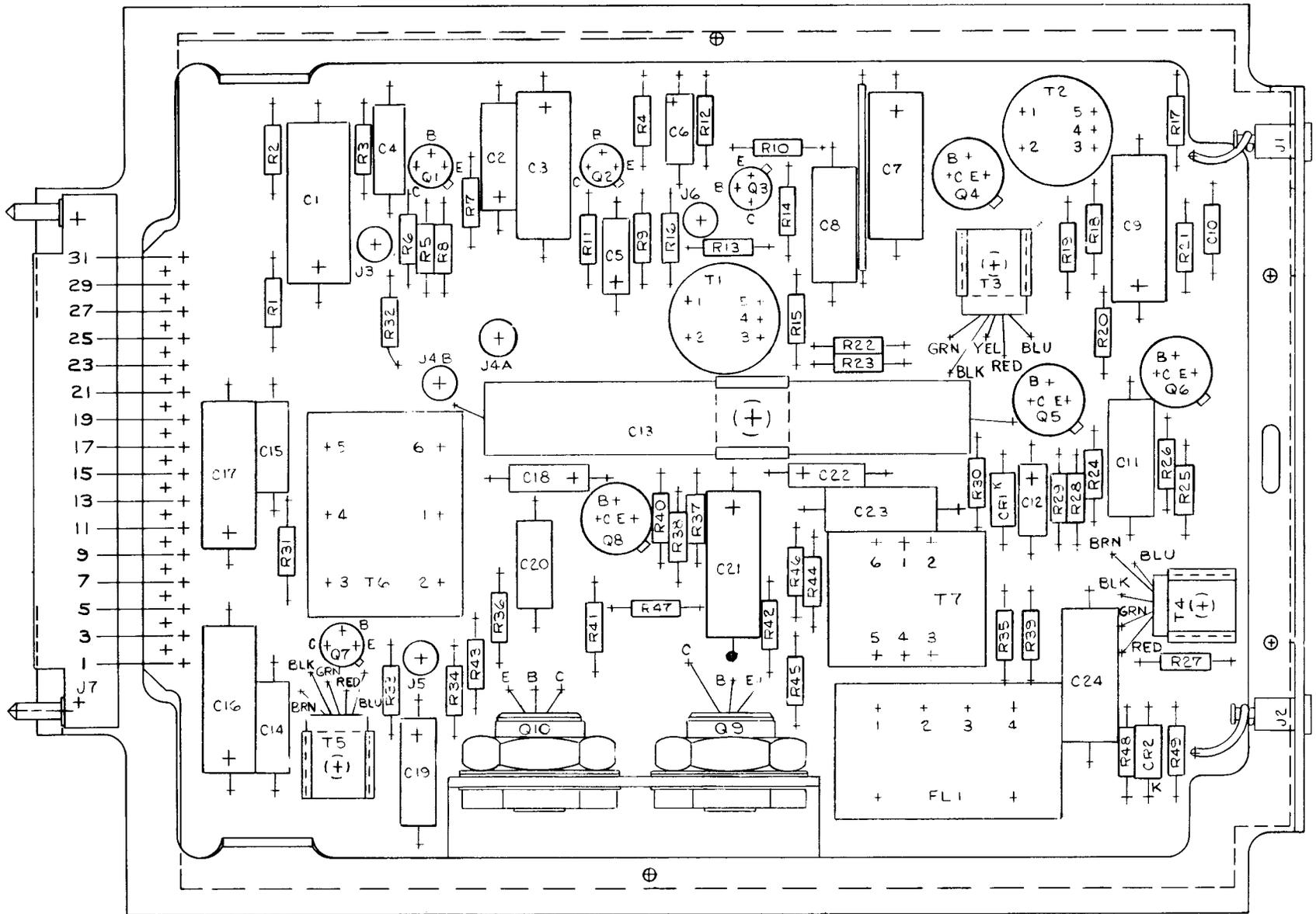


Figure 6-2. Panel 6A3, top view.



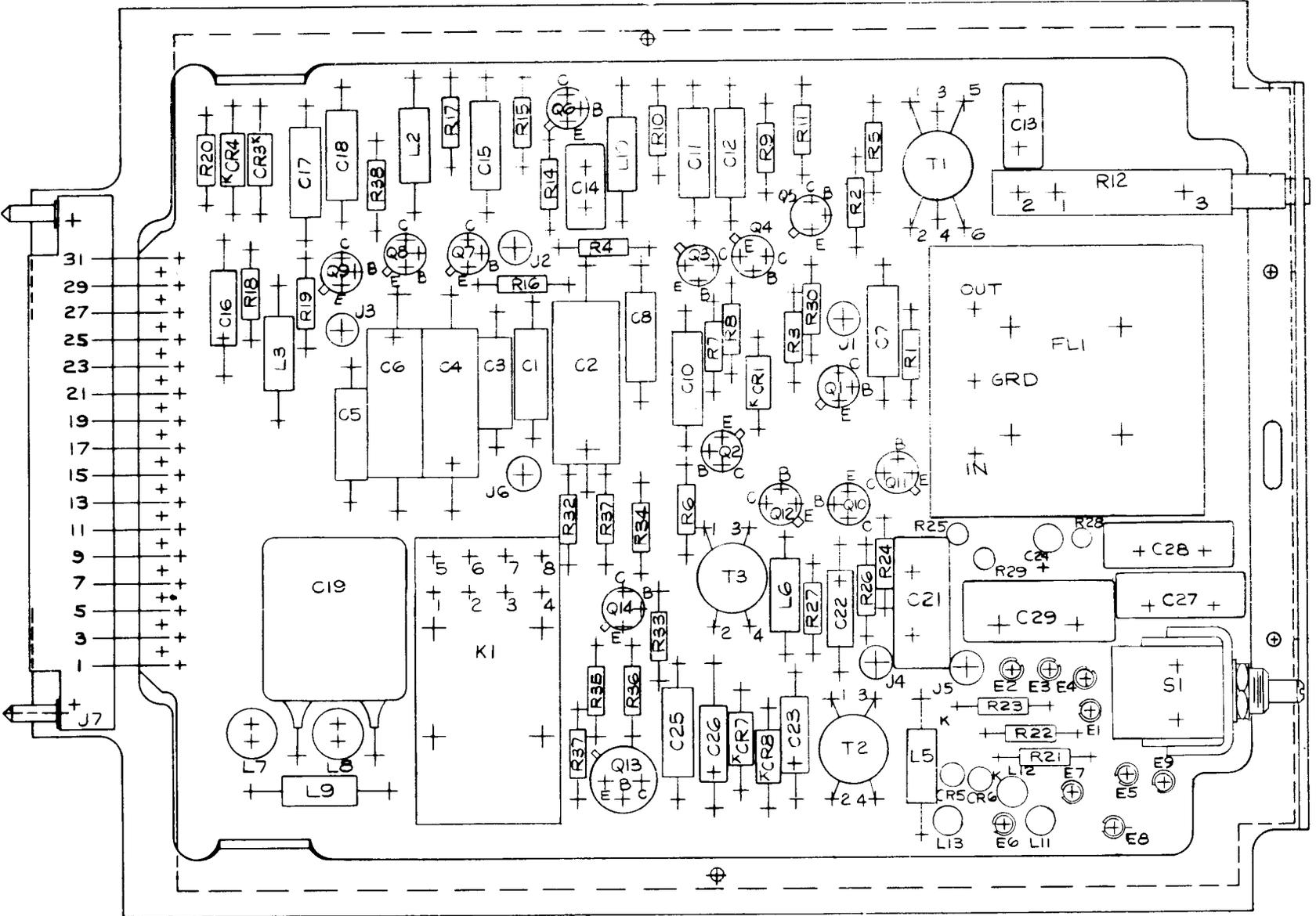


Figure 6-3. Panel 6A4, top view.

Figure 6-4. Panel 6A5, top view.

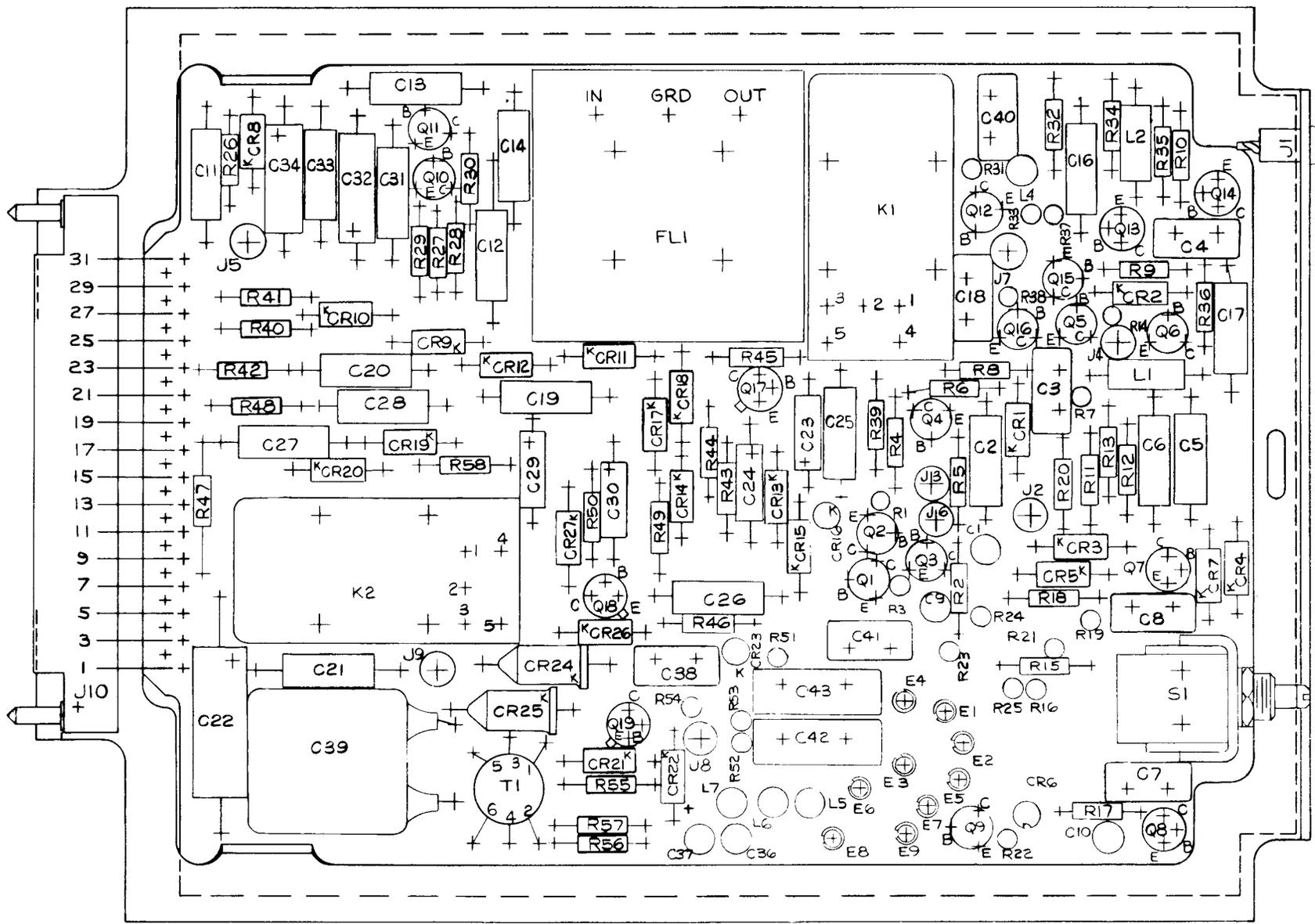
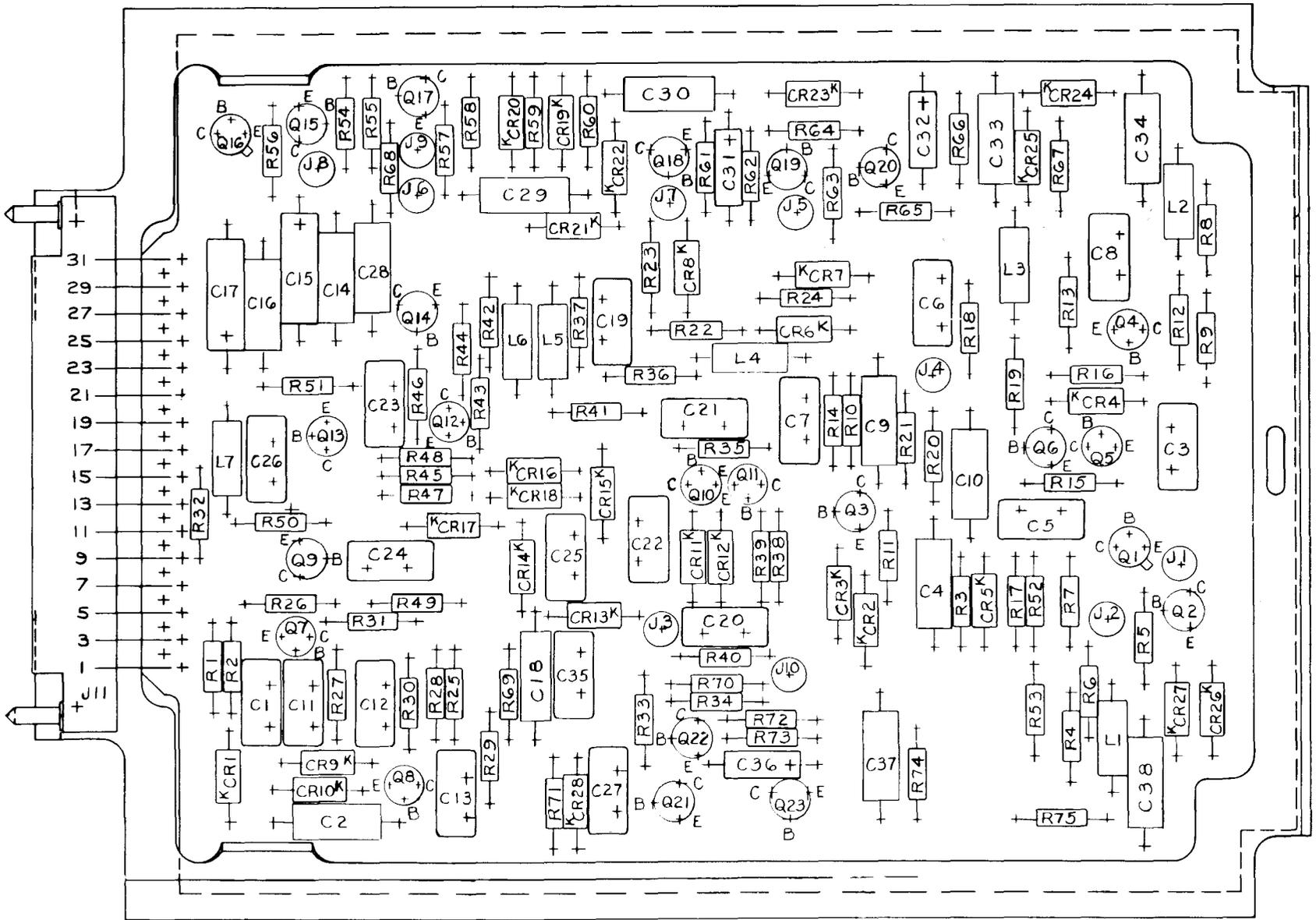
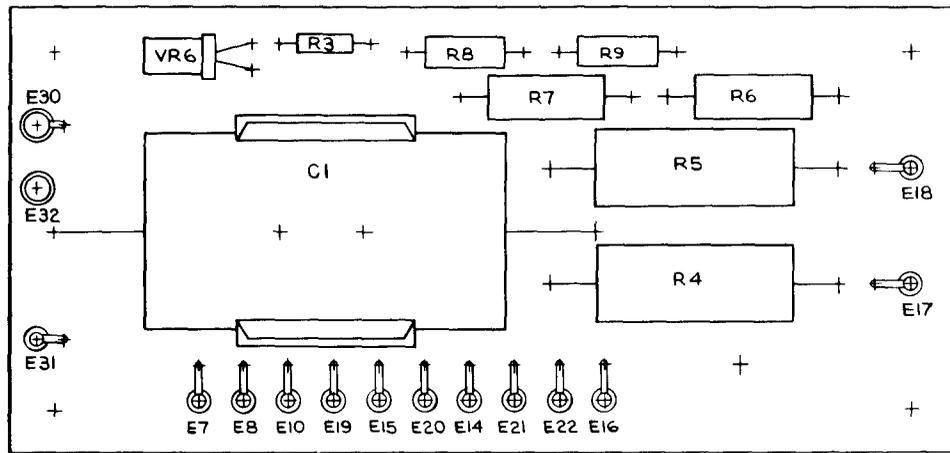


Figure 6-5. Panel 6A6, top view.

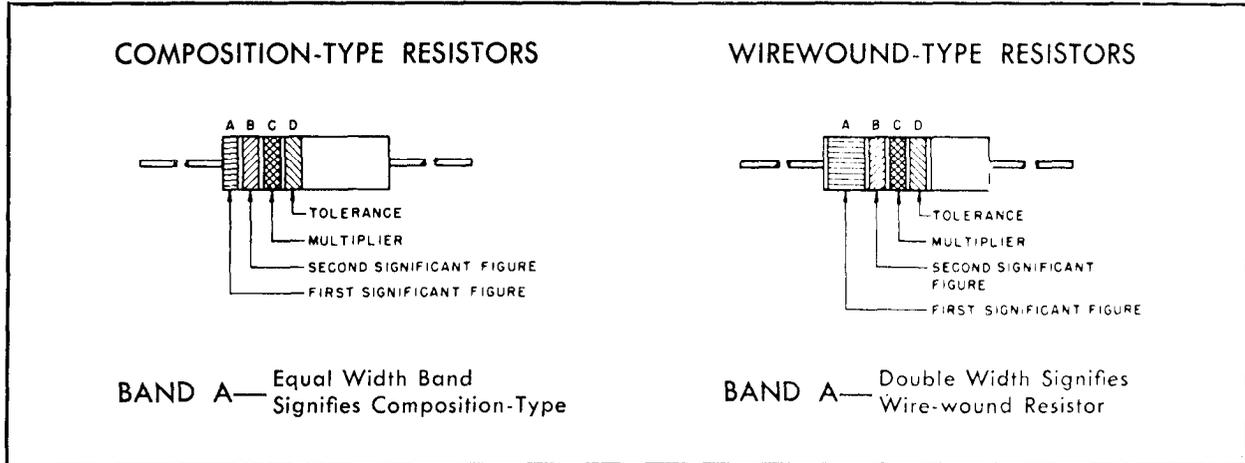




TM5805-367-35/2-60

Figure 6-6. Panel 6A8, top view.

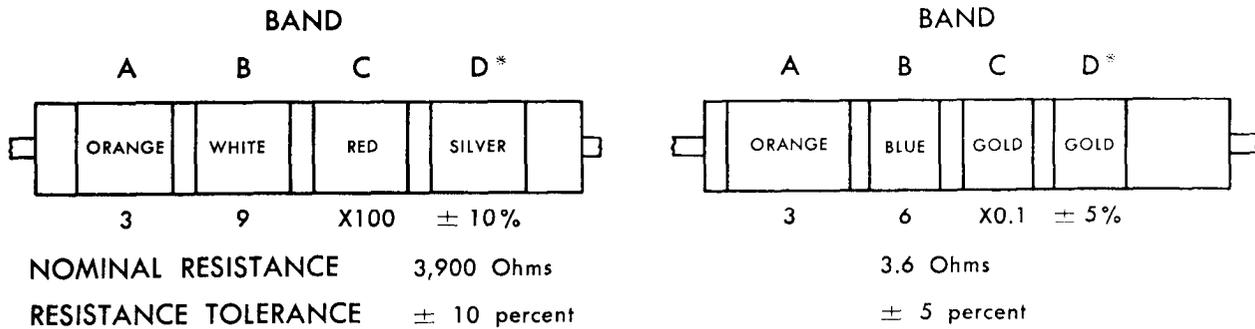
COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS



COLOR CODE TABLE

BAND A		BAND B		BAND C		BAND D*	
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)
BLACK	0	BLACK	0	BLACK	1		
BROWN	1	BROWN	1	BROWN	10		
RED	2	RED	2	RED	100		
ORANGE	3	ORANGE	3	ORANGE	1,000		
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	± 10
GREEN	5	GREEN	5	GREEN	100,000	GOLD	± 5
BLUE	6	BLUE	6	BLUE	1,000,000		
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7				
GRAY	8	GRAY	8	SILVER	0.01		
WHITE	9	WHITE	9	GOLD	0.1		

EXAMPLES OF COLOR CODING



STD-R2

*If Band D is omitted, the resistor tolerance is ± 20%, and the resistor is not Mil-Std.

Figure 6-7. MIL-STD resistor color code marking.

APPENDIX

REFERENCES

DA Pam 310-1	Consolidated Index of Army Publications and Blank Forms
TB SIG 222	Solder and Soldering
TB SIG 355-1	Depot Inspection Standard for Repaired Signal Equipment
TB SIG 355-2	Depot Inspection Standard for Refinishing Repaired Signal Equipment
TB SIG 355-3	Depot Inspection Standard for Moisture and Fungus Resistant Treatment
TM 11-664	Theory and Use of Electronic Test Equipment
TM 11-2044	Attenuators TS-402/U and TS-402A/U
TM 11-2150	Telephone Carrier Systems Using Terminals, Telephone AN/TCC-7 and AN/TCC-50; Repeater, Telephone AN/TCC-8 (AN/TCC-21); Repeater, Telephone AN/TCC-11, and Telephone Test Set TS-712/TCC-11
TM 114000	Troubleshooting and Repair of Radio Equipment
TM 11-5540	Electric Light Assembly, MX-1292/PAQ (NSN 6995-00-378-5499)
TM 11-5805-367-12	Operator's and Organizational Maintenance Manual Multiplexer, TD-202/U (NSN 5805-00-884-2176), TD-203/U (5805-00-884-2177), TD-204/U (5805-00-900-8200), TD-352/U (5805-00-900-8199) and TD-353/U (5805-00-985-9153) Restorers, Pulse Form, TD-206/G (5805-00-868-8078) and TD-206B/G (5805-01-020-2251) and Converters, Telephone Signal, CU-1548/G (5805-00-069-8795) and CU-1548A/G (5805-00-069-8795) (Reprinted W/Basic Incl C1-6)
TM 11-6625-218-12	Organizational Maintenance Manual for Frequency Meter, AN/TSM-16
TM 11-6625-218-35	Direct Support, General Support, and Depot Maintenance Manual: Frequency Meter AN/TSM-16 (FSN 6625-542-1666)
TM 11-6625-320-12	Operator's and Organizational Maintenance Manual: Voltmeter, Meter ME-30A/U and Voltmeters, Electronic ME-30B/U, ME-30C/U, and ME-30E/U
TM 11-6625-320-35	Direct Support, General Support, and Depot Maintenance Manual: Voltmeter, Meter ME-30A/U and Voltmeters, Electronic ME-30B/U, ME-30C/U and ME-30E/U
TM 11-6625-366-15	Operator's, Organizational, Direct Support, General Support and Depot Maintenance Manual: Multimeter TS-352B/U (NSN 6625-00-553-0142) (Reprinted W/Basic Incl C1-4)
TM 11-6625-535-15	Operator's, Organizational, Direct Support, General Support and Depot Maintenance Manual: Oscilloscope AN/USM-140A
TM 11-6625-535-15-1	Organizational, Direct Support, General Support and Depot Maintenance Manual (Including Repair Parts and Special Tools Lists): Oscilloscope AN/USM-140B, AN/USM-140C, AN/USM-14A and AN/USM-141B (Reprinted W/Basic Incl C1-3)
TM 11-6625-539-15	Operator's, Organizational, Field and Depot Maintenance Manual: Transistor Set, TS-1836/U

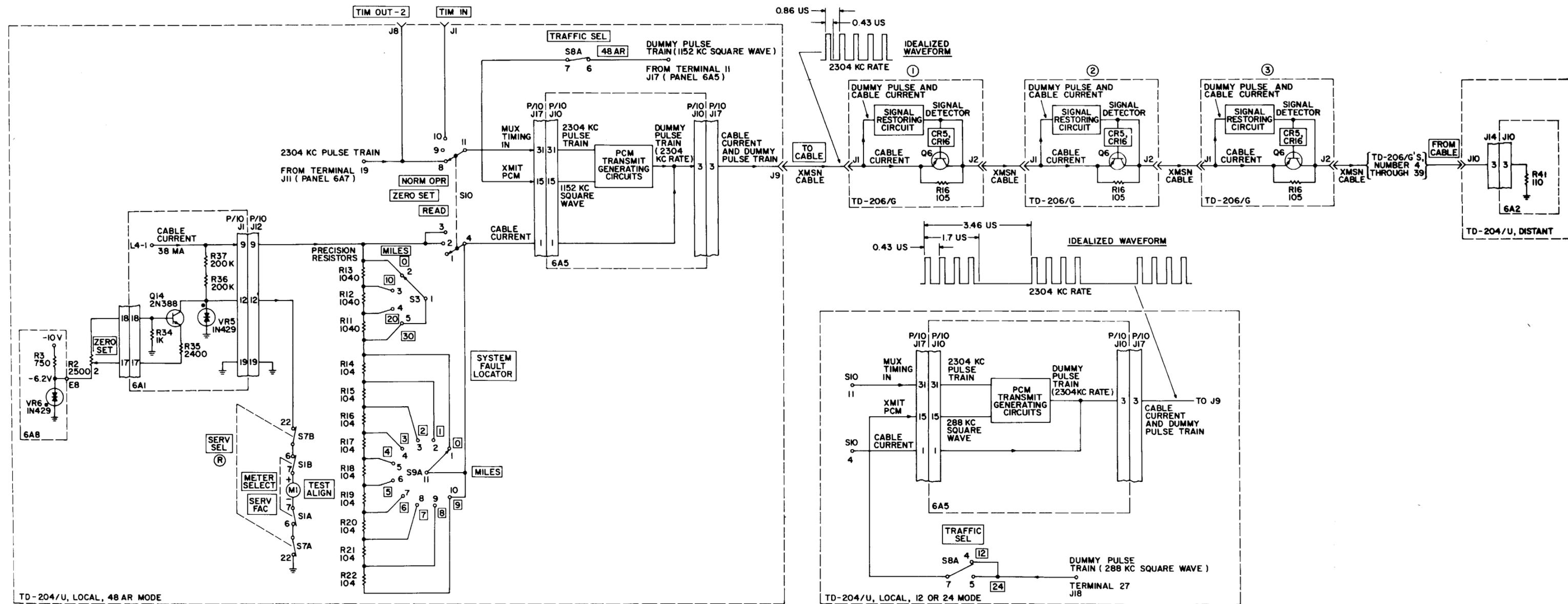
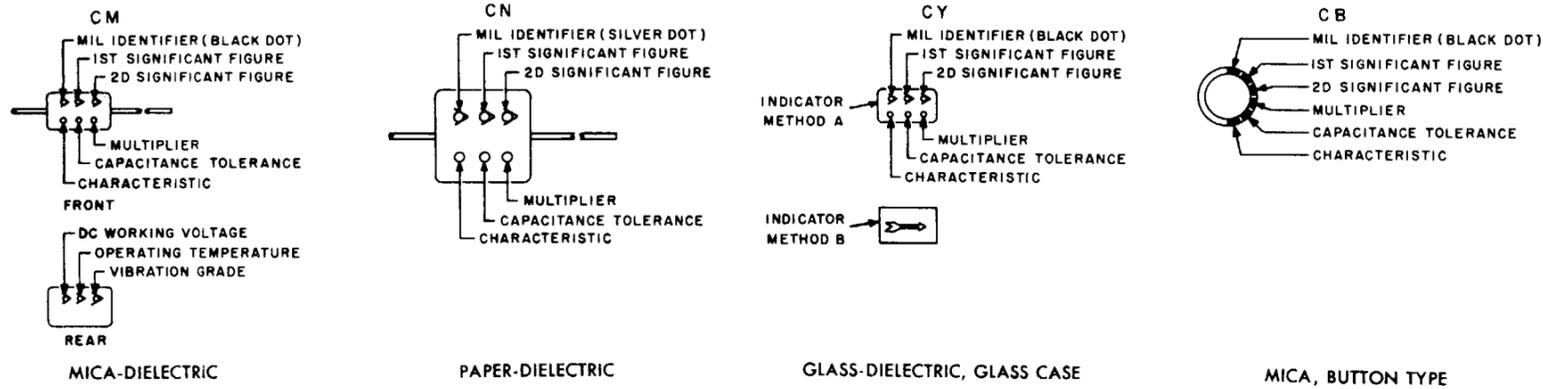


Figure 6-30. Restorer, Pulse Form TD-206/G fault-locating system, functional diagram.

COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS

GROUP I Capacitors, Fixed, Various-Dielectrics, Styles CM, CN, CY, and CB



COLOR CODE TABLES

TABLE I - For use with Group I, Styles CM, CN, CY and CB

COLOR	MIL ID	1st SIG FIG	2nd SIG FIG	MULTIPLIER ¹	CAPACITANCE TOLERANCE				CHARACTERISTIC ²				DC WORKING VOLTAGE	OPERATING TEMP. RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CY	CB	CM	CM	CM
BLACK	CM, CY, CB	0	0	1			± 20%	± 20%		A				-55° to +70°C	10-55 cps
BROWN		1	1	10					B	E		B			
RED		2	2	100	± 2%		+ 2%	+ 2%	C		C			-55° to +85°C	
ORANGE		3	3	1,000		+ 30%			D			D	300		
YELLOW		4	4	10,000					E					-55° to +125°C	10-2,000 cps
GREEN		5	5		± 5%				F				500		
BLUE		6	6											-55° to +150°C	
PURPLE (VIOLET)		7	7												
GREY		8	8												
WHITE		9	9												
GOLD				0.1			± 5%	± 5%							
SILVER	CN				± 10%	± 10%	± 10%	± 10%							

GROUP II Capacitors, Fixed Ceramic-Dielectric (General Purpose) Style CK

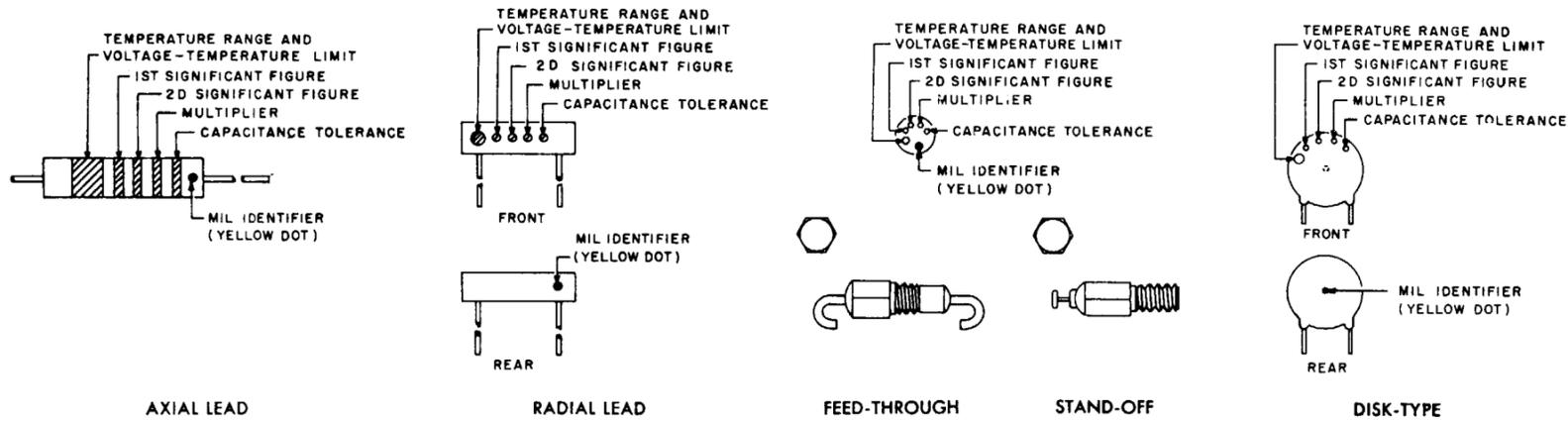


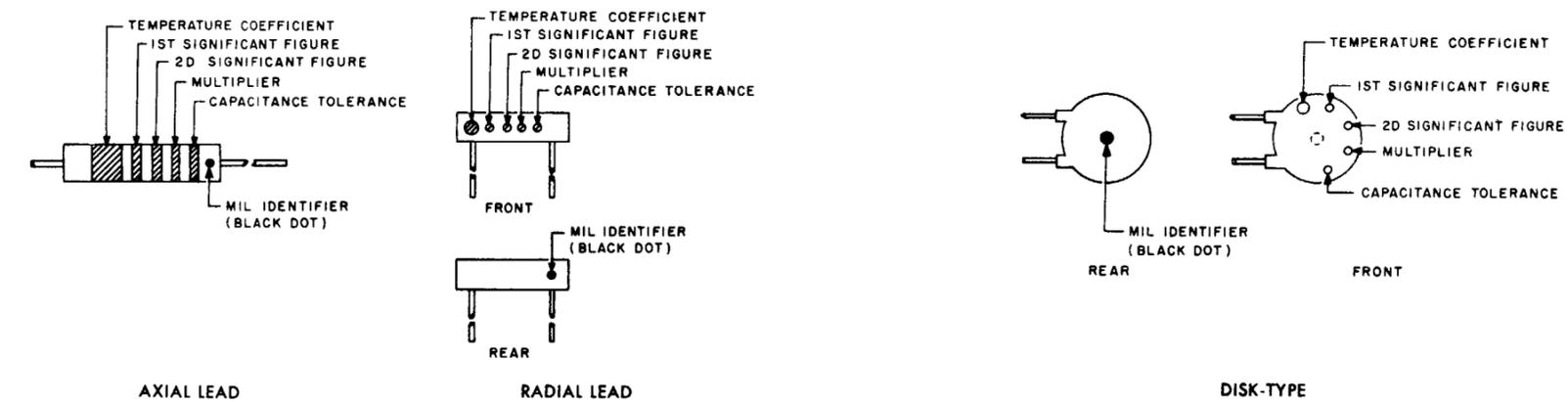
TABLE II - For use with Group II, General Purpose, Style CK

COLOR	TEMP. RANGE AND VOLTAGE - TEMP. LIMITS ³	1st SIG FIG	2nd SIG FIG	MULTIPLIER ¹	CAPACITANCE TOLERANCE	MIL ID
BLACK		0	0	1	± 20%	
BROWN	AW	1	1	10	± 10%	
RED	AX	2	2	100		
ORANGE	BX	3	3	1,000		
YELLOW	AY	4	4	10,000		CK
GREEN	CZ	5	5			
BLUE	BV	6	6			
PURPLE (VIOLET)		7	7			
GREY		8	8			
WHITE		9	9			
GOLD						
SILVER						

TABLE III - For use with Group III, Temperature Compensating, Style CC

COLOR	TEMPERATURE COEFFICIENT ⁴	1st SIG FIG	2nd SIG FIG	MULTIPLIER ¹	CAPACITANCE TOLERANCE		MIL ID
					Capacitances over 10uuf	Capacitances 10uuf or less	
BLACK	0	0	0	1		± 2.0uuf	CC
BROWN	-30	1	1	10	± 1%		
RED	-80	2	2	100	± 2%	± 0.25uuf	
ORANGE	-150	3	3	1,000			
YELLOW	-220	4	4				
GREEN	-330	5	5		± 5%	± 0.5uuf	
BLUE	-470	6	6				
PURPLE (VIOLET)	-750	7	7				
GREY		8	8	0.01			
WHITE		9	9	0.1	± 10%		
GOLD	+100					± 1.0uuf	
SILVER							

GROUP III Capacitors, Fixed, Ceramic-Dielectric (Temperature Compensating) Style CC



1. The multiplier is the number by which the two significant (SIG) figures are multiplied to obtain the capacitance in uuf.
2. Letters indicate the Characteristics designated in applicable specifications: MIL-C-5, MIL-C-91, MIL-C-11272, and MIL-C-10950 respectively.
3. Letters indicate the temperature range and voltage-temperature limits designated in MIL-C-11015.
4. Temperature coefficient in parts per million per degree centigrade.

Figure 6-8. MIL-STD capacitor color code marking.



Figure 6-9(2). Multiplexer TD-204/U, schematic diagram
(part 2 of 2).

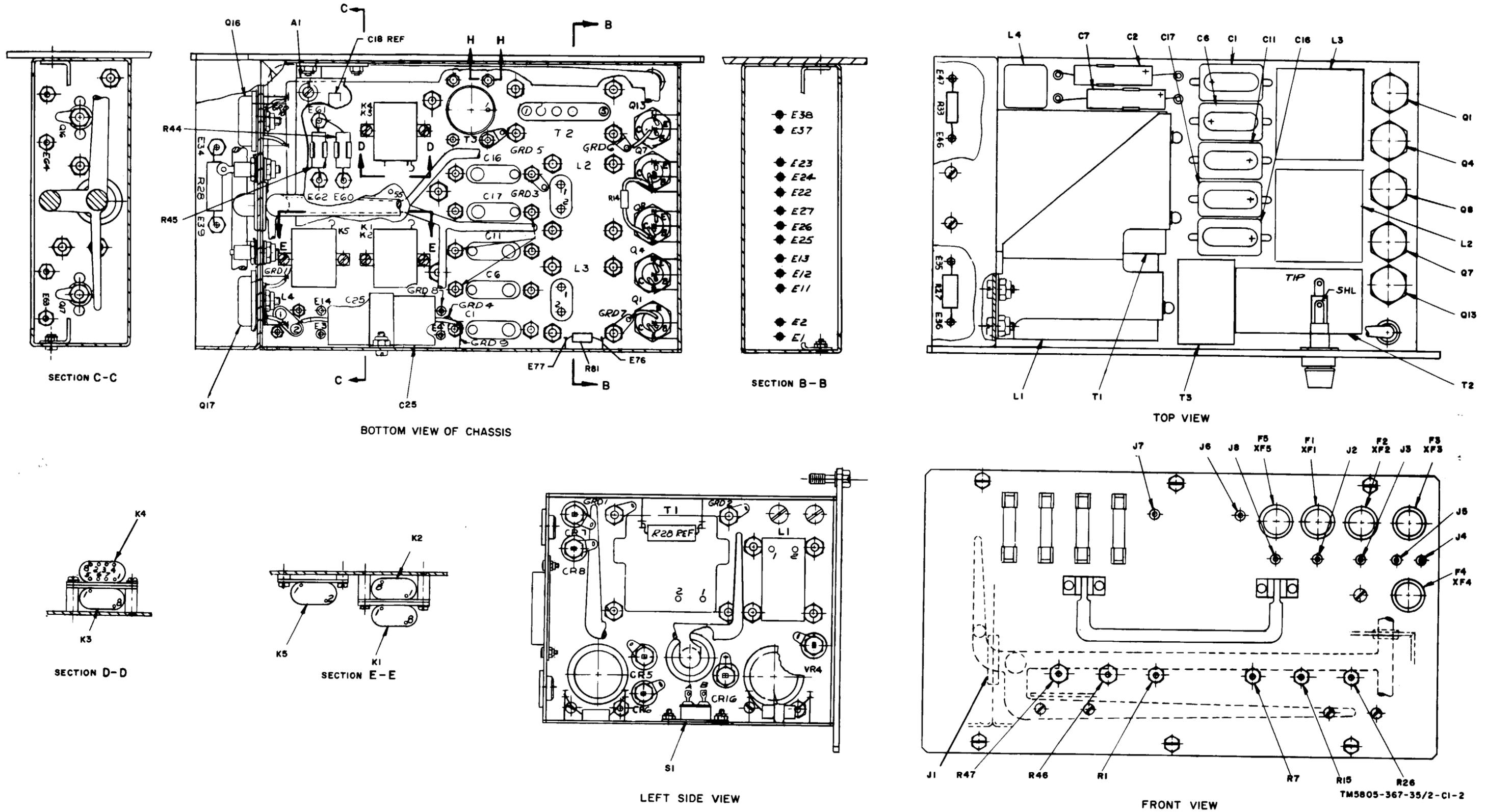


Figure 6-10①. Panel 6A1, component location diagram (part 1 of 2).

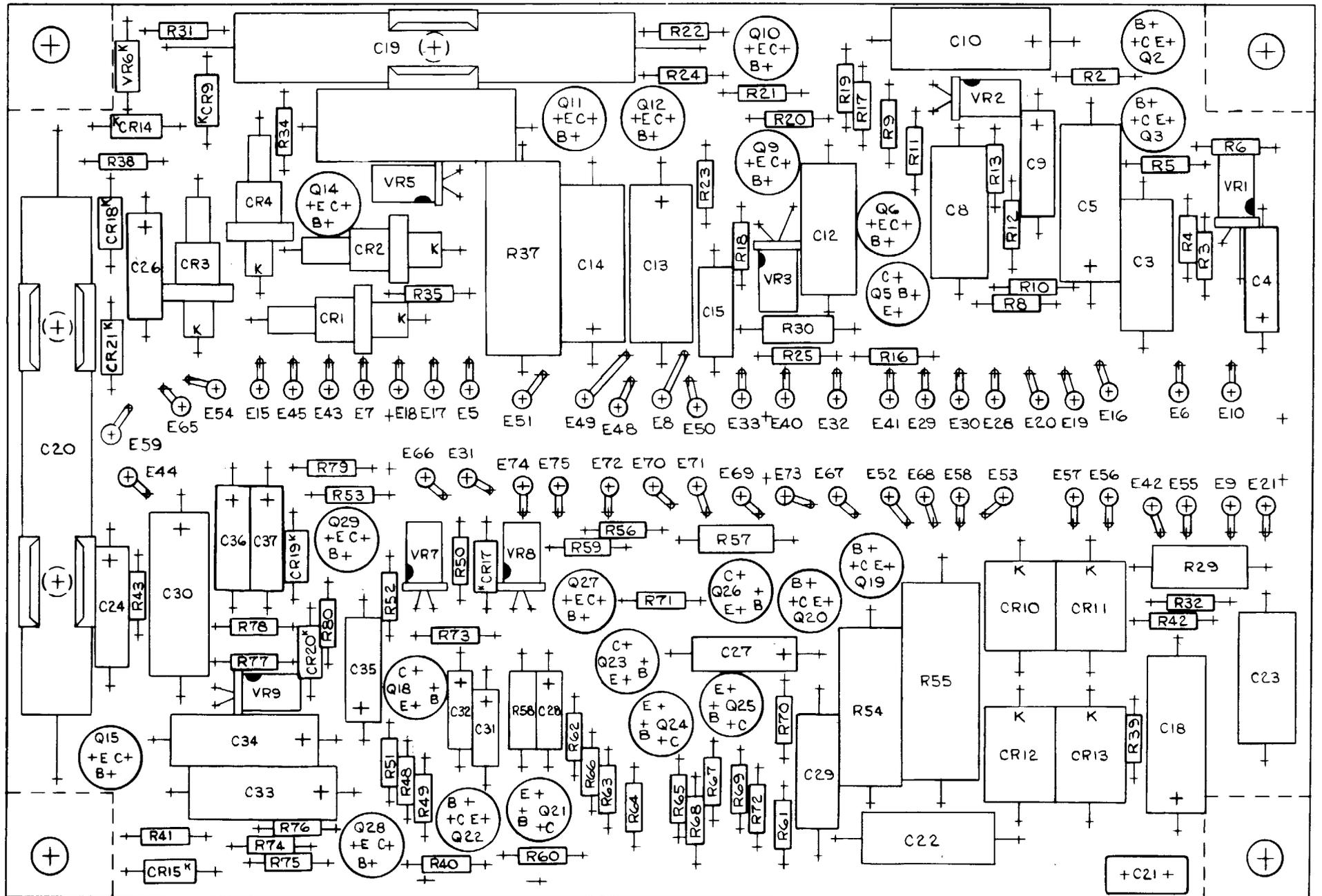
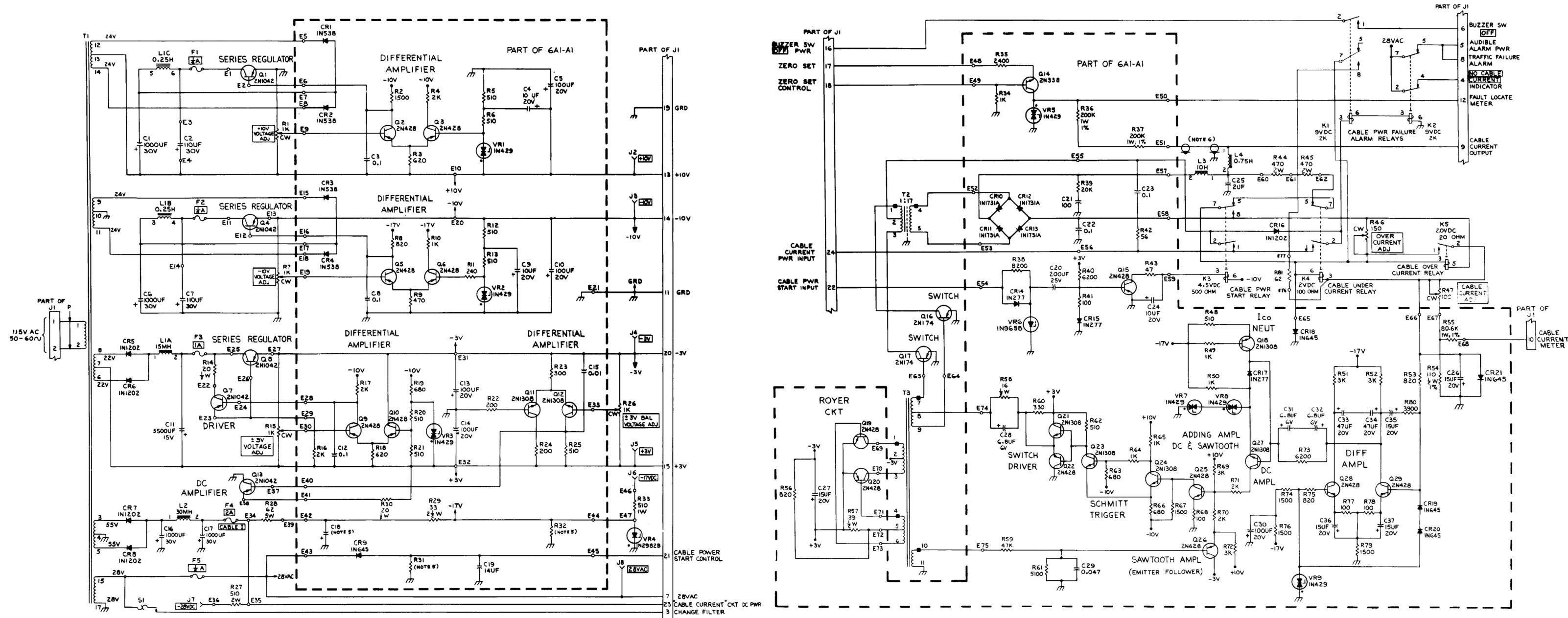


Figure 6-10. Panel 6A1, component location diagram
(part 2 of 2).



- NOTES:
- PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S)
 - UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICRO-MICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 - UNLESS OTHERWISE INDICATED ALL RESISTORS ARE $\frac{1}{4}$ WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 - INDICATES EQUIPMENT MARKING
 - COMPONENT VALUES FOR C18, R31, AND R32 ARE AS FOLLOWS:

COMPONENT	TD-204/U SERIAL NO. EFFECTIVITY	
	1 THROUGH 188	189 AND ON
C18	100 UF 20V	47 UF 35V
R31	3300	6800
R32	1K	3300

- COAX IS USED BETWEEN E51 AND TERMINAL 1 OF L4 STARTING WITH TD-204/U SERIAL NO. 189 AND ON.

Figure 6-11. Panel 6A1, schematic diagram.

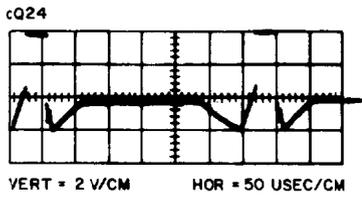
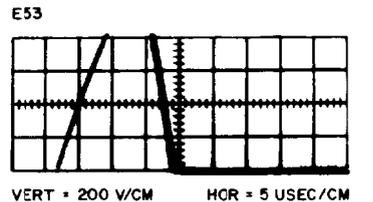
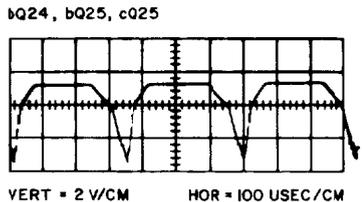
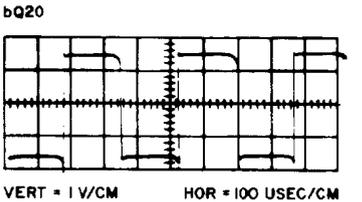
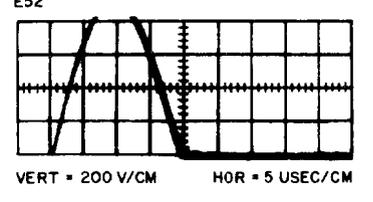
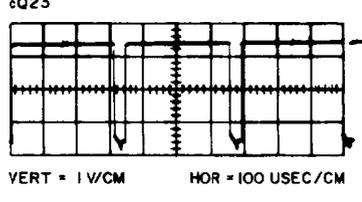
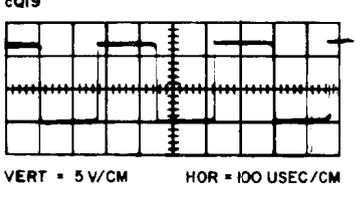
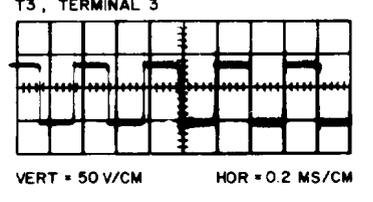
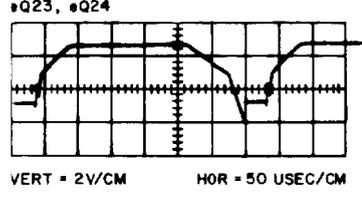
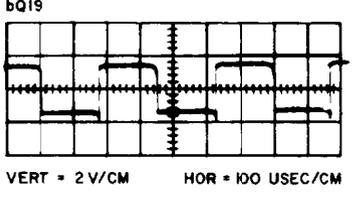
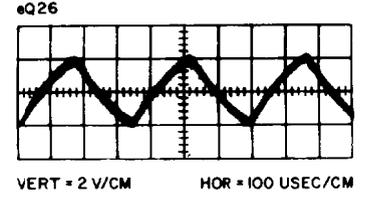
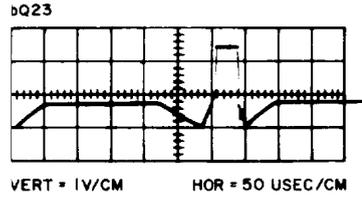
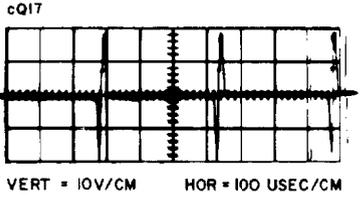
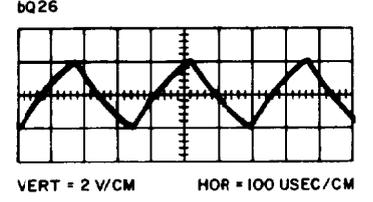
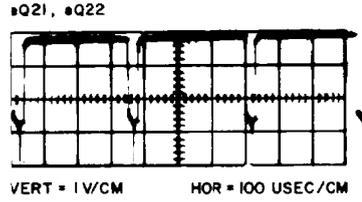
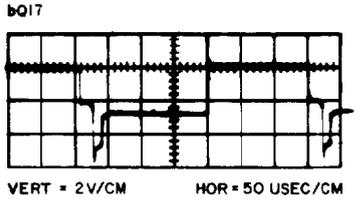
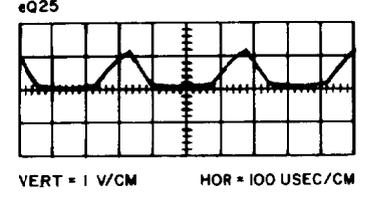
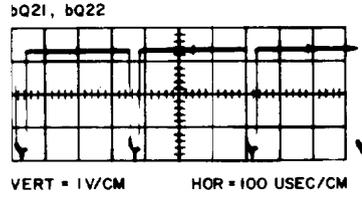
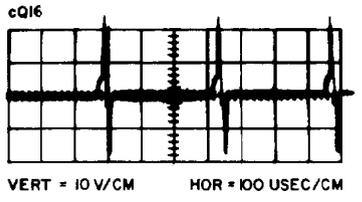
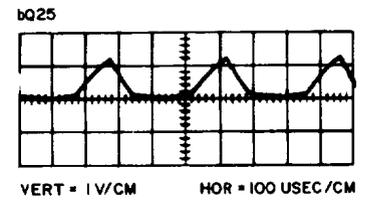
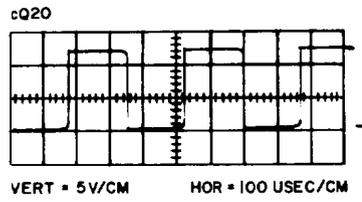
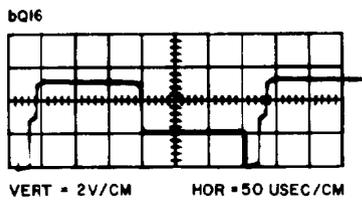


Figure 6-12. Panel 6A1, troubleshooting waveforms.

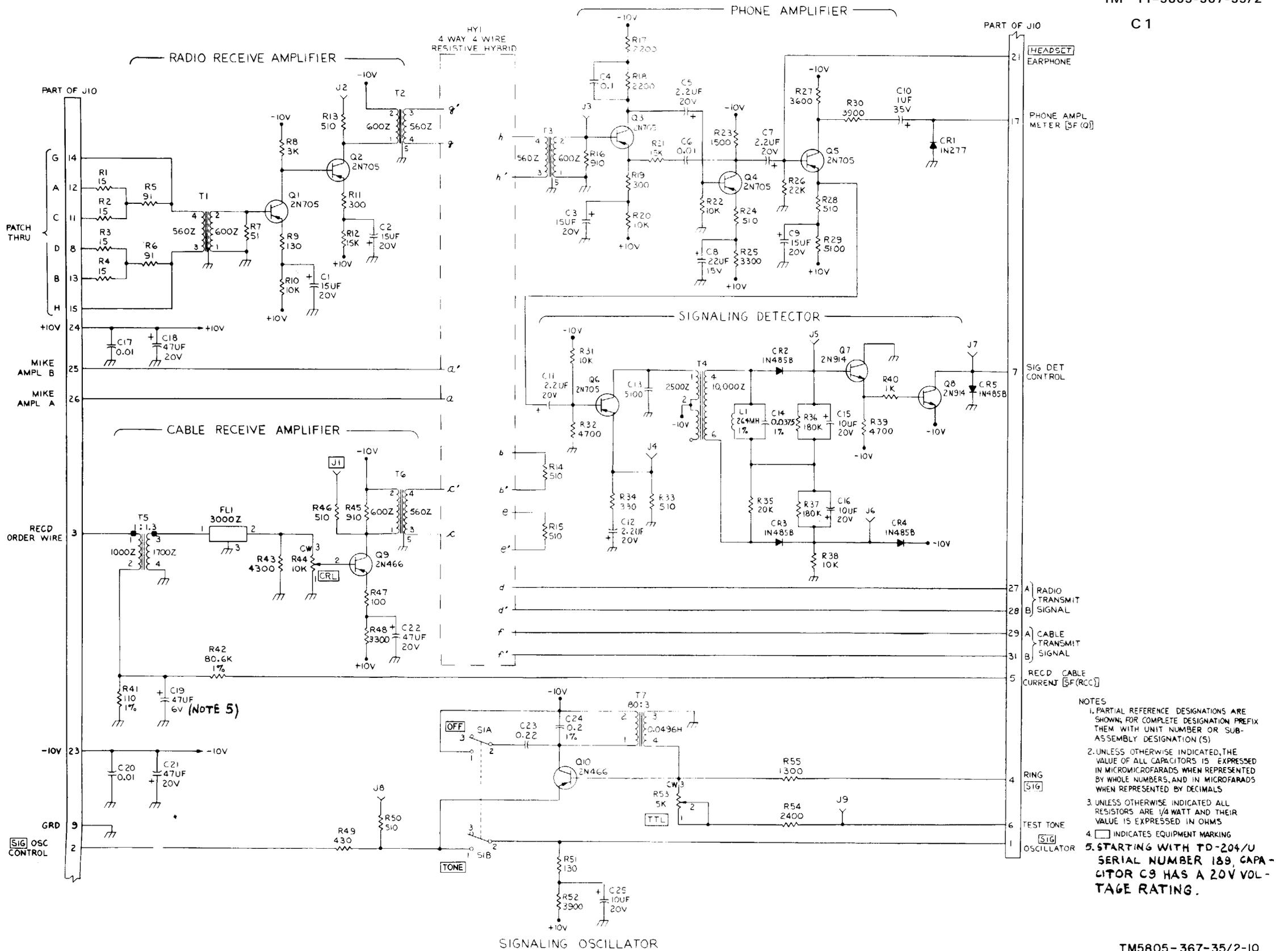
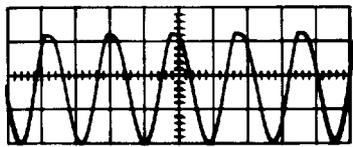


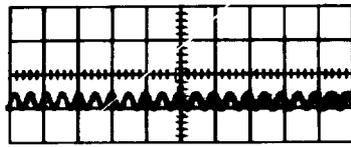
Figure 6-13. Panel 6A2, schematic diagram.

cQ10



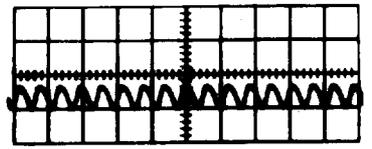
VERT = 5 V/CM HOR = 0.2 MS/CM

T3, TERMINALS 3 AND 4



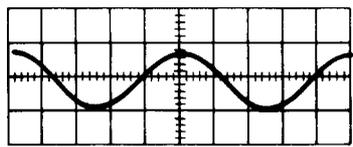
VERT = 0.5 V/CM HOR = 2 MS/CM

T4, TERMINALS 4 AND 6



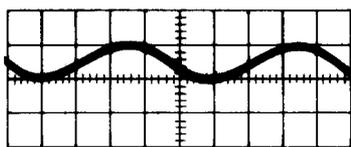
VERT = 0.5 V/CM HOR = 1 MS/CM

TERMINALS 31 AND 29



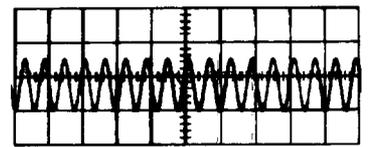
VERT = 1V/CM HOR = 0.2 MS/CM

TERMINALS 27 AND 28



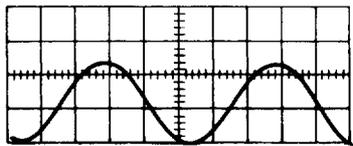
VERT = 100 MV/CM HOR = 200 USEC/CM

J8



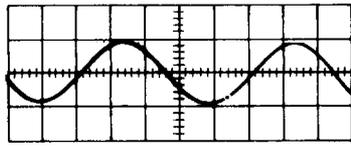
VERT = 0.5 V/CM HOR = 1 MS/CM

TERMINAL 21



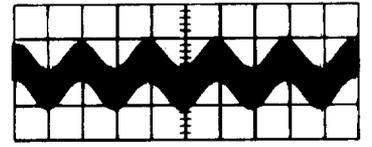
VERT = 2 V/CM HOR = 0.2 MS/CM

J1



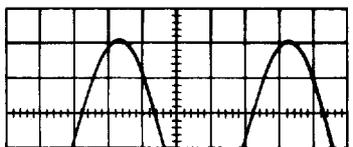
VERT = 0.5 V/CM HOR = 0.2 MS/CM

bQ1



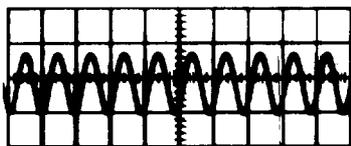
VERT = 0.5 V/CM HOR = 0.5 MS/CM

J2



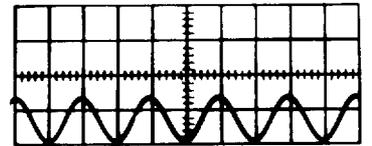
VERT = 2 V/CM HOR = 200 USEC/CM

T6, TERMINALS 3 AND 4



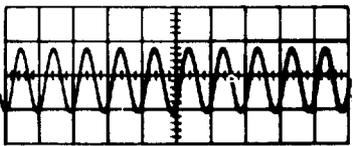
VERT = 0.5 V/CM HOR = 2 MS/CM

cQ1



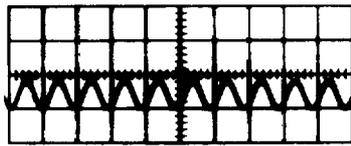
VERT = 0.5 V/CM HOR = 0.5 MS/CM

T2, TERMINALS 3 AND 4



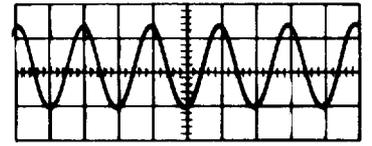
VERT = 0.5 V/CM HOR = 1 MS/CM

FL1, TERMINAL 2



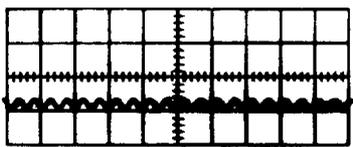
VERT = 0.5 V/CM HOR = 1 MS/CM

cQ3



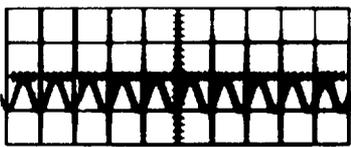
VERT = 0.5 V/CM HOR = 0.5 MS/CM

T1, TERMINALS 3 AND 4



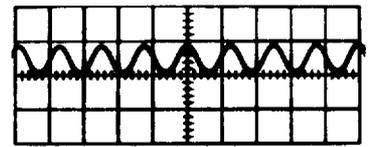
VERT = 0.5 V/CM HOR = 2 MS/CM

T5, TERMINALS 3 AND 4



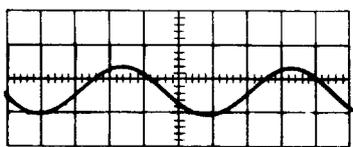
VERT = 0.5 V/CM HOR = 1 MS/CM

bQ6



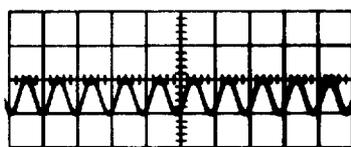
VERT = 0.5 V/CM HOR = 0.5 MS/CM

J3



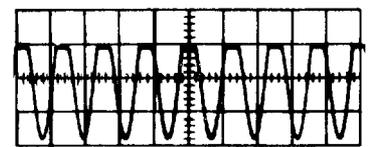
VERT = 0.1 V/CM HOR = 0.2 MS/CM

TERMINAL 3



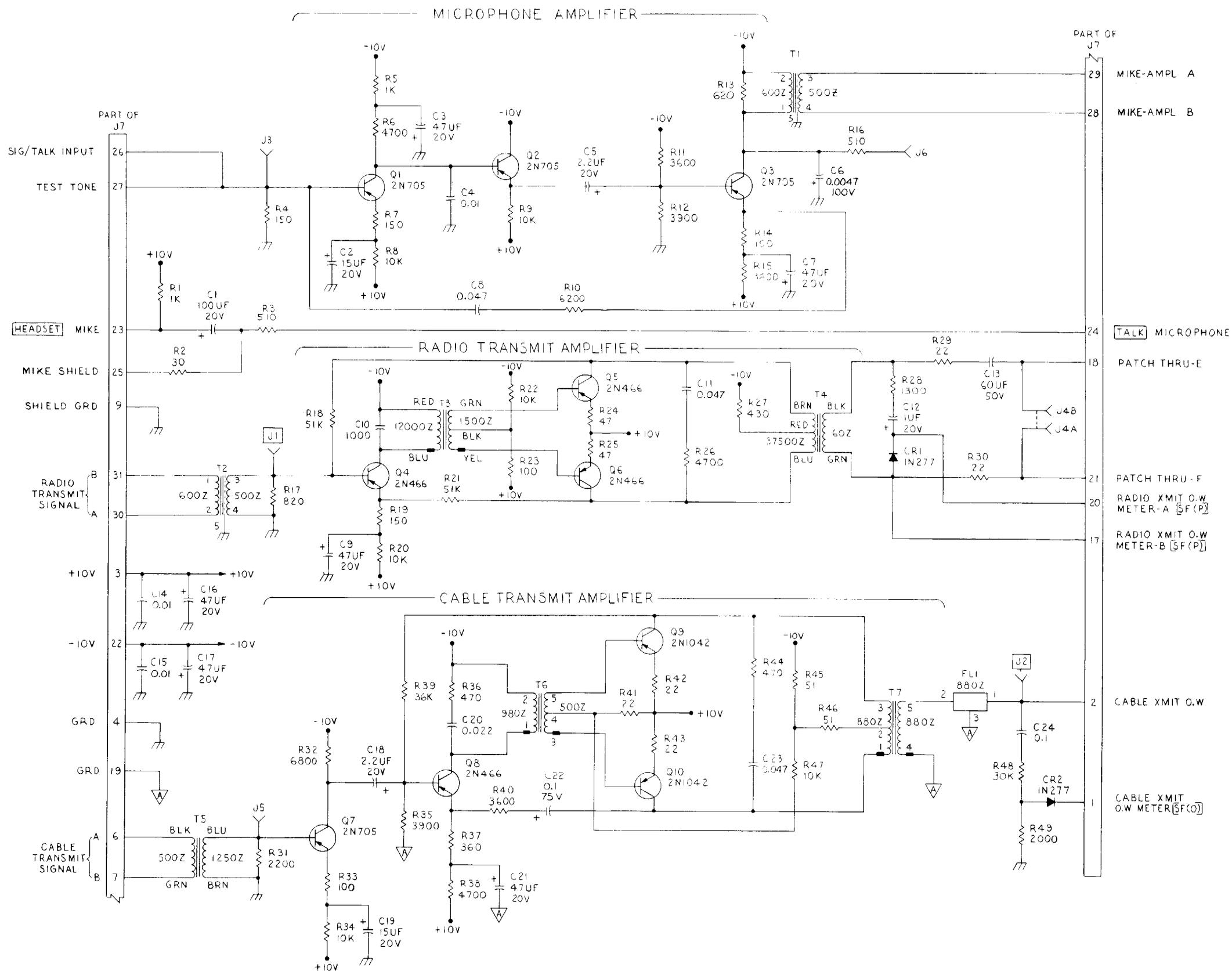
VERT = 0.5 V/CM HOR = 1 USEC/CM

cQ6



VERT = 0.5 V/CM HOR = 0.5 MS/CM

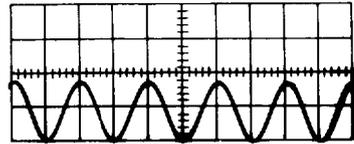
Figure 6-14. Panel 6A2, troubleshooting waveforms.



- NOTES
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION (S)
 2. UNLESS OTHERWISE INDICATED THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS; AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/4 WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 4. INDICATES EQUIPMENT MARKING

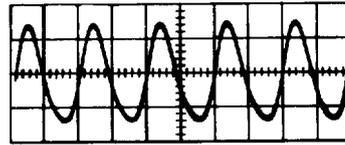
Figure 6-15. Panel 6A3, schematic diagram.

TERMINALS 28 AND 29



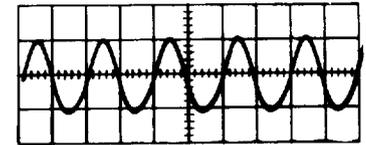
VERT = 0.5 V/CM HOR = 0.5 MS/CM

cQ6



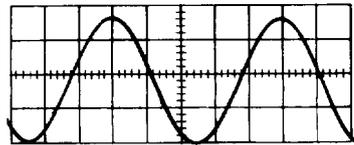
VERT = 5 V/CM HOR = 0.2 USEC/CM

bQ9



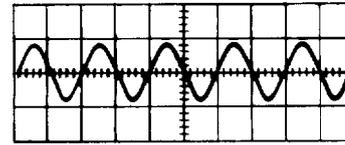
VERT = 1 V/CM HOR = 0.5 MS/CM

J6



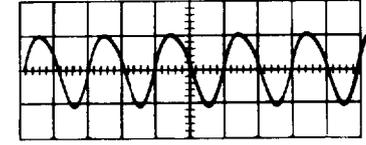
VERT = 0.2 V/CM HOR = 0.2 MS/CM

cQ4



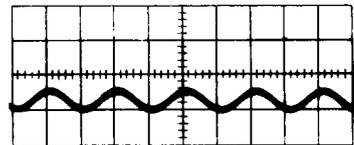
VERT = 2 V/CM HOR = 0.5 MS/CM

bQ10



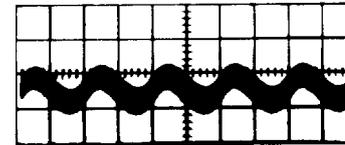
VERT = 1 V/CM HOR = 0.5 MS/CM

J3



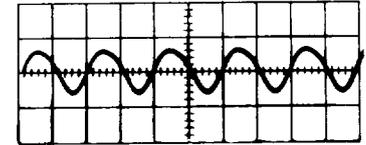
VERT = 0.05 V/CM HOR = 0.5 MS/CM

J1



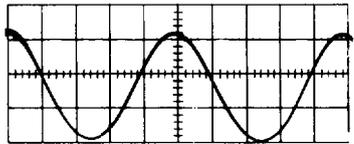
VERT = 0.1 V/CM HOR = 0.5 MS/CM

cQ8



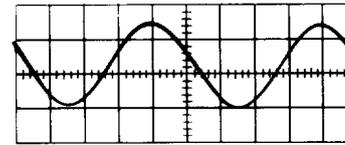
VERT = 5 V/CM HOR = 0.5 MS/CM

TERMINALS 21 AND 18



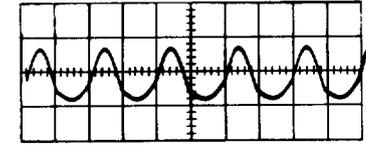
VERT = 0.2 V/CM HOR = 0.2 MS/CM

J2



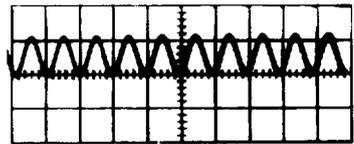
VERT = 10 V/CM HOR = 0.2 MS/CM

cQ7



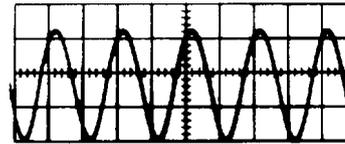
VERT = 1 V/CM HOR = 0.5 MS/CM

bQ2, bQ3



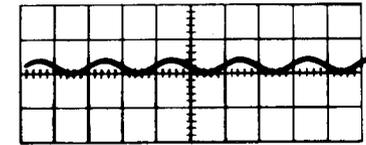
VERT = 0.5 V/CM HOR = 1 MS/CM

T7 SECONDARY



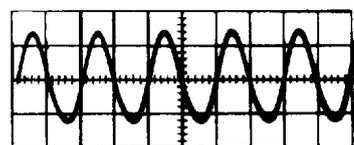
VERT = 10 V/CM HOR = 0.5 MS/CM

J5



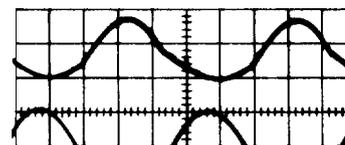
VERT = 0.5 V/CM HOR = 0.5 MS/CM

cQ5



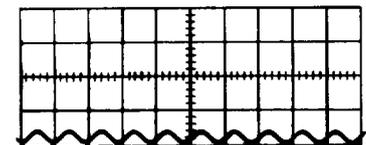
VERT = 5 V/CM HOR = 0.2 USEC/CM

cQ9 (TOP), cQ9 (BOTTOM)



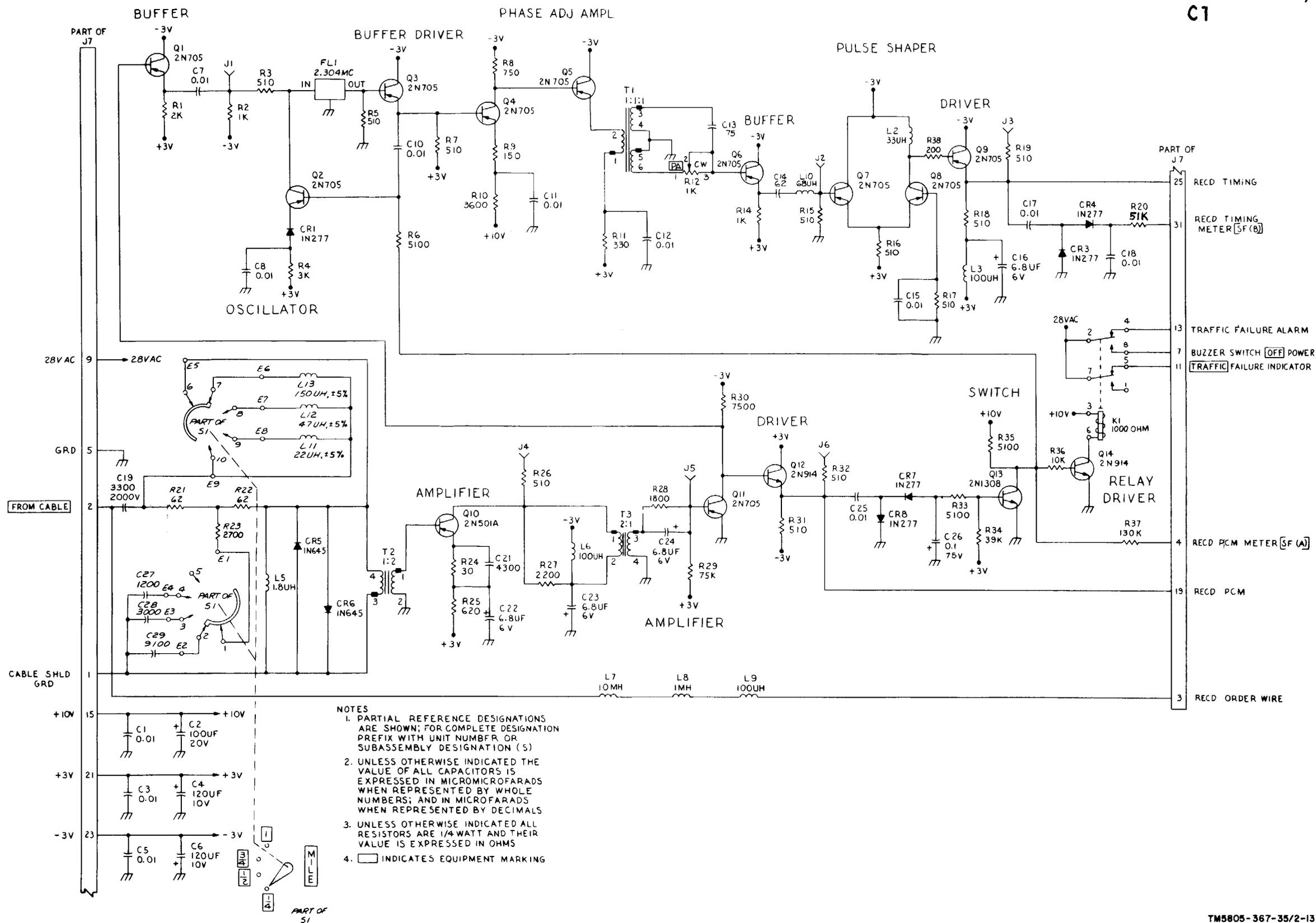
VERT = 10 V/CM HOR = 0.2 MS/CM

TERMINAL 24



VERT = 10 V/CM HOR = 0.5 MS/CM

Figure 6-16. Panel 6A3, troubleshooting waveforms.



- NOTES
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBFR OR SUBASSEMBLY DESIGNATION (S)
 2. UNLESS OTHERWISE INDICATED THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS; AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/4 WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 4. INDICATES EQUIPMENT MARKING

Figure 6-17. Panel 6A4, schematic diagram.

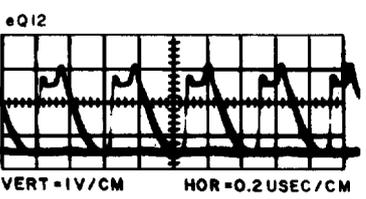
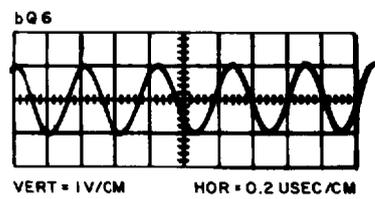
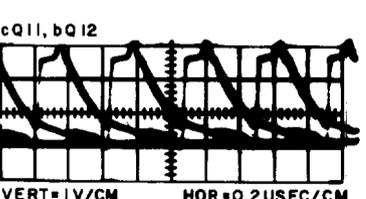
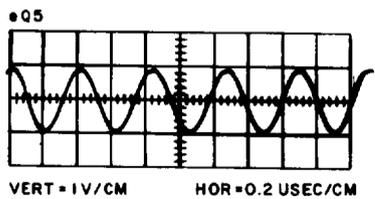
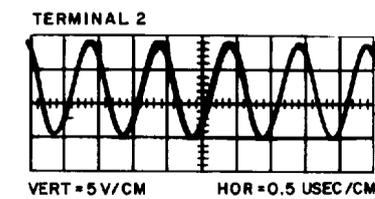
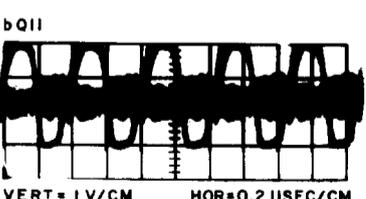
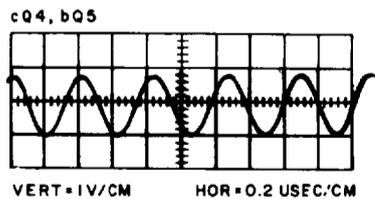
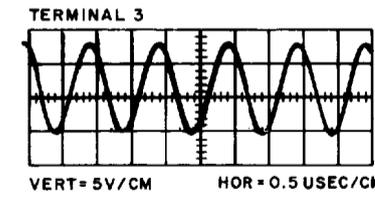
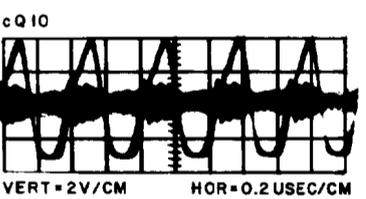
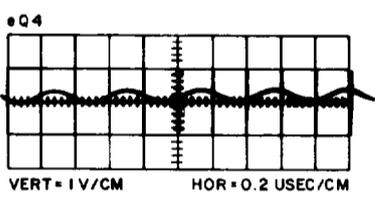
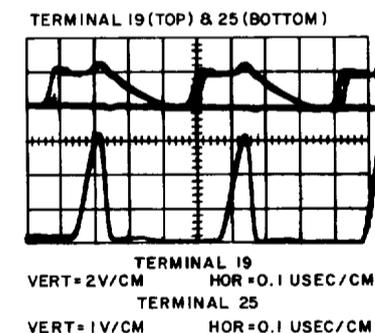
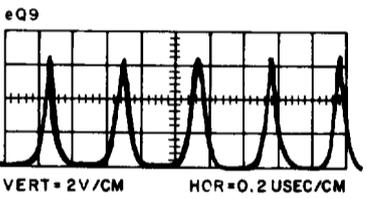
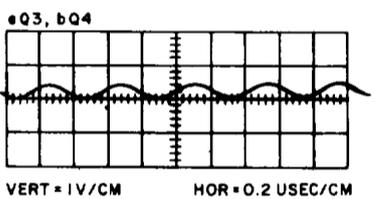
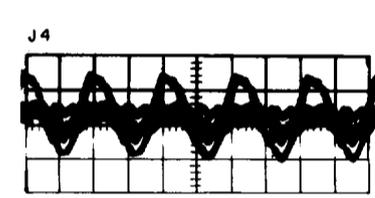
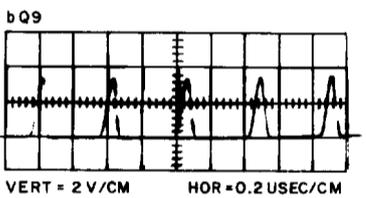
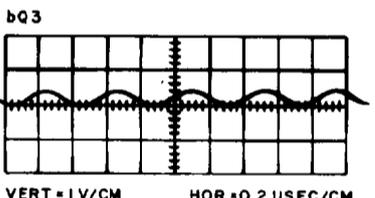
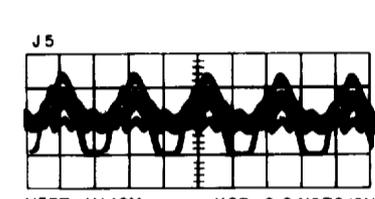
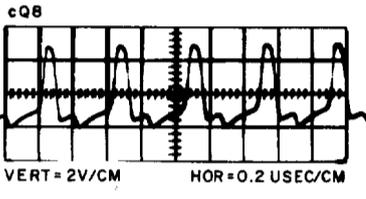
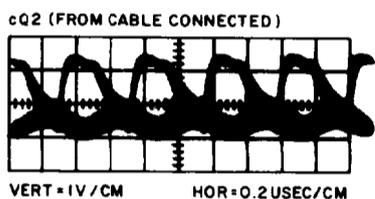
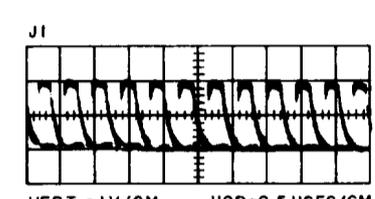
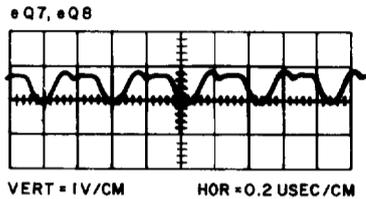
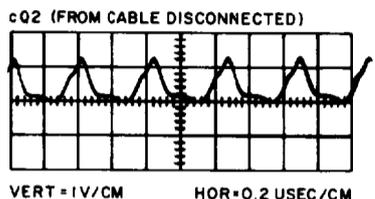
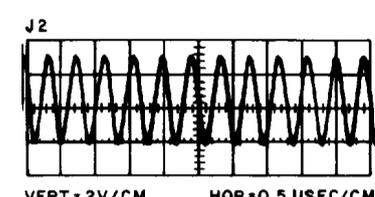
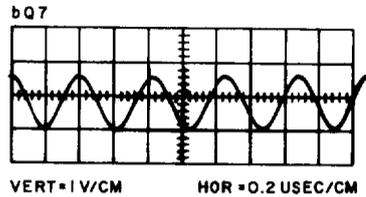
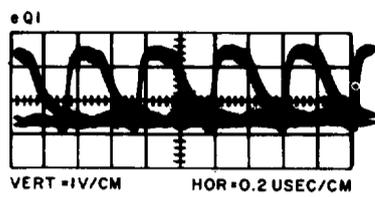
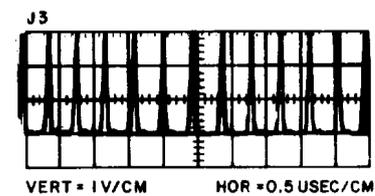
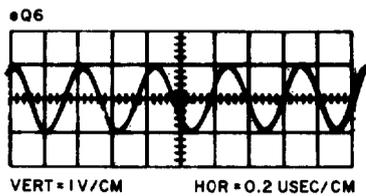
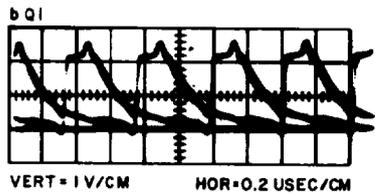
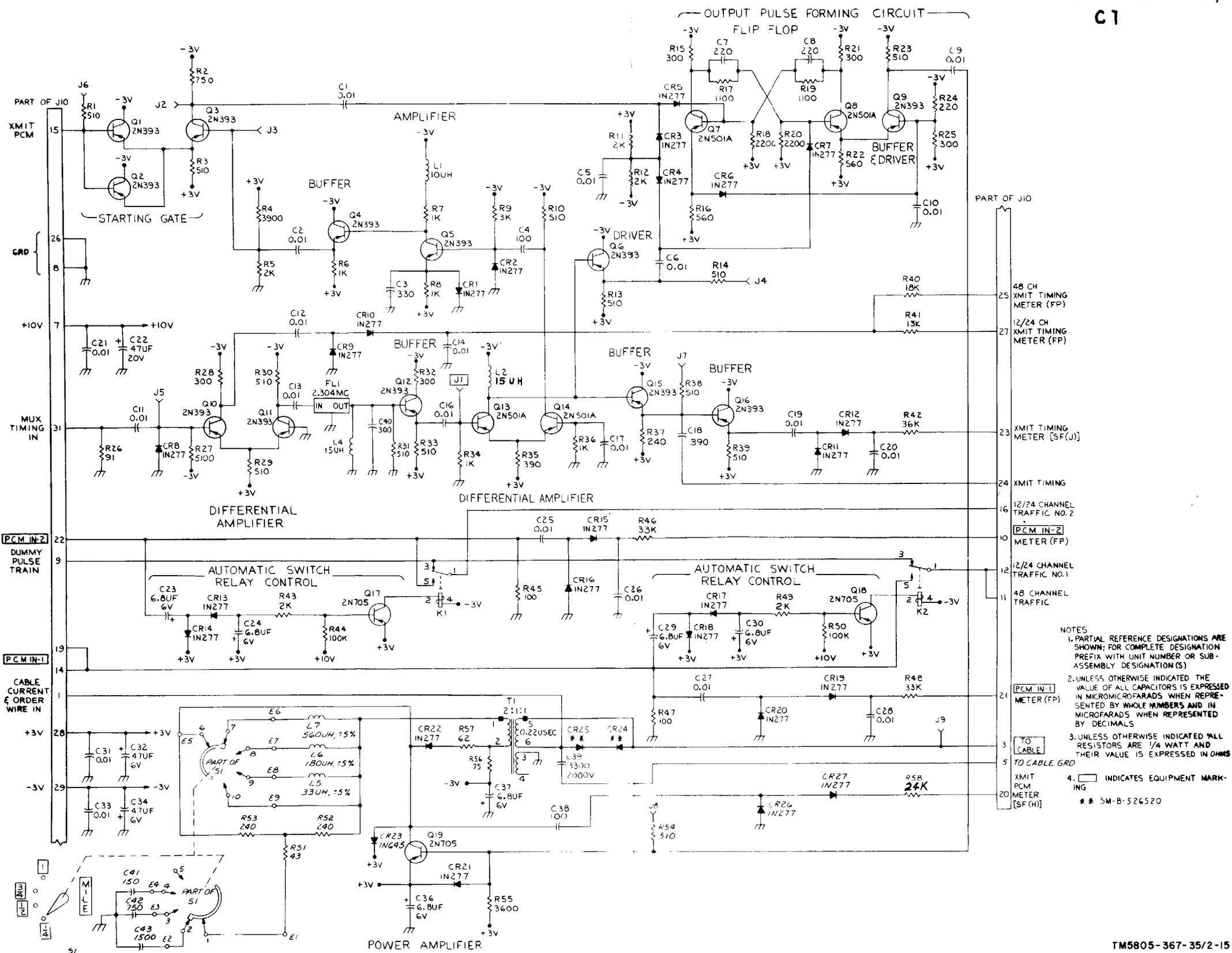


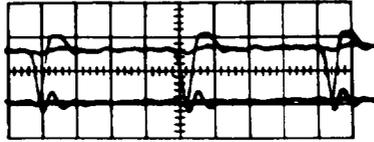
Figure 6-18. Panel 6A4, troubleshooting waveforms.



- NOTES
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUB-ASSEMBLY DESIGNATION (S)
 2. UNLESS OTHERWISE INDICATED THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/4 WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 4. INDICATES EQUIPMENT MARKING
- ** SM-B-526520

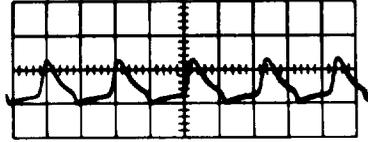
Figure 6-19. Panel 6A5, schematic diagram.

J6 - bQ1, bQ2



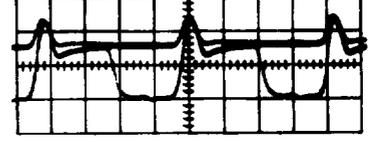
VERT = 1V/CM HOR = 0.1 USEC/CM

bQ5



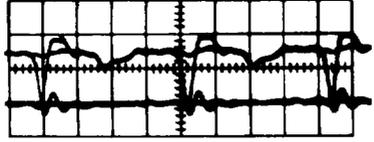
VERT = 1V/CM HOR = 0.2 USEC/CM

cQ7



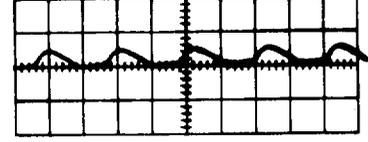
VERT = 1V/CM HOR = 0.1 USEC/CM

eQ1, eQ2, eQ3



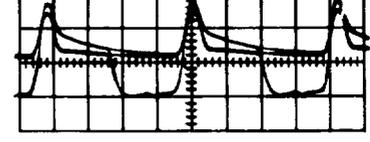
VERT = 1V/CM HOR = 0.1 USEC/CM

eQ5



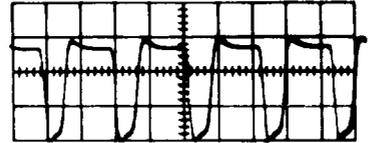
VERT = 1V/CM HOR = 0.2 USEC/CM

bQ8



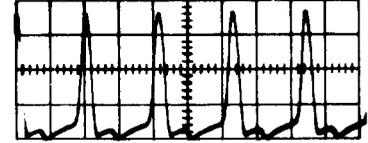
VERT = 1V/CM HOR = 0.1 USEC/CM

J3 - bQ3



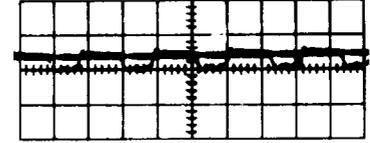
VERT = 1V/CM HOR = 0.2 USEC/CM

bQ6, bQ15, cQ13



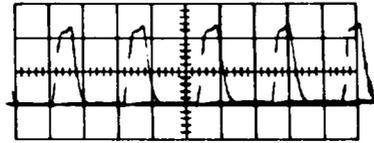
VERT = 1V/CM HOR = 0.2 USEC/CM

eQ8, eQ9



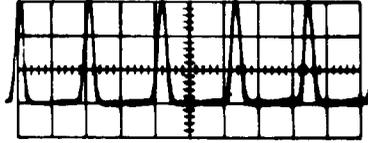
VERT = 1V/CM HOR = 0.2 USEC/CM

J2 - cQ3



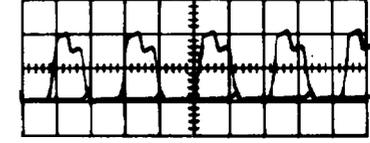
VERT = 1V/CM HOR = 0.2 USEC/CM

eQ6



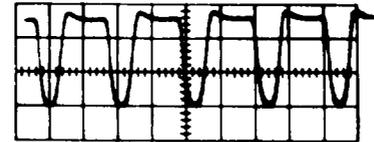
VERT = 1V/CM HOR = 0.2 USEC/CM

cQ8



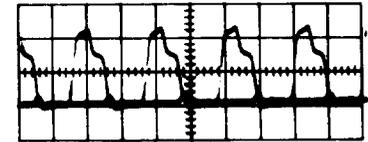
VERT = 1V/CM HOR = 0.2 USEC/CM

bQ4, cQ5



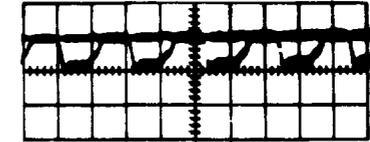
VERT = 1V/CM HOR = 0.2 USEC/CM

bQ7



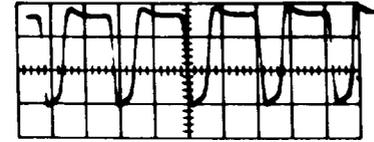
VERT = 1V/CM HOR = 0.2 USEC/CM

J8 - cQ9, bQ19



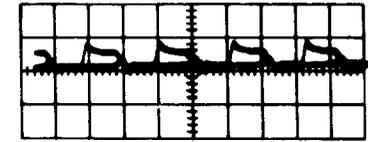
VERT = 1V/CM HOR = 0.2 USEC/CM

eQ4



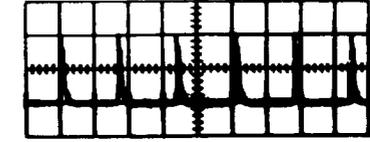
VERT = 1V/CM HOR = 0.2 USEC/CM

eQ7



VERT = 1V/CM HOR = 0.2 USEC/CM

J5 - bQ10



VERT = 1V/CM HOR = 1 USEC/CM

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Figure 6-20. Panel 6A5, troubleshooting waveforms (part 1 of 2).

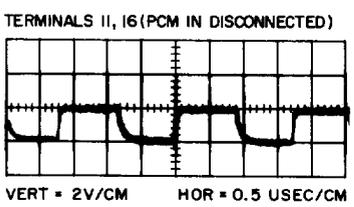
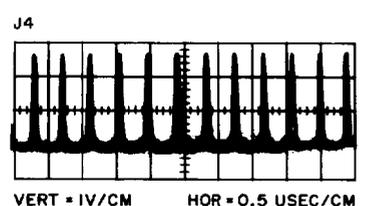
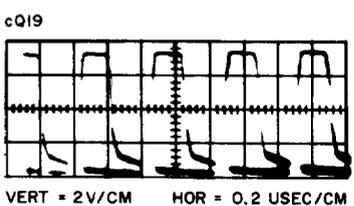
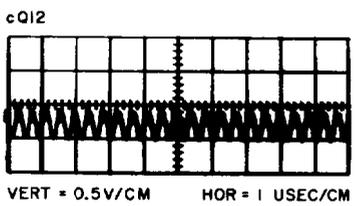
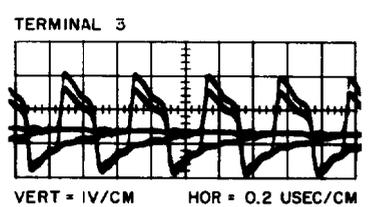
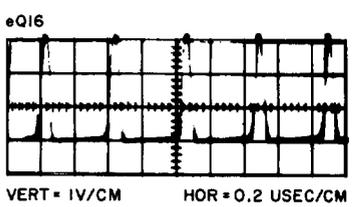
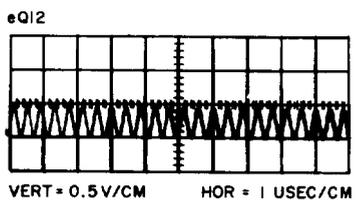
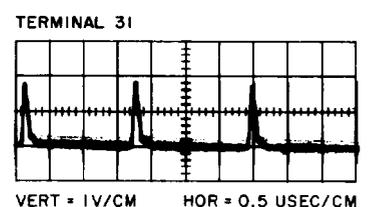
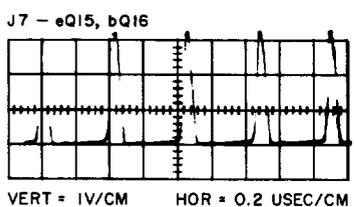
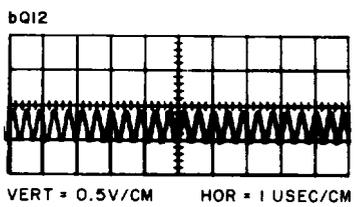
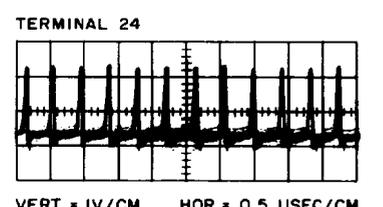
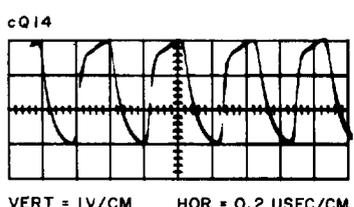
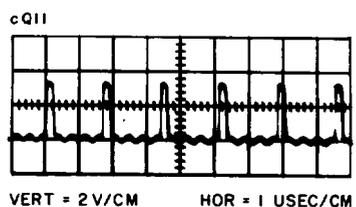
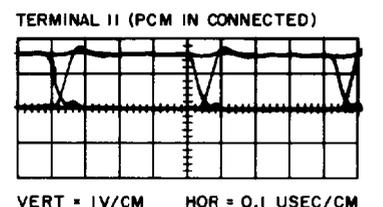
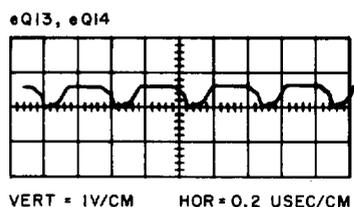
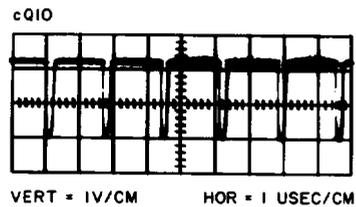
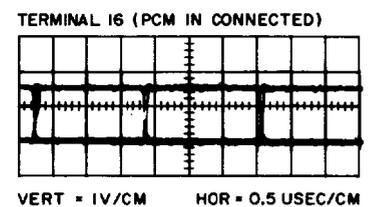
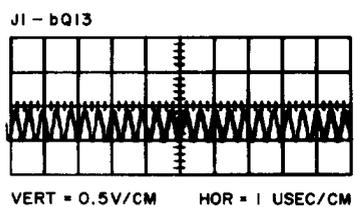
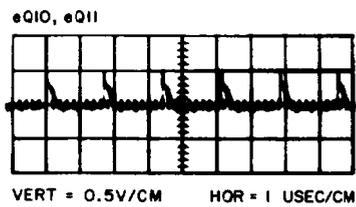
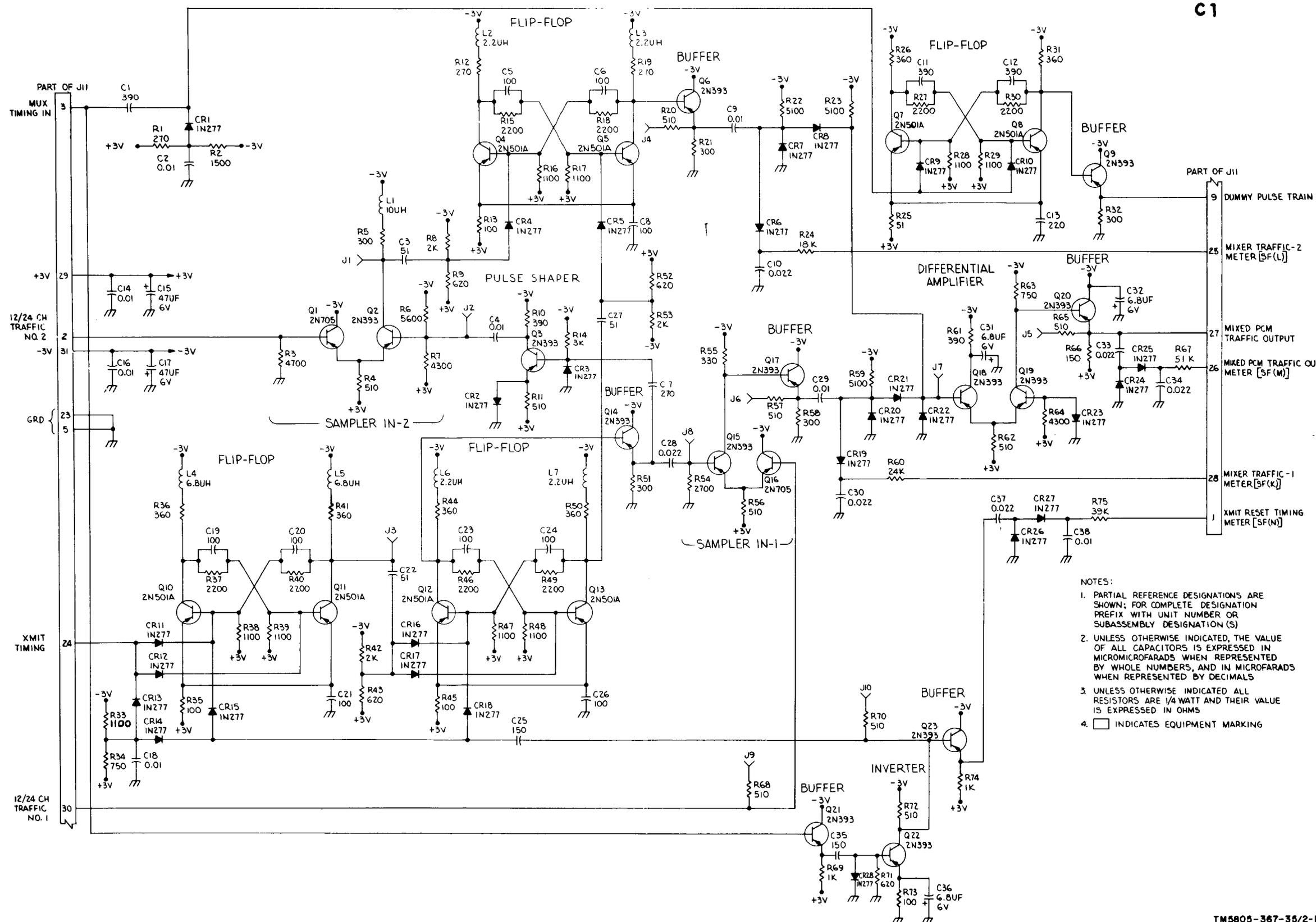


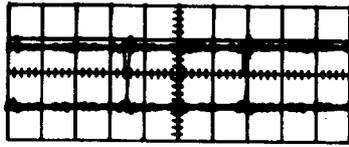
Figure 6-20(2). Panel 6A5, troubleshooting waveforms (part 2 of 2).



- NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION (S)
 2. UNLESS OTHERWISE INDICATED, THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS, AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/4 WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 4. □ INDICATES EQUIPMENT MARKING

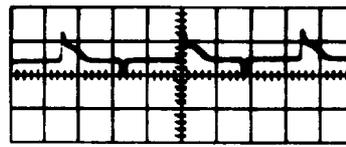
Figure 6-21. Panel 6A6, schematic diagram.

bQ1



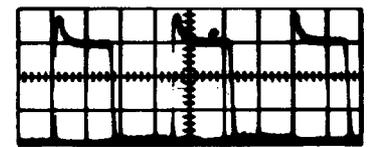
VERT = 1V/CM HOR = 0.5 USEC/CM

eQ3



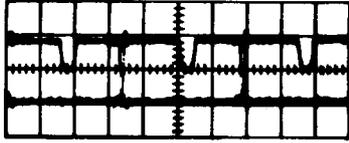
VERT = 1V/CM HOR = 0.5 USEC/CM

cQ5, bQ6



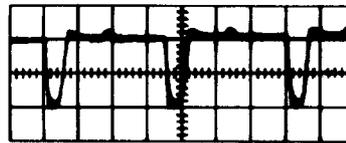
VERT = 1V/CM HOR = 0.5 USEC/CM

eQ1



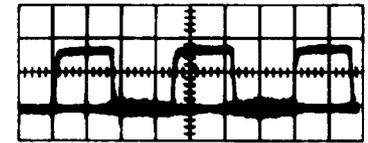
VERT = 1V/CM HOR = 0.5 USEC/CM

cQ3



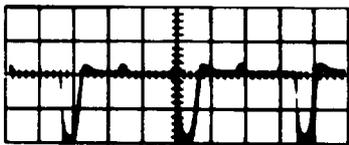
VERT = 1V/CM HOR = 0.5 USEC/CM

eQ6



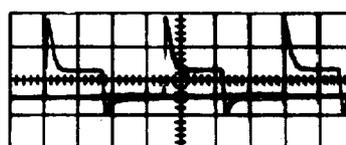
VERT = 1V/CM HOR = 0.5 USEC/CM

bQ2



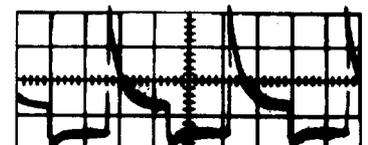
VERT = 1V/CM HOR = 0.5 USEC/CM

bQ4



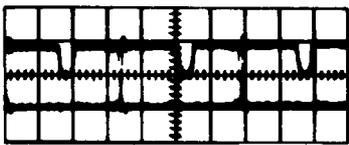
VERT = 1V/CM HOR = 0.5 USEC/CM

bQ7



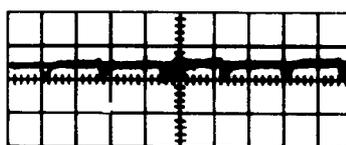
VERT = 1V/CM HOR = 1 USEC/CM

eQ2



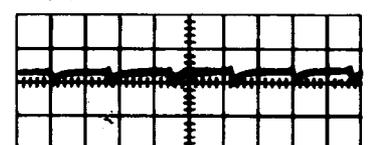
VERT = 1V/CM HOR = 0.5 USEC/CM

eQ4, eQ5



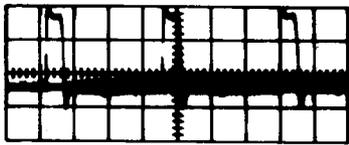
VERT = 1V/CM HOR = 0.5 USEC/CM

eQ7, eQ8



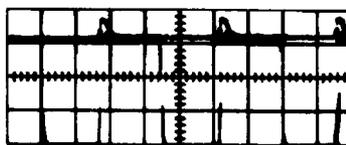
VERT = 1V/CM HOR = 1 USEC/CM

cQ2



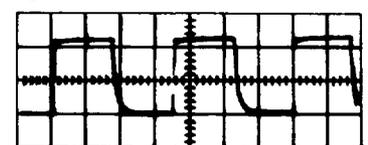
VERT = 1V/CM HOR = 0.5 USEC/CM

cQ4



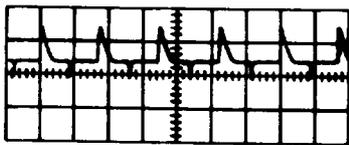
VERT = 1V/CM HOR = 0.5 USEC/CM

cQ7



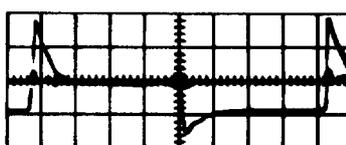
VERT = 2V/CM HOR = 1 USEC/CM

bQ3



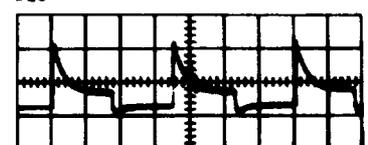
VERT = 1V/CM HOR = 1 USEC/CM

bQ5



VERT = 1V/CM HOR = 0.5 USEC/CM

bQ8

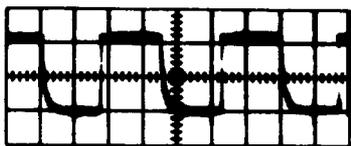


VERT = 2V/CM HOR = 1 USEC/CM

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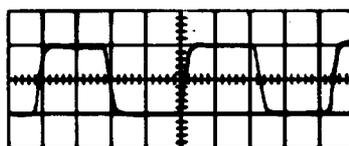
Figure 6-22①. Panel 6A6, troubleshooting waveforms (part 1 of 3).

cQ8, bQ9



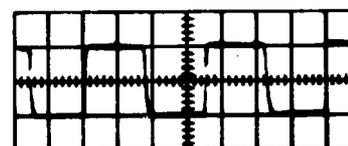
VERT=2V/CM HOR=1 USEC/CM

cQ11



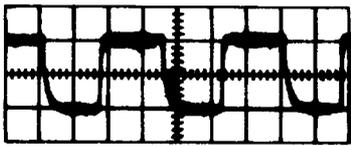
VERT=2 V/CM HOR=0.2 USEC/CM

eQ14



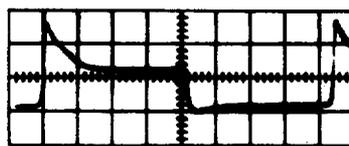
VERT=1V/CM HOR=0.5 USEC/CM

eQ9



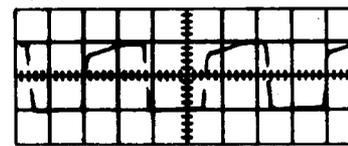
VERT=1V/CM HOR=1 USEC/CM

bQ12



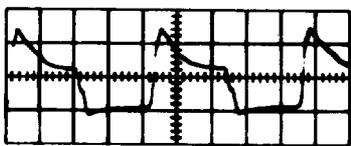
VERT=1V/CM HOR=0.2 USEC/CM

bQ15



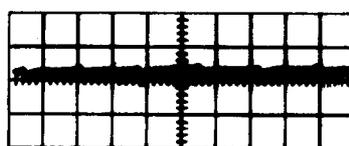
VERT=1V/CM HOR=0.5 USEC/CM

bQ10



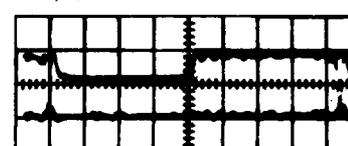
VERT=1V/CM HOR=0.2 USEC/CM

eQ12, eQ13



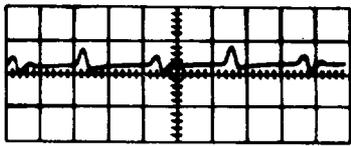
VERT=1V/CM HOR=0.5 USEC/CM

eQ15, eQ16



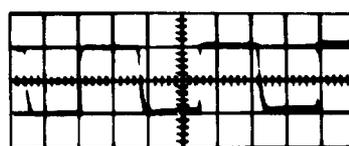
VERT=1V/CM HOR=0.2 USEC/CM

eQ10, eQ11



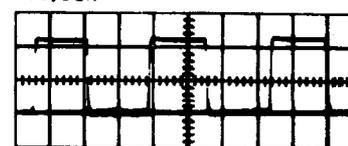
VERT=1V/CM HOR=0.2 USEC/CM

cQ12



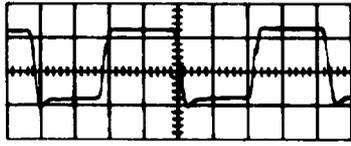
VERT=2V/CM HOR=0.5 USEC/CM

cQ15, bQ17



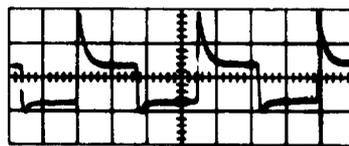
VERT=1V/CM HOR=0.5 USEC/CM

eQ10



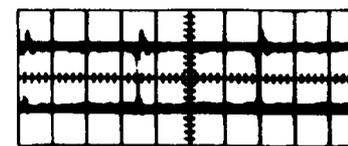
VERT=2V/CM HOR=0.2 USEC/CM

bQ13



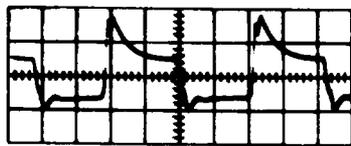
VERT=1V/CM HOR=0.5 USEC/CM

bQ16



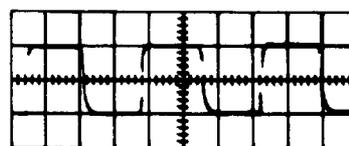
VERT=1V/CM HOR=0.5 USEC/CM

bQ11



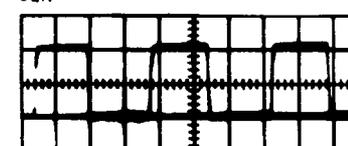
VERT=1V/CM HOR=0.2 USEC/CM

cQ13



VERT=2V/CM HOR=0.5 USEC/CM

eQ17



VERT=1V/CM HOR=0.5 USEC/CM

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Figure 6-22(3). Panel 6A8, troubleshooting waveforms (part 2 of 3).

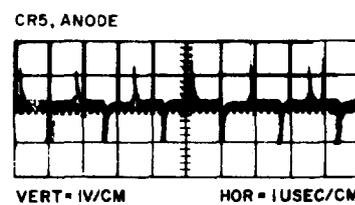
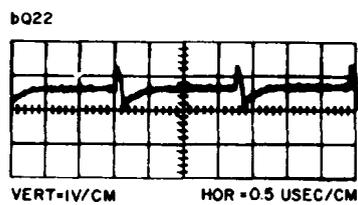
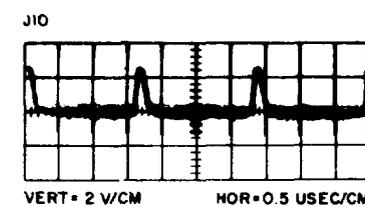
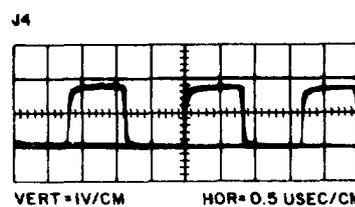
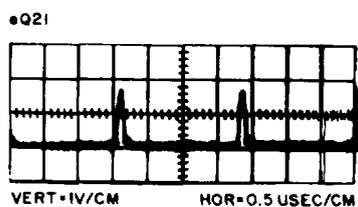
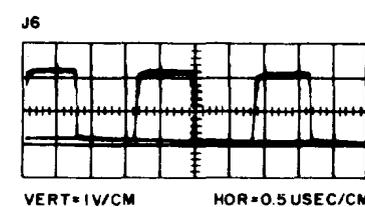
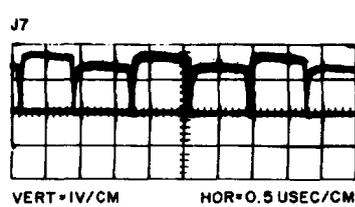
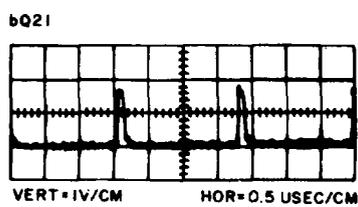
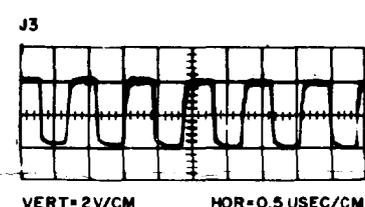
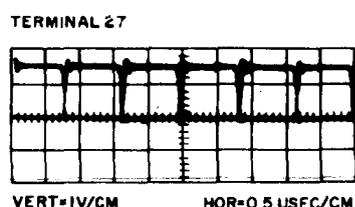
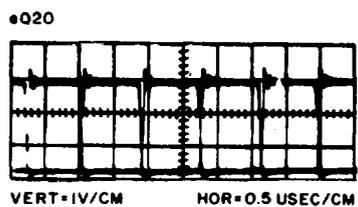
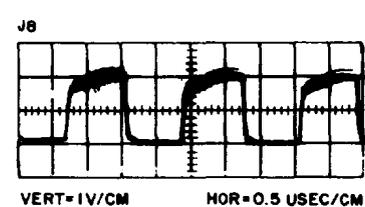
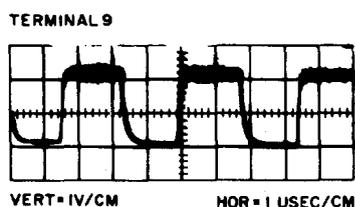
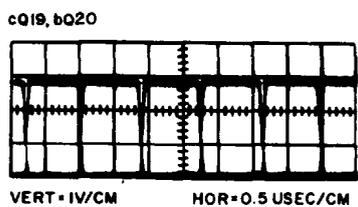
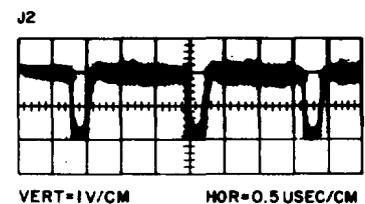
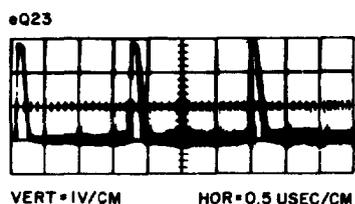
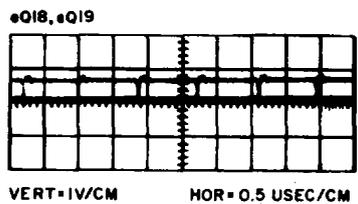
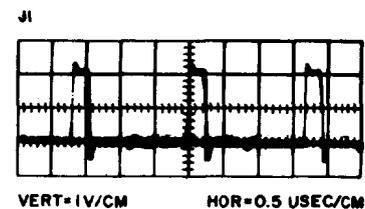
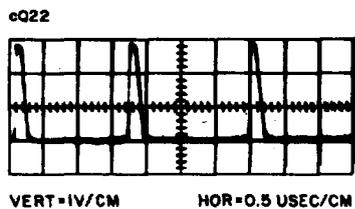
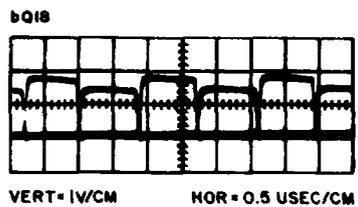
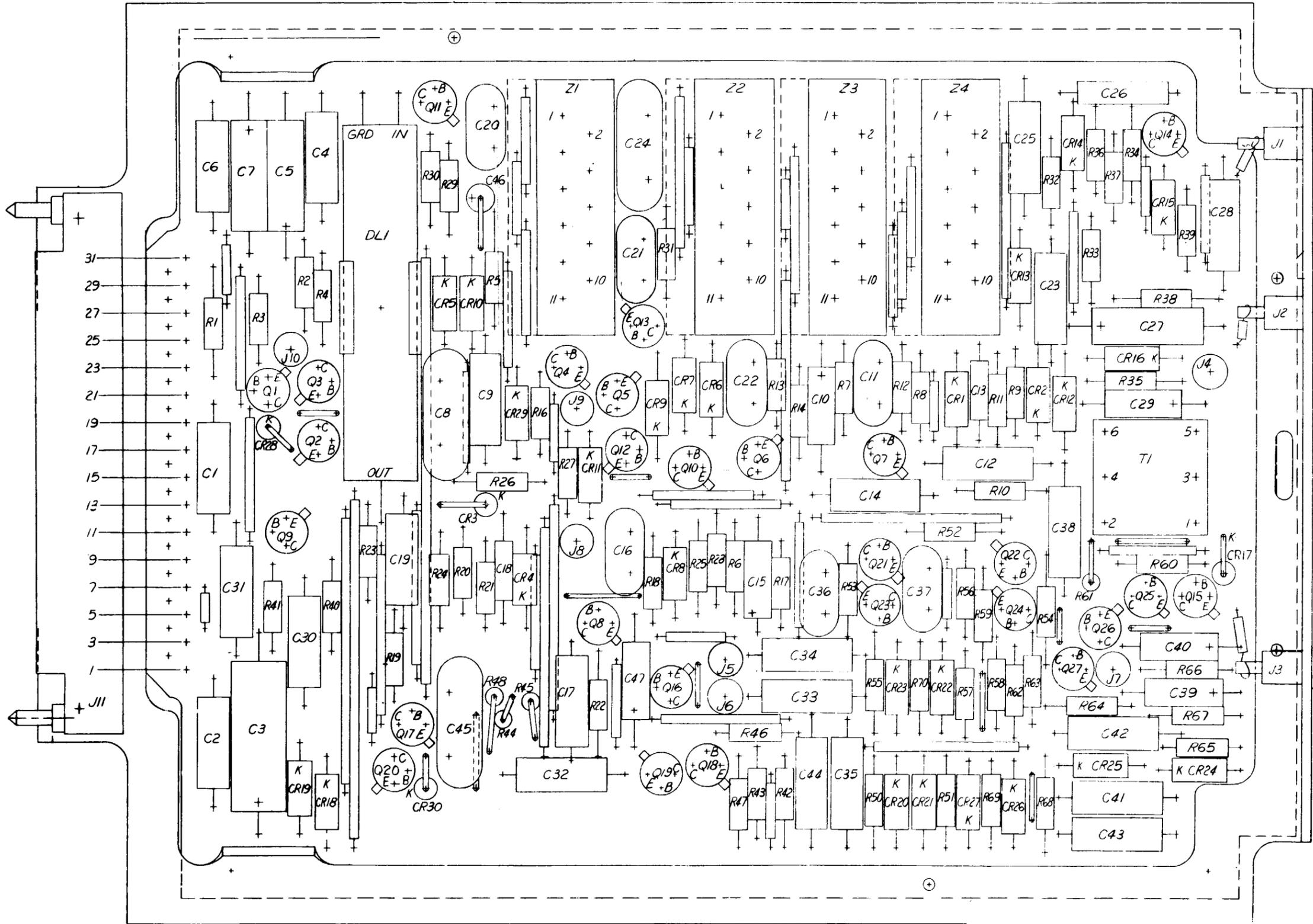
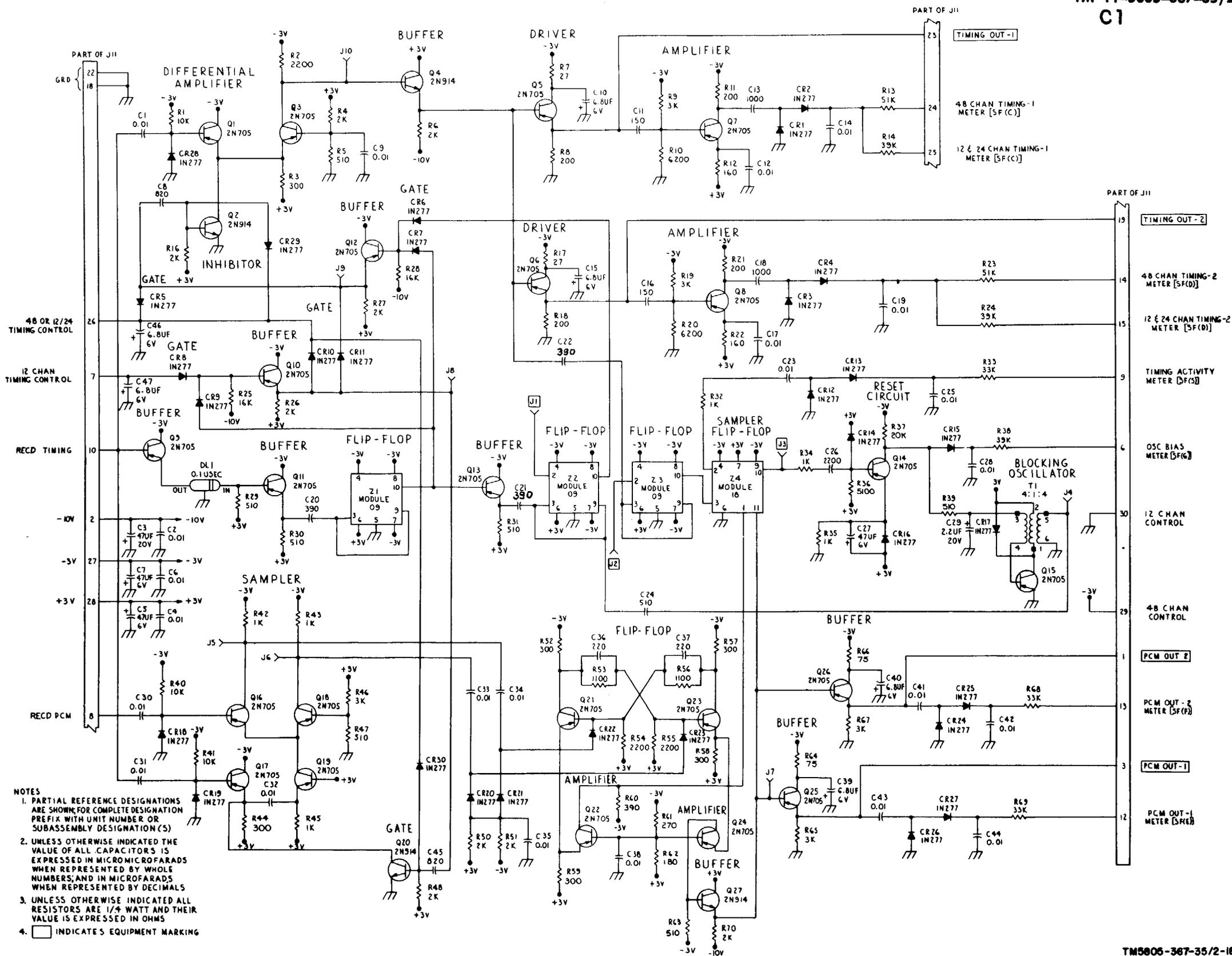


Figure 6-22(3). Panel 6A6, troubleshooting waveforms (part 3 of 3).



- NOTES:
1. SCHEM SM-E-527533
 2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION (S)
 3. ASSEMBLE PER STD-MK-57D-275. SOLDER WITH ITEM 7
 4. TEST PER SM-B-527545
 5. APPLY CONFORMAL COATING (ITEM B), .005 ± .002 THK TO ALL EXPOSED SURFACES OF PRINTED WIRING PANEL (ITEM 2) AND COMPONENTS MOUNTED THEREUNTO. NO COATING SHOULD BE APPLIED TO FRAME (ITEM 1), EXCEPT FOR FILLETS RESULTING FROM COATING PANEL. NO COATING SHOULD BE APPLIED TO INTERNAL SURFACES OR GUIDE PINS OF PANEL CONN (ITEM 5) OR TO INTERNAL SURFACES OF ANY TEST JACKS OR THE ADJUSTABLE SURFACES OF ANY ADJUSTABLE COMPONENTS
 6. WHEN REQUIRED, HAND SOLDER PER SM-C-526772 SOLDER WITH ITEM 63
 7. ASSEMBLY OF PARTS SHALL BE ADJUSTED TO MEET THESE DIMENSIONS.
 8. COMPONENT REFERENCE DESIGNATIONS AND THEIR RESPECTIVE TERMINAL DESIGNATIONS ARE SHOWN FOR INFORMATION ONLY. FOR ACTUAL PANEL MARKINGS SEE SM-E-527535 SHEET 3
 9. TEST JACKS, RIVETS, EYELETS, ETC. MUST BE MECHANICALLY SECURED AFTER INSERTION PRIOR TO SOLDERING.

Figure 6-23. Panel 6A7, top view.



- NOTES
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION (S)
 2. UNLESS OTHERWISE INDICATED THE VALUE OF ALL CAPACITORS IS EXPRESSED IN MICROMICROFARADS WHEN REPRESENTED BY WHOLE NUMBERS; AND IN MICROFARADS WHEN REPRESENTED BY DECIMALS
 3. UNLESS OTHERWISE INDICATED ALL RESISTORS ARE 1/4 WATT AND THEIR VALUE IS EXPRESSED IN OHMS
 4. INDICATES EQUIPMENT MARKING

Figure 6-24. Panel 6A7, schematic diagram.

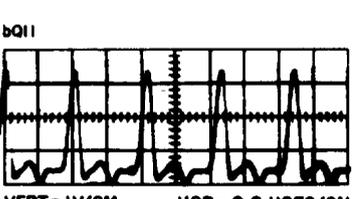
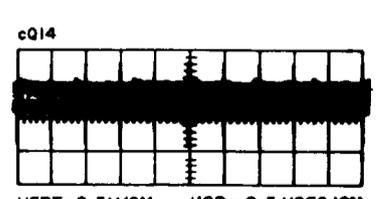
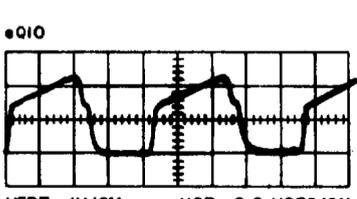
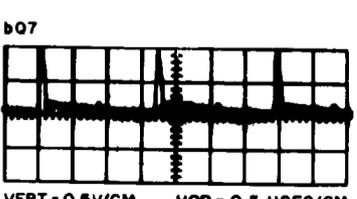
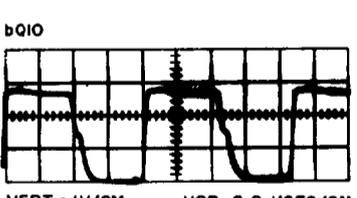
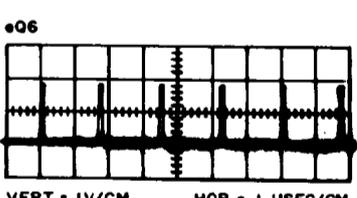
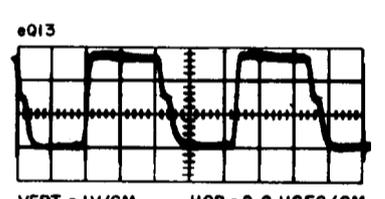
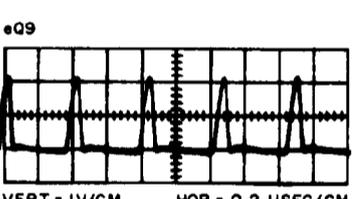
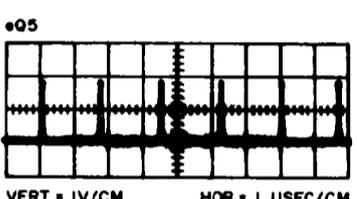
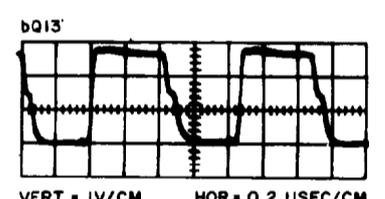
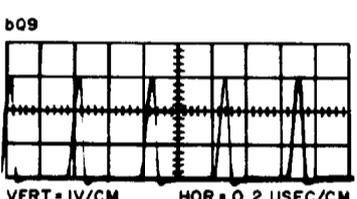
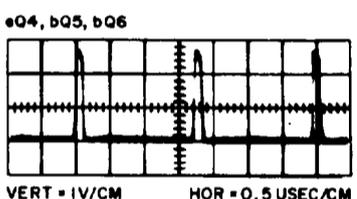
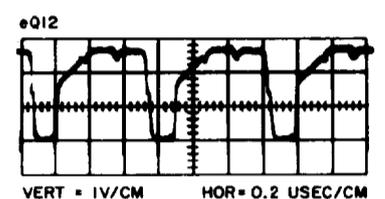
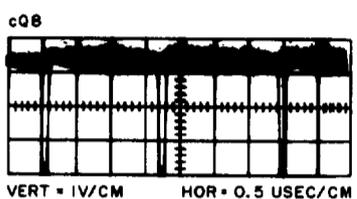
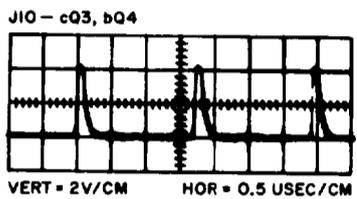
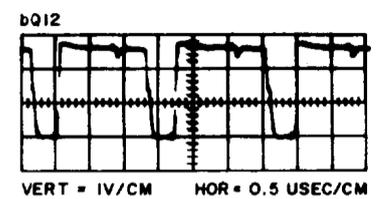
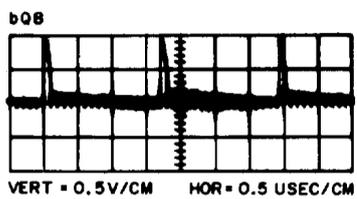
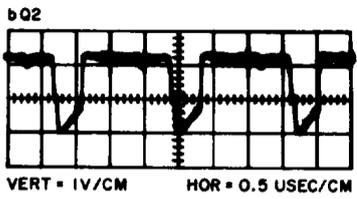
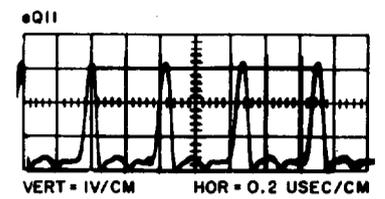
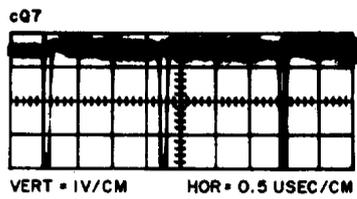
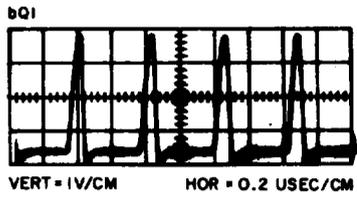


Figure 6-25①. Panel 6A7, troubleshooting waveforms (part 1 of 3).

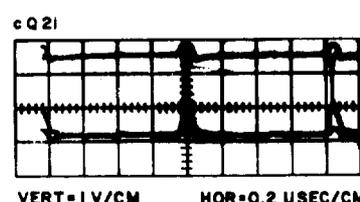
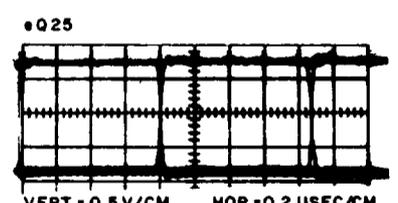
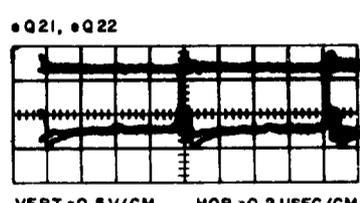
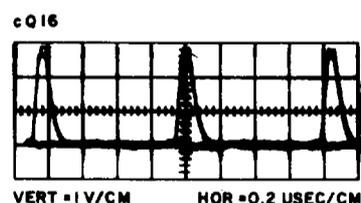
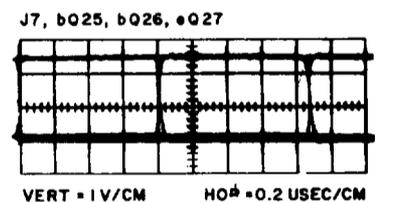
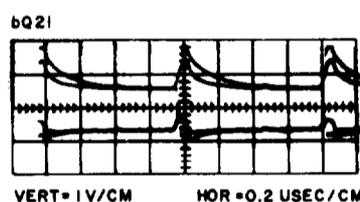
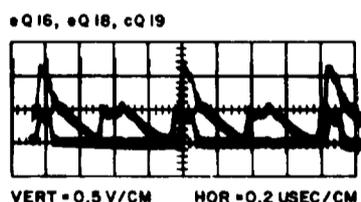
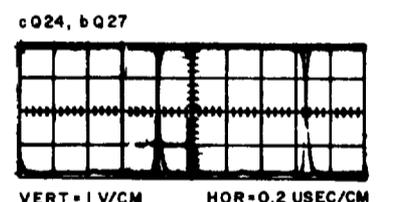
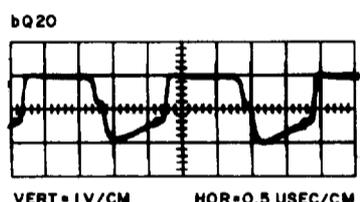
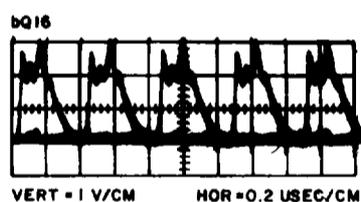
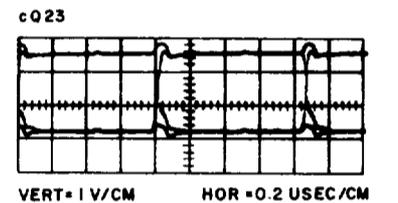
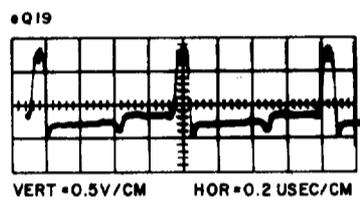
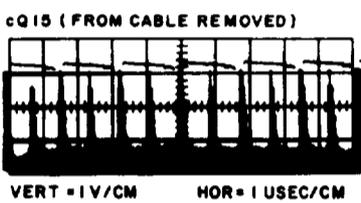
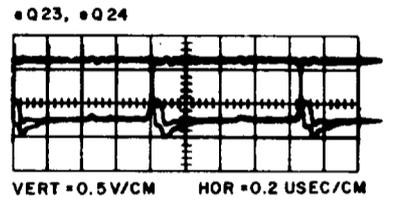
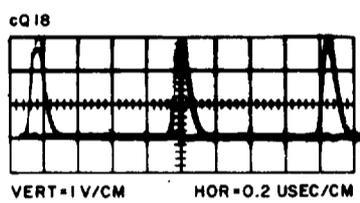
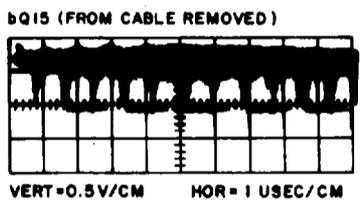
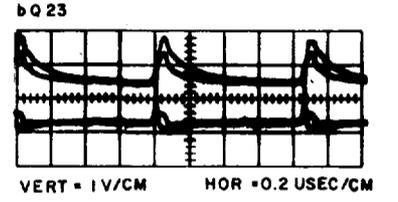
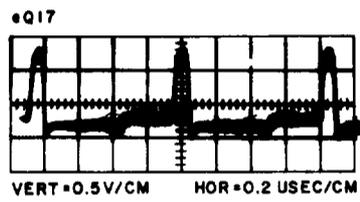
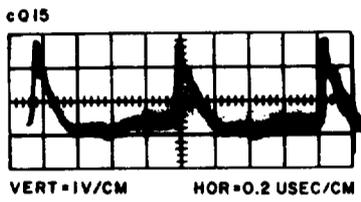
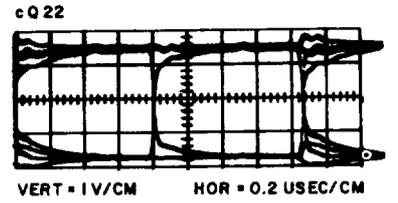
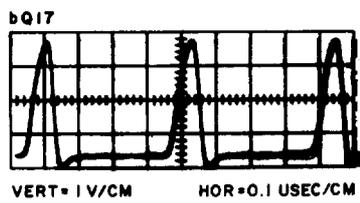
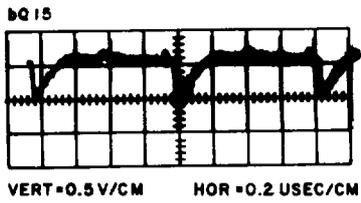


Figure 6-25(3). Panel Q47, troubleshooting waveforms (part 2 of 3).

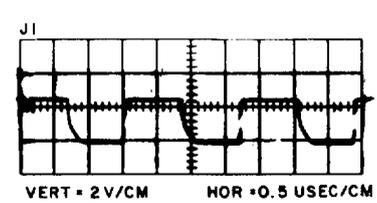
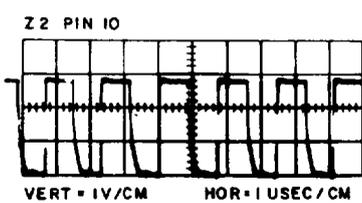
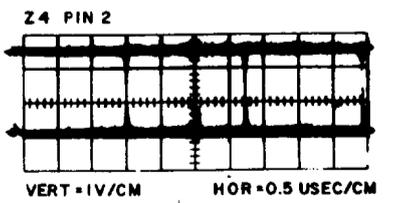
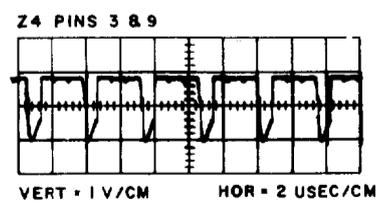
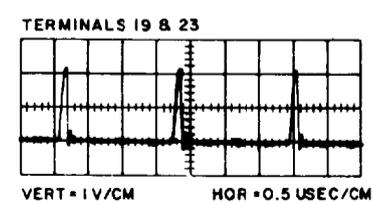
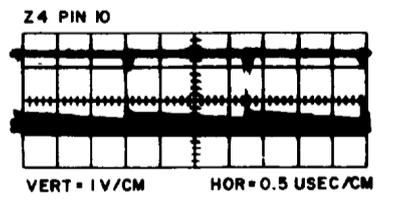
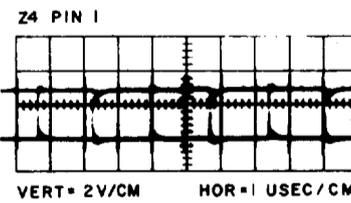
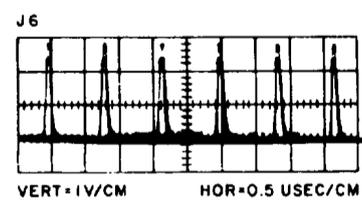
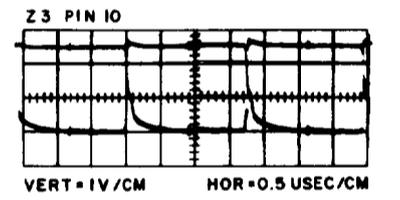
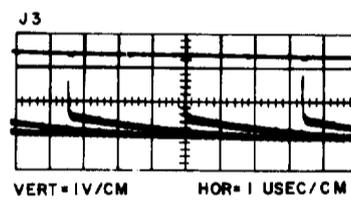
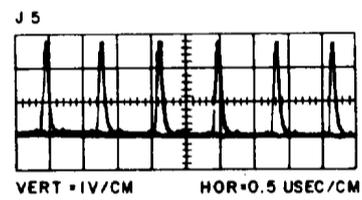
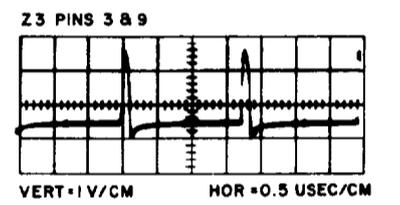
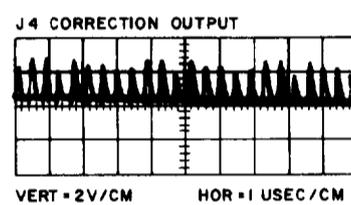
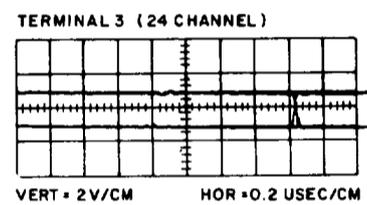
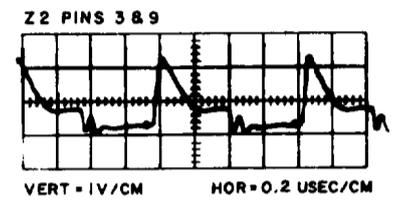
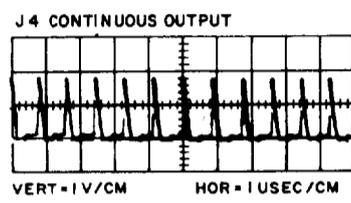
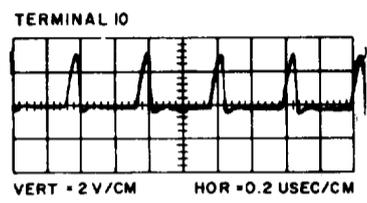
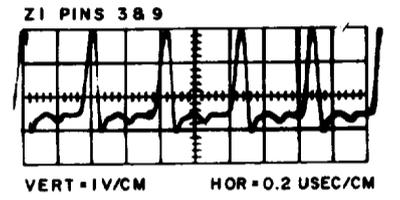
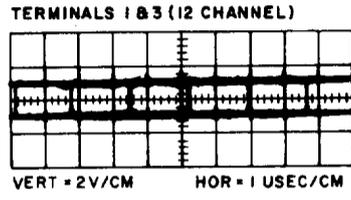
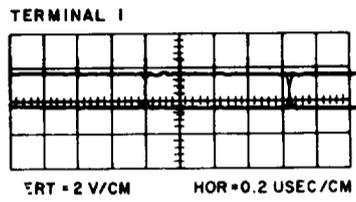
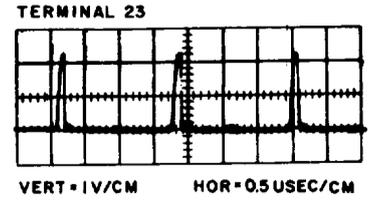
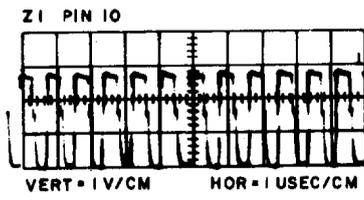
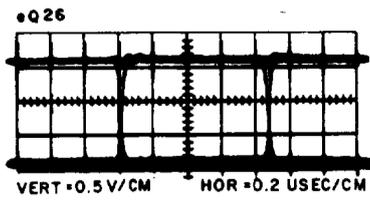
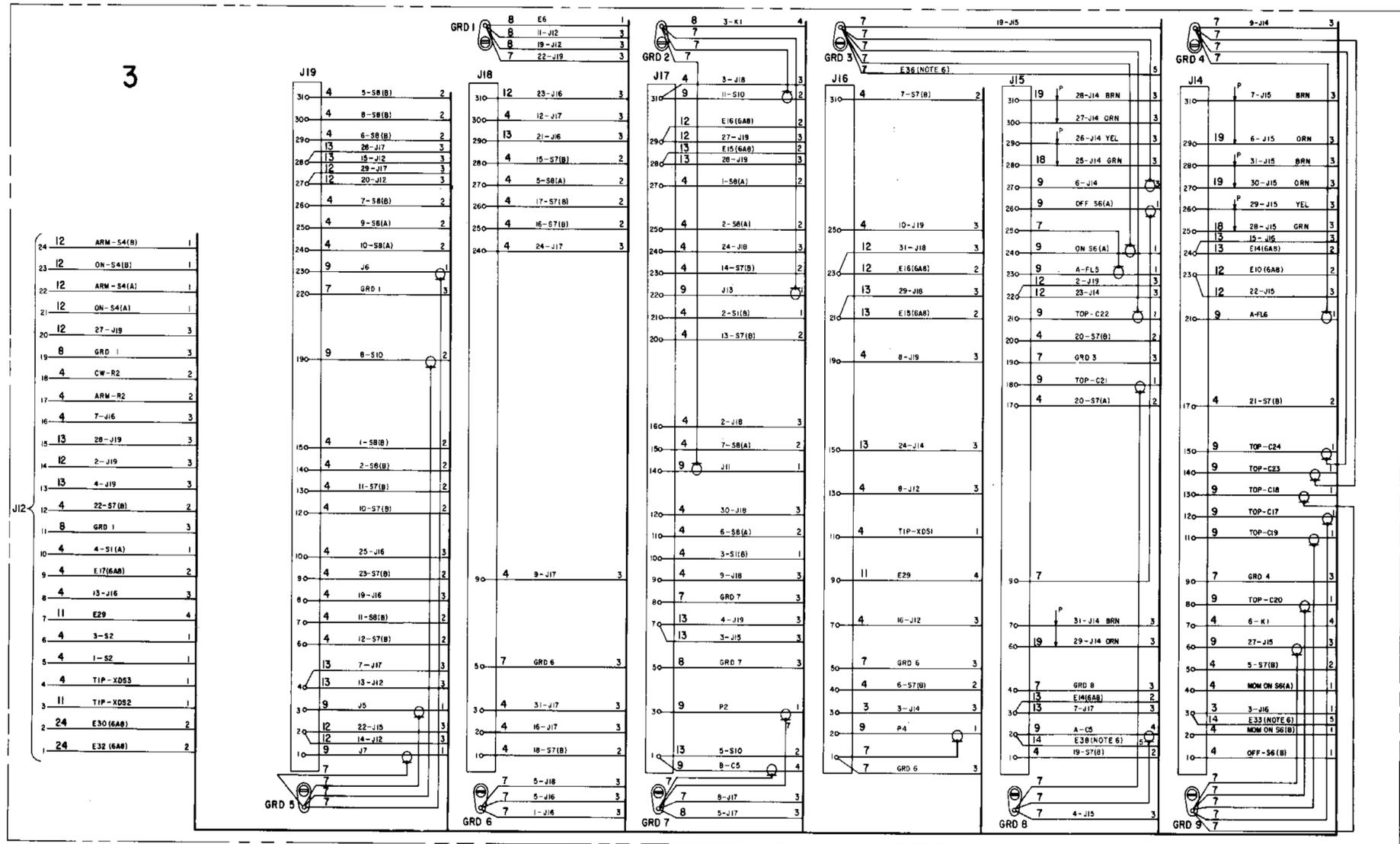
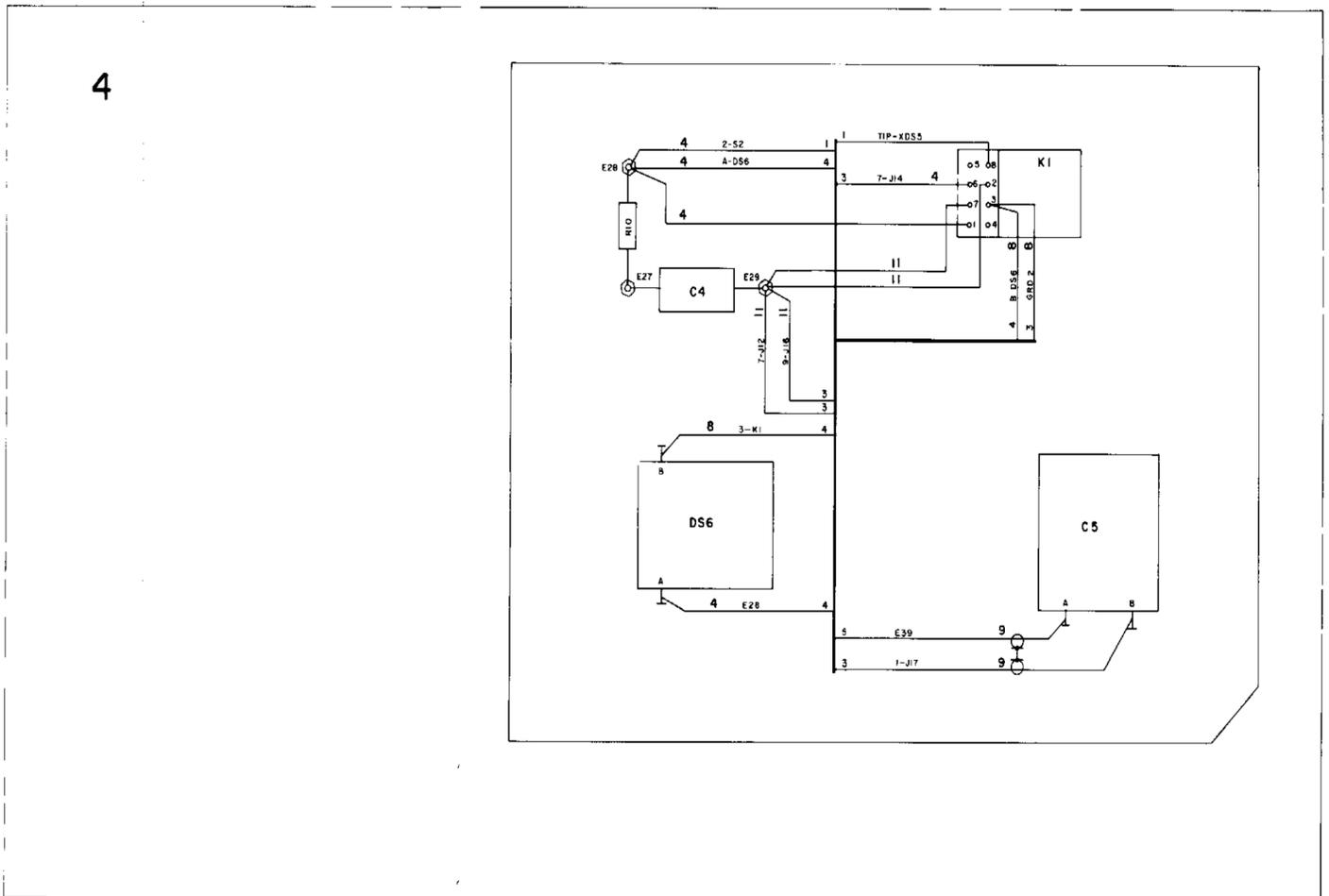


Figure 6-25(3). Panel 6A7, troubleshooting waveforms (part 3 of 3).

6-33

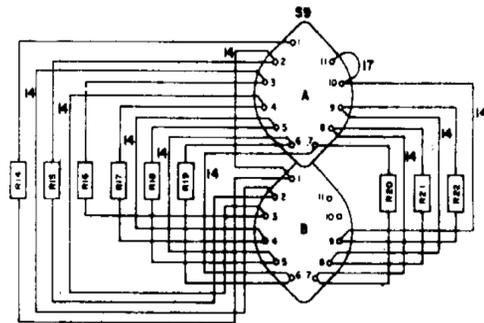


LEFT SIDE VIEW

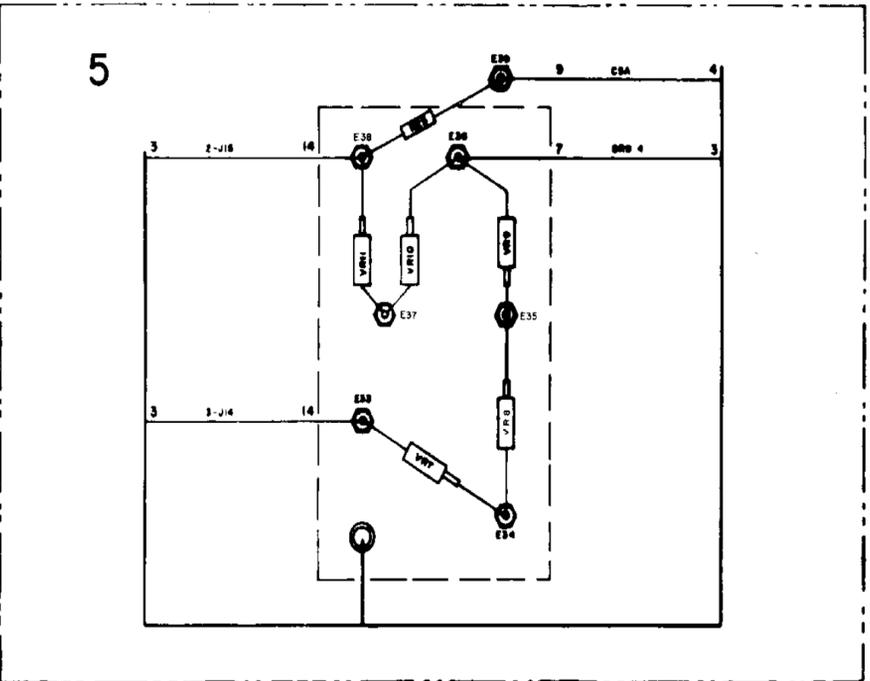


REAR VIEW OF REAR CHASSIS

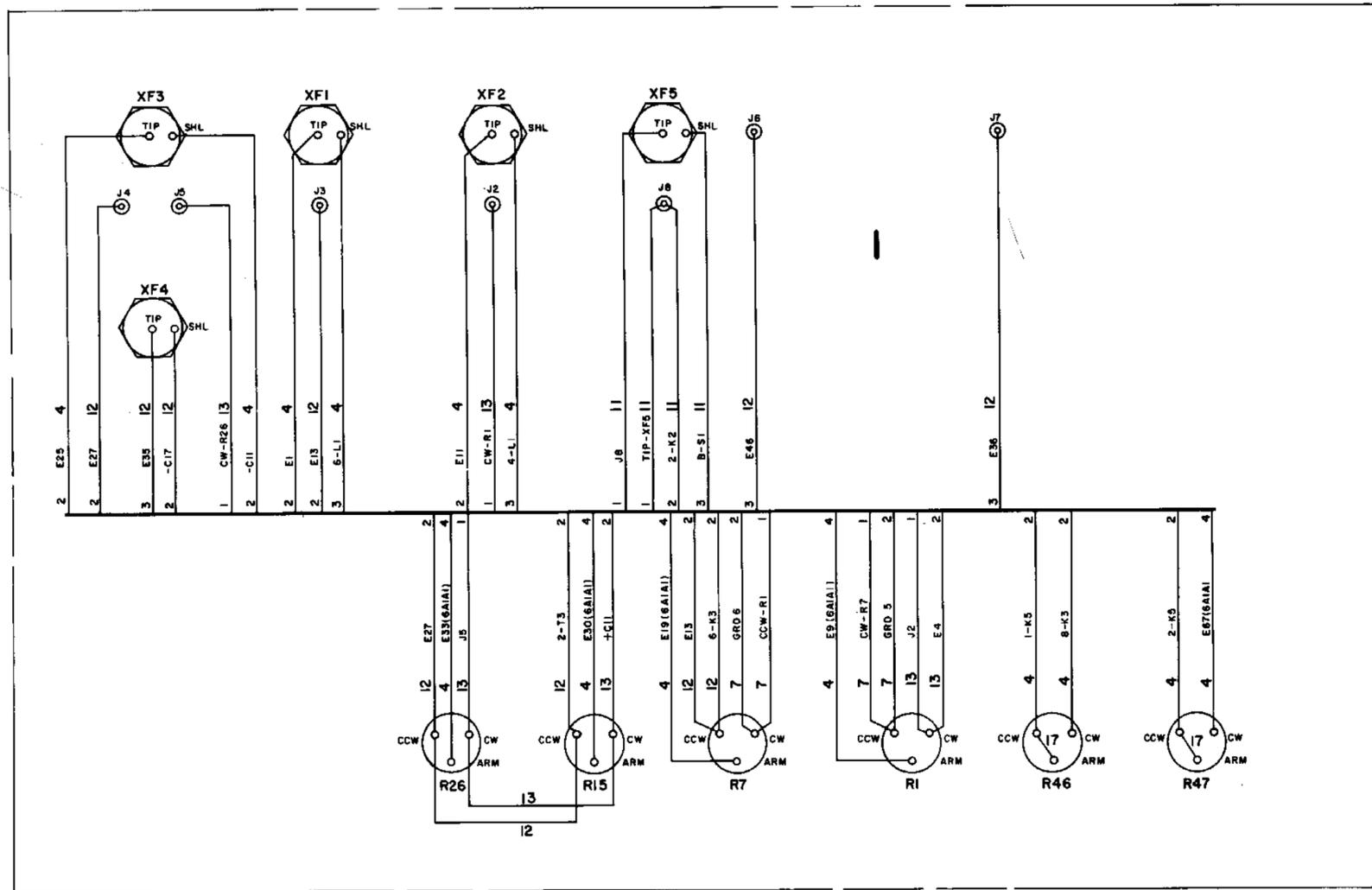
Figure 6-26. Multiplexer TD-201/U, wiring diagram (part 2 of 2).



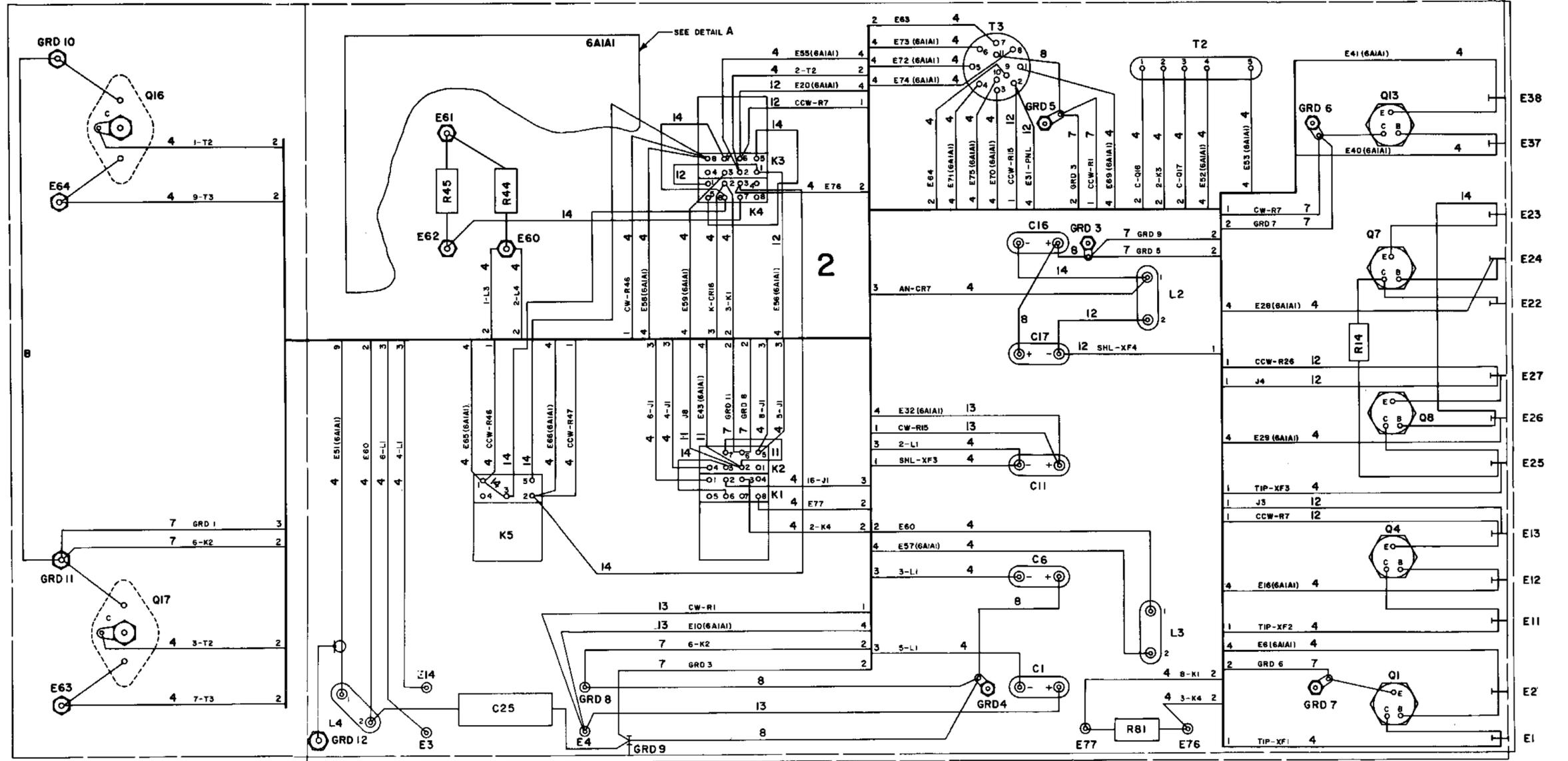
DETAIL A



DIODE PANEL MOUNTED BETWEEN J14 AND J15

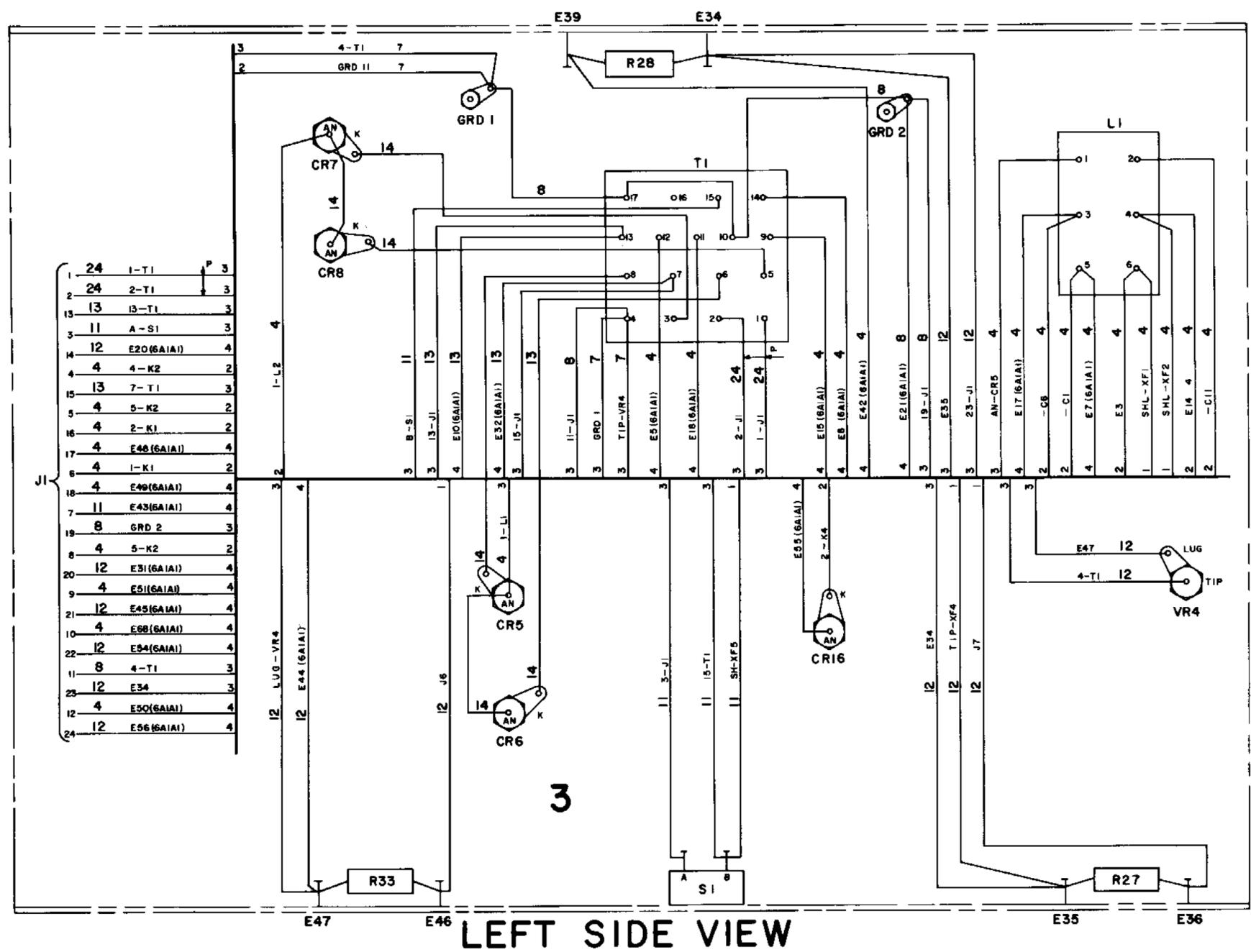


REAR VIEW OF FRONT PANEL

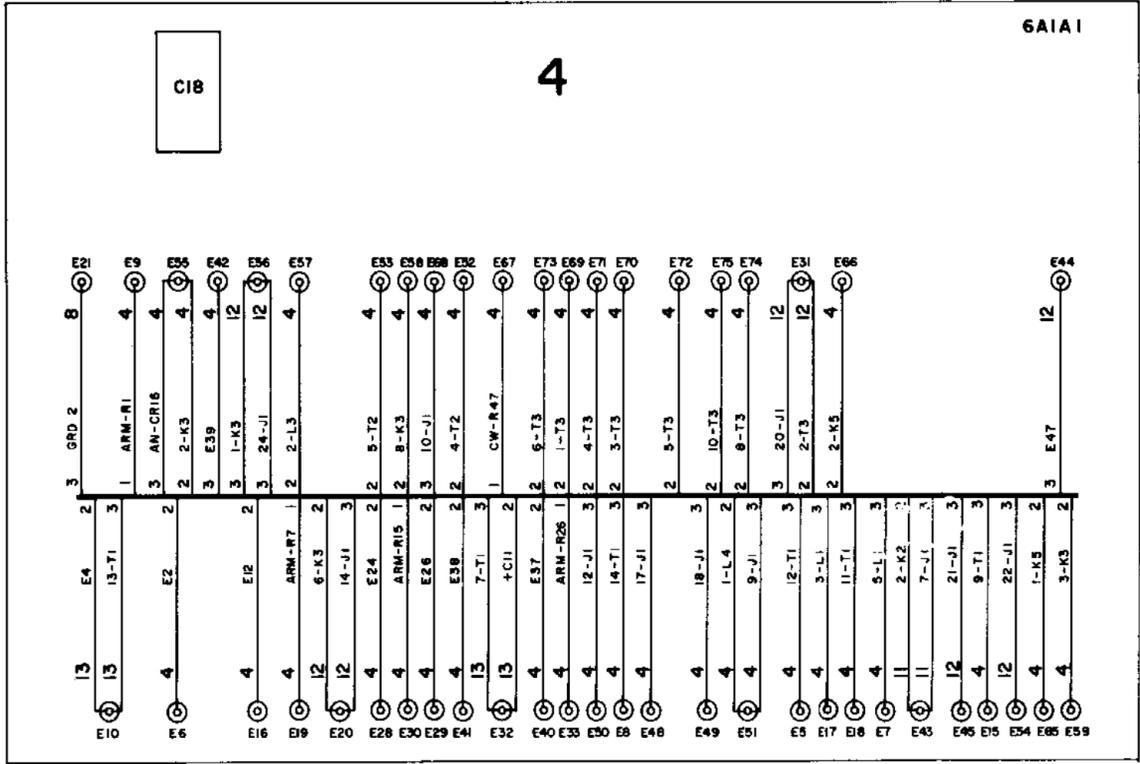


BOTTOM VIEW OF CHASSIS

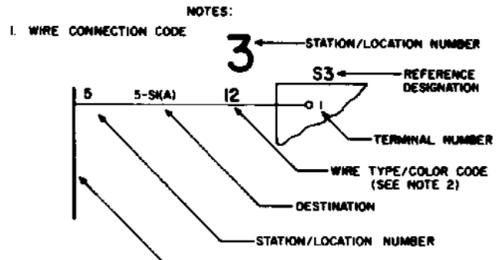
Figure 6-27(1). Power supply panel 6A1, wiring diagram (part 1 of 2).



LEFT SIDE VIEW



DETAIL A



1. WIRE CONNECTION CODE
2. WIRE TYPE/COLOR CODE
- | CODE | TYPE/COLOR |
|------|--|
| 1 | RG-108A/U COAXIAL |
| 2 | 3-CONDUCTOR TWISTED (WHT/GRN/BLK/SHLD) |
| 3 | 24 AWG YELLOW |
| 4 | 24 AWG WHITE |
| 5 | 20 AWG PURPLE |
| 6 | 20 AWG RED |
| 7 | 22 AWG BLACK |
| 8 | 20 AWG BLACK |
| 9 | RG-196A/U COAXIAL |
| 10 | 2-CONDUCTOR TWISTED (WHT/BLK/SHLD) |
| 11 | 22 AWG GREY |
| 12 | 22 AWG PURPLE |
| 13 | 22 AWG RED |
| 14 | 22 AWG WHITE |
| 15 | 22 AWG YELLOW |
| 16 | 18 AWG BARE WIRE |
| 17 | 22 AWG BARE WIRE |
| 18 | YEL/GRN TWISTED PAIR 24 AWG |
| 19 | ORN/BRN TWISTED PAIR 24 AWG |
| 20 | RG 180B/U COAXIAL |
| 21 | 24 AWG PURPLE |
| 22 | 24 RED |
| 23 | 24 BLACK |
| 24 | 20 GRAY |
| 25 | 20 WHITE |
| 5 | SLEEVE |
3. DENOTES COAXIAL CABLE
4. DENOTES SHIELDED CABLE
5. DENOTES TWISTED PAIR (CODE 24, NOTE 2)
- $\frac{1}{4} \pm \frac{1}{4}$ TURNS PER INCH

Figure 6-27(2). Power supply panel 6A9, wiring diagram (part 2 of 2).

NOTE
RIGHT SIDE VIEW IS APPLICABLE
TO TD-204/U SERIAL NUMBERS
1 THROUGH 333 ONLY.

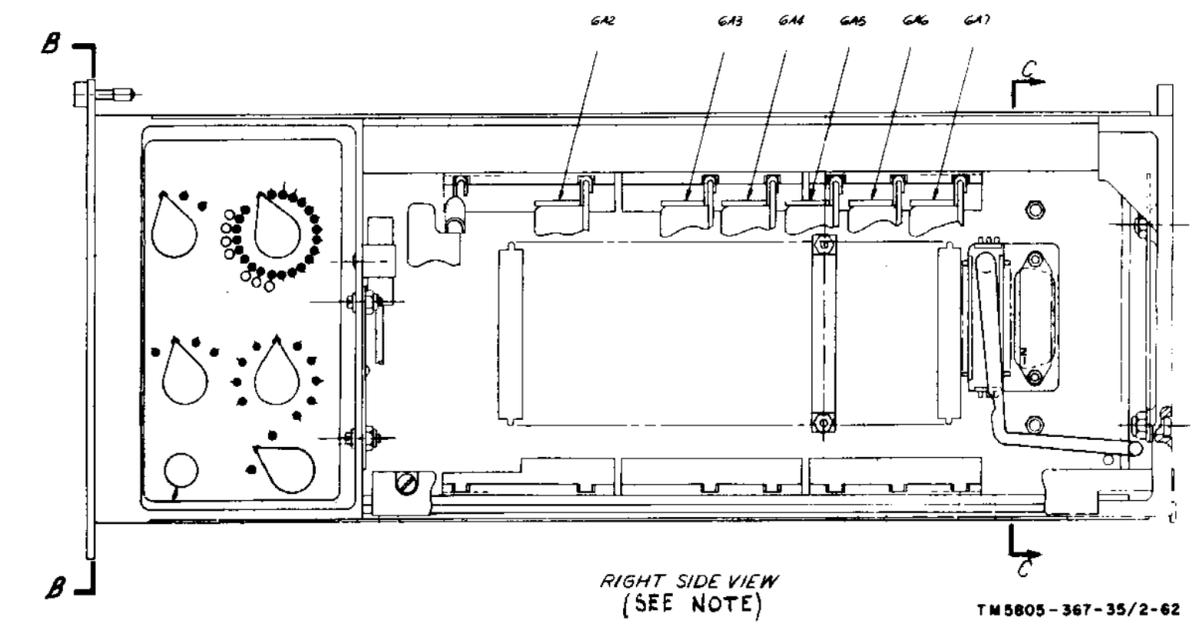
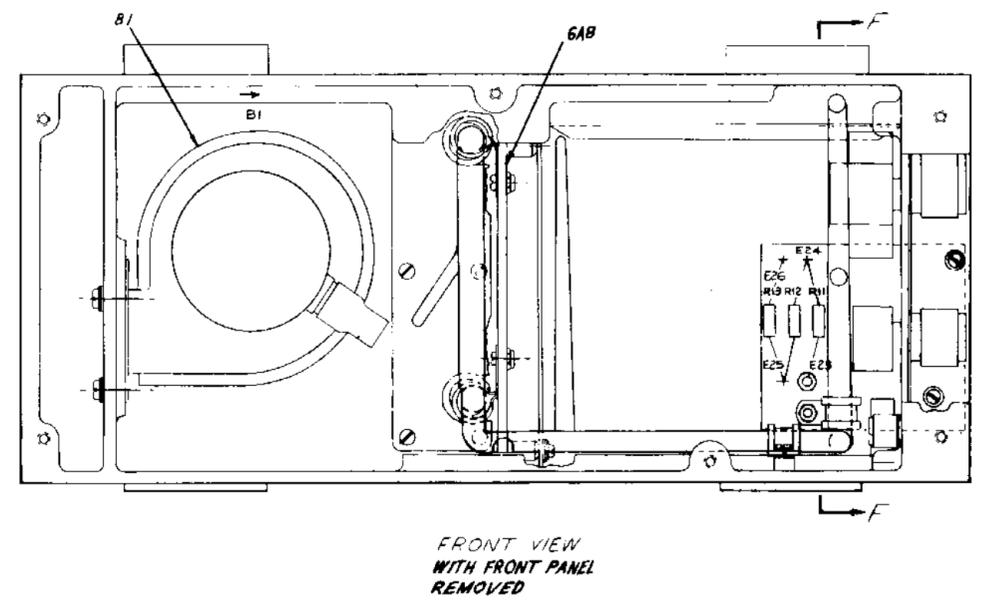
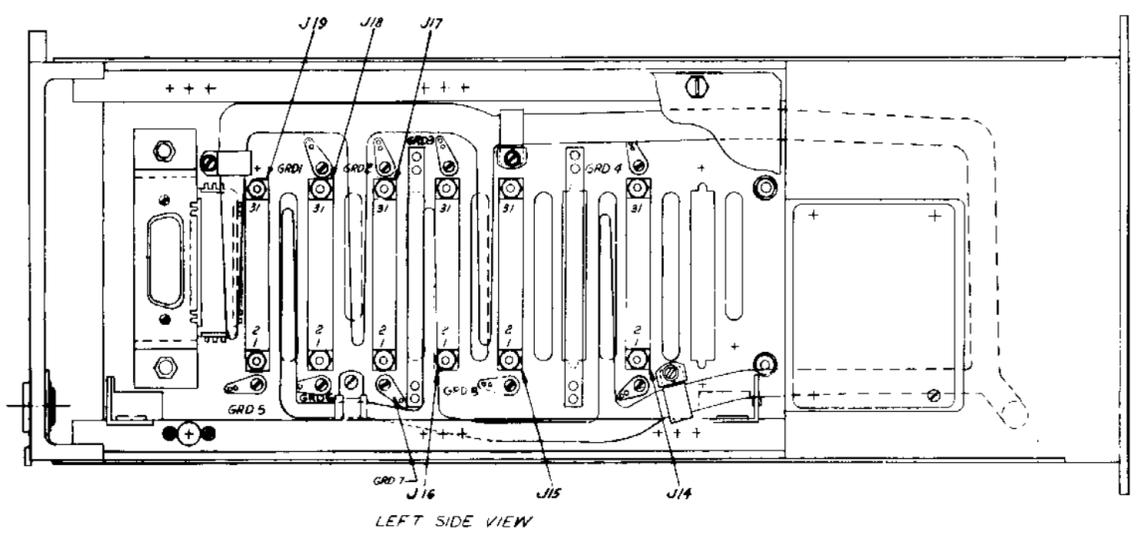
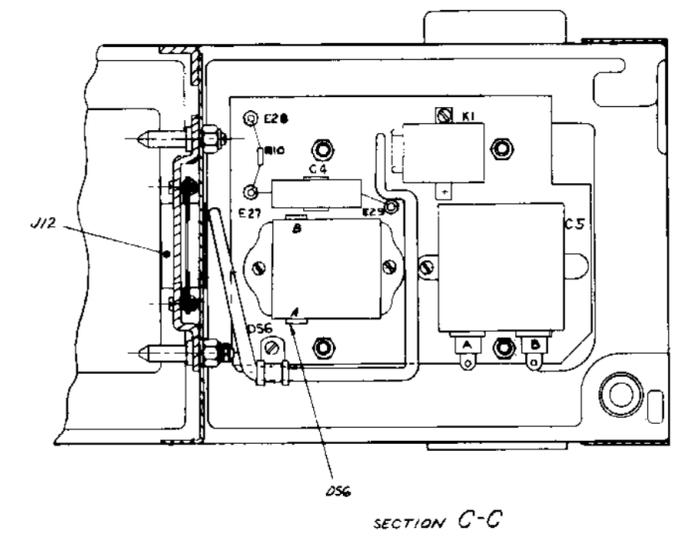
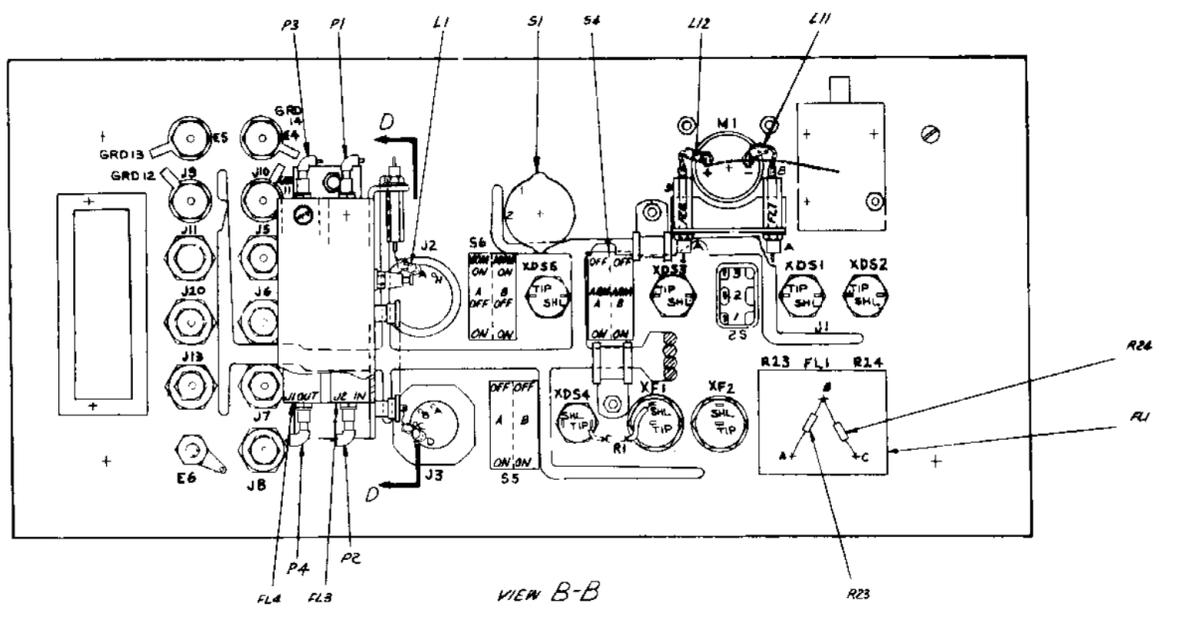
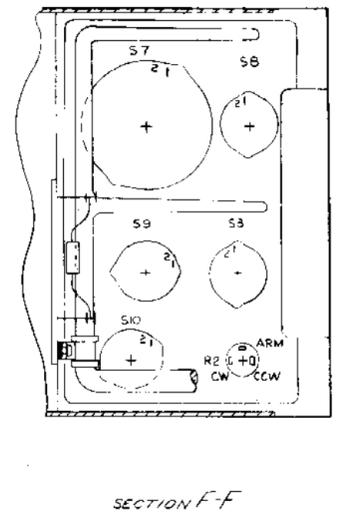
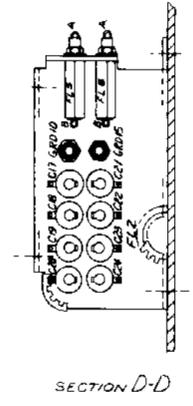
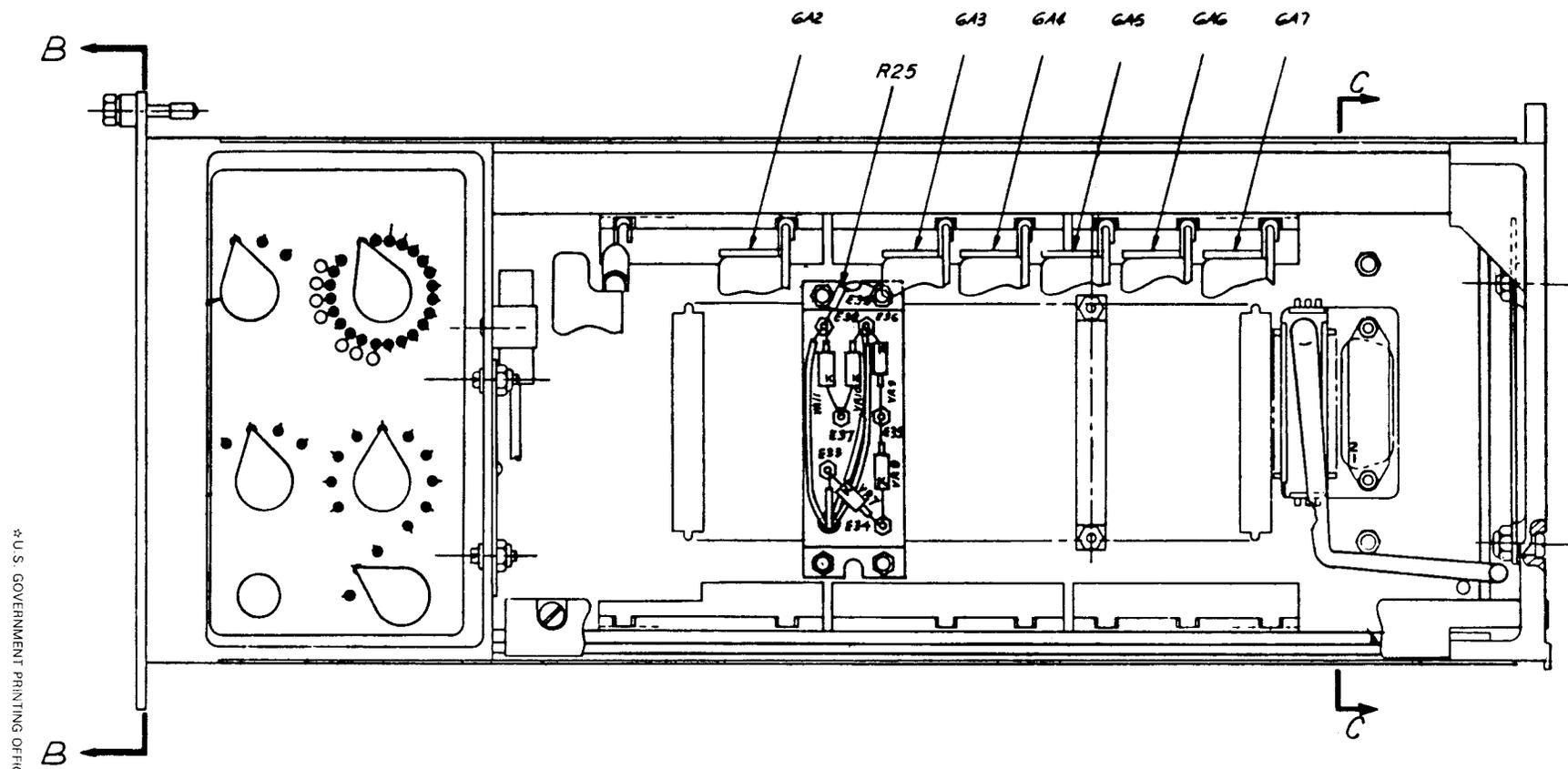


Figure 8-28. Multiplexer TD-204/U, chassis parts location.



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RIGHT SIDE VIEW

TM5805-367-35/2-CI-4

Figure 6-29. Multiplexer TD-204/U (serial numbers 314 and up), right side view, parts location.

C 1, TM 11-5805-367-35/2

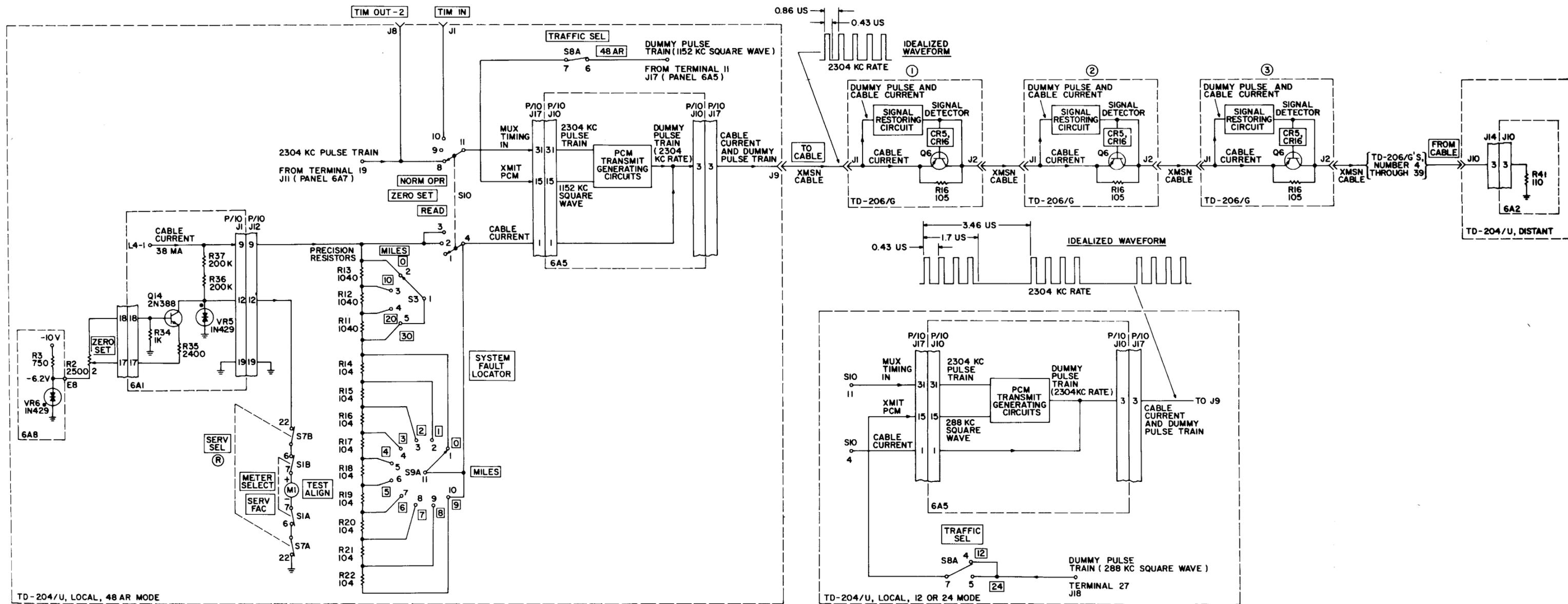


Figure 6-30. Restorer, Pulse Form TD-206/G fault-locating system, functional diagram.

By Order of the Secretary of the Army:

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General, United States Army,
Chief of Staff.

Official:

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USAAMS (2)
USAARMS (2)
USAIS (2)
ASAES (2)
USASESCS (20)
USATC Armor (2)

USATC Engr (2)
USATC Inf (2)
USASTC (2)
WRAMC (1)
Army Pic Cen (2)
USACDCEC (10)
Instl (2) except
Fort Gordon (10)
Fort Huachuca (10)
WSMR (5)
Fort Carson (21)
Fort Knox (12)
Army Dep (2) except
LBAD (14)
SAAD (30)
TOAD (14)
LEAD (7)
SHAD (3)
NAAD (5)
SVAD (5)
CHAD (3)
ATAD (10)
GENDEPS (2)
Sig Sec GENDEPS (5)
Sig Dep (12)
Sig FLDMS (2)
AMS (1)
USAERDAA (2)
USAERDAW (13)
USACRREL (2)
Units org under fol TOE:
(2 cys each)
11-57
11-97
11-98
11-117
11-127
11-155
11-157
11-158
11-500 (AA-AC)
11-587
11-592
11-597

NG: State AG (3).

USAR: None.

For explanation of abbreviations used, see AR 320-50.

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS



THEN...JOT DOWN THE DOPE ABOUT IT ON THIS FORM. CAREFULLY TEAR IT OUT, FOLD IT AND DROP IT IN THE MAIL.

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FIGURE NO.

TABLE NO.

IN THIS SPACE, TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT.

TEAR ALONG PERFORATED LINE

PRINTED NAME, GRADE OR TITLE AND TELEPHONE NUMBER

SIGN HERE

THE METRIC SYSTEM AND EQUIVALENTS

WEIGHT MEASURE

1 Centimeter = 10 Millimeters = 0.01 Meters = 0.3937 Inches
 1 Meter = 100 Centimeters = 1000 Millimeters = 39.37 Inches
 1 Kilometer = 1000 Meters = 0.621 Miles

WEIGHTS

1 Gram = 0.001 Kilograms = 1000 Milligrams = 0.035 Ounces
 1 Kilogram = 1000 Grams = 2.2 lb.
 1 Metric Ton = 1000 Kilograms = 1 Megagram = 1.1 Short Tons

LIQUID MEASURE

1 Milliliter = 0.001 Liters = 0.0338 Fluid Ounces
 1 Liter = 1000 Milliliters = 33.82 Fluid Ounces

SQUARE MEASURE

1 Sq. Centimeter = 100 Sq. Millimeters = 0.155 Sq. Inches
 1 Sq. Meter = 10,000 Sq. Centimeters = 10.76 Sq. Feet
 1 Sq. Kilometer = 1,000,000 Sq. Meters = 0.386 Sq. Miles

CUBIC MEASURE

1 Cu. Centimeter = 1000 Cu. Millimeters = 0.06 Cu. Inches
 1 Cu. Meter = 1,000,000 Cu. Centimeters = 35.31 Cu. Feet

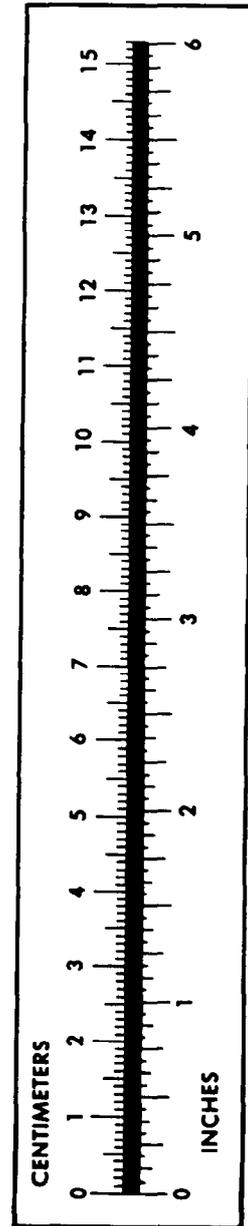
TEMPERATURE

$5/9(^{\circ}\text{F} - 32) = ^{\circ}\text{C}$
 212° Fahrenheit is equivalent to 100° Celsius
 90° Fahrenheit is equivalent to 32.2° Celsius
 32° Fahrenheit is equivalent to 0° Celsius
 $9/5^{\circ}\text{C} + 32 = ^{\circ}\text{F}$

APPROXIMATE CONVERSION FACTORS

TO CHANGE	TO	MULTIPLY BY
Inches	Centimeters	2.540
Feet	Meters	0.305
Yards	Meters	0.914
Miles	Kilometers	1.609
Square Inches	Square Centimeters	6.451
Square Feet	Square Meters	0.093
Square Yards	Square Meters	0.836
Square Miles	Square Kilometers	2.590
Acres	Square Hectometers	0.405
Cubic Feet	Cubic Meters	0.028
Cubic Yards	Cubic Meters	0.765
Fluid Ounces	Milliliters	29.573
its	Liters	0.473
arts	Liters	0.946
allons	Liters	3.785
Ounces	Grams	28.349
Pounds	Kilograms	0.454
Short Tons	Metric Tons	0.907
Pound-Feet	Newton-Meters	1.356
Pounds per Square Inch	Kilopascals	6.895
Miles per Gallon	Kilometers per Liter	0.425
Miles per Hour	Kilometers per Hour	1.609

TO CHANGE	TO	MULTIPLY BY
Centimeters	Inches	0.394
Meters	Feet	3.280
Meters	Yards	1.094
Kilometers	Miles	0.621
Square Centimeters	Square Inches	0.155
Square Meters	Square Feet	10.764
Square Meters	Square Yards	1.196
Square Kilometers	Square Miles	0.386
Square Hectometers	Acres	2.471
Cubic Meters	Cubic Feet	35.315
Cubic Meters	Cubic Yards	1.308
Milliliters	Fluid Ounces	0.034
Liters	Pints	2.113
Liters	Quarts	1.057
ers	Gallons	0.264
ms	Ounces	0.035
ograms	Pounds	2.205
Metric Tons	Short Tons	1.102
Newton-Meters	Pounds-Feet	0.738
Kilopascals	Pounds per Square Inch	0.145
meters per Liter	Miles per Gallon	2.354
meters per Hour	Miles per Hour	0.621



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