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TM 32-5820-030-14 & P

TECHNICAL MANUAL

COMBINED
OPERATIONS AND MAINTENANCE
INSTRUCTIONS
WITH
PARTS BREAKDOWN
(ORGANIZATIONAL AND INTERMEDIATE)

RADIO RECEIVER
TYPE
R-2174(P)/URR
AND
R-2174A(P)/URR

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7-56 Blank	0
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7-101 - 7-106	0
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8-1	2
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8-3	0
8-4 Blank	0
8-5	0
8-6 Blank	0
8-7	0
8-8 Blank	0
8-9	0
8-10 Blank	0
8-11	0
8-12 Blank	0
8-13	0
8-14 Blank	0
8-15	0
8-16 Blank	0
8-17	0
8-18 Blank	0
8-19	0
8-20 Blank	0
8-21	0
8-22 Blank	0
8-23	0
8-24 Blank	0
8-25	0
8-26 Blank	0
8-27	0
8-28 Blank	0
8-29	0
8-30 Blank	0
8-31	0
8-32 Blank	0
8-33	0
8-34 Blank	0
8-35	0
8-36 Blank	0
8-37	0
8-38 Blank	0
8-39	0
8-40 Blank	0
8-41	0
8-42 Blank	0
8-43	0
8-44 Blank	0
8-45	0
8-46 Blank	0
8-46.1	2
8-46.2 Blank	2
8-47	0
8-48 Blank	0
8-49	0
8-50 Blank	0
8-51	0
8-52 Blank	0
8-52.1	2
8-52.2 Blank	2
8-52.3	2
8-52.4 Blank	2
8-52.5	2
8-52.6 Blank	2
8-53	0
8-54 Blank	0
8-55	0
8-56 Blank	0
8-57	0
8-58 Blank	0
8-59	0
8-60 Blank	0
8-60.1	2
8-60.2 Blank	2
8-61	0
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WARNING
HIGH VOLTAGE

is used in the operation of this equipment

DEATH ON CONTACT

may result if personnel fail to observe safety precautions.

Learn the area containing the high voltage within the equipment.

Be careful not to contact high voltage connections when installing or operating this equipment.

Before working inside the equipment, turn power off and ground points of high potential before touching them.

SAFETY SUMMARY

The following are general safety precautions that are not related to any specific procedures and therefore do not appear elsewhere in this publication. These are recommended precautions that personnel must understand and apply during many phases of operation and maintenance.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must at all times observe all safety regulations. Do not replace components inside the equipment with the power supply turned on. Under certain conditions, dangerous potentials may exist when the power control is in the off position, due to charges retained by capacitors. To avoid casualties, always remove power and discharge ciruits to ground before touching any circuit components. Remove watches and rings before performing any maintenance procedures.

DO NOT SERVICE OR ADJUST ALONE

Under no circumstances should any person reach into or enter the enclosure for the purpose of servicing or adjusting the equipment except in the presence of someone who is capable of rendering aid.

RESUSCITATION

Personnel working with or near high voltages should be familiar with modern methods of resuscitation. Cardiopulmonary resuscitation procedures are outlined in TO 31-1-141-1, and annual refresher training requirements are outlined in AFOSH STD 127-50.

The following WARNINGs, CAUTIONs, NOTEs and indicators appear in the text of this volume, and are explained here for emphasis.

WARNING

Bodily harm or death can occur.

CAUTION

Damage to equipment can occur.

NOTE

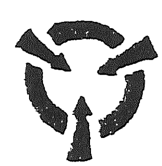
Annotates condition or parameter.

Indicator

HANDLING OF ELECTROSTATIC DISCHARGE SENSITIVE DEVICES (ESDS)

Electrostatic Discharge Sensitive Devices (ESDS) must be handled with certain precautions that must be followed to minimize the effect of static build-up.

Consult TO 00-25-234, DOD Std-1686, and DOD HDBK 263. ESDS devices are identified in this technical order by the following symbol:



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NOTE

An alphabetical index is located at the back of this manual. The introduction (preceding Section I) explains the material covered in each section.

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INTRODUCTION

This technical manual provides operation and maintenance instructions for the R-2174(P)/URR and R-2174A(P)/URR Radio Receiver, along with an Illustrated Parts Breakdown and Schematic Diagrams. The manual is prepared in accordance with specifications MIL-M-38798B and MIL-M-38807 and other specifications and publications as called for by these two specifications. The Operation, Maintenance and Schematic Diagrams were prepared in accordance with MIL-M-38798B while the Illustrated Parts Breakdown was prepared in accordance with MIL-M-38807. The manual consists of eight chapters along with a cross reference index and alphabetical index.

The original R-2174 contains 11 major modules numbered A1 through A10 with the A5 and A6A1 being optional. The edgelighting configuration in the R-2174 utilizes incandescent bulbs. Also in this model, two configurations for the A7 board exist.

The improved R-2174A version contains the same 11 modules, however the A2 (First Mixer Assembly) and A8 (Second LO/BFO Synthesizer Assembly) boards have been redesigned and assigned new part numbers. Additionally, the edgelighting configuration now includes the use of LEDs. Changes in the R-2174A version are directly interchangeable with the original R-2174 version. This manual includes both the R-2174 and the R-2174A versions.

Chapter 1 presents general information about the Receiver, which includes its physical and operating characteristics. Chapter 2 contains two sections with the first section providing information on installation logistics. Section II provides procedures for installing the Receiver and for checking its performance. Preparation for use and reshipment is presented in Chapter 3. This information includes procedures for unpacking the equipment and preparing it for installation. Procedures are also included in this chapter for repacking the unit and preparing it for storage or reshipment. Chapter 4 contains information on operation of the Receiver. This information is designed to acquaint the technician with the unit, and to describe its controls indicators and operating characteristics. Step by step procedures are also provided for operating the Receiver in various modes.

The theory of operation is presented in two ways in Chapter 5. The first method, contained in Section I, describes the system function while the second method provides a detailed circuit analysis and is contained in Section II. Chapter 6 provides information for all functions of maintenance to be performed at organizational and intermediate levels. An Illustrated Parts Breakdown is provided in Chapter 7 which includes a listing of all component parts, contained in the Receiver. Chapter 8 contains schematic diagrams, for all the electronic circuits of the Receiver. An alphabetical index as well as a cross reference index is included at the end of the manual to provide the user with a convenient method for locating information.

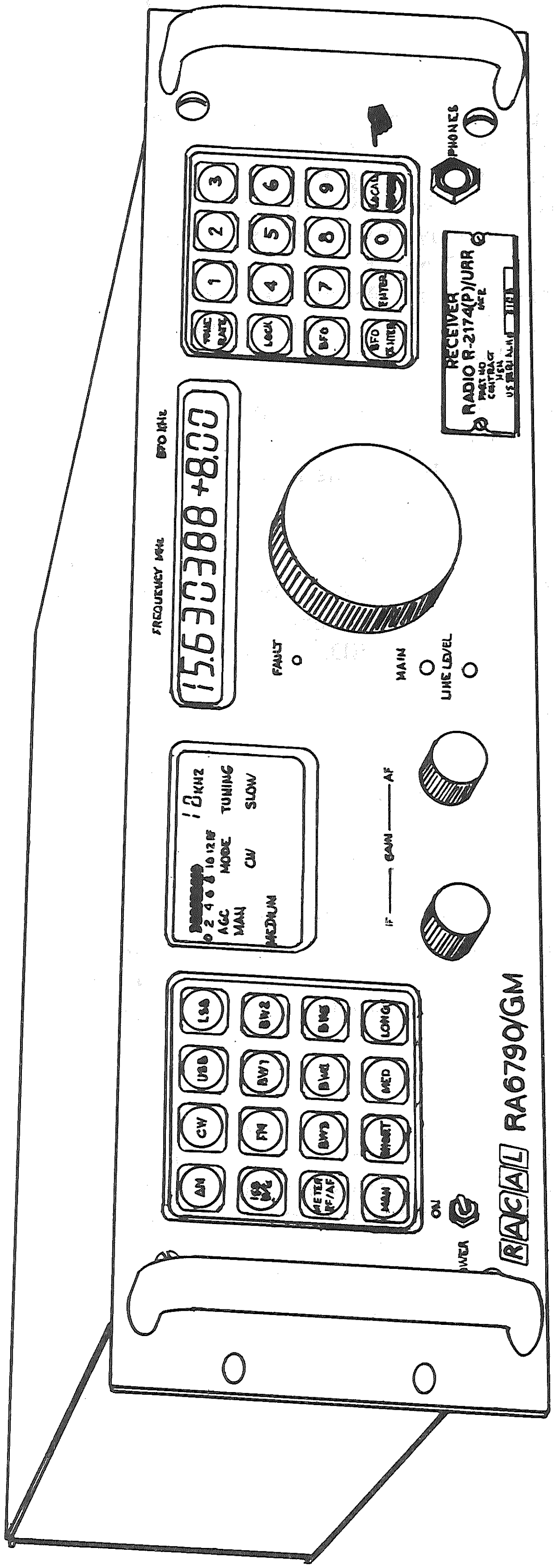


Figure 1-1. Radio Receiver R-2174 (P)/URR, Overall View

CHAPTER 1
GENERAL INFORMATION

1-1. INTRODUCTION. Chapter 1 provides general information on the R-2174(P)/URR Radio Receiver. This information describes the equipment, gives its purpose, leading particulars, capabilities and limitations. Figure 1-1 shows an overall view of the R-2174(P)/URR Radio Receiver. A list of the equipment supplied, test equipment and technical manuals related to the Receiver are also provided in this chapter.

1-2. DESCRIPTION AND PURPOSE. The R-2174(P)/URR Radio Receiver is designed to receive and demodulate HF signals within frequency range from 0.5 to 29.999 MHz with reception capabilities for AM (A3), FM (F3), CW (A1), LSB/USB (A3J) and optionally ISB (A3B). Reception mode codes are defined in Table 1-1. The unit is a fully synthesized, solid state, microcomputer controlled Receiver that can be operated from its front panel or optionally from a remote location. The Receiver can be tuned over its frequency range by selecting incremental digits from the tens MHz to 1 Hz. Convenient fron panel control of most receiver functions is achieved through pushbutton keypads and an easy spin tuning knob with readouts presented on two liquid crystals displays.

a. Selectivity. Receiver bandwidth is selectable through plug-in filters. Any number of filters, from 1 to 7, of various bandwidths may be installed in the Receiver with selection of a particular bandwidth (filter) made through Receiver control. Fifteen different filters are available that cover bandpass from 400 Hz to 16 kHz including two sideband filters for upper, lower and optional independent sideband modes. The optional available filters are listed in Table 1-5.

b. Receiver outputs. In addition to a front panel audio PHONES jack for audio monitoring, audio, IF, reference frequencies, diversity AGC and fault indicating outputs are available at the rear panel.

(1) Audio. The front panel PHONES jack provides a nominal 10 milliwatts into 600 ohms and is adjustable with the front panel AF GAIN control. A nominal 1 milliwatt, 600 ohm balanced line and a nominal 1 Watt, 8-ohm line is output to the rear panel. When the receiver is equipped with the optional ISB circuit card, two additional 1 milliwatt, 600 ohm balanced lines are output to the rear panel for sideband audio.

(2) IF Output. A 455 kHz IF output of −10 dBm nominal into 50 ohms is available through a separate connector on the rear panel.

(3) Reference Frequencies. When the receiver is operated in the internal mode (using the internal reference oscillator), one of three selectable reference frequencies (1 MHz, 5 MHz or 10 MHz) of (approximately) 0 dBm into 50 ohms is available through a separate connector on the rear panel.

(4) Diversity AGC. Automatic gain control outputs from the MAIN IF-AGC circuits, and when installed, from the ISB-AGC circuits are routed to the rear panel for diversity AGC.

(5) Fault Indication Output. In addition to a fault indicator on the front panel a fault indicating circuit that provides a TTL level, related to a fault condition, is output to the rear panel.

c. Receiver Control Capabilities. The Receiver may be operated from its front panel or, with an optional plug-in circuit card, it may be operated from a remote location.

(1) Front Panel (local) Control. Two sets of keypads provide for receiver tuning, mode selection, AGC control, bandwidth selection, RF/AF metering and Built In Test Equipment (BITE) functions. A tuning knob is used to tune BFO offset frequency or may be used as an alternate means for receiver tuning. An IF GAIN control can be used to set AGC threshold levels or may be disabled with fully automatic AGC. An AF GAIN control and two line level controls are used to control audio output levels. Two liquid crystal displays monitor and display receiver functions.

(2) Remote Control. With the optional A6A1 circuit card installed, the Receiver can be controlled from a remote location using serial asynchronous (ASCII-7 bit) character oriented data at one of 16 selectable baud rates from 50 baud to 19.2 kilobaud. Receiver parameters that can be controlled through the remote option include; receiver frequency, BFO, bandwidth, detection mode, AGC, RF/IF manual gain, system status, fault status and BITE control. When remote equipment is in place and operating there is both remote and front panel indication of receiver status when controlled either remotely or locally, with remote indications being sent upon request from the remote controller.

d. Built In Test Equipment (BITE). The Receiver contains a built in test system that can find and isolate faults to a circuit card. The BITE, when initiated locally or remotely runs a self test sequence on various receiver parameters and provides a coded fault readout when faults are detected. The coded readout can then be used to determine the nature of the fault and its location.

1-3. **FUNCTIONAL DESCRIPTION.** Figure 1-2 shows a simplified block diagram of the Receiver which will aid in understanding this functional description. The description is divided into six functions that best describe the functions of the Receiver: primary signal flow, oscillator synthesizers, automatic gain control, receiver control, built in test equipment and receiver power.

a. Primary Signal Flow. Input signals from an antenna are connected directly to a modular RF lowpass filter which rejects signals above the 30 MHz upper range of the Receiver. The RF output of the filter is routed to the first mixer circuit card and mixed with the synthesized first local oscillator signal. The oscillator is variable between 40.955 and 70.454999 MHz and when mixed with the RF signal yields a difference frequency of 40.455 MHz. This first IF signal is coupled through a bandpass filter, that provides a 20 kHz bandpass, to an AGC controlled amplifier. This AGC level controlled IF signal is then routed to the second mixer circuit card. This circuit card provides additional AGC control and bandpass filtering before coupling the signal to the second mixer. The second mixer with a 40 MHz input from the second local oscillator along with the 40.455 MHz first IF input yields the difference frequency of 455 kHz which is used as the second IF. The second IF signal is filtered and coupled to an IF amplifier to restore gain and for coupling to the plug-in bandpass filters on the main IF/AF circuit card. Any number (up to seven) filters may be plugged into the filter slots which are then selected through receiver control to provide selected bandwidth to the IF signal. The output of filter slot FL1 can be linked to the optional ISB circuit card or linked to the common selected output of the six other filter slots. This output is coupled to an AGC controlled IF amplifier which provides gain and filtering to the IF signal with a selected bandwidth. A portion of this signal is routed through an IF output amplifier to the rear panel. The IF signal is also routed to two detectors along with the BFO oscillator frequency. In CW and sideband modes the BFO, through receiver control, is routed through a limiting amplifier for carrier reinsertion at the product detector. In the AM mode the AM carrier is routed through the same path. In the FM mode the carrier is removed by the FM detector. Receiver control selects the output from the appropriate detector and routes it through an audio lowpass filter to a crosspoint switch. This switch, through receiver control, directs this audio along with ISB audio, when present, through level controls to audio output amplifiers. In non ISB modes three outputs are available; the front panel PHONES jack and a loud speaker output at the rear panel, both controlled by the AF GAIN control and a balanced 600 ohm 1 milliwatt MAIN LINE rear panel output controlled by the MAIN LINE LEVEL control. In the ISB mode two additional balanced 600 ohm 1 milliwatt lines are output to the rear panel. The outputs contain the USB (line 1) and the LSB (line 2) and are controlled by the MAIN and I-LSB LINE LEVEL controls,respectively. The MAIN LINE, PHONES and loudspeaker outputs may contain either the USB or LSB as selected through receiver control. In this ISB mode the output of IF bandpass filter FL1 is linked to the input of the optional ISB circuit card and processed in the same manner as the main IF except the BFO is routed through an amplifier directly to the product and synchronous detector and the audio output routed through an emitter follower to the crosspoint switch on the MAIN IF/AF circuit card. This signal is then processed as described above.

b. Oscillator Synthesizers. The Receiver contains a first local oscillator synthesizer for frequency input to the first mixer, a second local oscillator synthesizer for frequency input to the second mixer and a beat frequency oscillator synthesizer for carrier reinsertion to the product detectors in CW and sideband modes.

(1) First Local Oscillator Synthesizer. The first local oscillator output, variable between 40.955 and 70.454999 MHz, is used as the input to the first mixer. Its frequency, controlled through receiver control, determines reception frequency when mixed with the RF signal, to always yield a difference frequency of 40.455 MHz as the first IF signal. The voltage controlled oscillators frequency is adjustable through a phase lock loop which is controlled through conversion of digital inputs from receiver control.

(2) Second Local Oscillator Synthesizer. The second local oscillators output, fixed at 40 MHz, is used as the input to the second mixer. This signal is mixed with the first IF signal of 40.455 MHz and yields a difference frequency of 455 kHz which forms the second IF signal. The voltage controlled oscillator operates at 20 MHz through a phase lock loop which keeps the oscillator locked on frequency. The 20 MHz output is coupled through a frequency doubler circuit to provide 40 MHz to the second mixer. The output of this oscillator is also used to provide reference frequencies, through divide by circuits, to the first local oscillator, (1 MHz) the BFO (1 MHz) and to the rear panel of the Receiver (1,5, or 10 MHz). The second local oscillator receives its reference frequency either from the internal reference (5 MHz) or from an external reference.

(3) Beat Frequency Oscillator. The beat frequency oscillator (BFO) output, variable between 447 and 463 kHz, is used as carrier reinsertion at the product detectors for CW and sideband operation. The oscillator operates at a center frequency of 22.75 MHz, 50 times above the BFO output frequency. The oscillator is variable through a phase lock loop that is controlled through conversion of digital inputs from receiver control. The output of the oscillator is routed through a divide by 50 circuit to the product detectors on the main IF/AF circuit card and to the optional ISB circuit card when installed.

c. Automatic Gain Control. The Receiver contains Automatic Gain Control (AGC) circuitry for maintaining audio and IF output levels with large variations in the incoming RF signals. The AGC operates in one of three selectable modes; automatic, manual, or automatic with a manually set threshold. The AGC receives a portion of the second IF signal, detects it, provides three different hang times (long, medium or short) provides for automatic or manual threshold control, filters and distributes the gain control signal to both the first and second IF amplifiers. Two similar AGC circuits, just described, are contained; one on the MAIN IF/AF circuit card, the second on the optional ISB circuit card, but with their outputs integrated with each other. In non ISB modes the system operates as described above through the MAIN IF-AGC circuits. In ISB modes, the stronger of the two signals, from upper and lower sidebands, control the first IF amplifiers while the second IF amplifiers are controlled independently with their respective AGC circuits.

d. Receiver Control. The Receiver is controlled through a pre-programmed microcomputer contained on a circuit card within the Receiver. Receiver control instructions, are routed through computer controlled interface circuits to the microcomputer. These receiver control instructions are processed by the microcomputer which in turn sends instructions through interface circuits to the appropriate receiver function to be controlled and to indicating circuits. Front panel (local) instructions are routed through the receiver control circuit card while remote instructions are routed through an optional interface circuit card. In either remote or local mode the microcomputer instructions are routed through the receiver control circuit card to receiver functions and to two liquid crystal displays on the front panel. Receiver status information is stored in the microcomputer and can be routed to a remote controller, on request, through the optional interface circuit card. The microcomputer processed instructions control; receiver frequency (first local oscillator), BFO (BFO oscillator), bandwidth (filter selection), AGC mode and level (AGC circuits) receiver mode (detector selection) audio output (MAIN/ISB selection), built in test equipment (BITE), and readouts for the above functions along with AF/RF metering.

e. Built In Test Equipment. The built in test equipment (BITE) is a system of microcomputer programs that reads receiver parameters to determine performance of various circuits. The BITE sequence controls receiver functions to read parameters under various modes, frequencies, bandwidths, etc. The tests performed by BITE include; readability of the microcomputer RAMs (random access memory), lock condition and settling time of all three frequency synthesizers, locating and measuring the bandwidth of installed IF bandpass filters, AGC operation including ISB AGC (if installed), product detector operation and metering circuit operation.

f. Receiver Power. The receiver contains a modular power supply which can be operated from 100, 120, 220 or 240 Volt, 48 to 420 Hz, single phase power. The power supply converts the ac input into six different dc voltages for distribution throughout the receiver. Four of the dc voltages (+5, +15, −15 and +20) are regulated while two (+5 and +15) are non regulated.

TABLE 1-1. RECEPTION MODE CODES

Complete Designation Example:

2 A 2 H

Bandwidth in kHz — 2

Type of Transmission — A

A = AM
F = FM
P = PCM

Purpose — 2

0 = No modulation
1 = Telegraphy (on-off)
2 = Telegraphy (modulation)
3 = Telephony
4 = Facsimile
5 = Television
6 = Duplex Telegraphy
7 = Multichannel Telegraphy
9 = None of the above

Supplementary Characteristics — H

A = Single sideband reduced carrier
B = Two independent sidebands
C = Single sideband, vestigial
H = Single sideband, full carrier
J = Single sideband, suppressed carrier
(None) = Double sideband, full carrier

Abbreviations:

AFC = Automatic Frequency Control
AM = Amplitude Modulation
CW = Continuous Wave
FM = Frequency Modulation (or Phase)
FSK = Frequency Shift Keying
ISB = Independent Sideband
LSB = Lower Sideband
MCW = Modulated Continuous Wave
PCM = Pulse Coded Modulation
SSB = Single Sideband
USB = Upper Sideband

1-4. MECHANICAL DESCRIPTION. A rigid, die-cast, full width chassis is used as the base for the mainframe of the Receiver. Mounted within compartments on the underside of this chassis are the mixer boards and the frequency generation system. The input lowpass filter, (A1), main IF/AF, (A4), optional ISB IF/AF (A5) and power supply modules (A10) are located on the top surface of the die-cast chassis while the control (A9) and digital I/O modules (A6A1 and A6A2) are attached to the Receiver mainframe. All modules are accessible for maintenance and can be removed or replaced using simple hand tools without the use of a soldering iron.

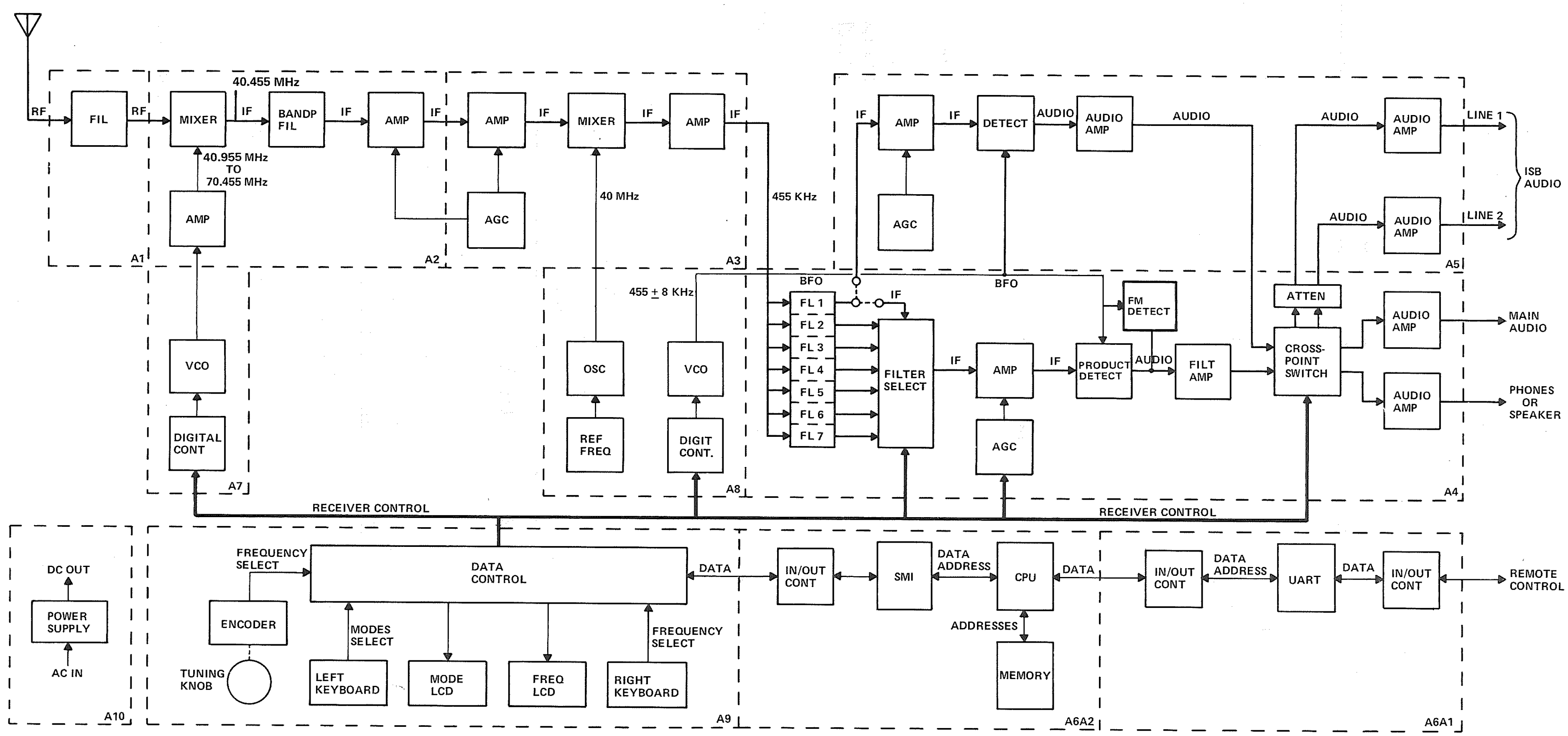


Figure 1-2. Radio Receiver R-2174(P)/URR, Simplified Block Diagram

a. Manual controls and indicators for operation of the Receiver are contained on the front panel while input/output jacks and connectors are provided on the rear panel. A PHONES jack, for audio connection to optional headphones, is contained on the front panel for convenient access. A primary power fuse is accessible from the rear panel.

1-5. **LEADING PARTICULARS.** Table 1-2 lists the leading particulars for the Receiver. These particulars include official nomenclature, common name, physical descriptions, storage and cabling requirements.

1-6. **CAPABILITIES AND LIMITATIONS.** Table 1-3 describes functional characteristics for the Receiver along with individual component characteristics and ambient conditions for operation. The left column of the table lists the Receiver function while the right column describes the capability or limitation.

1-7. **EQUIPMENT SUPPLIED.** Table 1-4 lists the equipment supplied with the Receiver. Equipment shown as optional may or may not be supplied with the Receiver.

1-8. **EQUIPMENT REQUIRED BUT NOT SUPPLIED.** All equipment required for normal installation and operation of the Receiver is supplied and listed in Table 1-4. No other equipment is required to place the unit in operation.

1-9. **OPTIONAL ITEMS.** Optional filters, assemblies, and other items that are available for use with the Receiver are listed in Table 1-5.

1-10. **TEST EQUIPMENT.** Test equipment required for intermediate level maintenance is listed in Table 1-6. No other tools or test equipments are required for organizational level maintenance.

1-11. **RELATED TECHNICAL MANUALS.** A list of the technical manuals related to the Receiver are presented in Table 1-7. The publication number, title, and equipment nomenclature for each manual is shown.

1-12. **MNEMONICS.** Table 1-8 lists mnemonics and acronyms used throughout this manual.

TABLE 1-2. LEADING PARTICULARS

Leading Particular	Description
Nomenclature	Receiver, Radio R-2174(P)/URR.
Common Name	Receiver
Type	Superheterodyne HF, Solid State, RF and Logic Modular Circuitry.
Package	Modular circuit card assemblies, packaged in an aluminum frame using a die-cast internal support and housing.
Primary Power Requirements	100, 120, 220 or 240 ±10% Volts and 43 to 420 Hz at 50 Watts (nominal) consumption.
Primary Power Selection	Printed circuit card switch for selection of one of 4 above listed voltages.
Physical Size	Chassis size: Height, 5.1 inches high; 16.6 inches wide; 18.4 inches deep. Front panel size: 5.25 inches high; 19.0 inches wide. Overall depth with handles: 20.0 inches.
Weight	30 Pounds.

TABLE 1-2. LEADING PARTICULARS (Cont.)

Leading Particular	Description
Mounting	Designed for standard rack mounting with two front panel handles for ease and safety in handling during installation or removal.
Storage Requirements	May be stored in ambient -40^{o} to $+70^{o}C$ with humidity from 10 to 95 percent non-condensing.
Cabling Requirements	See Chapter 2, Installation.

TABLE 1-3. CAPABILITIES AND LIMITATIONS

Receiver Function	Capability or Limitation
Frequency Range	500 kHz to 29.999999 MHz.
Frequency Selection	1 Hz increment.
Frequency Tuning	By keyboard entry or continuous tuning with selectable rate, FAST (1 kHz increments), SLOW (30 Hz increments) and FINE (1 Hz increments). BFO continuous in 10 Hz increments.
Frequency Indication	(a) 8 digit electronic readout of tuned frequency to 1 Hz. (b) 3 digit and sign readout of BFO relative to IF center ±8 kHz
Frequency Stability	The stability of the internal frequency standard shall be at least ±5 parts in 10^8 per day for any 10°C increment within the temperature range 0°C to 50°C.
Frequency Translation	10 Hz maximum.
Modes of Operation	USB/A3J Upper Side Band; LSB/A3J Lower Side Band; ISB/A3B Independent Side Band (optional); CW/A1 Continuous Wave; AM/A3 Amplitude Modulation; FM F3 Frequency Modulation.
Input Impedance	50 Ohms nominal, 2.1 VSWR; type N connector, and unbalanced input
AGC Range	The change in IF or AF output level for a change in input level of –100 dBm to –10 dBm is less than 6 dB.
AGC Time Constants	The attack time of the AGC system is less than 15 msecs. The decay time for the three selectable time constants are: SHORT less than 30 milliseconds MEDIUM 200 ±100 milliseconds LONG 3.75 ±1.25 seconds
Image/Spurious Rejection	80 dB, 25 kHz or more removed from tuned frequency.
Internal Spurious Responses	Not greater than –123 dBm except for one spurious in each MHz which may be as high as –116 dBm.
Sensitivity 500 kHz - 29.999 MHz	Single Sideband: –113 dBm (.5uv) for 10 db (S+N)/N ratio in a 3.24 kHz bandwidth. AM: –99 dBm (2.5 uv) for 10db (S+N)/N ratio in a 6 kHz bandwidth.

TABLE 1-3. CAPABILITIES AND LIMITATIONS (Cont.)

Receiver Function	Capability or Limitation
Reciprocal Mixing	The apparent noise at the input of the Receiver with a 3.24 kHz IF bandwidth will be less than −113 dBm when the Receiver is subjected to the following interfering signal conditions. (a) ±15 kHz offset from the Receiver tuned frequency at a level of −23 dBm. (b) ±500 kHz offset from the Receiver tuned frequency at a level of ±2 dBm.
Noise Figure	16 dB from 0.5 MHz to 1.499999 MHz; 13 dB from 1.5 MHz to 29.99999 MHz.
Intermodulation (In Band)	Better than −50 dB for two −36 dBm input signals when measured at the IF or line AF output.
Intermodulation	Third order input intercept point greater than +20 dBm. Second order input intercept point greater than +60 dBm.
Cross Modulation	The cross modulation appearing on a −45 dBm unmodulated tuned signal due to a 30% AM signal which is no closer to the tuned signal than ±100 kHz will be less than 10% if the level of the interfering signal is +15 dBm.
Test Tone to Total Distortion (TTDR) Ratio	The receiver TTDR is greater than 33 dB for an AM signal modulated at 1 kHz to a depth of 75%, or any level between −83 dBm and −10 dBm, when a 6.8 kHz IF bandwidth (optional Special Filter No. 4) is used.
Outputs	(a) Phone output to front panel. 10 mW nominal into 600 Ohm load. 3% distortion. AM signal modulated 30% at 1 kHz. (b) Line output at rear panel. 1 mW nominal at 600 Ohms. 2% distortion at 1 mW. Adjustable from front panel. AM signal modulated 30% at 1 kHz. (c) Loudspeaker output at rear panel. 1 Watt nominal at 8 Ohms. 3% distortion. AM signal modulated 30% at 1 kHz. (d) 455 kHz IF output at rear panel. BNC connector. −10 dBm nominal at 50 ohms.
Rear Panel Connectors	Antenna Input Connector (N). IF Output Connector (BNC). REF Input/Output Connector (BNC). Power Input Connector. Ground Terminal. Digital I/O Connector. AF/AGC outputs (D Connector).
Remote Control (Option)	Full remote control of the following receiver parameters using serial asynchronous, (ASCII-7 bit) character oriented data at one of 16 selectable baud rates from 50 baud to 19.2 kilobaud. Tuned Frequency, BFO Tuning – BFO ON/OFF, IF Bandwidth, Detection Mode, AGC Time Constants – AGC ON/OFF, RF/IF Gain, FAULT Status, BITE Control, system status.
Status Indication	Front panel indication of status under remote control, remote indication of status under local or remote control.
RFI/EMI	Meets specification MIL-STD-461.

TABLE 1-4. EQUIPMENT SUPPLIED

Quantity Per Unit	Nomenclature	Description
1	R-2174(P)/URR	Receiver
1	W18	Cable W18, Primary Power Input
1	P3	Mating Connector for J3

TABLE 1-5. OPTIONAL ITEMS

Nomenclature		Description	
ISB Circuit Board A5		Printed circuit board for lower sideband signal path. (Optional).	
Interface Circuit Board A6A1		Printed circuit board for remote control of the Receiver. Supplied with mating connector (Optional).	
		Filters*	
0.4 kHz B.P.	Filter #1	454800 to 455200 Hz Band Pass Filter	General Purpose/1
1.2 kHz B.P.	2	454400 to 455600 Hz Band Pass Filter	General Purpose/1
6.8 kHz B.P.	3	451600 to 458400 Hz Band Pass Filter	General Purpose/1
3.24 kHz B.P.	4	455350 to 458050 Hz Band Pass Filter	General Purpose-Offset Sideband/1
3.24 kHz B.P.	5	451950 to 454650 Hz Band Pass Filter	General Purpose-Offset Sideband/1
0.4 kHz B.P.	6	454800 to 455200 Hz Band Pass Filter	Defined Delay/2
1.2 kHz B.P.	7	454400 to 455600 Hz Band Pass Filter	Defined Delay/2
3.24 kHz B.P.	8	453380 to 456620 Hz Band Pass Filter	Defined Delay/2
6.8 kHz B.P.	9	451600 to 458400 Hz Band Pass Filter	Defined Delay/2
16.0 kHz B.P.	10	447000 to 463000 Hz Band Pass Filter	Defined Delay/2
0.5 kHz B.P.	11	454750 to 455250 Hz Band Pass Filter	Linear Phase/3
1.0 kHz B.P.	12	454500 to 455500 Hz Band Pass Filter	Linear Phase/3
2.0 kHz B.P.	13	454000 to 456000 Hz Band Pass Filter	Linear Phase/3
3.0 kHz B.P.	14	453500 to 456500 Hz Band Pass Filter	Linear Phase/3
6.0 kHz B.P.	15	452000 to 458000 Hz Band Pass Filter	Linear Phase/3
Overload Protector 09621		Used to protect the radios front end in High RF environments.	

*All filters are optionally procured, so that some filters listed may not be available as stock items.

NOTE: Some filters may be assigned as fixed items to the Receiver, otherwise seven filter slots are available for plug-in filters to the A4 Module.

/1 General Purpose Filters

General purpose filters (filters #1 thru #5) provide coverage of reception modes A1, A2, A3, A3H, A3J and A3B (with ISM module A5, installed).

This group of filters provides the specified optional standard intermediate frequencies (IF) as follows:

Filter Number	3dB BW Hz Min	60 dB BW Hz Max
1	400	2480
2	1200	7200
3	6800	22440

The general purpose offset sideband filters conform to the requirements of MIL-STD-188C Figure 18.

Filter Number	Frequency Corners of Template Referred to AF			
	Lower 3 dB	Upper 2 dB	Lower 60 db	Upper 60 db
4 (LSB)	-350	-3050	+300	-4000
5 (USB)	+350	+3050	-300	+4000

For both filters, envelope delay distortion is maintained within 800 usecs between the frequencies 750 to 2750 Hz.

NOTE

It is essential to install filter #4 in slot FL1.

/2 Defined Delay Filters

This group of filters form part of the specified optional special IF bandwidths. Some similarity exists between the bandwidths and those in the general purpose group, but shape factors are much lower, and the envelope delay is now specified. All are symmetrical about the intermediate frequency.

Defined delay filters are described below:

Filter Number	1 dB BW Hz Min	3 dB BW Hz Min	60 dB Bw Hz Max	Envelope Delay usecs over Hz BW	
6	–	400	1000	2000	300
7	–	1200	2400	900	1200
8	3100	3240	4300	1000	2800
9	6400	6800	13600	1000	6400
10	12000	16000	32000	60	12000

General purpose coverage of reception modes A1, A2, A3, A3H, A3J is provided with added capability of F4, F1 and F4 emissions.

Filter #8 can be used for the reception SSB signals. If it is plugged into the FL1 slot, the receiver BITE routine will recognize it as a "symmetrical sideband" filter, and when LSB or USB are selected, the adjustment to the first and last local oscillators will be made automatically.

/3 Linear Phase Filters

Filters 11 thru 15 complete the range of specified optional special IF bandwidths. All have minimum delay variation over their specified bandwidths.

Filter Number	3 dB BW Hz Min	60 dB BW Hz Max	Envelope Delay usecs over Hz BW	
11	500	3000	80	500
12	1000	6000	40	1000
13	2000	12000	20	2000
14	3000	18000	20	3000
15	6000	36000	20	6000

These filters become essential where preservation of pulse slopes are important. The bandwidth is dependent upon the pulse rate and rise time.

TABLE 1-6. TEST EQUIPMENT LIST (INTERMEDIATE LEVEL MAINTENANCE ONLY)

TYPE DESIGNATION	MFR CODE OR NAME/ADDRESS	FIGURE AND INDEX NO.	NOMENCLATURE	USE	
4960PT3T	28480		Spectrum Analyzer,	Para. 6-9	Intermediate
010-6105-03	80009		X10 Oscilloscope Probe	Para. 6-9 Table 6-3	Intermediate
1121A	28480		HI-Impedance Probe, Spectrum Analyzer	Para. 6-9 Table 6-3	Intermediate
465M	80009	6-18	Oscilloscope, Dual Trace, Portable AN/USM-425(V)1	Para. 6-9	Intermediate
8040A-01	89536		Digital Voltmeter	Para. 6-9	
8640B-003	28480	6-18	SG-1093/U AM/FM Signal Generator	Para. 2-11.c. Para. 6-9	Intermediate Intermediate

TABLE 1-7. RELATED TECHNICAL MANUALS

Publication Number	Publication Title	Equipment Nomenclature
31R2-2URR-256WC-1	Scheduled Periodic Inspection Work Cards	Receiver, Radio, R-2174(P)/URR

TABLE 1-8. MNEMONICS AND ACRONYMS

Mnemonic or Acronym	Description
ACC	Accumulator
ACK	Acknowledge
A/D	Analog to Digital
ALU	Arithmetic Logic Unit
ASCII	American Standard Code for Information Interchange
ASR	Automatic Send and Receive
BCD	Binary Coded Decimal
BITE	Built In Test Equipment
BFO	Beat Frequency Oscillator
BPS	Bits Per Second
BSC	Binary Synchronous Communication
CAM	Contents Addressable Memory
CLK	Clock
CMOS	Complementary Metal Oxide Semiconductor
CPS	Characters Per Second
CPU	Central Processor Unit
CRC	Cyclic Redundancy Check
CROM	Control Read Only Memory
CRT	Cathode Ray Tube
CRTC	Cathode Ray Tube Controller
CTS	Clear to Send
D/A	Digital to Analog
DMA	Direct Memory Access
DTL	Diode-Transistor Logic
DØ - D7	Data Lines Zero thru 7
EBCDIC	Extended Binary Coded Decimal Information Code
ECL	Emitter Coupled Logic
EOR	Exclusive OR
EPROM	Erasable Programmable Read Only Memory
FE	Framing Error
FET	Field Effect Transistor
FF	Flip-Flop
FIFO	First In First Out
GPIB	General Purpose Interface Bus

TABLE 1-8. MNEMONICS AND ACRONYMS (cont'd.)

Mnemonic or Acronym	Description
IC	Integrated Circuit
INT	Interrupt
I/O	Input - Output
IOCS	Input Output Control System
IRQ	Interrupt Request
ISB	Independent Sideband
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LIFO	Last In First Out
LOC	Loop On-Line Control
LSB	Lower Sideband
LSD	Least Significant Digit
MOS	Metal Oxide Semiconductor
MPU	Microprocessor Unit
MSD	Most Significant Digit
MUX	Multiplexer
OE	Overload Error
OOL	Out of Lock
OV	Overflow
PC	Printed Circuit
PIC	Priority Interrupt Control
PLL	Phase Locked Loop
PROM	Programmable Read Only Request
ROM	Read Only Memory
ROMC	Read/Write and Clock
RPROM	Reprogrammable Programmable Read Only Memory
RPT	Repeat
RST	Restart
RTC	Real Time Clock
RTS	Request to Send
R/W	Read/Write
SMI	Static Memory Interface
S/N	Signal to Noise
SR	Service Request
STB	Strobe
TDSR	Transmit Data Service Request
TTL	Transistor - Transistor Logic
UART	Universal Asynchronous Receiver Transmitter
USB	Upper Sideband
USRT	Universal Synchronous Receiver Transmitter
XOR	Exclusive OR

CHAPTER 2
INSTALLATION

2-1. INTRODUCTION. This chapter provides information for receiving, handling and installation of the R-2174(P)/URR Radio Receiver. Section I describes the logistics involved in unpacking, receiving, mounting requirements, ventilating requirements and cable connections. Section II of Chapter 2 describes manpower requirements, the step by step instructions for installing the options in the Receiver and the initial checkout procedure to ensure proper installation.

Section I. INSTALLATION LOGISTICS

2-2. UNLOADING AND UNPACKING. The carton containing the Receiver is 3.6 cubic feet and weighs approximately 34 pounds. No special unloading equipment or procedures are required, except to handle the carton with the normal care given to any shipping carton containing electronic equipment. Any options that may be used with the receiver are normally supplied in a separate package. The packaging details for the options are dependent on the individual site requirements. To unpack the Receiver, refer to Figure 2-1 and perform the following procedures:

a. Open the top of the shipping carton and fold back the flaps.

b. Lift out the top foam cushion.

c. Carefully lift out the wrapped box containing the Receiver. Because of the weight of the receiver (approximately 30 pounds) it is recommended that two people lift out the Receiver.

d. Remove the barrier wrapping from the interior container.

e. Open the interior container and carefully lift out the Receiver.

f. Place the Receiver on a convenient work bench and visually inspect the Receiver for any damage.

g. Replace all packaging material back in the shipping carton. Save all material in the event that the Receiver must be reshipped.

2-3. HOUSING. The unit may be housed (stored) from inclement weather in any structure that will sustain a temperature between -40° and $+70^{\circ}C$ and a relative humidity of 10 to 95 percent. The unit has an indefinite shelf life stored under the above conditions except for the nickel cadmium battery contained on circuit card assembly A6A2. Shelf life is reduced to 3 years if the battery is left fitted to the circuit board.

2-4. RECEIVING DATA. Table 2-1 shows dimensions and weights of the cartoned Receiver as well as the Receiver. Figure 2-1 illustrates the shipping carton for the Receiver.

TABLE 2-1. DIMENSIONS AND WEIGHTS

Item	Dimensions	Weight
Cartoned Receiver	10.5 inches high; 23.5 inches wide; 25.5 inches deep. Cubage: 3.64 cubic feet.	Approximately 34 Pounds.
Receiver	Rack size: 5.1 inches high; 16.6 inches wide; 18.4 inches deep. Front Panel: 5.25 inches high; 19.0 inches wide. Overall depth with handles; 20.0 inches. Cubage: 0.9 cubic feet.	30 Pounds.

TABLE 2-2. ITEM LIST REQUIRED FOR INSTALLATION

Item	Description/Purpose
1.	Receiver, Radio R-2174(P)/URR.
2.	Power Cable, W18. Connects Receiver to primary power source.
3.	IF Bandwidth Filter. The Receiver may be operated with from one to seven different bandwidth filters with a restriction of 5 maximum symmetrical filters. A total of 15 different filters are available.
4.	Mating Connector. Mates with Receiver rear panel AF OUT connector J3.
5. (Optional)	ISB Circuit Card Assembly, A5. Permits the Receiver to operate in the ISB mode (receiving both upper and lower sidebands simultaneously).
6. (Optional)	Remote Control Circuit Card Assembly, A6A1. Permits the receiver to be operated from a remote control device. A mating connector is supplied with this option.

2-5. **INSTALLATION REQUIREMENTS.** The Receiver is designed to be mounted in a standard 19 inch rack. The sides of the Receiver have been drilled and tapped to accept Jonathan type 110QD-16-2 slides. The use of slides, however, is optional and is dependent on the individual site requirements. If slides are installed, it is recommended that cable retractors be used to simplify extending the Receiver out of the rack. If the unit is rack mounted without the slides, access to the rear panel must be provided for connection of cables and test equipment. Refer to Table 2-1 for space dimensions required for mounting the equipment and to Table 2-2 for a list of the items required for installing the Receiver.

WARNING

Prior to installation of slide rails, visual inspection of receiver shall be performed to prevent injury to personnel and damage to equipment.

a. Remove top cover (see page 7-12, Fig. 7-1, Index 1-1). Observe routing of AC Line Switching Cable, W20 (see page 7-15, Fig. 7-1, Index 1-64). If cable W20 is located opposite (predrilled and tapped holes) cable should be bent 90 degrees at AC Connector J2. This should remove cable from opposite (predrilled and tapped holes). Use only 10-32 x 3/8 inch screws to mount slides. MIL-STD-454G states that turns of screws exposed should not be more than 1 1/2 times the diameter of the thread (past drilled and tapped holes).

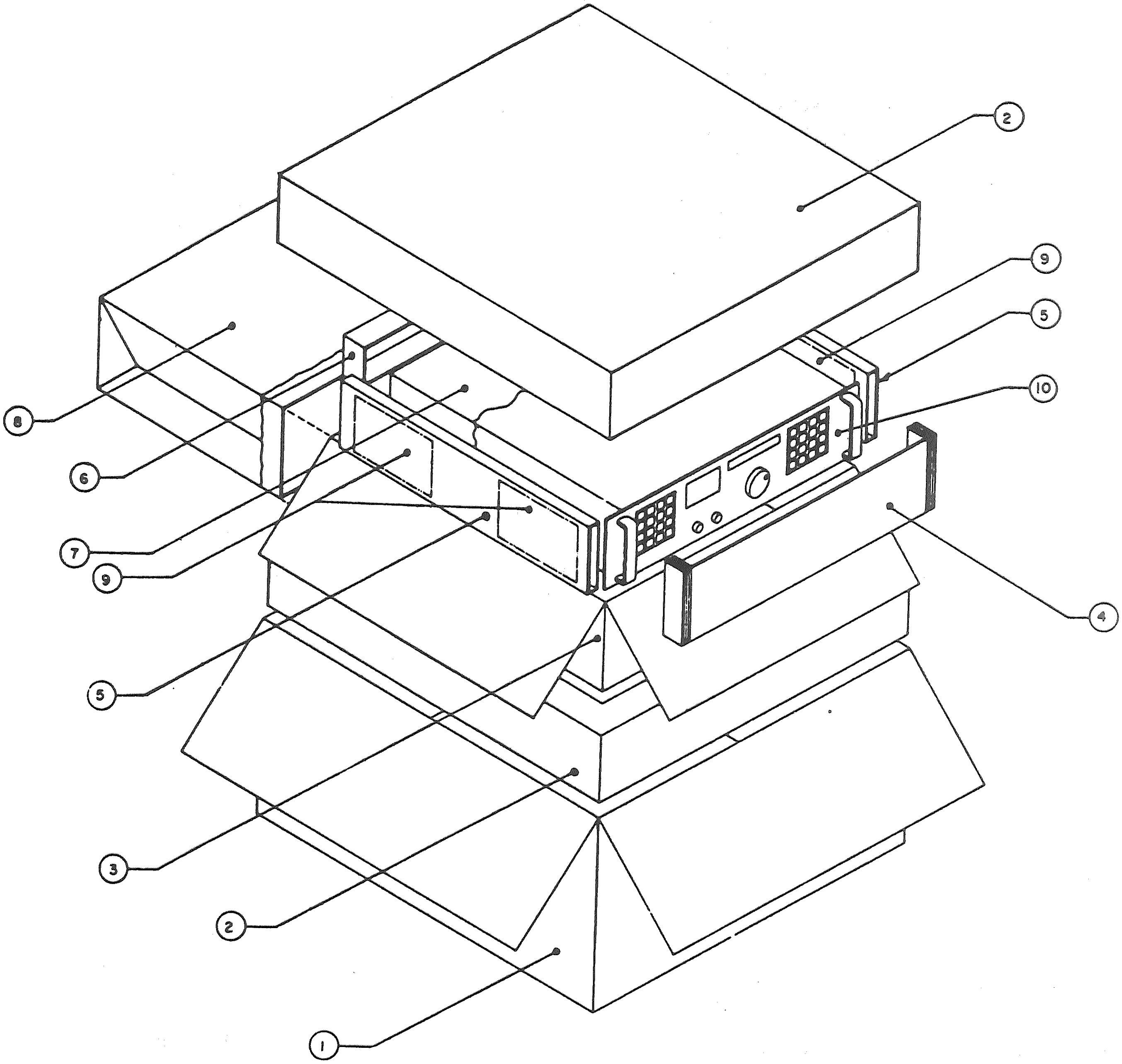


Figure 2-1. Packaging Details, Receiver

1. Exterior Container – 25-1/2" long by 23-1/2" wide by 10-1/2" deep.
2. Top and Bottom Cushions – 25-5/8" long by 23-5/8" wide by 5-1/4" deep.
3. Interior Container – 21" long by 19-1/4" wide by 5-1/4" deep.
4. Front Panel Cushion – 19" long by 1-1/2" wide by 5-1/4" deep.
5. Side Cushions – 19" long by 4-1/2" wide by 3/4" deep.
6. Rear Panel Cushion – 16-1/4" long by 4-5/8" wide by 1-5/8" deep.
7. Intimate Wrap.
8. Barrier Wrap.
9. Desiccant.
10. R-2174(P)/URR Radio Receiver

CAUTION

The top and bottom covers on the Receiver, as well as the heat sinks on the rear panel, must be unobstructed to permit proper air circulation. The power dissipation of the Receiver is approximately 50 Watts with half of the power dissipated as heat. In most installations, special cooling will not be required.

b. The options associated with the Receiver include plug-in IF bandwidth filters, independent sideband operation, and operating the Receiver through a remote control device. One or more of the plug-in filters must be installed before the receiver can operate. The ISB and remote control capabilities, however, are optional. Because of the different possible filter combinations and the options, it is recommended that a Receiver configuration chart or log book be maintained for each Receiver. The configuration chart or log book would list the IF bandwidth filters currently in the Receiver and the operating options installed.

c. All system interface connections to the Receiver are made through the rear panel connectors listed in Table 2-3.

TABLE 2-3. REAR PANEL CONNECTORS

Reference Designation	Nomenclature	Function
J1	RF IN	N-type connector providing Receiver input from antenna.
J2	IF OUT	BNC-type connector providing Receiver second IF output signal of 455 kHz.
J3	AF OUT	25 pin "D" type connector providing audio AGC and status output signals. Refer to Table 2-5 for detailed listing of these connections.
J7	REF IN/OUT	BNC-type connector used in conjunction with switch S2 to accept an external reference source (S2 in EXT position) or to provide an output of the internally generated reference signal (S2 in INT position).
A6A1W1J1	–	Round, 26 pin MIL-Type (MC3723-02R-1626N) connector for external Receiver control (optional).
A10J1	J1	Connection for ac line cord is standard 3 prong male.

Section II. INSTALLATION PROCEDURES

2-6. **MANPOWER REQUIREMENTS.** To install the options in the Receiver, install the Receiver in the system, and perform the tests required to ensure operational performance requires one man for one hour.

2-7. **INSTALLATION.** The installation procedures for the Receiver are divided into three main steps. The first step is to install the plug-in filters and any options that may be associated with the Receiver. The second step is to perform an initial check-out of the Receiver, and the third step is to make the required system connections to the Receiver. Paragraphs 2-8, 2-9 and 2-10 contain detailed instructions for performing these steps.

2-8. **INSTALLATION OF RECEIVER OPTIONS.** The three primary operating options associated with the Receiver include:

- Operation with different bandwidth options through the use of plug-in bandwidth filters.
- Operation of the Receiver with a remote device.
- Operation of the Receiver in the ISB mode.

The following paragraphs detail the steps necessary to install these options.

a. IF Bandwidth Filter Installation. The Receiver may be supplied with from 1 to 7 plug-in filters. Table 1-5 lists the filters available with the initial procurement. Additional filters may be available through later procurements, refer to Table 1-5. The filters are mounted on the A4 board, accessible from the top of the Receiver. To gain access to the A4 board, loosen the six quarter-turn fasteners holding the top cover to the Receiver and remove the top cover. An RF shield is mounted over the filter sockets on the A4 board. Remove the three screws holding this shield to the chassis and remove the shield. Figure 2-2 illustrates the seven filter slots on the A4 board.

(1) If a Receiver configuration chart has been prepared for this particular Receiver (as recommended in Paragraph 2-5a.) refer to the chart and determine if the Receiver is to be operated with the ISB option. If a Receiver configuration chart was not prepared, determine if an ISB option is to be included by checking the shipping data or the station manual, as appropriate. If the Receiver is to be operated with the ISB option, both upper and lower sideband filters must be installed in the Receiver.

NOTE

If LSB is specified for installation, it must be installed in filter slot FL1.

If the Receiver is not to be operated with the ISB option, either a lower sideband filter or symmetrical sideband filter may be installed in the FL1 position. If a lower sideband filter is installed, the companion upper sideband filter must also be installed in one of the remaining filter positions. If a symmetrical filter is to be used to provide sideband operation, the Receiver will use the filter installed in the FL1 position. This is for both sidebands by putting a 1.8 kHz in the appropriate frequency offset in the first and last local oscillators. (This assumes a 3.2 kHz symmetrical filter will be used for this application.)

(2) The remaining filters may be installed in any sequence in filter positions FL2 through FL7. (NOTE: only 5 symmetrical filters allowed.) However, in order to simplify system operation and troubleshooting, it is recommended that a format be established and used for all Receivers at a particular site. A typical format would be to insert the USB filter (if used) in position FL2 and insert filters with increasing bandwidths in filter positions 3 through 7.

(3) Once the filter complement and arrangement has been determined, the following procedure should be used to insert the filters into the Receiver. Refer to Figures 2-2 and 2-3.

(a) Working from the front of the Receiver, position the filter to be used for LSB operation over filter position FL1 (the filter position closest to the rear of the Receiver). Make certain that the large pins are aligned with the large sockets and the smaller pins are aligned with the smaller sockets.

(b) Carefully push down on the filter to insert the pins into the sockets. Relatively light pressure is required to insert the pins into the sockets. If the filter does not easily slide into place, recheck the pin/socket alignments.

(c) Insert the appropriate filters into filter positions FL2 through FL7 (as required), using the procedures described in steps 1 and 2.

(d) After all filters have been inserted, visually inspect the filters to insure that they are properly seated. The bottom of the filters should be flat against the surface of the A4 board.

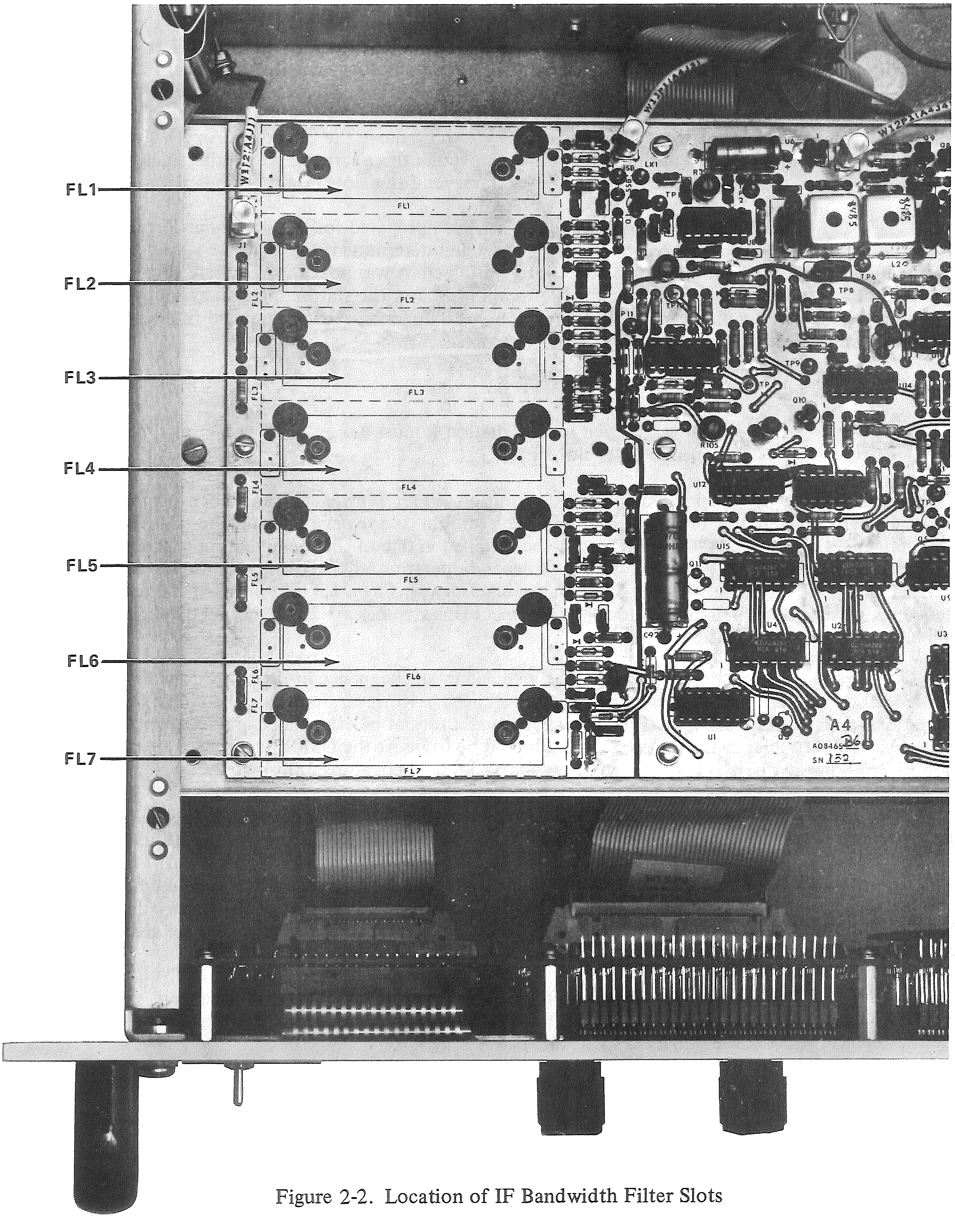


Figure 2-2. Location of IF Bandwidth Filter Slots

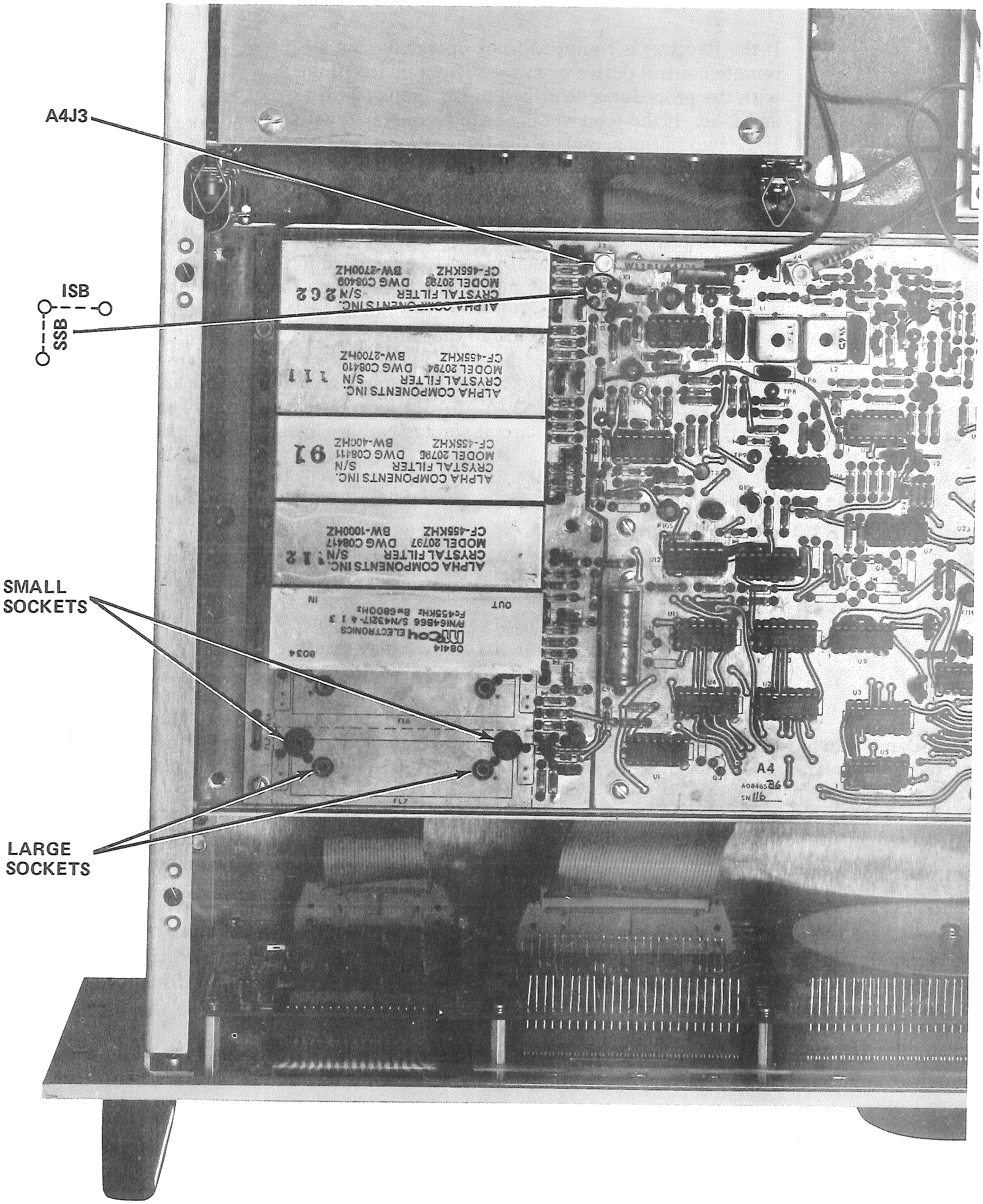


Figure 2-3. Location of Filters and Jumpers, A4 circuit card assembly.

(e) Replace the RF shield over the filters and secure the shield in place by tightening the three screws.

NOTE

If the Receiver is equipped to be operated from a remote control device or in the ISB mode, continue with the procedures described in Paragraphs 2-8b and 2-8c. If the Receiver is not to be operated with these two options, replace the top cover on the Receiver chassis and refer to the initial checkout procedure described in Paragraph 2-9.

b. Remote Control Interface Installation. If the receiver is to be operated with the remote control option the A6A1 circuit card assembly must be installed in the Receiver. In order to install this card the A6A2 circuit card assembly must be removed from the Receiver and mated with the A6A1 card. The two cards are then inserted back into the Receiver as an assembly. The following procedure details the steps necessary to install the cards.

(1) Working from the front of the Receiver, disconnect the A9W1 cable assembly from the A6A2 card. This cable assembly connects to A6A2J1 located on the front of the A6A2 card. Figure 2-4 illustrates the A6A2 and A6A1 circuit card assemblies installed in the Receiver and the location of A9W1.

(2) Remove the three screws located along the top edge of the A6A2 card and carefully remove the card from the Receiver.

CAUTION

Do not place the A6A2 circuit card assembly on any conductive material. Failure to comply may result in shorting the battery contained on this card.

(3) Check the rear panel of the Receiver. A blank plate may be covering up the hole (located on left hand side of the rear panel) for the remote control interface socket. If the blank plate is present, remove the two screws and lock washers holding the plate and remove the plate, saving the screws and lock washers.

(4) A hard-wired link, designated LK1, must be removed from the A6A2 card when the remote control option is used. The link is physically located between U1 and U2 (the two 40 pin LSI chips located near the J2 connector). Use a pair of cutters (or a low wattage soldering iron) to remove the link. Refer to Figure 2-5 for location of the link.

(5) There are six different mechanical links located on the A6A1 circuit card assembly that must be installed according to the external data procotol to be used. Table 2-4 lists the mechanical links required for each interface. Use a low wattage soldering iron to install or remove the links as required for data protocols. Refer to Figure 2-6 for location of the links.

(6) Align the 50 pin male connector on the A6A1 circuit card assembly with the 50 pin female connector on the A6A2 circuit card assembly as shown in Figure 2-7. Mate the two connectors.

(7) Carefully place the two cards into the receiver chassis. Make certain the remote control interface connector (A6A1J1) clears the hole in the rear panel.

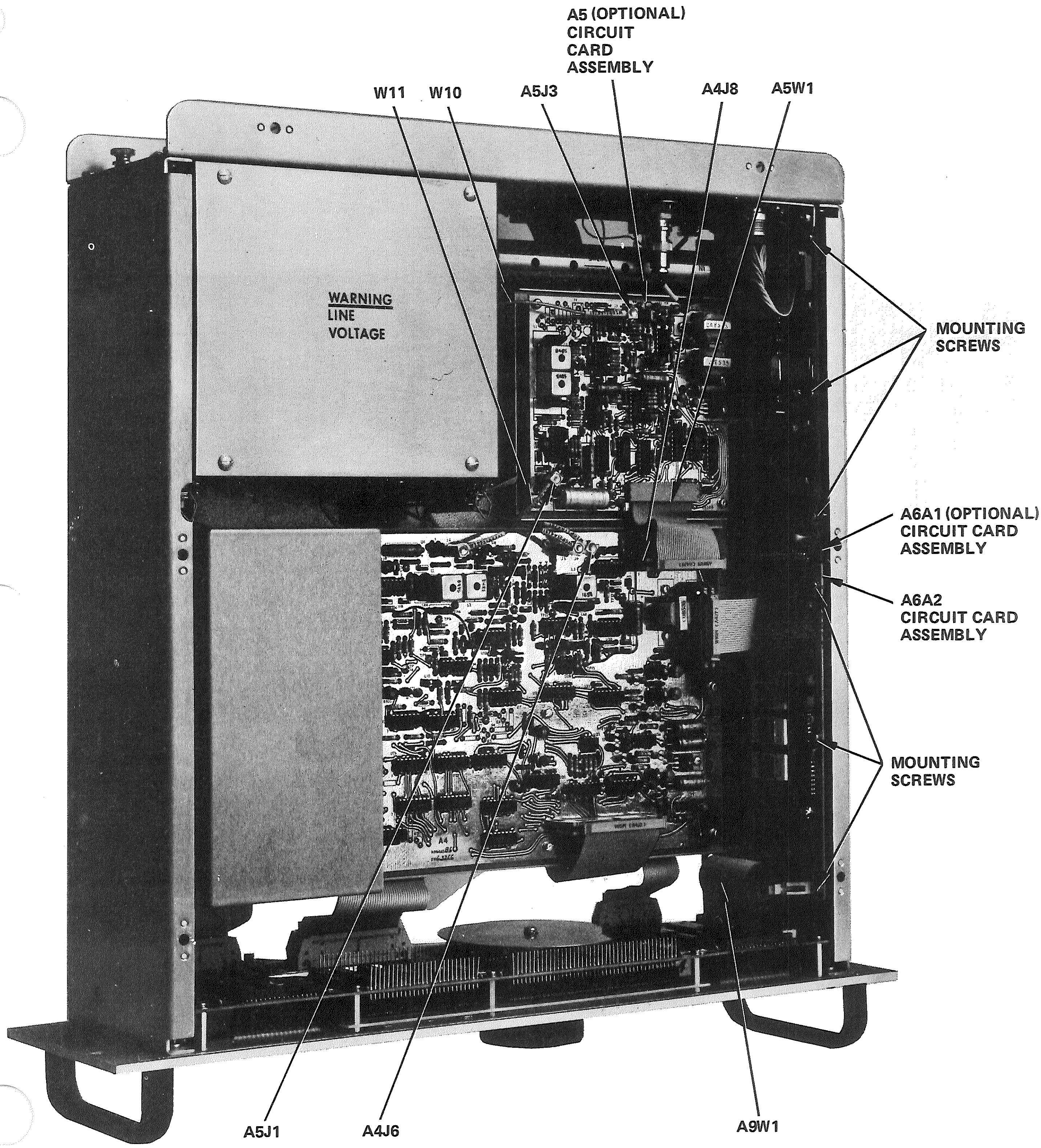


Figure 2-4. Receiver Options Installation Detail

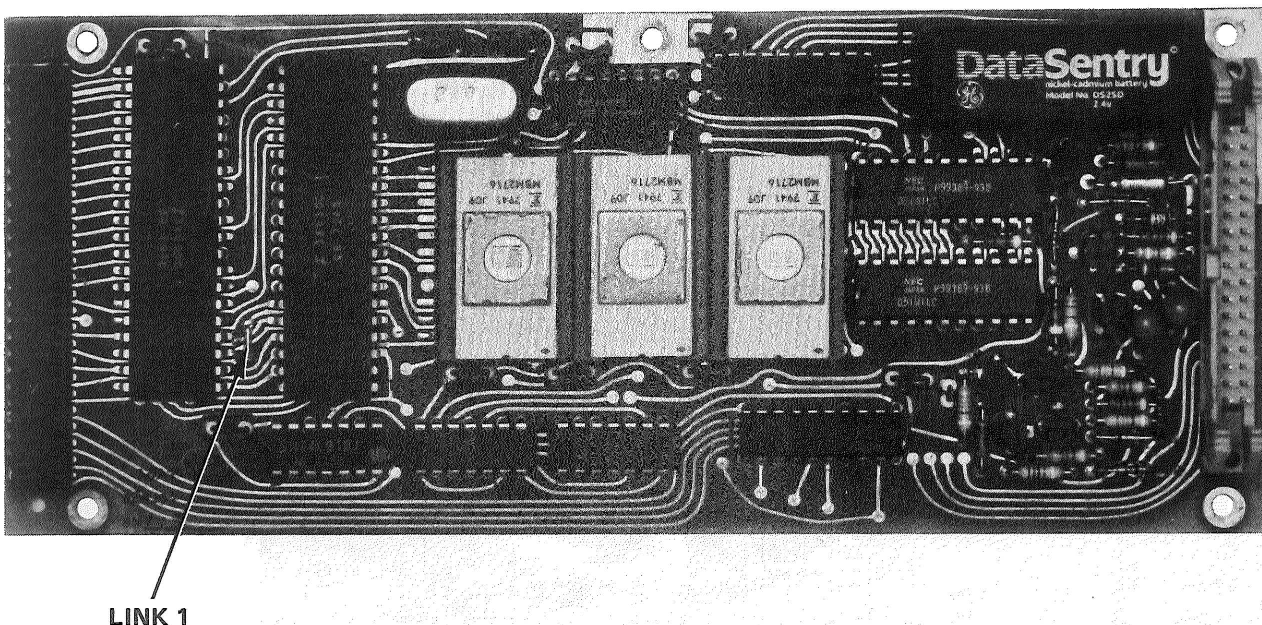


Figure 2-5. A6A2 Circuit Card Assembly, Location of Jumper

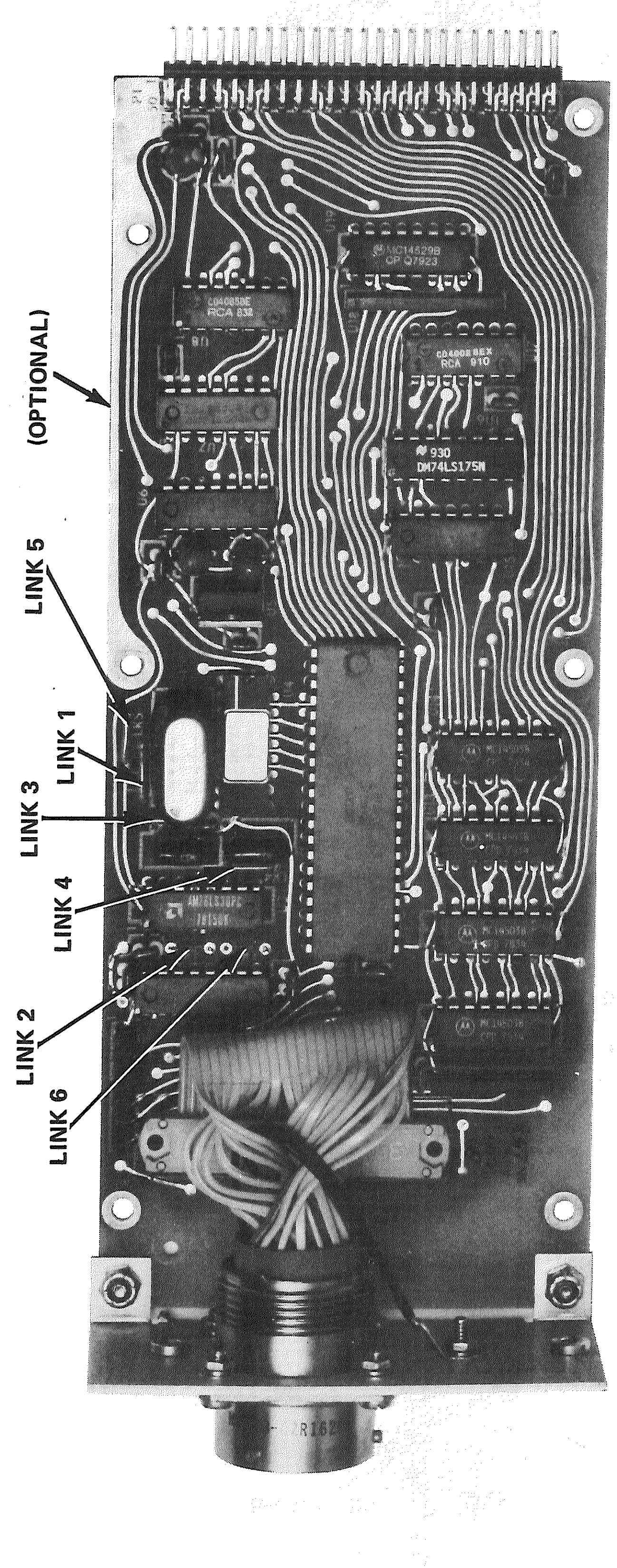


Figure 2-6. Optional A6A1 Circuit Card Assembly, Location of Jumpers

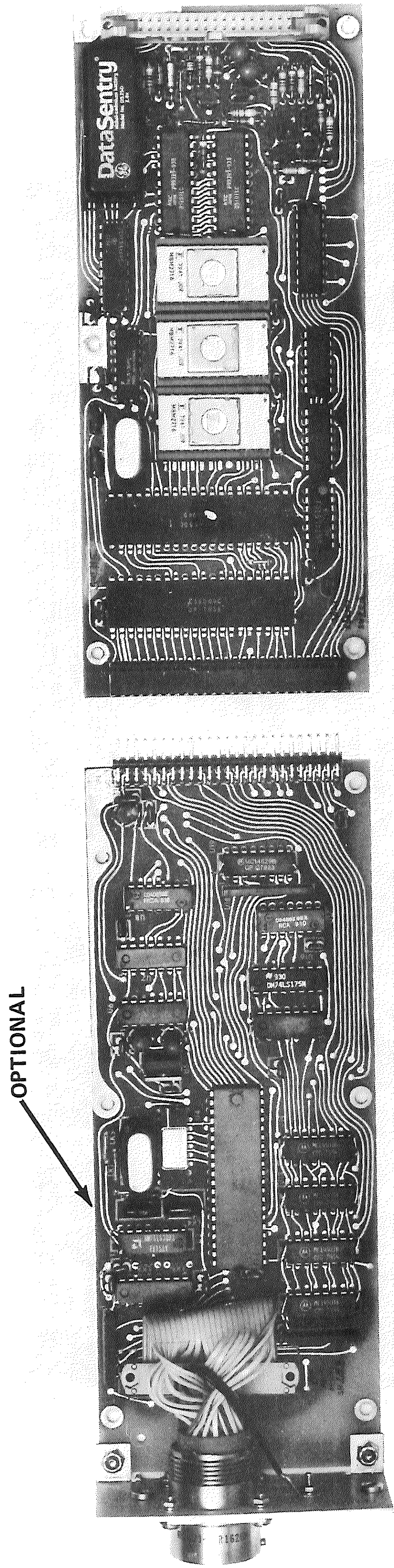


Figure 2-7. Mating A6A1 and A6A2 Circuit Card Assemblies

CAUTION

If a nylon washer is supplied as part of the hardware kit for A6A1 this must be used on center-top of A6A1 circuit card with attached screw to prevent the mounting post from shorting the circuit card.

(8) Position the two cards in the card guide attached to the receiver chassis. Be sure the cards are fitted firmly in the bottom of the card guides. Secure the cards to the side of the chassis with 6 screws (3 screws on each card) and nylon washer on center post of A6A1 if required. Secure the interface connector to the rear panel with two screws and lock washers saved from blanking plate. Figure 2-4 illustrates the two cards installed in the Receiver.

(9) Reconnect the A9W1 cable assembly (removed in step 1) to connector A6A2J1.

c. Independent Sideband Option Installation. If the Receiver is to be operated in the ISB mode the A5 circuit card assembly must be installed in the Receiver. The A5 card is physically located towards the rear of the Receiver, between the A1 assembly and the A4 circuit card assembly; as shown in Figure 2-4. The following procedure details the steps necessary to install the A5 circuit card assembly. Refer to Figures 2-3 and 2-4 for the location of cables and connectors.

(1) Place the metal baseplate shield (curved edge upwards) on the four standoffs and secure with four screws into the standoffs using screws and washers supplied. (NOTE: Flat washer against plate.)

(2) Position the A5 circuit card assembly so that the ribbon cable is opposite the J8 connector on the A4 circuit card assembly. Secure the A5 circuit card assembly to the metal baseplate with 4 screws and washers with flat washers next to circuit card.

(3) Plug in the ribbon cable (A5W1) from the A5 card into J8 on the A4 board. Connect coaxial cable W10 between A4J6 and A5J3. Connect coaxial cable W11 between A4J3 and A5J1.

(4) The mechanical jumper on the A4 circuit card assembly must be properly positioned for ISB/SSB operation. The jumper, designated LK1, is physically located to the right of filter position FL1 when looking from the front of the Receiver. Refer to Figure 2-3. With the A5 circuit card assembly installed, the jumper must be connected across the two terminals designated ISB.

TABLE 2-4. JUMPER OPTIONS, REMOTE CONTROL INTERFACE

Link Designation	188C/232C/423 Interface	RS422 Interface
LK1	Install	Install
LK2	Remove	Remove
LK3	Install	Remove
LK4	Install	Remove
LK5	Install	Remove
LK6	Remove	Install

2-9. INITIAL CHECKOUT PROCEDURE. The following procedure is designed to insure that the receiver is in an operational condition. Before attempting this procedure, make certain that all steps described in Paragraph 2-8 have been completed as required.

a. Place the Receiver on a convenient work table.

b. Verify that the front panel POWER switch is set to the OFF position.

c. Connect a ground strap between the GROUND lug on the rear panel and a good electrical ground.

d. Determine the power source, in terms of voltage and frequency, that will supply the primary power for the receiver. Ensure that frequency is between 43 and 420 Hz and the voltage is either 100, 120, 220, or 240 Volts. Change fuse to ½ amp for 240-Volt operation.

e. On the rear of the Receiver, slide the transparent plastic cover to the left, remove the printed circuit card switch and reinsert it so that the primary power voltage (±10%), to be connected to the Receiver, is visible after reinsertion of the circuit card switch. Slide the plastic cover to the right.

f. Connect the primary power cable W18 plug P2 to connector A10J1 on the rear panel of the Receiver.

g. Connect Plug P1 of primary power cable W18 to the primary power source.

h. Place the front panel POWER switch to the ON position.

i. The Receiver will probably indicate a random display since the Receiver has not been initialized. To initialize the Receiver, depress the LOCK pushbutton and while still holding the LOCK in, depress the AM pushbutton; then release in the opposite order they were depressed. This will cause the microprocessor to initiate the BITE sequence, to check and record the filters and other operating parameters of the Receiver. During the initialization sequence (which takes approximately 1 minute) the Receiver display will change to indicate that the sequence is in process. At the completion of the sequence, the Receiver will display the last entered data. If the sequence fails, refer to Chapter 6 for maintenance procedures.

j. To verify that the microprocessor and the front panel control logic are operating properly, depress the TUNE RATE pushbutton and turn the frequency selection knob. Verify that the FREQUENCY display increases and decreases accordingly. Depress the USB, LSB, then CW and BW1 through BW5 pushbuttons in sequence. Verify that the correct filter value is displayed. Depress the ENTER pushbutton and depress pushbuttons 0, 1, 2, 3, 4, 5, 6, and 7. Verify that the digits are displayed in the FREQUENCY display.

k. After verifying frequency display select all AGC modes, all detector modes and in turn verify the operation and display on the mode LCD, also verify the BFO by stepping to CW then selecting BFO CENTER, BFO and tuning the BFO (tuning knob).

l. Set the POWER switch to the off position and disconnect the power cord.

m. This completes the initial checkout procedure for the Receiver. Continue with the procedures detailed in Paragraph 2-10 to install the Receiver in the system.

2-10. SYSTEM CONNECTIONS. System connections for the Receiver are based on the individual site requirements and the options associated with a Receiver. The following paragraphs describe in detail all of the procedures required to install the Receiver. If a particular paragraph does not apply it should be ignored. Additionally, the individual site requirements will determine the most effective method of installing the Receiver. In some installations, it may be easier to pre-wire an entire equipment rack and then install the Receivers. In other cases it may be easier to install the Receiver and then add the wiring. Figure 2-8 illustrates the connectors located on the rear panel of the Receiver.

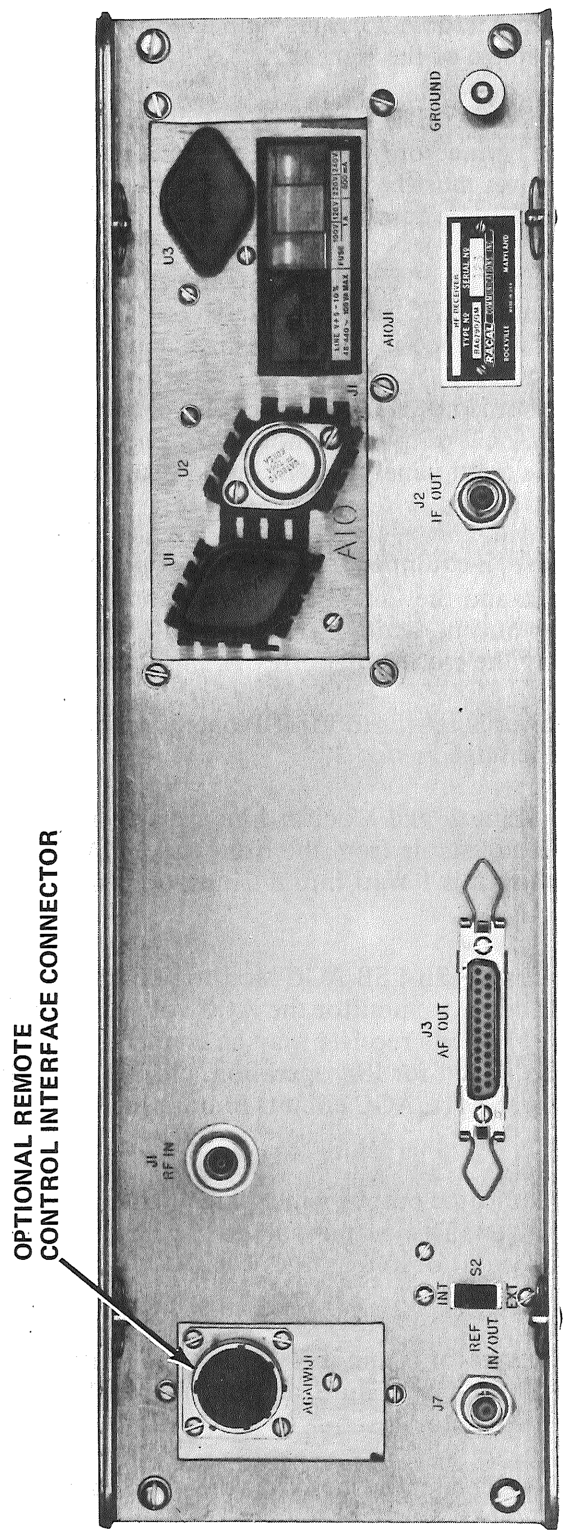


Figure 2-8. Rear Panel Connectors and Controls

a. RF IN, Connector J1. The RF input from the antenna to the Receiver is made through the rear panel connector, J1. This connector is a standard N-type female connector and will mate with any standard N-type male connector. The Receiver is shipped with a plastic dust cover over connector J1, which must be removed before the antenna connection can be made. The input impedance at the connector is 50 ohms, unbalanced, with a VSWR of less than 2:1 over the operating frequency range of the Receiver.

b. IF OUT, Connector J2. The second IF output signal at 455 kHz is brought through this female BNC-type connector; which will mate with any standard male BNC-type connector. The plastic dust cover must be removed before the connection can be made. The output signal level at the connector is approximately –10 dBm into 50 Ohms.

c. AF OUT, Connector J3. The AF OUT connector on the rear panel is a 25 pin D-type connector providing audio, AGC, and fault status outputs. Table 2-5 lists the signal outputs on each pin which are further described in the following paragraphs:

(1) If the Receiver is not equipped for ISB operation (A5 circuit card assembly is not installed) the Line 1 and Line 2 outputs are not used. The Monitor Line output and the Loudspeaker output, along with the front panel PHONES jack, provide the audio output for the Receiver for all operating modes.

(2) If the Receiver is equipped for and is to be operated in the ISB mode, the Line 1 output will contain the USB audio and the Line 2 output will contain the LSB audio. The Monitor Line output, the Loudspeaker output, and the front panel PHONES jack will provide either USB or LSB audio; as controlled by the front panel ISB U/L pushbutton.

(3) If the Receiver is equipped for ISB operation but is not operating in the ISB mode, audio output will be the same as step 2.

(4) The Line 1, Line 2, and Monitor Line provide a 1 mW balanced output at 600 Ohms. The amplitude level is adjustable from the front panel MAIN and I-LSB LINE LEVEL controls. The Loudspeaker output is 1 Watt into 8 Ohms, controlled from front panel AF GAIN control.

(5) The Main IF and ISB-LSB AGC Monitor/Input terminals may be used to control the AGC for diversity combining or to monitor the AGC voltage. For diversity combining, the Main IF AGC signal (on pin 21) of one receiver may be connected to pin 21 of the second Receiver. If the Receiver is equipped for ISB operation, pin 22 of one Receiver may be connected to pin 22 of the second Receiver. The AGC circuits in both receivers will automatically respond to the proper signal.

(6) The Fault Indicator output will be high (logical 1, +2 Volts to +5 Volts) when a fault is not present in the receiver. This output will go low (logical 0, 0 Volts to +0.8 Volts) when one of the synthesizer circuits is out of lock.

(7) A mating connector (Cannon Type DB-25P) with a connector shell is supplied with the receiver. Use the following procedure, and the pin number/signal designation information in Table 2-5 to wire the connector.

(a) Slide the connector shell over the cable to be used.

(b) Solder the cable wires to the connector as required (refer to Table 2-5). The connector pin numbers are indicated on the front of the connector.

(c) Slide the connector back into the connector shell. Place one of the spring clips on top of the connector with the curved edge pointing upwards. Secure the spring clip and the connector to the connector shell with the self-tapping screw. Repeat this procedure for the other side of the connector.

(d) Connect the wired cable to the rear panel connector J3* and secure with the two connector spring latches.

TABLE 2-5. AF OUT J3 PIN CONNECTIONS

Pin Number	Signal Designation	
1 2 14	Output Center Tap Output	Line 1 Output (Used only with ISB Option). Provides USB output during ISB operation; AM/FM/CW/USB output during non-ISB operation.
3 16 15	Output Center Tap Output	Line 2 Output (Used only with ISB Option). Provides LSB output during ISB operation.or SSB operation.
4 5 17	Output Center Tap Output	Monitor Line Output. Provides AM/FM/CW/SSB output during non-ISB operation; provides switch controlled selection of USB or LSB during ISB operation.
18 6	Output Signal Ground	Loudspeaker Output. Same as Monitor Line Output.
7, 8, 9	Ground (Cable Shield)	
10, 11, 12, 13 19, 20, 24, 25	Not connected	
21	Main IF Diversity AGC Monitor/Input	
22	ISB Lower Sideband Diversity AGC Monitor/Input (used only with ISB option)	
23	Fault Indicator (Low Indicates Fault)	

d. REF IN/OUT, Connector J7. This rear panel connector is used in conjunction with rear panel switch S2. With the switch set to the EXT position the Receiver will accept an external 1, 5, or 10 MHz reference input through connector J7. With switch S2 set to the INT position, the Receiver will supply a 1, 5, or 10 MHz reference output through connector J7*. Connector J7 mates with any standard male BNC-type connector. The input circuit has an input impedance of 50 Ohms and will operate with peak-to-peak signal levels of 1.0 Volts, ±0.5 Volts.

e. Remote Control, Connector A6A1W1J1. The Receiver is supplied with a mating connector for the remote control interface connector. Table 2-6 lists the pin numbers and signal designations for this connector. Note that the function on the first nine pins (A through J) vary according to the interface to be used. The remaining pins (K through c) are the same for all interfaces. Table 2-7 lists the pin number/baud rate selection for the receiver, and Table 2-4 lists the A6A1 circuit card assembly jumpers for the different interfaces. (NOTE: These pins must be connected to ground or left unconnected to provide correct address, baud rate and parity for correct operation.)

*Refer to Figure 6-13A and Figure 8-11 for frequency selection link options.

(1) Slide the mating connector shell over the cable to be used for the remote control.

(2) Connect the pins on the wires, and then using the special insertion tool provided, insert the pins into connector housing in accordance with Table 2-6 for the interface to be used. The connector pins are designated on the front of the connector.

(3) After carefully checking all wiring, slide the connector into the connector shell and secure the cable clamp. Attach the connector to A6A1W1J1 and secure.

(4) Visually inspect the A6A1 circuit card assembly to insure that all jumpers are installed in accordance with Table 2-4.

WARNING

The Voltages associated with the power input to the Receiver can be dangerous to personnel. Use caution when connecting or disconnecting the power cable.

f. Power Cable, Connector A10J1. The power cable, W18, attaches to the rear panel connector A10J1. Before attaching this cable, verify that the printed wiring card switch is properly inserted (the operating voltage designation is visible). Access to the card is made by sliding the transparent plastic cover to the left. Additionally, the receiver should be grounded by attaching a suitable ground wire to the rear panel GROUND lug before the ac power cable is attached.

2-11. **INITIAL OPERATING PROCEDURE.** The following procedure provides an overall check on the Receiver operation and the system interface connection. Before attempting this procedure, verify that all appropriate options have been installed in accordance with Paragraph 2-8 and that all appropriate system interface connections have been made in accordance with Paragraph 2-10.

a. Turn the Receiver on by setting the front panel POWER switch to the ON position.

b. A random display may be present on the Receiver. To correct this, the Receiver must be initialized by running the BITE sequence (Built In Test Equipment). This is accomplished by depressing the LOCK pushbutton and, while still holding LOCK in, press the AM pushbutton; then release in the opposite order they were depressed. The Receiver will automatically run through the entire BITE sequence. If no errors are detected, the Receiver will return to the last entered setting upon completion of the BITE sequence. If an error is detected, the BITE sequence will stop and display a number. If this occurs, refer to the fault isolation procedures contained in Chapter 6 (Table 6-2) of this manual for further action. If the BITE sequence successfully completes but the resulting display continues to be erroneous, it may be due to a loss of memory back-up. If this occurs, ensure that the receiver is in LOCAL Mode and exercise all pushbutton front panel functions including MAIN and BFO Tuning. If this does not produce a coherent display, refer to Chapter 6 for further fault isolation. After verifying display select all AGC modes, all detector modes and in turn verify the operation and display on the mode LCD; also verify BFO by selecting CW and BFO CENTER, BFO and then tuning the BFO.

c. Connect the signal generator, listed in Table 1-5, to connector J1 RF IN. Adjust the signal generator for a 3.5000000 MHz output at −97 dBm. Set Receiver frequency to 03.5 MHz, CW mode, BFO offset to plus 1 kHz and short AGC time constant.

d. Press the METER RF/AF pushbutton for AF indication in the upper left portion of the liquid crystal display (LCD). The AF should indicate 0 dB. If indication is not 0 dB, use a screwdriver to adjust the MAIN-LINE LEVEL adjust on the front panel for 0 dB indication on the LCD.

e. If the Receiver is equipped with the ISB option, depress the ISB U/L pushbutton to obtain an I-LSB indication on the display (the pushbutton may have to be depressed twice). NOTE: The Receiver frequency must be adjusted to 1.8 kHz higher than the generator frequency to obtain

TABLE 2-6. REMOTE CONTROL INTERFACE CONNECTOR SIGNAL DESIGNATION

Pin Designation	MIL STD 188C Interface (See Note)	EIA-RS232C/RS423 Interface (See Note)	EIA-RS422 Interface (See Note)
A	System Ground	System Ground	System Ground
B	Not Used	Data Out A - Mark Neg.	Data Out A - Mark Neg.
C	Data Out Ground	Data Out Ground	Not Used
D	Data Out	Not Used	Data Out B - Mark Pos.
E	Jumper to Pin F	Not Used	Not Used
F	Jumper to Pin E	Data in A - Mark Neg.	Data In A - Mark Neg.
G	Data In Ground	Data In Ground	Not Used
H	Data In	Jumper to Pin J	Data In B - Mark Pos.
J	Not Used	Jumper to Pin H	Not Used
K	Receiver Address D1-1*	Receiver Address D1-1*	Receiver Address D1-1*
L	Receiver Address D1-2*	Receiver Address D1-2*	Receiver Address D1-2*
M	Receiver Address D1-4*	Receiver Address D1-4*	Receiver Address D1-4*
N	Receiver Address D1-8*	Receiver Address D1-8*	Receiver Address D1-8*
P	Receiver Address D2-1*	Receiver Address D2-1*	Receiver Address D2-1*
R	Receiver Address D2-2*	Receiver Address D2-2*	Receiver Address D2-2*
S	Receiver Address D2-4*	Receiver Address D2-4*	Receiver Address D2-4*
T	Receiver Address D2-8*	Receiver Address D2-8*	Receiver Address D2-8*
U	/Parity Select*	/Parity Select*	/Parity Select*
V	Even/Odd Parity*	Even/Odd Parity*	Even/Odd Parity*
W	Baud Rate B4 **	Baud Rate B4 **	Baud Rate B4 **
X	Baud Rate B3 **	Baud Rate B3 **	Baud Rate B3 **
Y	Baud Rate B2 **	Baud Rate B2 **	Baud Rate B2 **
Z	Baud Rate B1 **	Baud Rate B1 **	Baud Rate B1 **
a	Ground	Ground	Ground
b	Ground	Ground	Ground
c	System Ground	System Ground	System Ground

NOTE: Circuit Card A6A1 must be linked as shown in Table 2-4 for each interface configuration. D1=LSD, D2=MSD.

*Logic 1 = open circuit; Logic 0 = ground for Address, Parity option and Baud rates.
**Refer to Table 2-7 for Baud rates.

TABLE 2-7. BAUD RATE SELECTION

Pin	Baud Rate															
Desig.	50	75	110	134.5	150	300	600	1200	1800	2000	2400	3600	4800	7200	9600	19200
W	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
X	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
Y	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
Z	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

an audio output. With the meter set to display AF, verify that a 0 dB indication is present. If a 0 dB indication is not present, use a screwdriver to adjust the I-LSB adjustment on the front panel to obtain a reading of 0 dB.

f. Remove the signal generator and connect an antenna to J1 RF IN on the rear panel.

g. Connect a headphone to the front panel PHONES jack. Depress the AM pushbutton and tune the Receiver to a local AM broadcast frequency. The Receiver may be tuned either with the front panel frequency selection control or set directly to the desired frequency through the use of the numeric keypad. When using the tuning knob, depress the TUNE RATE pushbutton to select the desired rate. The display will indicate FAST or SLOW under TUNING. If no display is present the Receiver will be in the fine tuning rate mode. When using the numeric keypad, depress the ENTER pushbutton and then enter the desired frequency with the numeric keys, including leading zeros.

h. Press the LOCK pushbutton and rotate the tuning dial in both directions. Frequency indication should not change and station selected should not change.

i. Select the desired bandwidth by depressing the appropriate bandwidth pushbutton (BW1 through BW5). Adjust the audio level in the headphone with the front panel AF GAIN control.

j. Depress the MAN, SHORT, MED, and LONG pushbuttons in sequence. Verify that the corresponding indication is present in the display. Note that these pushbuttons are push on/push off and that the manual mode may be used in conjunction with the short, medium, or long AGC modes.

k. The manual mode may be used to set the threshold level on any of the AGC modes. To set the threshold, press the MAN pushbutton and set the meter to display RF by depressing the METER RF/AF pushbutton. Adjust the front panel IF GAIN control to obtain the desired threshold level on the meter. With none of the AGC modes indicated the Receiver will operate in the manual mode. With any one of the AGC modes selected the receiver will operate in the AGC mode with the threshold level as set in the manual mode.

l. Press the BW1 through BW5 pushbuttons in sequence and verify that the proper bandwidth is indicated in the display and the audio quality in the PHONES varies with the bandwidth selected.

m. Press the CW and BFO pushbuttons. Verify that the BFO display varies as the front panel tuning knob is turned. Press the BFO CENTER pushbutton and verify that the BFO display returns to zero. Set the front panel POWER switch to the off position.

n. This completes the initial operating check of the Receiver. Refer to the operating instructions contained in Chapter 4 for additional information on the operation of the Receiver.

CHAPTER 3
PREPARATION FOR USE AND RESHIPMENT

3-1. **INTRODUCTION.** This Chapter provides information required for preparing the R-2174(P)/URR Radio Receiver for use from a shipped or stored condition and for preparing it from an operating condition for storage or shipment. Section I describes the information required for preparing the unit from a stored or shipped condition, and installation and checkout procedures required for preparing the Receiver for use. Section II describes the procedures required for removing the unit from an operational rack and then packing it for storage or shipment.

Section I. PREPARATION FOR USE

3-2. **UNPACKING.** To unpack the Receiver and prepare it for installation and operation, refer to Paragraph 2-2 in Chapter 2 of this manual and perform the procedures as spelled out in that paragraph. Table 2-2 lists the items required to install the Receiver.

3-3. **INSTALLATION AND PERFORMANCE CHECK.** To prepare the receiver for operation requires the installation of all options associated with the Receiver and the performance of an initialization sequence. Paragraph 2-8 in Chapter 2 of this manual provides detailed instructions for installing these options and Paragraph 2-9 contains an initial checkout procedure. After the required system interface connections are made, as described in Paragraph 2-10, the Receiver performance may be checked by performing the procedures described in Paragraph 2-11.

Section II. PREPARATION FOR RESHIPMENT

3-4. **REMOVAL.** The Receiver must be disconnected and removed from its mounting rack before being prepared for reshipment. The following procedures describe the recommended sequence.

a. Ensure Receiver is turned off, then disconnect primary power cable W18 from its primary power source. Disconnect the other end of the cable from A10J1 on the rear panel of the Receiver.

b. Disconnect the antenna cable from J1-RF IN on the rear panel.

c. Disconnect the ground strap from the GROUND lug space located on the rear panel.

d. Remove any other equipment or cables connected to connectors or jacks on the rear panel.

e. Remove headphones, if they are inserted, from the PHONES jack located on the front panel.

f. Remove the four mounting screws from the front panel securing the Receiver to the mounting rack.

WARNING

The Receiver weighs approximately 30 pounds. Be careful as you slide the unit out of the rack. Have a firm grip on the handles as the weight leaves the rack so that it does not drop causing injury to legs or feet.

g. Grasp the Receiver by the handles on the front panel and slide the unit out of the rack. Place the unit on a bench.

h. This concludes the removal procedures. The unit may now be packed for storage or reshipment.

3-5. **PACKING.** To prepare the Receiver for storage or reshipment, it must be carefully wrapped and packaged as described in the following procedures.

a. Refer to Figure 2-1 in Chapter 2 and make sure that the shipping carton and all packing materials are in good condition.

b. Visually inspect the Receiver for damage and that all parts are present and secure. Record any damage or missing parts before packing.

c. Wrap the Receiver in the intimate wrap and place the unit in the interior container with cushions and desiccant as shown in Figure 2-1.

d. Close the interior carton and wrap with the barrier wrap.

e. Place the bottom cushion in the exterior carton and carefully place the interior carton into the cup of the cushion. Place the top cushion over the top of the interior carton.

f. Close and seal the exterior carton.

CHAPTER 4
OPERATION

4-1. **INTRODUCTION.** This chapter provides detailed instructions for operation of the R-2174(P)/URR Radio Receiver. The information is presented in three sections within the chapter. Section I describes the controls and indicators, Section II presents detailed operating instructions while Section III provides instructions for emergency operation.

Section I. CONTROLS AND INDICATORS

4-2. **GENERAL.** The controls and indicators of the Receiver are shown in Figure 4-1 and listed and described in Tables 4-1 and 4-2. Both tables are printed in two columns. The left hand column, headed with NOMENCLATURE, lists the control or indicator exactly as it is spelled out on the Receiver front panel in upper case letters. If an item is not designated with nomenclature, such as the Tuning Knob, then it is listed in upper and lower case letters. The right hand column, headed with DESCRIPTION/FUNCTION, describes each control or indicator and gives its function.

TABLE 4-1. FRONT PANEL CONTROLS

Nomenclature	Description/Function
POWER-ON	Double pole, single throw toggle switch. Provides on-off control for Receiver by controlling primary power source to power supply.
Tuning Knob	Round black knob – optically coupled to a tuning encoder. Provides selection of Receiver operating frequency or BFO frequency. (See TUNE RATE and BFO pushbutton controls.) The rate of change of the frequency depends on the speed the tuning knob is rotated and the rate of tune selected through the TUNE RATE switch. Clockwise rotation increases frequency, counterclockwise rotation decreases the frequency. This knob is disabled by the LOCK pushbutton.
Left Keyboard	Pushbutton switches.
Mode Selection	
AM, CW, USB, LSB, ISB U/L, FM	These pushbuttons are used to select the operating mode of the receiver. These pushbuttons are the push-on type. That is, when a pushbutton is depressed the receiver will remain in that mode until a different mode is selected. The ISB U/L pushbutton will be enabled only if the Receiver is equipped with the ISB option. If the Receiver is equipped with this option, depressing the pushbutton will activate both the USB and LSB channels simultaneously. If the front panel display indicates I-USB the PHONES jack will be connected to the upper sideband channel. Depressing the ISB U/L pushbutton a second time will change the display to indicate I-LSB and connect the PHONES jack to the LSB channel. The Monitor Line and Loudspeaker outputs, through rear panel connector J3, will also be switched by use of the ISB U/L pushbutton.

TABLE 4-1. FRONT PANEL CONTROLS (Cont.)

Nomenclature	Description/Function
Filter Selection BW1, BW2, BW3, BW4, BW5	These pushbuttons are used to select specific bandwidths within the Receiver. The Receiver is capable of accepting up to 7 plug-in IF bandwidth filters. Receivers are usually configured with separate upper and lower sideband filters, leaving a capacity of up to five symmetrical filters. The upper/lower sideband filters will be automatically selected when the USB or the LSB mode is selected. The remaining filters (up to a total of 5) are selected by depressing the appropriate bandwidth selection pushbutton. BW1 pushbutton will select the narrowest bandwidth, BW2 will select the next-wider bandwidth, and so on. Like the mode selection pushbuttons, these pushbuttons are the push-on type, so that a new bandwidth is selected by depressing a different pushbutton. If only three symmetrical filters are installed, then only pushbuttons BW1 through BW3 will be in operation.
METER RF/AF	This pushbutton is used to cause the front panel meter to display either an RF scale or an AF scale. The receiver will always display either scale. Depressing the pushbutton will cause the display to switch either from RF to AF or AF to RF.
AGC Mode Selection MAN, SHORT, MED, LONG	The Receiver is designed to operate with three different gain control modes: Manual, Automatic, and Automatic with a selectable threshold. Depress the MAN pushbutton to cause the MAN indication to appear in the display. If an automatic indication (SHORT, MED, or LONG) is present in the display it may be deleted by depressing the corresponding pushbutton. The Receiver is now in the manual mode with the gain under control of the front panel IF GAIN control. When the Receiver is switched from the manual mode by pressing MAN when in manual mode only, it will automatically enter the SHORT AGC mode. The medium or long AGC modes may be selected by depressing the corresponding pushbuttons. The AGC mode with a manually set threshold is enabled by depressing an AGC mode pushbutton while in the manual mode or vice versa. The MAN pushbutton is the push-on/push-off type. In the manual mode the AGC pushbuttons are push-on/push-off; while in the automatic mode the pushbuttons are push-on.
Right Keyboard	Pushbutton switches.
TUNE RATE	Provides for fine (1 Hz increments), slow (30 Hz increments) and fast (1 kHz increments) selection of Receiver operating frequency through rotation of the tuning knob.
Frequency Selection 0 through 9, ENTER	These pushbuttons are used to set the receiver to a particular operating frequency. Depressing the ENTER pushbutton will enable the numeric keys. The first numeric key depressed will be recognized by the Receiver as the ten's MHz digit. Since the Receiver cannot be tuned above 29.999999 MHz, the Receiver will recognize only 0, 1, or 2 as the first digit entered. The second numeric key depressed will be recognized as the units' MHz digit; the third numeric key depressed as the hundreds' kHz digit; and so on. It is not necessary to enter all displayed digits.

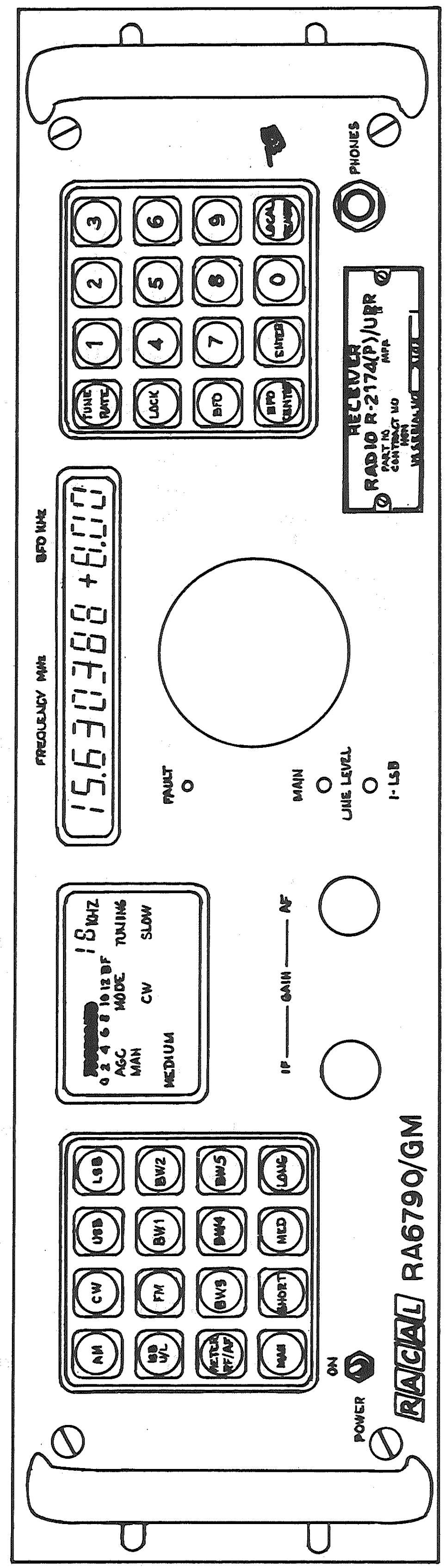


Figure 4-1. Front Panel Controls and Indicators, Radio Receiver R-2174(P)/URR

TABLE 4-1. FRONT PANEL CONTROLS (Cont.)

Nomenclature	Description/Function
LOCK	This pushbutton is the push-on type. When the lock mode is activated, as indicated by the display, the front panel tuning knob will be disabled. The lock mode can be disabled by depressing the TUNE RATE or BFO pushbutton.
BFO, BFO CENTER	These pushbuttons are enabled only if the Receiver is operated in the CW mode. Depressing the BFO pushbutton will permit selection of the BFO frequency through the front panel frequency knob. Depressing the BFO CENTER pushbutton will set the BFO to zero. Depressing the BFO CENTER pushbutton a second time will return the BFO to the previously selected frequency. The BFO pushbutton is disabled if the Receiver is in the BFO CENTER mode.
LOCAL/REMOTE	This push-on/push-off type pushbutton will set the receiver to operate either in the local mode (control of the receiver is through front panel) or the remote mode. Note that the Receiver must be equipped with the optional A6A1 remote control interface circuit card assembly to be operated in the remote control mode, however, if A6A1 is not installed selection of REMOTE will disable front panel control.
IF GAIN	This front panel control is used to establish the local Receiver IF GAIN control when the Receiver is operated in the manual mode; and to set the threshold level when the Receiver is operated in the automatic mode with a manually set threshold.
AF GAIN	This front panel control is used to control the level of the Receiver unbalanced audio outputs.
MAIN LINE LEVEL	This screwdriver set potentiometer is used to adjust the 600 ohm balanced line level when the Receiver is operated in the AM, FM, CW, or SSB modes. If the receiver is equipped to operate in the ISB mode (optional A5 circuit card assembly is installed) this control will also adjust the line level of the upper sideband when the receiver is operated in the ISB mode.
I-LSB LINE LEVEL	This screwdriver set potentiometer is used only when the Receiver is equipped with the optional A5 circuit card assembly. It is used to adjust the line level of the lower sideband when the receiver is operated in the ISB 600 ohm balanced.

TABLE 4-2. FRONT PANEL INDICATORS

Nomenclature	Description/Function
FAULT	Red LED indicator will be illuminated if any synthesizer is out of lock.
Right Display	Liquid Crystal Display (LCD) U3
FREQUENCY-MHz	Indicates the tuned frequency, in MHz, of the Receiver.
BFO kHz	Indicates selected BFO frequency in kHz with plus or minus sign to indicate direction of offset from IF frequency.

TABLE 4-2. FRONT PANEL INDICATORS (Cont.)

Nomenclature	Description/Function
Left Display	Liquid Crystal Display (LCD) U4
-10 0 +10 AF 0 2 4 6 8 10 12 RF	Located upper left corner. Indicates audio level in dBm (upper scale), for 600 ohm balanced monitor output line, RF in tens of dBs above 1 uVolt (lower scale). Scale selected through METER-RF/AF pushbutton switch.
BW-kHz *	Located upper right corner. Indicates the IF bandwidth selected by BW1 to BW5 pushbuttons switches, in kHz.
AGC, MAN, SHORT, MED, LONG	Located lower left corner. The AGC display is always present. The MAN display will be present when the receiver is being operated in the manual gain control mode. The AGC display (SHORT, MED, LONG) indicates the type of automatic gain control being used by the receiver. If both the MAN display and one of the AGC displays are present,it indicates that the receiver is being operated in an automatic gain control mode with a manually set threshold.
MODE, AM, CW, I-/L/USB, FM, AUX	Located lower middle. The MODE display is always present, the remaining displays indicate the operating mode of the receiver. Note that the I-display, associated with the LSB and USB displays, is used only when the Receiver is equipped with the ISB option (A5 circuit card assembly is installed). AUX is used when the forced bandwidth set-up is in operation.
TUNING, FAST, SLOW, LOCK, BFO, REMOTE	Located lower right. The TUNING display is always present. The FAST, SLOW, and LOCK displays are associated with frequency selection through the main tuning knob. The FAST and SLOW displays indicate the tuning rate of the Receiver. If both displays plus the LOCK and BFO displays are off,the Receiver is in the "fine" tuning mode. The LOCK display indicates that the main tuning knob is disabled. The BFO display indicates that the main tuning knob may be used to vary the BFO frequency. The REMOTE display indicates that the receiver is under the control of a remote device or that local control is disabled if remote option is not installed.

* NOTE

The BW-kHz INDICATOR is a nominal indication and cannot be used to accurately measure the bandwidth of installed filters.

Section II. OPERATING INSTRUCTIONS

4-3. **INTRODUCTION**. The Receiver is supplied as a basic unit with one or more options supplied separately. All options associated with a particular Receiver must be installed in the basic unit before the Receiver can be operated. Paragraphs 2-7 through 2-11 describe the installation of the Receiver options, an initial check-out procedure, and the system interconnections associated with the Receiver.

a. The options associated with the Receiver include plug-in IF bandwidth filters, independent sideband operation, and operating the Receiver through a remote control device. One or more of the plug-in filters must be installed before the Receiver can operate. The ISB and remote control capabilities, however, are optional. Because of the different possible filter combinations and the options, some portions of the operating procedures will be different for different Receivers. In order to simplify the operation of the Receiver, it is recommended that a Receiver configuration chart or log book be maintained for each Receiver. The configuration chart or log book would list the IF bandwidth filters currently installed in the Receiver, the operating options, the type of remote control interface, etc.

b. Before attempting to operate the receiver, verify that all options associated with the Receiver have been installed. Additionally, the front panel controls and indicators described in Tables 4-1 and 4-2 should be reviewed before operating the receiver.

CAUTION

Do not use sharp instruments to depress the keypads since this may damage the equipment.

4-4. LOCAL OPERATING PROCEDURES. The following paragraphs describe the basic operating procedures associated with the Receiver.

a. Initialization. The Receiver must be initialized after any plug in filters have been changed, any options have been installed or removed, or if the receiver memory data may have been disturbed. To initialize the Receiver, set the POWER switch to ON and depress the LOCK pushbutton and while still holding the LOCK in depress the AM pushbutton then release in the opposite order they were depressed. The Receiver will now perform an automatic initialization sequence to update the mircroprocessor memory with the current receiver configuration. At the completion of the initialization sequence (approximately 1 minute) the Receiver will return to its previous operating condition. If an error is detected during the initialization seqence the microprocessor will stop the sequence and display a two digit number in the frequency display. If this occurs, refer to the fault isolation procedures contained in Chapter 6 of this manual.

b. Mode Selection. The Receiver may be operated in the AM, FM, CW, USB, or LSB modes. Additionally, if the Receiver is equipped with the optional A5 circuit card assembly, in the ISB mode. Selection of the desired operating mode is made by depressing the appropriate pushbutton on the left keyboard.

c. Frequency. The operating frequency in any of the modes must be selected and entered into the Receiver. The frequency may be selected by depressing the TUNE RATE pushbutton and adjusting the indicated frequency with the tuning knob or by depressing the ENTER key, then the appropriate numeral keys. Once the desired frequency is entered either by the keypad or tuning knob it may be finely adjusted by selecting the "fine" rate with the TUNE RATE key then rotating the tuning knob. To lock the frequency, press the LOCK pushbutton. This disables the tuning knob and prevents inadvertent frequency change.

d. BFO. The internal beat frequency oscillator is tuned by depressing the BFO pushbutton and adjusting the BFO through the tuning knob. The BFO offset is indicated as above (+) or below (-) the IF frequency. Depressing the BFO CENTER pushbutton will cause the BFO to go to zero. Depressing the BFO CENTER pushbutton a second time will return the BFO to its previous setting.

e. Bandwidth. A total of seven different IF bandwidth filters may be installed in the Receiver. If sideband filters are installed, the Receiver will automatically switch in the appropriate filter when the LSB or USB operating mode is selected. If a symmetrical sideband filter is used for sideband operation the receiver will use the filter installed in the FL1 positon for both sidebands by putting an offset in the first and last local oscillators. During the initialization sequence the microprocessor will assign the remaining filters to front panel pushbuttons BW1 through BW5 in an ascending order. That is, depressing BW1 will select the narrowest bandwidth, BW2 the next widest bandwidth, and so on. For bandwidth changes, press LOCK and ISB U/L at the same time to go into AUX. Press ENTER and enter desired bandwidth. The radio will automatically assign the change to the correspondent filter. Press ENTER again to change the next bandwidth. Once you're done, press LOCK or ISB U/L to get out of AUX.

f. AGC Operation. The Receiver may be operated in any one of three different gain control operating modes: manual, automatic, and automatic with a manually set threshold. To set the Receiver for manual operation, depress the MAN pushbutton and verify that none of the automatic modes (SHORT, MED, and LONG) are shown in the display. If an automatic mode is shown, depress the corresponding pushbutton to delete the mode. Depress the METER RF/AF pushbutton (if required) to display the RF scale. Adjust the front panel IF GAIN control to select the desired gain. To set the receiver for automatic gain control operation, depress the MAN pushbutton. The receiver will switch out of the manual mode to the SHORT AGC mode. The medium and long AGC operating modes may be selected by depressing the MED or LONG pushbuttons. To operate the Receiver in the automatic mode with a manually set threshold, set the Receiver to the manual mode and adjust the threshold as previously described. When the desired level is set, select the AGC mode by depressing the SHORT, MED, or LONG pushbutton. The display will indicate both the MAN indication and the selected automatic mode. To change the automatic mode, depress the selected automatic gain control pushbutton.

g. Local/Remote. Provision is made on the front panel of the Receiver to operate the unit either from the front panel (LOCAL) or from a REMOTE location; provided the receiver is equipped with the optional circuit card assembly A6A1. Refer to Paragraph 4-6 for remote operation.

h. BITE. The Built In Test Equipment (BITE) can be initiated at any time during operation of the Receiver to determine its operating condition. This self test may be initiated either from the front panel or from a remote location. From the front panel BITE is controlled through different combinations of pushbuttons; LOCK with AM, CW or LSB. LOCK and AM will initiate the self test with the front panel indicators indicating progression of the test. LOCK and CW continues the test after a fault is indicated while LOCK and LSB provides for returning to the operating mode from a BITE routine. To apply either of these three routines the LOCK pushbutton must be pressed first and while still holding it depressed press its companion pushbutton (AM, CW or LSB) then release the pushbuttons in the opposite order to which they were depressed. If a fault is encountered, during the self test, the BITE will stop and the frequency display will indicate a two digit number. The fault isolation procedures described in Chapter 6 of this manual list the probable errors corresponding to the two digit numbers. To continue the test after a fault is indicated, press the LOCK and the CW pushbuttons as described above. If it is desired to return to the operating mode while the BITE sequence is in progress, press LOCK and LSB in the manner described. Refer to Paragraph 4-6 for remote operation of BITE.

4-5. TYPICAL OPERATING PROCEDURES. Because of the different operating options associated with the receiver, and the different applications for the receiver, the detailed operating instructions may be different for each site. The following procedure describes a typical operating sequence for selecting a station in the local AM broadcast band.

a. Set the POWER switch to ON and if it is desired to initialize the Receiver, depress the LOCK pushbutton and while still holding the LOCK in depress the AM pushbutton, then release in the opposite order they were depressed.

b. Depress pushbuttons BW1 through BW5 and observe the indicated bandwidth in the display. Select the desired bandwidth by depressing the appropriate pushbutton.

c. Depress the AM pushbutton and verify that the AM mode is indicated in the display.

d. Depress the ENTER pushbutton and the numeric keys to enter the frequency of the desired station. Note that the first digit entered will be the ten's MHz digit, the second will be the unit's MHz digit, and so on.

e. Select the desired AGC mode by depressing the appropriate pushbutton.

f. Depress the METER RF/AF pushbutton to display the AF scale.

g. Connect a set of headphones to the front panel PHONES jack and adjust the AF GAIN control to obtain a suitable audio level.

h. Depress the TUNE RATE pushbutton to select either FAST, SLOW, or fine tuning mode. Note that fine tuning rate is indicated by the absence of the FAST and SLOW indication.

i. Turn the front panel tuning knob to obtain the maximum signal strength as indicated by the meter and the audio level in the headphones.

j. Depress the LOCK pushbutton to disable the front panel tuning knob.

k. This completes the typical operating sequence for operation of the Receiver in the AM mode. Operating the Receiver in the remaining modes is similar to the procedure just described.

4-6. REMOTE OPERATION. If the Receiver is equipped with the optional A6A1 circuit card assembly it may be operated from a remote control device. Before attempting remote control operation, make sure the procedures described in Paragraphs 2-8b and 2-10e have been incorporated.

a. The data character used for remote control is the standard ASCII asynchronous format consisting of a start bit, seven data bits (one ASCII character), an optional parity bit, and two stop bits. Each command message to the receiver must be terminated with the carriage return character (an additional line feed character is not required).

b. The remote operation of the receiver, as described in the following paragraphs, may be divided into four main functions: remote control of the receiver, override commands, receiver status, and receiver monitoring. Up to 10 separate receivers may be connected to the remote control device on the same bus. Status and monitor commands may be sent to only one Receiver at a time.

c. Receiver Control. The Receiver will respond to the following control commands:

(1) Receiver Address. The command $(N) will select a particular Receiver designated by (N) where N represents the Receiver number. That is $7 will select Receiver number 7. More than one Receiver may be addressed at the same time by inserting commas between the Receiver numbers. For example, $7, 23, 8 would select Receivers 7, 23 and 8. (Multiple addressing is not allowed for status return request.)

(2) Frequency Selection. The command F(N) is used to select the Receiver operating frequency designated by (N) where N represents the Receiver frequency. The frequency command may specify the desired frequency down to 1 Hz. For example, the command F03.415926 would tune the Receiver to 3.415926 MHz. If an exact frequency is not required, the leading and trailing zeros may be eliminated. For example the command F3.4 would tune the Receiver to 3.400000 MHz. Note that in both cases a decimal point is required to indicate MHz.

(3) Mode Selection. The desired mode is selected by sending one of the following commands:

D1 AM Operation
D2 FM Operation
D3 CW Operation with variable offset, see Paragraph (4)
D4 CW Operation with zero offset
D5 ISB Operation (if ISB option is installed)
D6 LSB Operation
D7 USB Operation

NOTE

To monitor status on controller refer to Paragraph e (4).

(4) BFO Offset. The BFO offset frequency may be set in the CW mode by sending the command B(N) where (N) indicates the offset frequency in kHz. For example, the command B + 1.82 will set the BFO offset 1.82 kHz above the center frequency; B–4.65 will set the offset 4.65 kHz below the center frequency.

(5) Bandwidth Selection. The desired bandwidth is selected by sending the command I(N) where (N) indicates the filter bandwidth in kHz. For example, the command I3.24 would select the 3.24 kHz filter. If a command is received that does not match the filter in the Receiver, the Receiver will automatically select the closest filter. For example, the command I7. could select a 6.8 kHz filter. Note that the decimal point is used to indicate kHz.

(6) Gain Control Mode. The desired gain control mode is selected by sending one of the following commands:

M1 Selects short AGC time constant
M2 Selects medium AGC time constant
M3 Selects long AGC time constant
M4 Selects manual gain control, see Paragraph (7).
M5 Selects short AGC with preset threshold, see Paragraph (7).
M6 Selects medium AGC with preset threshold, see Paragraph (7).
M7 Selects long AGC with preset threshold, see Paragraph (7).

NOTE

To monitor status on controller refer to Paragraph e (4).

(7) Manually Set Gain Control. The Receiver will respond to remote commands to set a manual gain. The Receiver IF gain is controlled by adding attenuation, gain controlled in 150 steps over AGC range of approximately 120 dB. Any position can be selected by sending number from 0 to 150. This feature may also be used in conjunction with the AGC operation to establish a minimum threshold level for the AGC. The command for setting the level is A(N) where (N) represents an amount of attenuation, to be added to the circuit. For example, the command A3 would send 3 to the AGC control circuit; A104 would send 104.

d. Status Commands. The status commands provide the remote controller with the status of a particular Receiver. Status commands may be sent to only one Receiver at a time since some of the status commands will result in monitor data from the Receiver back to the remote control device. The Receiver will respond to the following status commands:

S1 Set Receiver to local control
S2 Set Receiver to remote control
S3 Initiate BITE self test sequence, see Paragraph (1)

S4 Terminate BITE self test sequence, see Paragraph (1)
S5 Send bandwidth of installed IF filter, see Paragraph (1)
S6 Send BITE results, see Paragraph (1)
S7 Force bandwidth setup, see Paragraph (1)
S8 Enable remote AGC dump, see Paragraph (2)
S9 Inhibit remote AGC dump, see Paragraph (2)

(1) If the Receiver is in the override mode command S1 will be ignored. If the Receiver successfully completed the BITE self test sequence (command S3), sending S6 will result in a response OK08 (CR). The carriage return (CR) indicates the end of the message. If the self test was not completed successfully, the Receiver might respond with something like; :4, 17, 33, END 08(CR).

The colon will be sent at the start of the test. For each step of the test that fails, the Receiver will send the step number (as in the example steps 4, 17, and 33) up to a total of 5 steps. The typical Receiver response for command S5 would be L, 1.2, U, .4, ,16, ,(CR) indicating the type or bandwidth of filter installed in filter slot sequency (FL1, FL2, etc.). When no filter is installed digits will not appear between commas in the return information as shown in the example for filter slots FL5 and FL7. The S7 command is used only for maintenance and is described in Chapter 6.

(2) Status commands S8 and S9 are used for AGC dump control. When the Receiver is being operated remotely, these commands will be extremely useful to prevent "signal blasting" during tuning procedures. The S9 command, Inhibit remote AGC dump, will prevent the Receiver microprocessor from effectively causing the AGC to run wide open when remotely tuning in small frequency increments, e.g., 1 to 30 Hertz steps. If the AGC dump were not inhibited, the Receiver would run at full signal gain each time there was a 1 Hertz frequency change, causing high level audio signals to be sent over the voice links to the remote control area. This could result in possible link damage or severe crosstalk in the system. Upon completion of the fine tuning activity, the S8 command restores the AGC dump to microprocessor control. The S9 functions will not be needed for large frequency increments, typically 1 MHz or greater.

e. Monitor Commands. The remote control device may command a particular Receiver to provide monitor data. The response from the Receiver will be in the following sequence: frequency detector, AGC mode, IF bandwidth, BFO frequency, IF attenuation, and status. All unnecessary information will be eliminated. For example, if the Receiver is in the AM mode, BFO data will not be included. The Receiver will respond to the following monitor commands:

G Receiver will respond with all relevant data
T Receiver will respond with specific data.

(1) The Receiver will respond to a T command according to the data specified in the command. For example, the command TFI will result in frequency and bandwidth response; TFD will result in frequency and detector mode response.

(2) The status data will be sent as the last item in each monitor response from the Receiver. The status data is a one or two digit number representing the following conditions:

0 Receiver is operating in local control mode
1 Receiver is operating in remote control mode
2 Synthesizer is out of lock
4 Receiver is in the Override mode
8 Last command sequence has character transmission error
16 Last command sequence had data error
32 Lost Data error in last sequence

(3) If two or more conditions are present the numbers representing the conditions will be added together and transmitted as one number. For example, 17 (1 + 16) would indicate that the Receiver is in remote control (1) and last command sequence had a data error (16); 13 (1 + 4 + 8) would indicate remote operation (1), override mode (4) and character transmission error (8).

(4) The Receiver will respond to a G command with a response reflecting all Receiver operating conditions. Let us assume that the Receiver address is 10 and the Receiver is set to 12.34 MHz, CW mode, BFO offset of +1.2 kHz, MAN AGC, with manual gain set with (A20), see Paragraph 4-6c (7), and Bandwidth of 6.8 kHz. The return information to the remote controller will be formatted as follows:

Data Stream to Receiver: $10G (CR)
Data Stream from Receiver: F12.34, D3, M4, I6.8, B1.2, A20, S1(CR)

It can be seen by analyzing the Status (S) data that the Receiver is operating in the remote control mode.

f. Override Operation. The remote control device may command a Receiver to switch to an override mode. In the override mode, some of the automatic operating features of the Receiver are disabled. That is, the first local oscillator is always tuned to 40.455 MHz above the entered frequency and the IF slot is always enabled regardless of the type of filter installed. Therefore, the remote controller must decide what the filter should be used for, the type of detection mode to employ, and the BFO offset to receive a signal. For instance, in sideband detection with a symmetrical filter, the first local oscillator and BFO must be properly offset to correctly demodulate the signal. The controller also assumes the responsibility for insuring that the filter is installed in the selected slot, since an empty slot will cause a dead Receiver. The override mode blanks the display except for remote indication. In addition, override signals cannot be handed off to the operator, since the machine has no way of deciding the difference between a sideband signal with virtual carrier offset or a CW signal with a BFO offset. The override mode is invoked when both detector and bandwidth are sent in the same command with the = sign. For example I=4 will select the filter in filter socket 4 instead of a filter at or near 4 kHz as when I4 command is sent. Sending either without the equals stores the = data but leaves the Receiver in the modal command mode. The Receiver will respond to the following override commands: The Receiver requires both D=(N) and I=(N) to go into override mode.

(1) Mode Selection. The desired mode is selected by sending one of the following commands:

D=1 Selects envelope detector
D=2 Selects continuous wave detector
D=3 Selects frequency modulation detector
D=4 Selects ISB operation

NOTE

To monitor status on controller refer to Paragraph e (4).

(2) Filter Selection. In the override mode the filters are selected according to the filter socket number instead of the filter bandwidth. The command is I=(N) where (N) corresponds to the filter socket number. For example, the command I=3 will select the filter inserted in filter socket 3. **Override mode is disabled by sending a normal I or D command.**

NOTE

To monitor status on controller refer to Paragraph e (4).

(3) Other operating commands (Frequency, AGC, Manual AGC, Attenuation and BFO) can be entered in the normal way.

4-7. **SHUTDOWN PROCEDURES.** The Receiver is shutdown simply by setting the POWER switch to the off position. When the Receiver is switched back on, it will automatically return it its last setting.

Section III. EMERGENCY OPERATION

4-8. **EMERGENCY OPERATING PROCEDURES.** The emergency operating procedures applicable to the Radio Receiver R-2174(P)/URR are dependent on the particular operating mode being used. For example, if the Receiver is being operated in the remote control mode and a failure occurs in the remote control circuitry, it may be switched to the local mode and manually operated with the front panel controls.

CHAPTER 5
THEORY OF OPERATION

5-1. INTRODUCTION. This chapter contains the theory of operation for the R-2174(P)/URR Radio Receiver. The theory describes the primary signal flow as it progresses through the various components of the receiver and explains the functional relationships of each component to the signal flow. The description or theory is divided into three main sections to best describe the receiver function. Section I describes the primary signal flow as related to the receiver's functional operation. Section II describes in detail each circuit card assembly and the components included on each card. Section III describes the functional operation of mechanical assemblies. Simplified functional block diagrams and timing diagrams are used throughout the text to aid the technician in understanding the various functions.

SECTION I. FUNCTIONAL SYSTEM OPERATION

5-2. GENERAL. Section I provides a description of the functional operation of the Receiver. This description traces the primary signal from the antenna input, through the Receiver, to the audio output and describes secondary functions as they are related to that primary signal flow. To simplify the description and for a basic understanding of the receiver operation the functions are divided into five major divisions. These five divisions, as shown in Figure 5-1, are: primary signal (RF, IF and AF), oscillator synthesizers, Automatic Gain Control (AGC), receiver control, and power supply.

a. The primary signal function consists of circuit card assemblies A1, A2, A3, A4 and A5. This function describes the signal flow from the RF input at the antenna to the audio termination into headphones or speaker. The second major division describes the operation of the oscillator synthesizers (circuit card assemblies A7 and A8). This description includes the first local oscillator signal to the first mixer, the second local oscillator to the second mixer and the beat frequency oscillator function for CW operation. The third major division describes the operation of the Automatic Gain Control (AGC) which is contained primarily on circuit card assembly A4 along with IF and AF components. Some other AGC circuits are located on A3 and A5. The fourth major division describes the function of the receiver control circuitry which is contained on the front panel and circuit card assemblies A6A1, A6A2 and A9. The fifth major functional division of the Receiver is the power supply contained in assembly A10. Figure 5-2 shows a simplified overall functional block diagram of the Receiver and should be followed in reading the description.

5-3. PRIMARY SIGNAL – RF, IF AND AF. The primary signal consists of the radio frequency (RF) signal, the intermediate frequency (IF), and the audio signal (AF). The description that follows divides the primary signal into those three functions to more clearly present their operation.

a. RF Signal. The antenna signal is connected through the rear panel of the Receiver to a low-pass filter located on assembly A1. The four section elliptical low-pass filter rejects frequencies above 35 MHz and at the same time prevents local-oscillator and IF frequencies from being radiated back through to the antenna. Each section of the filter contains a coil-capacitor tank circuit, with the coil of each stage adjustable for peaking the tank circuit. This provides optimum rejection at its designed frequency. The output of this first low pass filter is routed to another filter located on circuit card assembly A2. This filter operates much in the same manner as the one just described but also provides for impedance matching to the first mixer stage and to reduce peak to peak ripple on the carrier signal. The output of this filter is connected directly to the first mixer where the RF signal is mixed with the variable frequency from the first local oscillator to form the first IF signal.

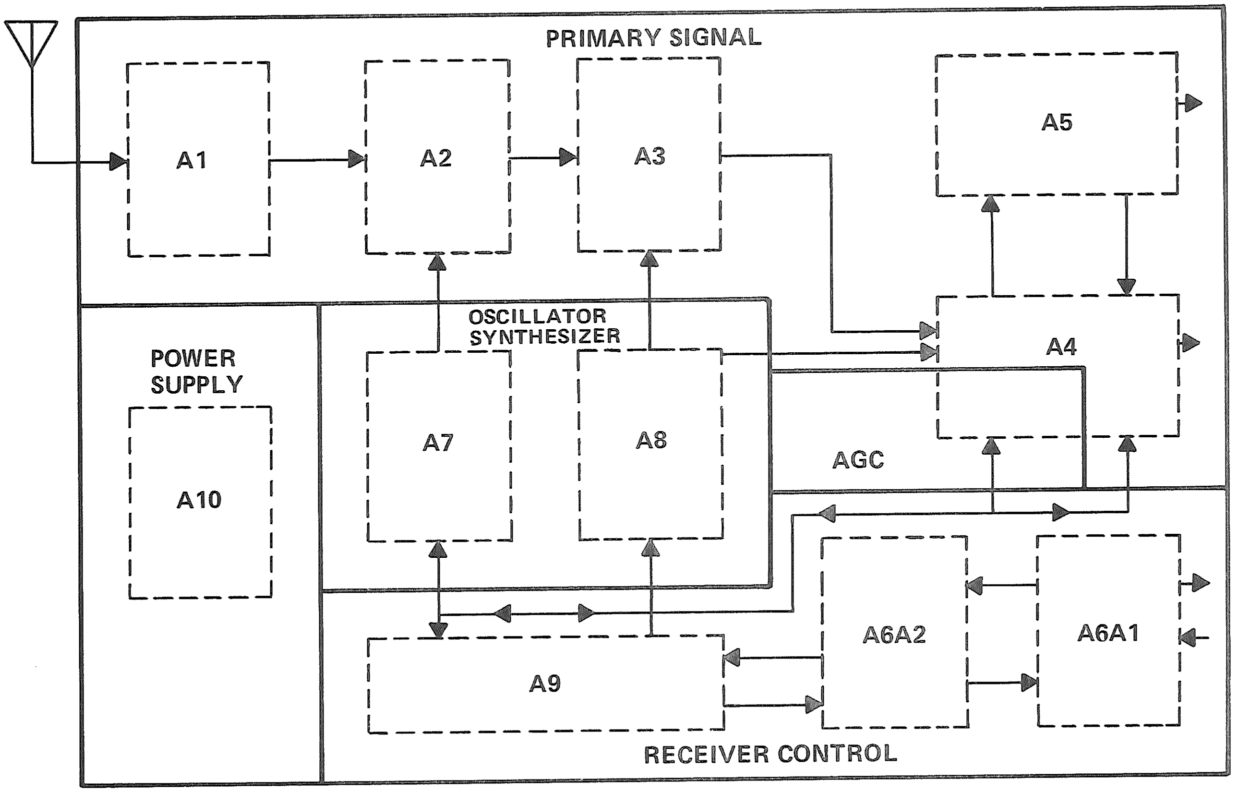
b. IF Signal. The first IF signal is developed in the first mixer stage where the RF signal is mixed with the variable output frequency of the first local oscillator. The first local oscillator frequency is varied in direct relation to the RF frequency selected from the control section and varies between 40.955 (0.5 MHz selected) and 70.454 MHz (29.999 MHz selected). This variable frequency produces a difference frequency in the mixer of 40.455 MHz. This difference frequency along with all other resultant frequencies is routed to a filter which rejects all other frequencies except the desired 40.455 MHz carrier with intelligence. The filter has a 20 kHz bandwidth and is coupled to a linear buffer amplifier. This amplifier stage is controlled by a control signal from the AGC circuit to maintain a constant amplitude output.

(1) The AGC controlled IF signal is routed to circuit card assembly A3, where it is connected to a two stage IF amplifier, with additional between stage filtering. These two stages provide additional level control of the IF signal. This AGC controlled IF signal is impedance coupled to a band pass filter consisting of four stages of tuned filter traps. An adjustable amplifier just prior to the filters provides for adjusting the gain through the filters. The IF output from the filter is connected to the second mixer where the IF is mixed with the second local oscillator to form the second IF signal. The second local oscillator output of 40 MHz is mixed with the 40.455 MHz first IF, which provides a difference frequency of 455 kHz. This difference frequency is transformer coupled to a filter network which rejects all frequencies except the desired 455 kHz second IF signal. The output of the filter network is coupled to an IF amplifier to restore gain and for coupling to the plug-in band pass filters, contained on circuit card assembly A4.

(2) The IF signal from A3 is coupled directly to seven plug-in bandwidth filter slots. The number of filters plugged in and the bandwidth of each filter depends on the option of the operator. Any number, up to seven, may be plugged into the card at any one time. The filter bandwidth desired for operation is then automatically switched into the IF circuit when it is selected from the front panel or remotely. When the optional independent sideband (ISB) is used, filter slot FL1 must contain a lower sideband filter. All bandpass filter slots are permanently connected to a diode switch, including FL1. This filter may be connected, through a movable link, from the diode switch to a bus that leads directly to the ISB circuit card assembly A5.

(3) In all modes of operation, including ISB, the diode switch selects the desired filter slot. The control circuitry automatically selects the filters in an ascending bandwidth order regardless of the order in which they are plugged into the sockets; that is, bandwidth 1 (BW1) selects the narrowest bandwidth and so on with BW5 selecting the widest bandwidth. Two slots are generally reserved for upper sideband (USB) and lower sideband (LSB) which are also automatically selected when that mode is directed from the control section. The IF signal output of the selected bandwidth filter is impedance coupled to a two stage AGC controlled amplifier. The output of this amplifier is then coupled to a bandpass filter for additional filtering of the IF signal. A portion of this signal is routed through a buffer amplifier to J2-IF OUT, on the rear panel, as the IF output signal.

(4) The IF signal is also coupled through a buffer amplifier to one input of an RF switch and to the product and synchronous AM detector. The RF switch also has the beat frequency oscillator (BFO) as an input with the output of the switch coupled directly to the FM detector. The switch has two modes of operation and is switched through the control circuitry. In



Circuit Card Assembly	Nomenclature	Function
A1	RF Low Pass Filter	Primary Signal
A2	First IF Mixer	Primary Signal
A3	Second IF Mixer	Primary Signal
A4	Main IF/AF	Primary Signal/AGC
A5 (optional)	ISB IF/AF	ISB-Primary Signal
A7	First LO Synthesizer	Oscillator Synthesizer
A8	Second LO/BFO Synthesizer	Oscillator Synthesizer
A6A1 (optional)	Serial Asynchronous Interface	Receiver Control
A6A2	Microcomputer	Receiver Control
A9	Front Panel Control	Receiver Control
A10	Power Supply	Receiver Power

Figure 5-1. Basic Receiver Functional Breakdown

the AM and FM modes the switch selects the IF signal, in all other modes, the switch automatically couples the BFO to the FM detector and limiting amplifier. Two outputs of the FM detector are then coupled to a detector select switch and to the carrier input of the product and synchronous detector. The output to the product and synchronous detector will be either the demodulated AM signal or BFO depending on the mode selected. The detector select switch is also controlled by the function modes of the control section. In the FM mode the select switch passes only the FM detected signal to an audio filter. In all other modes the detector select switch passes the output of the product and synchronous detector to the same audio filter.

(5) When the ISB is selected from the control section, the LSB portion of the IF signal is linked directly to circuit card assembly A5. The flow of the IF signal through the ISB circuit is very similar to that just described; except that the BFO is connected directly to the ISB detector. The USB portion of the IF signal is routed through the A4 circuit card in the ISB mode.

c. AF Signal. The detected audio signal from either the FM detector or the product detector is selected by the detector select switch through receiver control. The selected audio is routed through a lowpass filter to a crosspoint switch. Through receiver control the crosspoint switch selects the various audio modes available as outputs from the Receiver. When the ISB option is installed, the audio output from that circuit card is also coupled to the switch. In non ISB modes the main audio (A4 card) is selected and routed to two separate audio amplifiers. The first amplifier is volume controlled through the AF GAIN control on the front panel. The output of this amplifier is routed both to the rear panel for loudspeaker output and to the phones jack on the front panel. The second amplifier is level controlled through a variable attenuator placed in the line to the second amplifier by the crosspoint switch. Attenuation is varied through a screwdriver adjustment on the front panel. This amplifier then drives an output transformer which provides the monitor line output to the rear panel. If the ISB circuit card is installed in this non ISB mode, the output of the attenuator will also be routed through circuits on the ISB card and appear on Line 1 output on the rear panel. This circuit is described in the ISB mode which follows.

(1) In the ISB mode either the main (USB) or the ISB (LSB) is selected and routed to the same circuits as described in non ISB mode. In addition, the crosspoint switch couples both the LSB and USB through variable attenuators to their respective amplifiers on the ISB circuit card. The two amplifiers drive output transformers which couple the USB (Line 1 output) and LSB (Line 2 output) to the rear panel. Level control of Line 1 output is through front panel screwdriver adjustment MAINLINE LEVEL. Line 2 output is controlled through I-LSB LINE LEVEL. These two adjustments vary the attenuators connected in their respective lines.

5-4. **OSCILLATOR SYNTHESIZERS.** The oscillator synthesizers consist of the first local oscillator (LO) synthesizer, the second LO synthesizer and the beat frequency oscillator (BFO) synthesizer. The three oscillator synthesizers are each independent separate oscillators except that the 1 MHz signal derived from circuitry in the second LO is used as a reference frequency to the other two oscillators.

a. First Local Oscillator Synthesizer. The first local oscillator provides the oscillator frequency to the first mixer where it is mixed with the RF signal to produce the first IF signal. This variable oscillator, located on circuit card assembly A7, is controlled from the receiver control frequency select. It is a voltage controlled single loop synthesizer oscillator with an output frequency variable between 40.955 and 70.454999 MHz in 1 Hz increments.

(1) The voltage controlled oscillator (VCO) generates the basic frequency which is applied to a drive amplifier located on circuit card assembly A2. This same output frequency is applied to a divide by N circuit. The value of N is determined by the digital control logic, also coupled to the divide by N circuit. This digital control logic depends on the RF frequency selection

UK and US Patents have been obtained covering the synthesizer circuits described on this page as follows: US Patent No. 4,204,174 Phase Locked Loop Variable Frequency Generator and US Patent No. 3,555,446 Frequency Synthesizer.

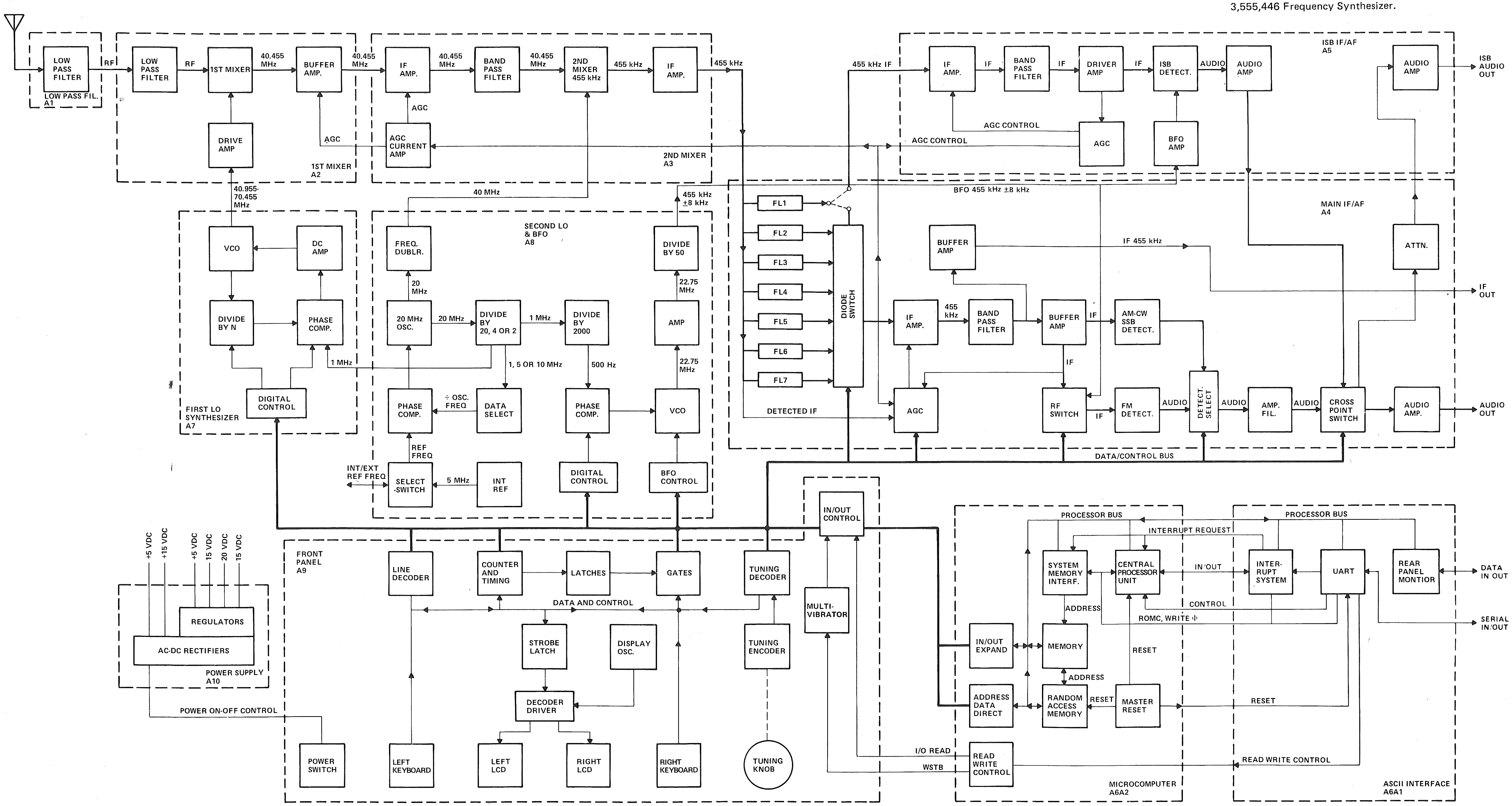


Figure 5-2. Overall, Simplified Functional, Block Diagram

inputs. The output of the divide by N circuit is coupled to a phase comparator to which a 100 kHz reference signal and the digital logic is also connected. The basic output of the phase comparator depends on the phase difference between the reference signal and the divide by N signal. This basic output is combined with the digital control logic, filtered and applied to the dc control amplifier. The output of this dc amplifier controls the frequency of the VCO. The output of the VCO is transformer coupled to a high pass filter, located on circuit card assembly A2, which rejects frequencies below the oscillator range. This filter output is applied to a transistor drive amplifier which routes the signal through an RF wideband transformer to the mixer. The VCO is varied between 40.955 MHz (RF selection of 0.5 MHz) and 70.454999 MHz (RF selection of 29.999 MHz). When this oscillator frequency is applied to the mixer and mixed with the RF signal a difference frequency of 40.455 MHz is obtained. It is this difference frequency that is used for the first IF signal.

b. Second Local Oscillator Synthesizer. The second local oscillator provides the oscillator frequency to the second mixer where it is mixed with the first IF signal to produce the second IF signal. The oscillator, located on circuit card assembly A8, is a constant frequency phase locked oscillator driven from a reference signal. The output of the oscillator is 20 MHz which is frequency doubled to provide the 40 MHz signal to the second mixer. A reference signal, either the internal reference signal or an external reference signal, is required for operation of the oscillator synthesizer. The internal reference signal comes from a crystal oscillator which has an output frequency of 5 MHz. An external reference signal may be applied through the REF IN/OUT connection on the rear panel. The REF INT/EXT switch, also located on the rear panel must be in the applicable position as to the reference selected. With the switch in the EXT position, the internal reference oscillator is turned off and the external reference signal is applied through a transistor switch and shaper circuit to a phase comparator. With the switch in the INT position, access to any external reference is turned off, the internal oscillator is turned on and applied through the transistor switch in the same manner as the external reference.

(1) The heart of the oscillator synthesizer is a 20 MHz crystal referenced oscillator whose output is coupled through a buffer amplifier to a divide by 2 circuit which in turn feeds another divide by 2 and a divide by 10 circuit. The resultant 10 MHz, 5 MHz and 1 MHz output of the circuit is coupled to a data select circuit. The 1 MHz signal is also routed to the BFO oscillator and to circuit card assembly A7, where it is used as a reference signal to the first local oscillator. The reference frequency output of the data select circuit is applied to the phase comparator which phase compares this signal to the internal or external reference described above. The phase difference signal (if any) is then applied through a digital to analog converter to the 20 MHz oscillator. If the oscillator tends to drift off frequency the phase difference between the reference signal and oscillator signal will be detected by the phase detector and the phase difference, applied through the digital to analog converter, will readjust the oscillator.

(2) The output of the oscillator is also coupled through another buffer amplifier to a frequency doubler. The 40 MHz output signal from this doubler is routed to circuit card assembly A3 and capacitor coupled to the second mixer. The difference frequency between this 40 MHz signal and the 40.455 MHz first IF signal is the second IF signal of 455 kHz.

c. BFO Synthesizer. The BFO provides the fixed and variable beat frequency for reinsertion of the carrier in the sideband and CW modes. The oscillator operates at the second IF signal frequency of 455 kHz and can be varied 8 kHz in either direction. The BFO oscillator, located on circuit card assembly A8, is a voltage controlled variable oscillator with a center frequency of 22.75 MHz. The oscillator output frequency is filtered and applied through a buffer amplifier to a divide by 50 circuit. The output of this divide by 50 circuit provides the variable 447 to 463 kHz BFO signal for reinsertion at the product detectors on circuit card assemblies A4 and A5.

(1) A digital control circuit is used to vary the basic oscillator frequency of 22.75 MHz. The output of this circuit is coupled to a phase comparator, along with a 500 Hz reference signal. This 500 Hz reference signal is derived by applying the 1 MHz reference signal, from the second local oscillator, to a divide by 2000 circuit. The phase comparator compares the output of the digital control circuit and the 500 Hz reference signal and applies the difference signal through a digital to analog converter to the VCO. The oscillator may be varied between 22.35 and 23.15 MHz in 500 Hz increments, which when applied to the divide by 50 circuitry provides a BFO frequency between 447 and 463 kHz variable in 10 Hz increments. The BFO frequency is filtered before being routed to the product detectors.

5-5. **AUTOMATIC GAIN CONTROL (AGC).** The AGC circuits provide the receiver with constant level AF output signal with large variations in the incoming RF signal. For example, the change in IF or AF output levels is less than 6 dB for a change in the input level of –100 dBm to –10 dBm. This automatic gain control is accomplished through AGC circuitry, located mainly on circuit card assembly A4. The optional ISB circuit card assembly A5 contains its own AGC for signal gain control in the ISB mode of operation.

a. The receiver may be operated in any one of three different gain control modes: manual, automatic, and automatic with a manually set threshold. In the manual mode the gain is set through a front panel control. In the automatic mode the AGC circuits will compensate for changes in the receiver input signal level. In the automatic/manual mode the front panel control is used to set the operating threshold of the AGC circuits.

b. The AGC operates from a portion of the IF signal taken after the gain controlled IF amplifier stage, thus maintaining a closed AGC loop. The AGC circuitry detects the IF signal, provides three different decay times, provides for automatic threshold control of the output signal or manual threshold control. The output of the AGC circuit is routed to the second IF amplifier on circuit card assembly A4 and to a current amplifier on circuit assembly A3. The current amplifier controls the first IF signal by controlling the gain of two IF amplifier stages; one located on circuit card assembly A3 and the other located on circuit card assembly A2.

5-6. **RECEIVER CONTROL.** Signals that control the receiver's operational parameters (such as operational mode, receiver frequency, BFO frequency, bandwidth, AGC and BITE sequence) are produced by the microcomputer (A6A2) and routed by the front panel receiver control circuit card assembly (A9). The microcomputer under program control follows instructions it receives from the front panel in LOCAL operation and from the remote controller in REMOTE operation. In both LOCAL and REMOTE, the microprocessor functions essentially the same; however, when being operated from a remote location, the power must be turned on at the front panel and the optional serial asynchronous interface assembly (A6A1) must be installed. The serial asynchronous interface circuit card assembly (A6A1) interfaces the external remote controller (when used) with the microcomputer.

a. Figure 5-2 shows the receiver control circuits and shows the signal flow between the front panel receiver control assembly (A9), the microcomputer circuit card assembly (A6A2) and the serial asynchronous interface circuit card assembly (A6A1). The front panel receiver control assembly (A9) contains the Liquid Crystal Displays (LCD), connects to both sets of keyboard switches and the receiver control circuits and routes data between these units and the microcomputer. The R-2174(P)/URR Radio Receiver interconnection diagrams contained in Chapter 8 show all connections to and from these modules.

b. As shown in Figure 5-2, the microcomputer (A6A2) directs receiver operations by interfacing with circuits on the receiver control assembly (A9) and serial asynchronous interface (A6A1) and sending control signals to various receiver circuits.

c. The receiver control assembly (A9) contains the tuning mode and frequency displays and the tuning control circuits and connects to the frequency select and the modes select keypads. The strobes and selection circuits that route data under microprocessor control are also on the receiver control assembly. The strobe and selection circuits control the transfer of information between the front panel and the microcomputer as well as between the microcomputer and the receiver circuitry.

d. The basic functions performed by the microcomputer (A6A2) include:

1. Initialize circuits following power application.
2. Read local input signals from front panel controls.
3. Update front panel displays.
4. Compute and send receiver tuning and operating data to the appropriate receiver circuits.
5. Receive commands from the remote controller and upon request, return receiver status.
6. Retain memory of receiver setting at power failure or turn-off and restore receiver to the operational modes when power is reapplied.

e. The microcomputer directs receiver operations by executing the control program that it obtains from the Erasable Program Read Only Memory (EPROM). During local operation, the receiver is controlled by the microcomputer as follows:

(1) The frequency and mode setting established by the front panel switches and the tuning control are continuously read at 25 ms intervals by the microcomputer. The actual scanning function of the microcomputer is under program control. As the microcomputer scans the front panel switch and controls, it also stores the current status of each control parameter in the memory (RAM).

(2) The microcomputer, again under program control, uses the stored control parameters that it placed in memory to compute the control signals that it sends to the receiver circuits (1st LO Synthesizer, 2nd LO and BFO, and main IF/AF). These digital control signals are then sent to the receiver circuits through the receiver control assembly (A9) to generate the desired operation.

(3) Periodically, as established by the control program, the microcomputer reads the receiver status that it has stored in memory (RAM) and sends this information to control the front panel displays.

(4) When the microcomputer senses a BITE (Built In Test Equipment) request from the front panel switches, it is directed to perform the BITE test sequence and follows the BITE program which is also contained in memory. During BITE sequence, the processor disables all external and local controls.

NOTE

The receiver control program and the BITE program have been developed by the manufacturer as part of the receiver design and cannot be changed or updated by the customer for either operational control or maintenance.

f. During Remote operation, the Receiver is controlled by the microcomputer, but in place of instructions from the front panel, the instructions to the microprocesser are obtained from the remote controller:

(1) During the front panel scan, the microprocessor monitors the position of the LOCAL-REMOTE switch. When this switch is in REMOTE, the microprocessor will branch to the remote mode portion of the program so that instead of responding to front panel switches, it will look for command words from the remote interface card (A6A1).

(2) Commands from the remote controller are received by the Serial Asynchronous Interface Assembly A6A1. As each command is received, an interrupt is sent to the microcomputer which directs the microcomputer to branch to specific portions of the program (or subroutine) to carry out the command. After responding to the command instructions, the microcomputer returns to the normal remote mode program until a new set of commands or requests are received from the remote controller.

(3) When the remote controller contains data for receiver control (such as frequency, AGC, or mode selection) the microcomputer stores the data in memory (RAM), and on completion of remote data interrogation transfers the information to the receiver circuits.

(4) When the remote controller command contains a request for receiver status, the microprocessor accesses the corresponding receiver status information stored in memory (RAM) and sends it via the Serial Synchronous Interface Assembly (A6A1) to the Remote Controller.

(5) In addition, the microcomputer under program control periodically (every 25 ms) reads the receiver parameters from memory (RAM) and continually updates the front panel displays.

g. When a request is received from the remote controller during LOCAL operation, the microprocessor will respond and return the status of the receiver as described in the above paragraphs. Remote commands received during LOCAL operation will be stored in memory but they will not be acted upon unless the receiver is placed in REMOTE operation.

h. The microcomputer directs all operations and communicates with other receiver control circuits through its 8 bit bi-directional data bus and the write/read and clock (ROMC) lines. The ROMC lines indicate the type of instructions to be performed with the write and clock lines providing the necessary information. The 8-bit bus provides both bi-directional data and unidirectional address capability (to the receiver). The operating control program is contained in the program memory EPROM (Erasable Program Read Only Memory). Temporary storage for receiver settings and for data computations is provided by the working Random Access Memory (RAMs), which can be written into and read out of by the CPU. These memories are addressed by the CPU, through the static memory interface (SMI). The CPU sends the ROMC, write and clock signals to the SMI. The SMI recognizes the ROMC code calling for a Memory Address operation. The SMI, in sequence, addresses the EPROM or RAM over the memory address bus. Then it sends a read signal to the EPROM (if it is addressed) or sends a read or write signal to the RAM (if it is addressed). The CPU places the data to be read by the RAM on the data bus or reads the data placed on the data bus by the EPROM or RAM, as appropriate.

i. The microcomputer (A6A2) also contains the RESET and RAM data retention circuitry. The RESET circuitry generates reset signals when power is applied and turned off. This reset signal is applied to the CPU. When power comes on, the CPU initializes all circuitry to its starting condition and causes the program to start at its initial program address.

j. When power is removed, due to power turn-off or power failure, the reset signal to the CPU goes low. The CPU now causes the system to come to an orderly halt. In addition, the memory data retention circuitry (at power turn-off) connects an internal battery to the RAMs so that the receiver settings are retained in this memory. Thus, when power is reapplied, the receiver will be reset to its last operational condition when power was interrupted. Also, at power turn off, the memory retention circuitry places the RAM in a low power drain mode which retains memory but draws a minimal amount of power from the internal battery. When external power is applied, the internal battery is charged by the external power supply.

k. The CPU, in programmed sequence, receives and sends data from and to the front panel displays and controls, and the receiver control circuitry (through A9) via the CPU data bus. The data is directed between the CPU data bus and the receiver control and front panel circuitry, in the correct program sequence, by the bi-directional, tri-state switch. This switch is controlled by the strobe logic which is driven by the ROMC, write and clock signals from the CPU. The addressing of the various receiver and front panel circuitry, to accept or supply data from or to the data bus, in the prescribed program sequence, is done by the strobe logic and tri-state latched switch. This switch is driven by the CPU data bus and its outputs latched to the input data from the bus, at the prescribed program times, by the strobe logic.

l. The CPU receives and sends data from and to the remote controller via the Serial Asynchronous Interface (module A6A1). Data to and from the CPU and module A6A1 are sent directly over the CPU data bus. Additional control signals between the CPU and the module A6A1 are sent via the CPU I/O (input-output) ports. A UART (Universal Asynchronous Receiver Transmitter) in the A6A1 module interfaces the parallel 8-bit data word on the CPU bus to the serial data streams in and out from and to the remote controller. The UART also generates and sends to the CPU an interrupt request whenever the remote controller sends commands or data. This interrupt causes the microcomputer to orderly stop its present program and jump to a program routine which will service the remote controller commands and data. The UART and interrupt logic on the A6A1 module will supply the CPU with the interrupt routine starting address by placing this interrupt vector address on the CPU data bus when the CPU acknowledges that it will service the interrupt request. The reset signal from the microcomputer module is also sent to the interface module to initialize its circuitry at power turn-on.

m. As indicated in the block diagram, Figure 5-2, the front panel receiver control, module A9, connects to the keyboard switch panels 1 and 2. These switches are continually read, in program sequence, by the CPU. The switches are read in groups, with the switches being selected by enabling their associated data select buffers. The data select and strobes circuitry selects the buffers, in the programmed sequence, as directed by the strobe logic and tri-state latched switch outputs from the microcomputer A6A2. The read data goes on to the buffered data bus and then through the data buffers and the bi-directional, tri-state switch to the CPU bus. The digital outputs from the tuning knob encoder and digital data outputs from the IF/AF (A4 module) are also read out the same as the switch data.

n. Both the tuning mode and frequency indicating front panel Liquid Crystal Displays (LCD) are contained on module A9. These displays are continually updated by the microcomputer CPU. The displays are driven by decoder-drivers which are enabled by their respective data select and strobes. The data from the CPU bus is applied to this circuitry, at the correct times in the program sequence, through the data buffers and bi-directional tri-state switch.

o. The operating and tuning data developed by the microprocessor is relayed to the appropriate receiver circuitry through module A9. The buffered data bus goes directly to the main IF/AF module, A4, with the data select and strobes circuitry supplying the strobes to the various circuits in this module. Data to the 1st LO and 2nd LO/BFO modules are generated, in the proper program sequence, through the data select and strobes circuitry in the A9 module. Data to the 1st LO consist of a strobed and clocked serial data stream. The 2nd LO/BFO data consist of a binary coded digital word for the BFO frequency and an ON-OFF signal for the BFO. It should be noted that OOL (Out of Lock) signals from the 1st LO, REF and BFO drive the OOL indicators located on the A9 card. The OOL overall signal, generated by the microcomputer, is sent to the front panel OOL indicator through A9.

p. The serial asynchronous interface module, A6A1, in addition to the UART and interrupt circuitry described earlier, contains circuitry for selecting and generating serial data mode and baud rates and for setting the receiver address when the receiver is used in the remote mode.

5-7. **BUILT IN TEST EQUIPMENT (BITE).** The BITE system of the Receiver has the ability to perform two major functions. First, it determines, organizes and displays the bandwidth of the IF filters installed in the Receiver. This allows the installation of these filters in any slot, with minimum limitations. Secondly, the BITE performs tests of functionality of the receiver modules. These tests provide overall verification of the operation of the Receiver, and specific verification of the operation of selected modules.

a. The BITE system performs the following functional tests in the Receiver: Readability of the RAM in the microcomputer; lock condition and timing of all phase locked loops; settling time in the frequency synthesizers; operation of the IF AGC; operation of the ISB AGC detector if it is installed; and measuring the bandwidth of all of the IF filters. In order for the Receiver to pass the above tests, all modules must have been operating properly; except for the A1 Lowpass Filter, A6A1 Remote Interface, and the audio portions of A4 Main IF/AF and A5 ISB (if installed) which are not interrogated during the BITE sequence.

b. BITE may be controlled by the operator from the front panel through the simultaneous use of two controls, one on each keypad. This minimizes the likelihood of accidental interruption of an operating Receiver. To initiate BITE from the front panel, the operator must press both the LOCK and the AM pushbutton switches, then release AM and then LOCK for initialization. The microcomputer then begins the full BITE sequence. As the microcomputer is executing the BITE program, the front panel display indicates what the Receiver is actually doing. For instance, frequency, BFO and mode data are displayed. Should an error be discovered the front panel frequency display is blanked except for a two digit error code which contains the number of the test that failed. The operator writes down the number of the test that failed then pushes both LOCK and CW and then releases CW and then LOCK, which tells the microcomputer to continue to the next test. The displays are reinstated and the testing proceeds. The displays remain active throughout the tests since the process takes approximately one minute to complete, and if the displays are moving, the operator has confidence that the tests are proceeding. When the test is finished, the Receiver will return to the signal it was monitoring prior to being told to perform the BITE test sequence. Should the operator wish to terminate the BITE cycle at any time, he may press and hold LOCK and LSB then release LSB then LOCK and the Receiver will revert to its normal pretest operation at a point in the sequence where disabling the process is allowed. In addition to being able to originate the test, to continue the test, and to stop the test, there is (for maintenance purposes) a loop facility which can be invoked by using both LOCK and USB pushbuttons (refer to section 6 of this manual). In this mode, the front panel controls, with the exception of LOCK and USB, are disabled but the microcomputer will continuously supply the signals required to perform the failed test so that additional fault isolation procedures, using external test equipment, may be employed.

c. The BITE sequence may also be initiated by a remote device. The remote control device sends a message to the Receiver telling it to initiate BITE. BITE will then report up to a maximum of five errors and then report a test complete code upon request. If the test complete code is received with no fault numbers, then the receiver passed the BITE tests. The control device may send a message to the Receiver asking for the installed IF filter bandwidths. The Receiver would then send the measured bandwidths to the controller showing the filter slot positions in which each filter is installed.

d. During initialization, BITE is initiated if the microcomputer determines that the memory has been corrupted for some reason. This automatically initiated BITE will determine the receiver filter complement, organize a filter assignment table, and return the Receiver to operation. When performing this test, the Receiver does not stop on errors but completes the testing and restores receiver operation. The Receiver also does not stop on errors when BITE is initiated under remote control, but completes the sequence and stores the fault numbers for remote interrogation. The following discussion describes the actual tests conducted to verify the proper operation of each module.

(1) Microcomputer. All 256 bytes of the Random Access Memory (RAM) in the microcomputer are tested to ensure that the memory may be written into and read out of correctly. A ones and zeroes memory pattern is used to perform this test.

(2) Second Local Oscillator and BFO. The lock status of both the BFO and the second local oscillator synthesizers is tested. The second local oscillator synthesizer should be locked at all times. The BFO is enabled by placing the receiver in the CW mode. The BFO synthesizer is then tested for a lock condition both at 455 kHz and all 500 Hz steps between and including plus and minus 8 kHz offsets. This dynamic program also checks the switching times of the BFO synthesizer as indicated by the out-of-lock circuitry on the BFO board. A failure in any of these tests is indicated as an error code to the operator or to the remote controller, on request.

(3) First Local Oscillator. Testing of lock, in 500 kHz intervals from 29.999 MHz to 0 MHz, is performed, and the switching time of the synthesizer throughout the band is tested utilizing out-of-lock signals as the indication for reaching lock after each step.

(4) IF Module. The IF module (A4) is checked to determine whether or not the AGC circuits operate properly on signals. The test routine enables the CW detector and BFO, and checks that an audio output is present during the initial filter tests. The manual IF gain attenuation system is tested by observing its control effects on the audio output level during the filter tests.

(5) ISB Module. When the optional ISB board (A5) is installed it is checked for proper AGC action along with the IF gain and the manual IF gain control, in the same way that the main IF board (A4) was checked.

(6) IF Filters. One of the major functions of the BITE is to determine the bandwidths of the IF bandwidth filters installed in the Receiver, and assign them to bandwidth selection switches BW1 through BW5. The filters are assigned in order of increasing bandwidth and allow the operator to select a desired bandwidth. In addition, two different types of single-sideband detection filters may be used and the bandwidth determination routines verify their correct installation. Two sideband filters may be installed in the Receiver for independent or normal sideband operation, one for upper sideband, the other for lower. (When ISB is installed these two filters are required.) If one symmetrical sideband filter is to be used for both sidebands it may be installed in filter slot FL1. Then for lower or upper sideband, the first and second local oscillators are offset by 1.8 kHz to accommodate the symmetrical filter. There is one restriction on the filter complement in the Receiver; the FL1 slot must contain the filter to be used for lower sideband. It may be either the independent offset sideband filter or a symmetrical filter, but in either case it must be the filter used for lower sideband. The BITE bandwidth routine checks the filter in the FL1 slot to determine whether or not it is a center-tuned filter or an offset filter. If center tuned, it uses the filter for both sidebands by putting a 1.8 kHz offset in the first and second local oscillator. If it is an offset filter, the filter slot that the filter is in is labeled for the lower sideband and the rest of the filter complement is searched for the matching USB filter. If a symmetrical filter is found to be installed in the FL1 slot, the offset for the first and second local oscillators is set to 1.8 kHz; however, if an offset sideband filter is found with a symmetrical filter in FL1 slot an error

will occur. If there are less than 5 symmetrical filters installed in the remaining slots of the Receiver, the symmetrical filter in FL1 is used as a center tuned filter which may be used for the AM, FM, or CW detection mode. If five other filters are present in the system, the symmetrical sideband filter will be used only for sideband reception. The remaining filter slots, FL2 through FL7, are checked for presence of a filter, except for a slot which has previously been identified as the USB slot. If there is a filter present in a slot, its bandwidth is measured. The first LO is scanned, in frequency, from a 10 kHz maximum offset back to the 3 dB point, based on a previously measured center frequency reference level. (NOTE: This reference level can vary from filter to filter.) The frequency difference between the center referenced level and the 3 dB point is designated as half the actual bandwidth. Having measured the bandwidth of all of the filters installed, the filters are sorted in order of increasing bandwidth so that when the BW1 pushbutton switch on the front panel of the receiver is pressed, the narrowest bandwidth available is selected. When the BW2 pushbutton switch is pressed, the next narrowest progressing to the widest at BW5 (if there are less than 5 symmetrical filters installed in slots FL1-FL7 the widest one is assigned a number corresponding to the maximum number of symmetrical filters installed). Future filters which may have different bandwidths from the fifteen presently defined may be used in this system without any change. The bandwidths of the filters installed in the Receiver can be reported to the remote controller upon command. In the remote operating mode, if the remote controller asks for a specific bandwidth, the Receiver selects the bandwidth that is nearest to the bandwidth requested. The Receiver reports the actual bandwidth used to the remote controller. This is an indirect check on the filters.

5-8. POWER SUPPLY. The power supply provides the various dc voltages required throughout the Receiver. The unit, located on assembly A10, contains a step-down transformer, diode rectifiers, filter capacitors, regulators, and an alternate ½ amp 250v fuse. Primary input power is controlled through a POWER ON switch located on the front panel. This primary input power may be either 100,120, 220 or 240 Volts from 43 to 420 Hz. The proper voltage is selected through a card select switch located on the rear panel of the Receiver. A stepdown transformer provides three different voltages for rectification, filtering and regulation. Six different dc voltages are provided at the output of the power supply. These voltages are +20 Vdc regulated, +15 Vdc regulated, +15 Vdc unregulated, −15 Vdc regulated, +5 Vdc regulated and +5 Vdc unregulated.

SECTION II. FUNCTIONAL (DETAILED) OPERATION OF ELECTRONIC CIRCUITS

5-9. GENERAL. This section provides a detailed description of the functional operation of all electronic circuits contained in the Receiver. Refer to Figure 5-2 for an overall functional block diagram. Figure 5-1 lists the circuit card assemblies in the order that they are described in the following paragraphs. Simplified functional block diagrams along with timing diagrams are used throughout the text to aid in simplifying the description. Components referred to throughout the text are referenced by their last two reference designators; such as A4C6 is called out in the text as C6. Block diagrams referred to and included throughout the text should be used in conjunction with applicable schematic diagrams in Chapter 8.

5-10. RF LOWPASS FILTER, A1. The incoming RF signal is passed from the RF IN connector J1 to a 50 ohm, 4 section elliptical lowpass filter which has a cut-off frequency of 35 MHz (refer to schematic diagram, Figure 8-2). This filter provides the necessary protection to the Receiver from image signals at frequencies between 81.4 and 111.4 MHz; and from signals at the first intermediate frequency of 40.455 MHz. The filter also prevents first local oscillator reradiation from the antenna connection. Each section of filter consists of a tank circuit, consisting of a tunable coil (L1 through L4) and capacitor (C2, C4, C6 and C8), connected sequentially in the receiver line with a second capacitor (C1, C3, C5, C7 and C9) connected from each tank circuit parallel to the signal flow. Each tank circuit is tuned to provide a high resistance to a particular frequency while other frequencies are reflected in the parallel capacitor which in turn reflects this signal to the next stage and so on.

5-11. **FIRST MIXER, A2.** Figure 5-3 is a simplified block diagram of the first mixer module A2. It consists of a signal lowpass filter, first mixer, bandpass filter, first IF amplifier and drive amplifier with its associated filters. The function of this module is to convert the incoming RF signal to the first intermediate frequency of 40.455 MHz, by mixing with the first local oscillator frequency of 40.955 to 70.455 MHz. The schematic diagram for the first mixer is shown in Figure 8-3.

a. RF Signal Lowpass Filter and Mixer. The output of the A1 module is connected to the first mixer through a two section elliptical lowpass filter, (L15-C23, L11-C24-C25 and L12-C26-C27), which has a cut off frequency of 35 MHz and serves to present a defined impedance to the mixer, U1, RF input port. This filter operates much in the same manner as the RF input filter described under Paragraph 5-10 above, except the first input coil L15 is non-adjustable. It offers a very low impedance to the incoming wanted RF signal, but an increasingly higher impedance to frequencies above 29.999 MHz. The mixer, U1, is used for mixing both the incoming RF signal (0.5 to 29.999 MHz) and the first local oscillator signal (40.955 to 70.455 MHz). The resultant frequencies are taken from the mixer, and filtered to provide a difference frequency of 40.455 MHz to form the first IF signal.

b. First Local Oscillator Input Filter and Drive Amplifier. The filter for the incoming first local oscillator signal is comprised of four sections of a tunable coil, (L1 to L4) connected in series with a capacitor, (C2, C4, C6 and C8) and with the combination of the two connected parallel to signal flow. A second capacitor, (C1, C3, C5 and C7) connected in series with signal flow separates each coil-capacitor. Each coil is tuned for maximum impedance for a desired frequency. The series capacitance acts as a high impedance to undesired frequencies below 40 MHz. The output of this filter is coupled to a common emitter amplifier Q2 through capacitor C9 and resistor R3. The mixer drive amplifier is comprised of transistors Q1, Q2, Q3 and Q4. The local oscillator signal from the filter, which may be monitored at TP2, is coupled to the base of common emitter amplifier, Q2, whose current is regulated by transistor Q1. The voltage at the base of Q1 is set by divider R1 and R2 which in turn sets the potential at the emitter of Q1. Thus the current through R6 is regulated by bias control of Q2 via R6 and L6. The output of Q2 is capacitance-coupled (C21 and C22) to a complementary pair amplifier made up of PNP transistor Q3 and NPN transistor Q4. The output of this pair is applied directly to transformer T1 to drive the LO input to mixer U1. The mixer also receives the RF input from A1 as described above.

c. AGC Controlled IF Amplifier. The output of the mixer is coupled to a bandpass filter FL1. This crystal bandpass filter is designed to reject all the resultant mixer frequencies, except the difference frequency of 40.455 MHz with a bandwidth of 16 kHz. This 16 kHz bandwidth provides an additional option in the AM, FM or CW modes of operation. This first IF signal is coupled through C44 to an impedance matching network of L16, C32 and R14, and to a linear amplifier consisting of field effect transistor Q5. A dual tapped transformer T3, makes up part of the load circuit of Q5, to which is connected a current controlled AGC signal. This AGC signal, in effect, varies the impedance of the load transformer which in turn varies the gain of Q5. A second signal from the AGC circuit is applied to the gate of Q5 which varies its bias in relation to the AGC signal strength. This results in a high linear AGC controlled first IF signal, for output to the second mixer circuit card assembly A3.

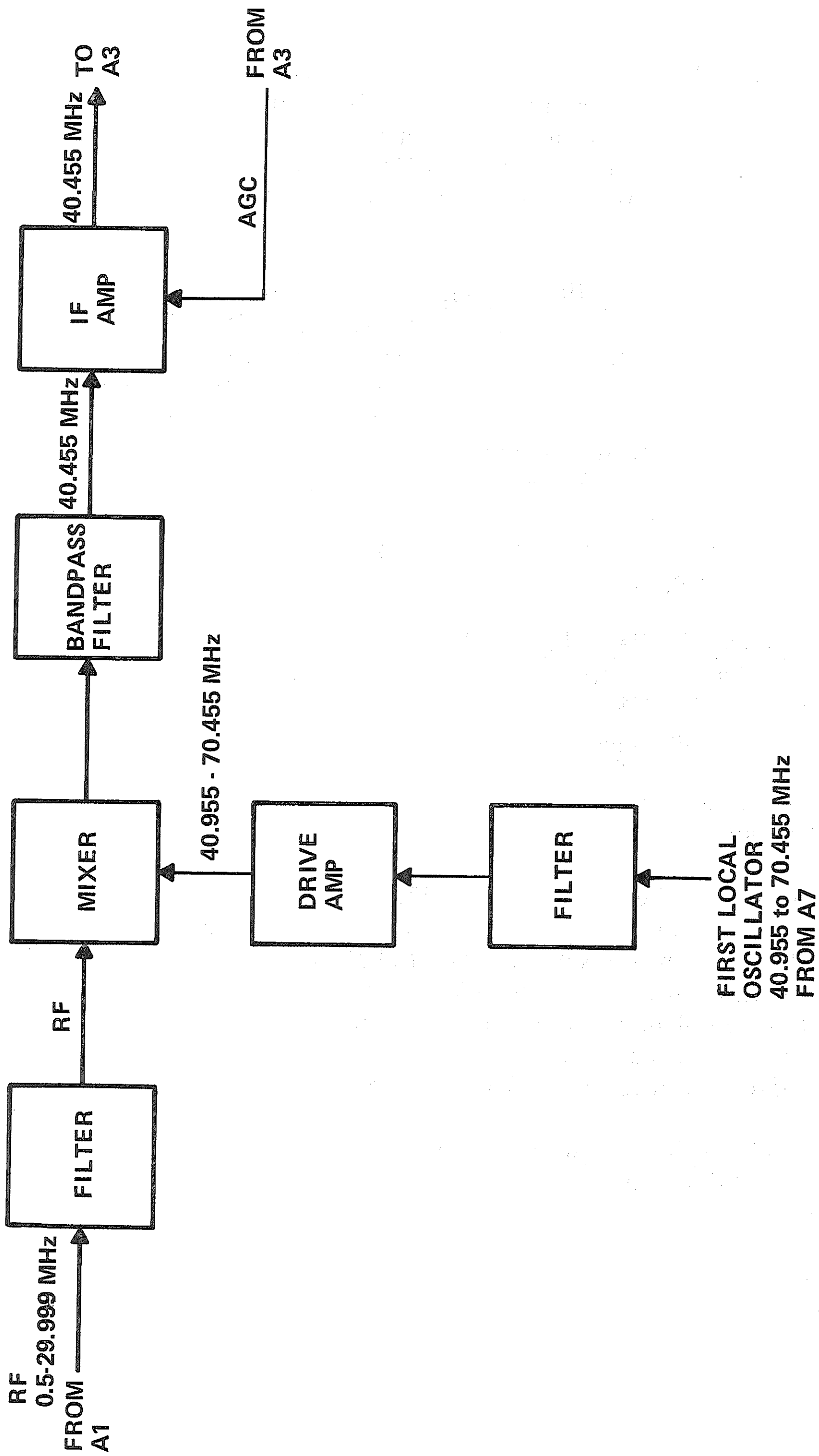


Figure 5-3. First Mixer, Functional Block Diagram

5-12. **SECOND MIXER, A3.** Figure 5-4 shows a simplified functional block diagram of the second mixer circuit card assembly A3. It consists of a three stage AGC controlled first IF amplifier, a bandpass filter, a mixer and output second IF amplifier. Input signals to the circuit card include; the first IF signal from A2, AGC signal from A4, and the second local oscillator signal from A8. The output signals consist of AGC output to A2 and the second IF signal to A4. Figure 8-4 shows the schematic diagram for the second mixer, A3.

a. First IF Amplifier. The first IF amplifier consists of three stages with the second stage gain controlled from the AGC signal. The third stage drives the signal for input to the bandpass filter. The 40.455 MHz signal routed from A2 is coupled to the drain of field effect transistor Q1, through capacitor C1. The grounded gate of this stage provides high gain for input to filter FL1 through capacitor C5. Filter FL1 provides for rejection of all frequencies other than the 40.455 IF signal. The output of the filter is connected through capacitor C6 to the drain of field effect transistor Q2, which also has a grounded gate. The load circuit of Q2 consists of resistors R16 and R18 and a dual tapped transformer T1. The AGC signal is connected to one tap of the transformer and, in effect, varies the impedance of the load transformer. This action varies the gain of the amplifier in relation to the AGC signal. The output of this stage is taken from the second tap on the transformer and coupled to the base of NPN transistor Q3, through capacitor C11 and resistor R20. A variable coil that forms part of the first section of a four section bandpass filter is connected into the load circuit of Q3. The output of Q3 is, therefore, reflected directly into the bandpass filter. A variable resistor R26 in the emitter circuit of Q3 provides for gain adjustment of this stage

b. Bandpass Filter, Mixer and Second IF Amplifier. The bandpass filter consists of four tunable tank circuits (C15-L5, C16-L6, C17-L7, and C18–C19–L8), each made up of a tunable coil and a capacitor. Each stage is tuned to resonate at the first IF signal frequency and reflects its output to the next section for finer tuning and so on. The output of this filter is coupled directly to the input of integrated circuit mixer U3. A 40 MHz signal from the second local oscillator is connected to a second input of the same mixer. A difference frequency of 455 kHz between the 40 MHz and the 40.455 MHz IF signal results in the mixer. It is this difference frequency that is used as the carrier for the second IF signal. All other frequencies are rejected through the filter consisting of capacitors C31 and C32 and coil L9. The output of the mixer, U3, is connected to a tapped load transformer T2. The output is taken from that transformer tap and coupled through C24 and the filter, just described, to an integrated amplifier U4. This stage provides amplification for the second IF signal output from A3.

c. AGC Amplifier. A two section AGC amplifier is contained on circuit card assembly A3 which provides for both voltage and current control of a signal from AGC circuits on A4. This controlled AGC signal is applied to two IF signal stages for level control. One of the IF stages controlled is located on circuit card assembly A2 and described in paragraph 5-11c. The second AGC controlled IF amplifier is on A3 and is described in Paragraph 5-12a. An AGC signal from the AGC circuit on A4 is routed through resistor R2 to two separate amplifiers. The first amplifier is a two stage feedback amplifier consisting of integrated operational amplifiers U2B and U2C. The highly regulated output of this amplifier is routed to circuit card assembly A2 and used as the bias control to the gate of that output IF amplifier. The same AGC signal through resistor R2 is routed to an integrated operational amplifier U2A. This amplifier has both its negative and positive inputs regulated through voltage regulating transistors U1A (positive) and U1B (negative). The action of these transistors control the bias voltage to the operational amplifier which in turn controls its output current flow. The output of this amplifier stage is then coupled to transistor U1C which amplifies the signal and applies it to the IF amplifier through resistor R19 and diode CR1. The diode prevents IF signal feedback to the amplifier. This signal then controls the gain of that IF amplifier in relation to the AGC signal from A4. The output of the operational amplifier U2A is also coupled to the base of transistor U1D which buffers the signal for application to the IF amplifier stage on A2.

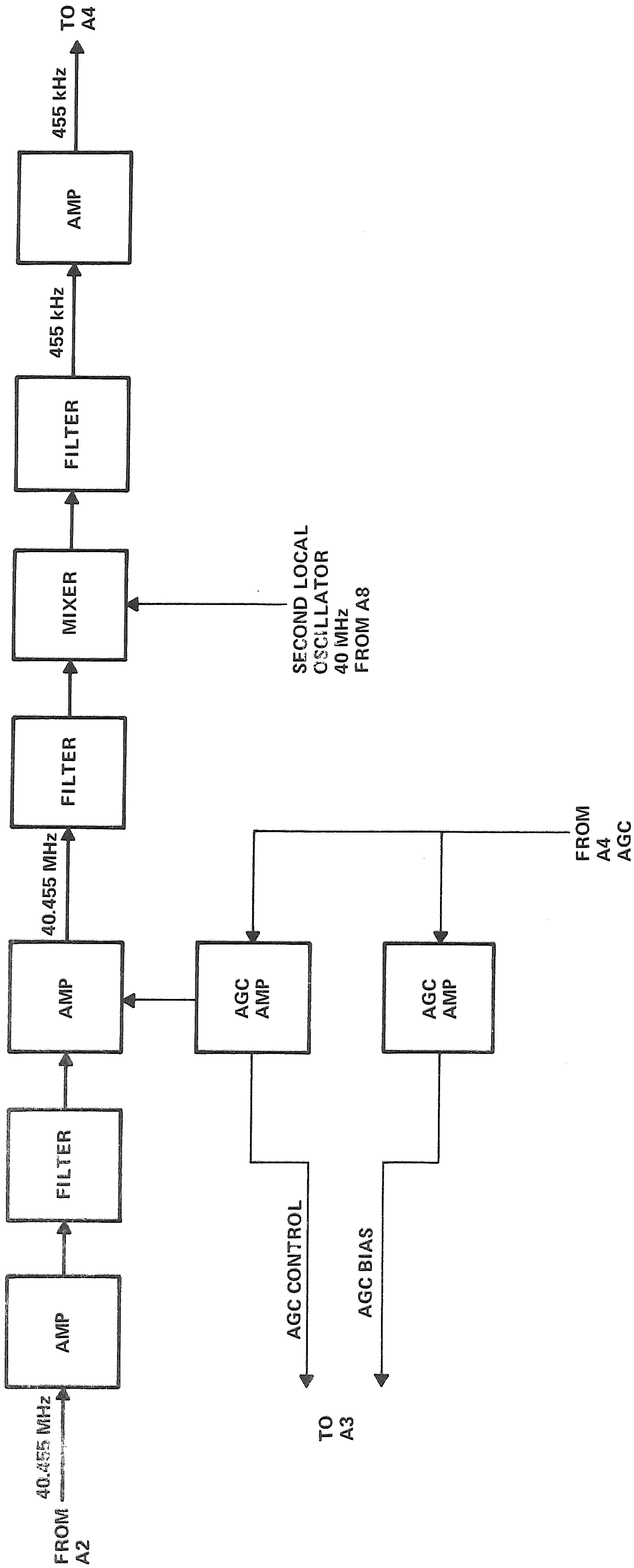


Figure 5-4. Second Mixer, Functional Block Diagram

5-13. MAIN IF/AF, A4. The Main IF/AF circuit card assembly A4 contains IF circuits, AF circuits, and AGC circuits. The description of these circuits are divided into those three basic functions and shown in three separate simplified block diagrams in Figures 5-5, 5-6, and 5-7. Receiver control circuits are also contained on A4 and are described under the A9 circuit card. Input signals to the circuit card include: the second IF signal from A3, the BFO signal from A8, audio and AGC signals from A5 and control signals from A9. Output signals from the board include: second IF signal to A5, BFO, audio and AGC signals to A5, audio signals to A9 and to the rear panel, AGC signals to A3, and control signals to A9. The schematic diagram for the A4 circuit card is shown in Figure 8-5.

a. IF Circuits. Figure 5-5 shows a functional block diagram of the IF circuitry as it functions on circuit card assembly A4. This circuitry consists of the plug in bandpass filters, their switching circuitry, a four stage IF amplifier, an IF output amplifier, an RF switch, a limiting amplifier and FM detector, and a product and synchronous AM detector. The second IF signal routed from A3 is connected directly to seven 455 kHz bandpass filter sockets FL1-FL7. These sockets provide for plugging in any number, up to seven, of preselected filters of various bandwidths. These filters optionally available in bandwidths from 0.4 kHz to 16 kHz, may be changed anytime at the customer's discretion (refer to Chapter 4). Selection of a particular installed filter is then accomplished automatically through the receiver control system. Each filter socket is connected to a diode switch which is controlled from the receiver control circuits. The output of the diode switch for filter FL1 must be linked to the common output of all the other filter switches, if it is used in A4 operation. If it is to be used for the ISB operation, then it must be linked to the output for that circuit card assembly A5. The receiver control is programmed to select and switch into the circuit the filters in ascending order of bandwidths, regardless of the order in which they are plugged into the sockets; that is, when BW1 is selected, from receiver control, the narrowest bandwidth contained in the seven sockets (six if ISB is installed) will automatically be selected. BW2 will select the next widest bandwidth and so on with BW5 selecting the widest bandwidth. Two filters are generally reserved for USB and LSB operation, which are also selected automatically when those modes of operation are called for through receiver control.

(1) The common output of the diode switch which consists of CR1 through CR14, R9 through R22 and C21 through C27, is connected through resistor R25 to the base of transistor Q1. This emitter follower stage acts as a buffer between the diode switch and the input to a two stage IF amplifier U8 with AGC control. An incoming AGC signal is applied to each stage of the integrated circuit amplifier and provides for level control of the IF signal. A variable resistor R39 connected between the output of the first stage and the input of the second stage provides for manual adjustment of the gain of the IF signal. Variable resistor R47 is used for adjusting the AGC signal level. The output of the two stage IF amplifier is connected to a filter consisting of capacitors C44, C46 and C47, resistor R50 and tunable coils L1 and L2. This double tank circuit provides for rejecting unwanted spurious signals. The output of the filter is routed through capacitor C49 to two separate functions; a three stage IF output amplifier and an emitter follower amplifier Q6. The first stage, Q7, of the IF amplifier is an emitter follower which provides buffering between the incoming signal and the second stage Q8. This second stage amplifies the signal and connects it to still another emitter follower stage Q9 for buffering to the IF OUT connector J2, located on the rear panel.

(2) The emitter follower amplifier Q6 acts as a buffer in the same manner as Q7 above but its output is routed to three separate functions; the AGC detector circuit, the product detector and the FM detector through the RF switch. The signal routed to the AGC detector is described in paragraph c under AGC control circuits. The IF signal routed to the FM detector U18 through the RF switch CR22-CR25 is operated by receiver control. Receiver control directs the switch to connect the IF signal to the detector in the AM and FM modes only. In all other modes of operation, the RF switch connects the BFO signal to the FM detector U18. The IF signal

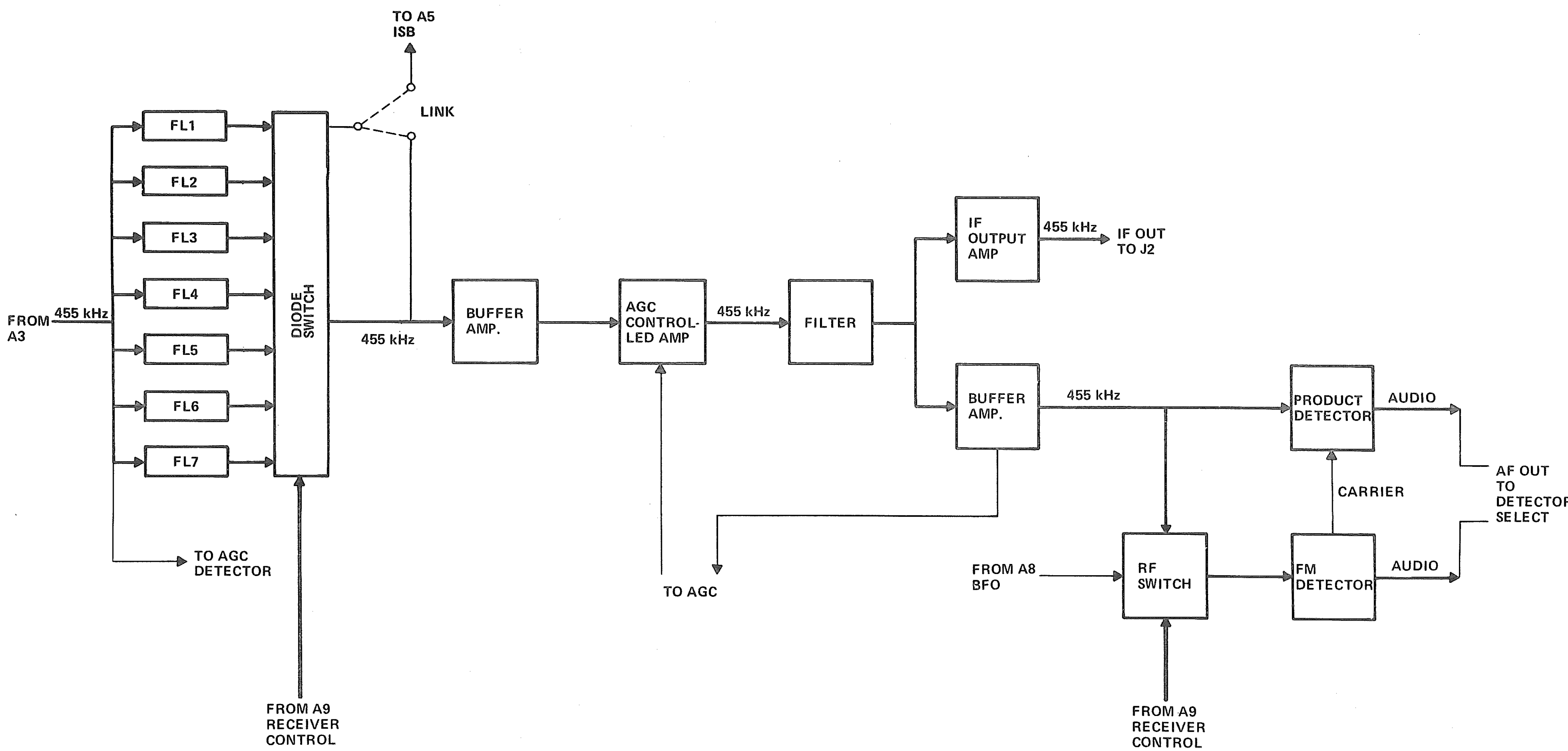


Figure 5-5. A4 IF Circuits, Functional Block Diagram

routed to the product detector is connected to its signal port. All signals applied to the FM detector; AM, FM or BFO are connected to a limiting amplifier which removes modulation from the AM carrier and passes it or BFO through the output carrier of the FM detector to the carrier input of the product detector. In the FM mode the signal is detected, its carrier rejected, and an audio signal, from the detector audio output, is connected to the detector select switch. This switch, an integrated circuit transistor gate U19A will select the detected FM audio, only in the FM mode, as directed by receiver control. In all modes except FM, a carrier frequency (AM or BFO) is applied to the carrier input of the product detector. In all modes of operation the signal selected, through receiver control, appears on the signal input of the detector. The detector removes the carrier and routes the audio, through its output, to the detector select switch U19A described above. Receiver control directs this switch to select that audio in all modes except FM.

b. AF Circuits. Figure 5-6 shows a functional block diagram of the audio circuits contained on circuit card assembly A4. This circuit consists of an audio lowpass filter stage, a crosspoint switch, two attenuators and two output amplifiers. The audio signal from detector select U19A is connected, through capacitor C85, to a lowpass filter and amplifier U28. The filter rejects any unwanted frequencies above the audio frequency that might have passed through the detector. The amplifier U28 operates in two different modes. In the AM and FM modes transistor switch U19B disconnects capacitor C113 from the circuit while in all other modes the capacitor is connected across R128 effectively shunting this resistor; thus reducing the signal level in these modes. The output of amplifier U28 is connected to an audio crosspoint switch U25. This switch, through Receiver control, controls audio switching from A4 circuits described above and from the optional A5 circuit card when installed. In non ISB modes the switch routes the A4 signal to the AF GAIN input and to variable attenuator U30. The signal through the AF GAIN control is coupled through capacitor C96 to an audio output amplifier U26. The output of this amplifier is coupled through C108 to AF OUT connector J3 on the rear panel and to the PHONES jack on the front panel. The signal through variable attentuator U30 is routed to connector J8 for output to the ISB circuit card and is also routed back to the crosspoint switch. The switch, in this non ISB mode, connects the attenuated signal through capacitor C95 to a second audio output amplifier on integrated circuit U26. This amplifier drives transformer T1 through C107 and is coupled to the Monitor Line output on connector J3 on the rear panel. The variable attenuator is controlled through screwdriver adjust MAINLINE LEVEL located on the front panel and provides level control of the main (A4) signal to the Monitor Line output in the non ISB mode.

(1) In the ISB mode either main (USB) or ISB (LSB) is selected and routed to the same circuits described in non ISB mode. In addition, the crosspoint switch couples both the USB and LSB through variable attenuators to their respective amplifiers on the ISB circuit card. The USB is routed through attenuator U30 and controls the signal as described in non ISB mode. The LSB signal is routed through attenuator U31 to J8 and back to the crosspoint switch in the same manner as USB. Attenuator U31 is controlled through screwdriver adjust I-LSB LINE LEVEL located on the front panel and provides level control of the LSB (A5) audio signal. The LSB and USB are routed through connector J8 to their respective amplifiers on circuit card A5 and returns through circuit card A4 to Line 1 Output (USB) and Line 2 output (LSB) on AF OUT Connector J3 on the rear panel.

(2) Two audio signals are routed to the AF metering circuit contained on circuit card A4. One signal is tapped from the AF GAIN control input and the second signal from the monitor output amplifier. These two signals are connected to transistor gate U19C which selects between the two signals on direction from receiver control. In all modes except BITE the signal from the monitor output amplifier is selected and routed to the AF metering circuit. This circuit is described under AGC circuits.

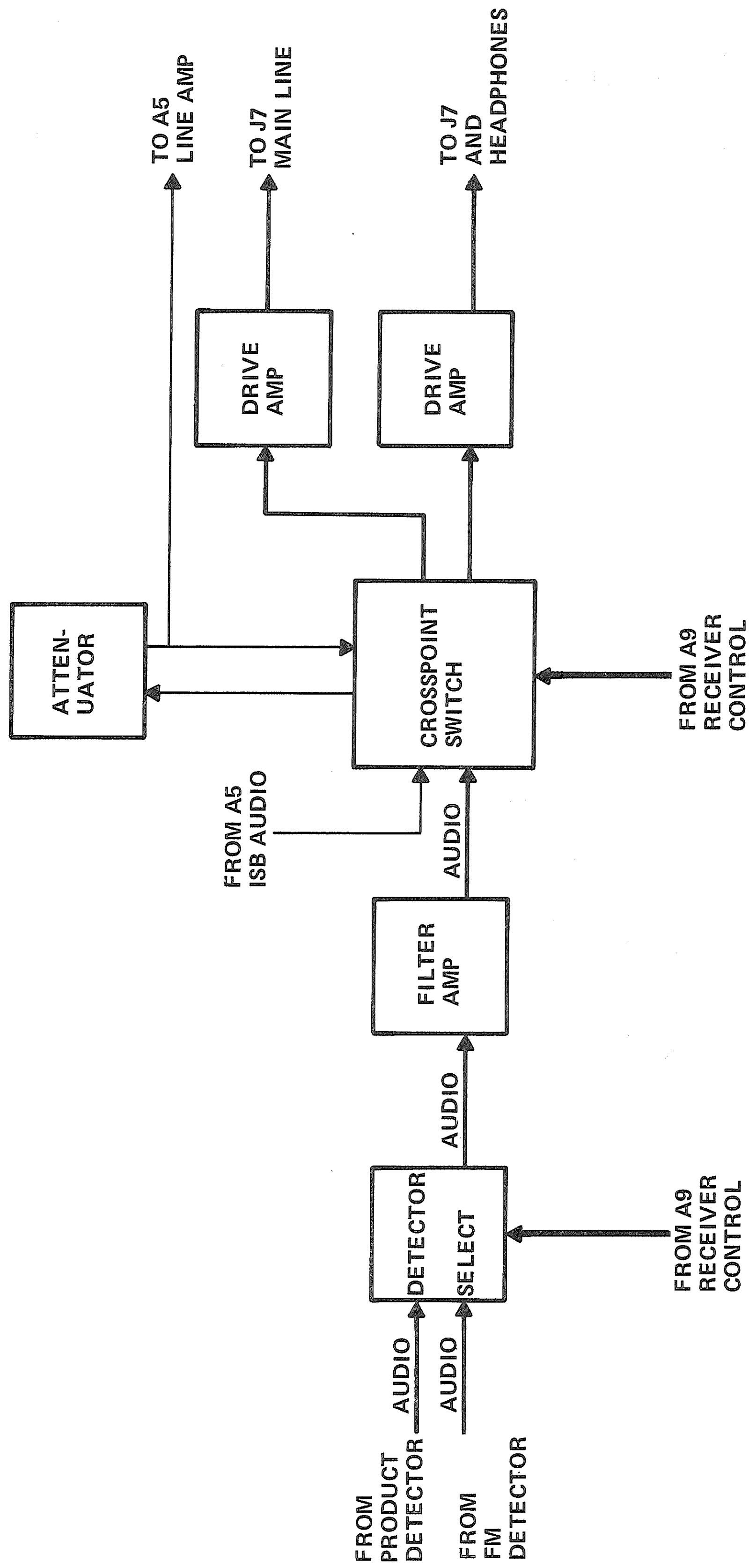


Figure 5-6. A4 AF Circuits Functional Block Diagram

c. AGC Control Circuits. Figure 5-7 illustrates a functional block diagram of the AGC circuitry contained on circuit card assembly A4. The circuits consist of an AGC detector, AGC decay, peak signal detector, decay time constants, an integrator, filter, a gain control distribution amplifier, a digital to analog converter and various electronic switches controlled from the receiver control circuits. The description also includes the AF/RF meter comparator circuit.

(1) The AGC circuitry is designed to provide three modes or techniques for controlling the gain of the Receiver; Manual, Automatic and Automatic with a selectable threshold. In the automatic mode the level of the IF amplifier U8 is controlled automatically with three selectable decay times; SHORT, MEDIUM and LONG. In the manual mode the IF GAIN control is used to control the level of the AGC signal applied to the IF amplifier U8. The IF GAIN control is used to select the threshold in the automatic with selectable threshold mode. The same decay times as in automatic are selectable in this mode.

(2) An IF signal taken from IF emitter follower Q6 is coupled through capacitor C31 to U10A for detection. The three transistor array U10 acts as a detector to the IF signal with U10C connected as an emitter follower for buffering the DC signal to two circuits; AGC decay and peak signal amplifier. Peak signal amplifier U7C couples the signal, across a decay time select circuit, to integrator amplifier U14A. The signal routed to the hang circuit which consists of amplifier U7A and U7B is time controlled through capacitor C42, resistors R45 and R146 and transistors Q2 and Q10. When short time decay is selected, Receiver control turns on transistor Q2 and transistor gate U12A. Capacitor C42 is shorted to ground through transistor Q2 which turns on transistor U10D and a short delay is asserted using combination resistors R52 and R55. When medium time decay is selected transistor Q10 and transistor gate U11A is asserted. Capacitor C42 discharges through the parallel resistance of R45 and R146 providing a short hang time, after which U10 is turned on and a medium delay is asserted through R52 and R53. When long time decay is selected capacitor C42 discharges through R45 providing a long hang time, after which U10 is turned on, decay time is through R52.

(3) The AGC applied to integrator amplifier U14A is mixed with signals from diversity AGC through amplifier U14B and gain control or threshold from amplifier U14C when AGC mode dictates. In the manual mode both transistor gates U11C and U12B are enabled through receiver control and the gain control voltage is asserted directly to the input of U14A. In the manual with automatic threshold mode U12B is turned off and the voltage from the IF GAIN control asserts itself through diode CR20 only when that level is higher than the AGC signal at the input of U14A. The digital to analog converter is coupled through U11D and is used to insert threshold level from a remote location through receiver control. Diversity AGC applied through transistor gate U11C to the input of U14C and to amplifier U14B influences the AGC signal only when its level is higher. When AGC dump is enabled (during certain BITE modes and local/remote operations that require dumping of AGC), receiver control enables flip flop U9A which turns on transistor U10E. This rapidly discharges capacitor C52 thereby preventing U14A from acting as an integrator.

(4) The integrator amplifier is coupled to AGC filtering; consisting of capacitor C59, resistors R76, R77, R81 and R83, diode CR21 and amplifier U17A. If AGC dump is asserted (in certain BITE modes) transistor gate U12D is turned on providing a much faster charge path for C59 through resistor R78. The output of the filter amplifier U17A is coupled to amplifier U17B. This amplifier provides the AGC signal to IF amplifier U8. At the same time U17B provides one input to A3 AGC drive amplifier U17D through diode CR26. If ISB is installed and enabled a second AGC signal from that circuit card is coupled to U17D through diode CR27. The two diodes bias the strongest of the two signals to the input of U17D. The output of this amplifier is coupled through J2 to AGC circuits on circuit card assembly A3.

(5) An AF/RF meter comparator circuit is contained on circuit card assembly A4. This circuit monitors the main RF, the ISB RF and the AF that may be input from either the main or the ISB signal. The circuits consist mainly of comparator amplifiers U24A (AF), U24B (ISB-RF)

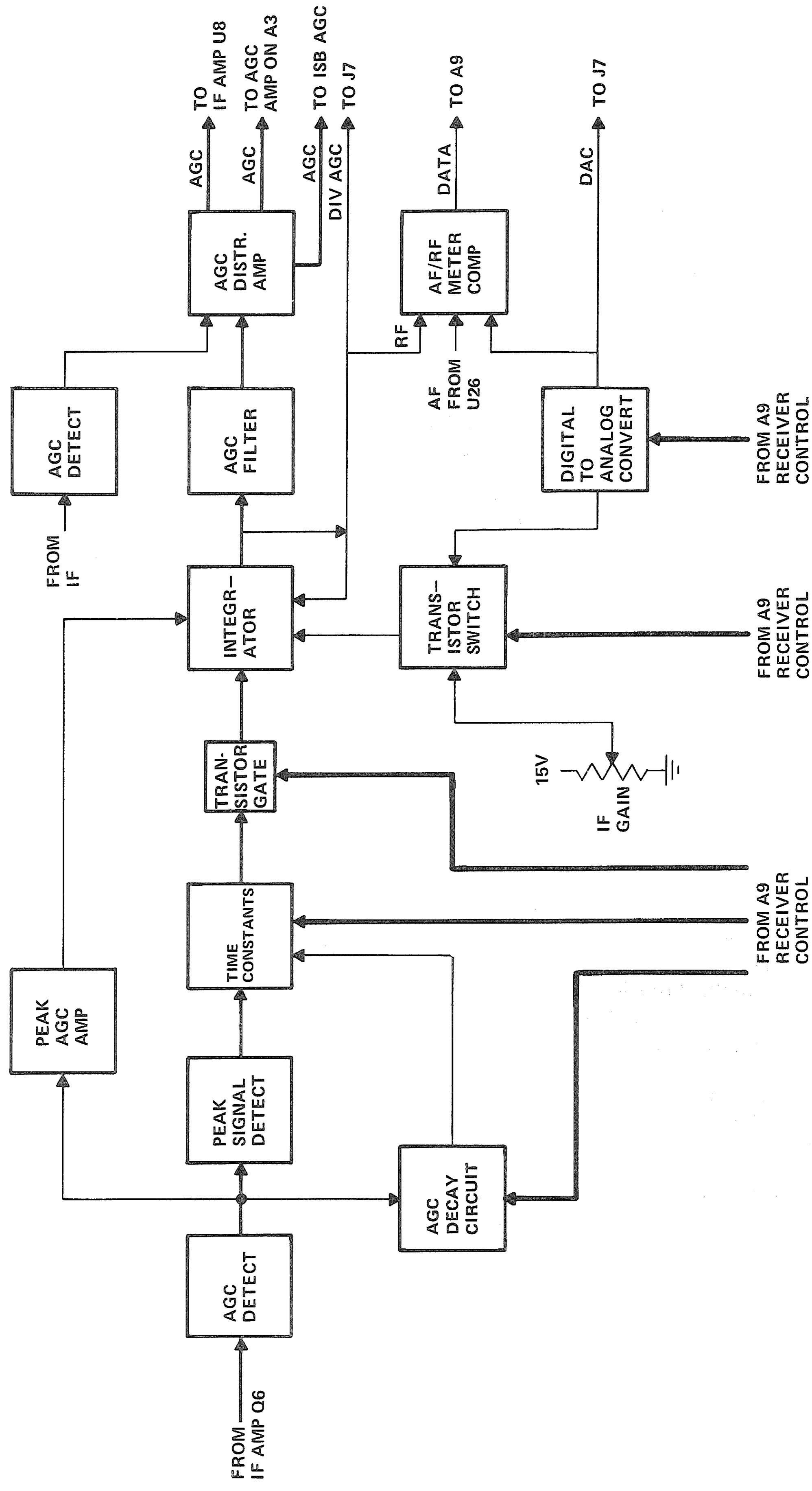


Figure 5-7. A4 AGC Circuits Functional Block Diagram

and U24C (main-RF). All three amplifiers operate in the same manner with their negative inputs accepting the AF or RF reference while the positive input is referenced from the digital-to-analog converter U21. The output of each amplifier is output through connector J2 to receiver control. From this information, the microprocessor adjusts the input to U21 which in turn adjusts the converter signal to the AGC in all modes except manual. The output of the three comparators are also processed to the front panel meter readout where the RF or AF signal level can be monitored.

5-14. **INDEPENDENT SIDEBAND (ISB), A5.** The Independent Sideband (ISB) circuit card assembly A5 contains IF circuits, AF circuits and AGC circuits. The description of these basic circuits are divided into those three basic functions and shown in two separate functional block diagrams in Figures 5-7 and 5-8. Input signals to the circuit card include; IF signal, BFO signal, AGC, and audio signals from A4. Output signals include; AGC and audio to A4, and AGC and audio to AF OUT-J3 on the rear panel, but through circuit card assembly A4. The ISB circuit card assembly schematic diagram is shown in Figure 8-6

a. IF Circuits. Figure 5-8 shows a functional block diagram of the IF circuitry as it functions on circuit card assembly A5 along with the AF function. This circuitry consists of a four stage IF amplifier, a BFO amplifier, a product detector, an audio amplifier, two audio line drive amplifiers, and AGC circuits. The IF signal is routed from bandpass filter FL1 by the filter selection switch, located on circuit card assembly A4 to the IF amplifier on A5. This filter is selected in the ISB mode of operation, so that an IF signal is routed to A5 only in that mode. The IF amplifier is identical to the one located on A4 and is described in Paragraph 5-13a. The IF signal from the AGC controlled IF amplifier is routed both to the AGC circuits and to the signal input port of a product detector U11. A BFO signal from A4 is applied to the base of transistor Q7 through capacitor C30, amplified and applied to the carrier input port of the same detector. The detector removes the carrier and applies, through its audio output port, the audio signal, through capacitor C43, to an audio amplifier.

b. AF Circuits. Figure 5-8 shows a functional block diagram of the AF circuitry, along with the IF circuits, as they function on circuit card assembly A5. This circuitry consists of an audio amplifier and two audio line driver amplifiers. The audio signal, as received from the product detector, is connected, through capacitor C43 and resistors R78 and R79, to the base of emitter follower amplifier Q8. The output of this amplifier is then routed to circuit card assembly A4. Refer to Paragraph 5-13b for a description of the ISB audio on A4. The attenuated audio signal is routed back to A5 and applied to the input of one line driver amplifier integrated in U12. The output of this amplifier drives transformer T2 with a center tapped 600 ohm output. This output is routed to AF OUT-J3 on the rear panel. The main audio signal from the A4 audio is connected to the second amplifier U12 and processed in the same manner as the ISB audio except through transformer T1.

c. AGC Circuits. Figure 5-7 shows a functional block diagram of the AGC circuits for circuit card assembly A4. These circuits are identical to ISB AGC circuits and are described in Paragraph 5-13c.

5-15. **FIRST LOCAL OSCILLATOR SYNTHESIZER, A7.** The first local oscillator synthesizer circuit card assembly A7 contains circuits to produce the first oscillator frequency of 40.955 to 70.454999 MHz for the first mixer which in turn produces the first IF signal of 40.455 MHz. The description of this circuitry is divided into three basic groups; operation of phase lock loops, the digital control circuitry and the oscillator control circuitry. Figures 5-9 through 5-11 respectively, show simplified block diagrams of the three basic circuit divisions. Input signals to the circuit card assembly include receiver control and a 1 MHz reference frequency. The only output signal from the assembly is the 40.955 to 70.454999 MHz oscillator signal.

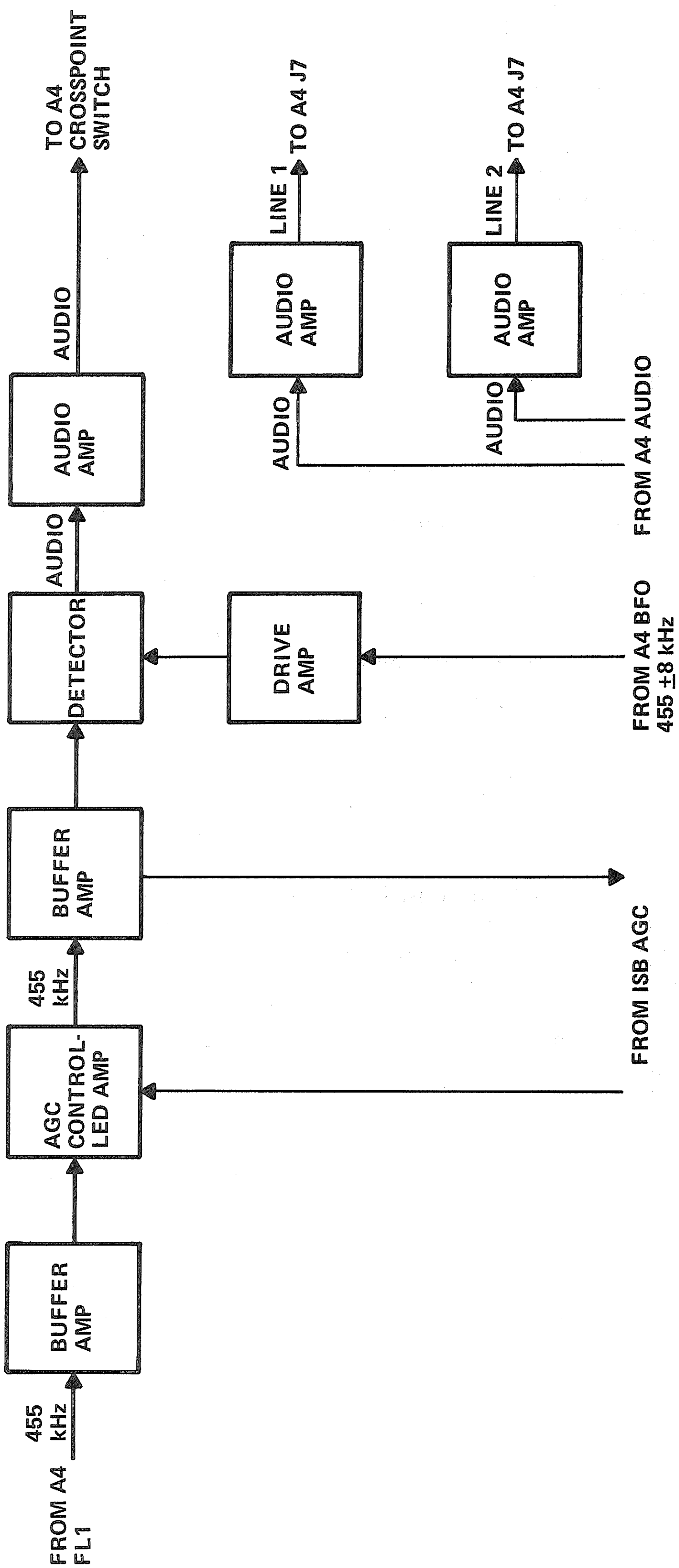
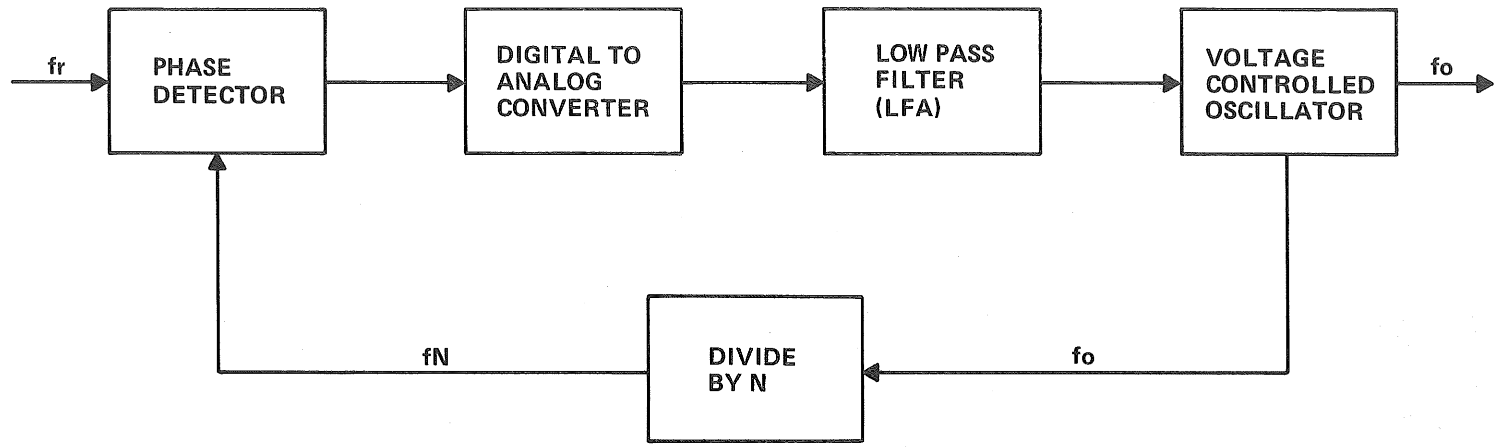


Figure 5-8. ISB Functional Block Diagram

a. Operation of Phase Lock Loops. A basic phase lock loop consists of essentially four main blocks. These are shown in Figure 5-9 and are a Voltage Controlled Oscillator (VCO), a divider capable of dividing the output of the VCO by an integer number (÷N), a phase detector (Ø), digital-to-analog converter and a Loop Filter Amplifier (LFA). a phase lock loop configured in this manner is capable of locking to the incoming reference frequency (F ref). This is derived from the fundamental formula for this type of loop which is Fo=F ref x N; therefore, to vary the main VCO Frequency (Fo) either Freq or N would have to be changed. Most loops perform frequency change by modification of N, the integer divide ratio. It is noted, however, that this type of simple single loop can only vary in frequency steps as small as the reference frequency (Fref). However, it is assumed that a system is possible whereby the main oscillator (Fo) frequency can effectively divide a fractional number, then it is possible to achieve a much finer resolution given the same higher frequency reference. Assume that Fo is 50.123467 MHz and the reference frequency is 100 kHz, then using the above formula the result is with n as the ratio, a non-integer number: 50.123467=0.1 x n; therefore, n=501.23467. If we split this number into its integer part and its decimal part, the result is a three decade integer and a five decade decimal number. Generating the non-integer part as an actual frequency is done by considering a portion of the frequency spectrum of interest between 50.1 MHz and 50.2 MHz where this finally generated frequency will occur. Thus, it is possible to generate any signal between these two frequencies by an averaging technique, that is to say (see Figure 5-11) if the signal at 50.2 MHz is sampled, 23,467 times and the signal at 50.1 MHz, 76,533 (100,000-23,467) times then the average or apparent signal produced by this sampling would occur at the frequency of interest at 50.123467 MHz. This type of sampling produces a large number of sampling sidebands on the main output frequency. These can be removed, however, by producing a signal equal and opposite to these predictable sidebands and adding this to the oscillator control signal and effectively nullifying the production of these sidebands.

(1) In the synthesizer, the circuits can be split in two; for the operating analysis, those circuits involved in the generation of the digital signals to control the generation of the 5-decade decimal part of the divide ratio number (n) which in turn controls the sampling technique and the signal to sum with the oscillator control signal, and those circuits including an oscillator, 3-decade integer divider, phase detector, summing amplifier and lowpass filter making up the components of a simple phase lock loop. These two parts in further discussions will be referred to as the digital control and the oscillator control circuitry. A separate section is included for auxillary circuitry which is provided to produce large frequency step control and out-of-lock indications for the receiver.

b. Digital Control. Figure 5-10 illustrates a simplified block diagram of the digital control circuitry. The circuitry associated with the time control, the incoming 1 MHz reference signal from A7J2, is used as the clock for accumulator and registers through the NOR gate U4D which drives U20, U21 and U22, and is routed directly to U3, U5 and U18. The Hex D flip-flops U3 and U5 with U1A and U1B provide a 10-level, ring counter. This counter is used to provide timed pulses to clock the accumulator from first accumulation to second accumulation and sequentially clock out the data in the latches U8 through U12 to the full adder U15. Flip-flop U3 provides a pulse 1 clock pulse wide but delayed 5 pulses from DØ the input, to Q1 the output. The output at U3Q4 is connected to the input DØ of U5. U5 also provides 1 clock pulse wide pulses but each output QØ through Q4 is used to drive the incoming data latches. U4A and U4B convert the narrow pulses from U3 QØ and U5 QØ into a 50% duty cycle square wave with a period of 10 clock pulses (each half cycle 5 clock pulses long). The 180^{o} out-of-phase outputs at U4A pin 1 and U4B pin 4 provide control to U2A, U22, U19A and U19B to ensure that these devices are enabled during the correct half cycle. The 100 kHz reference for the reference side of the phase comparator is taken from U5 output Q4. U5 output QØ is provided to U4C via U7C to reclock the CARRY IN to U15 and also to U6 to provide the clock for alignment of signals out of the HEX D flip-flop U6.



NOTE:
FOR NORMAL OPERATION
fo = fr x N
WHERE:
fo = OSCILLATOR FREQUENCY
fr = REFERENCE FREQUENCY
N = DIVIDE BY NUMBER

Figure 5-9. Typical Phase Lock Loop Functional Block Diagram.

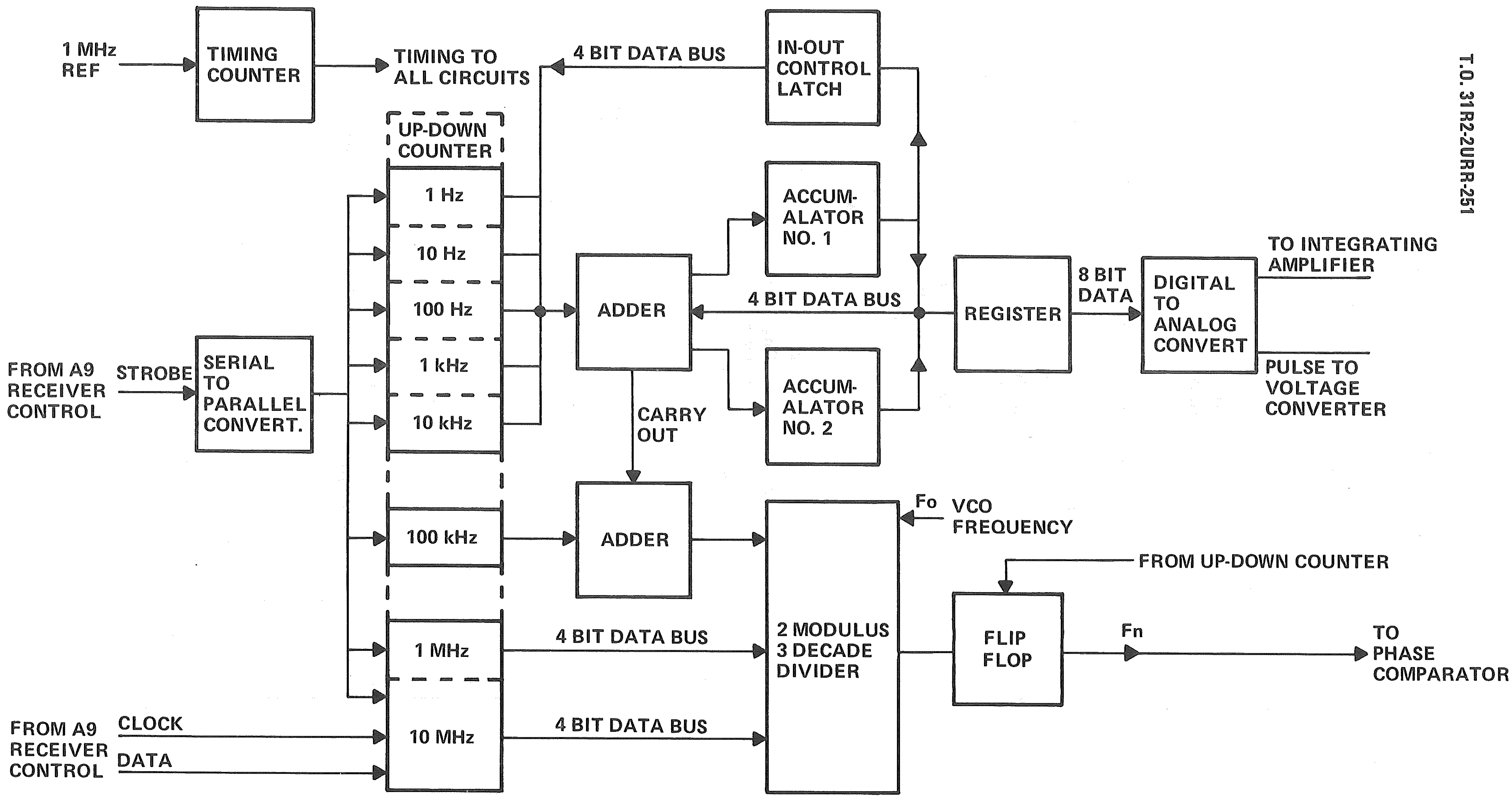
(1) Serial-to-Parallel Conversion. The incoming serial data stream from the A9 receiver control assembly consists of DATA, CLOCK and STROBE signals. The strobe is routed to U6 input D1 where its output is reclocked. This output at U6 Q1 is fed back to D2 and its output Q2 provides a strobe input to U13 and U14 one clock pulse delayed. The incoming CLOCK is fed to U14 through U8 in parallel. The serial DATA is fed first into U14 which from its output on U14 pin 10 to U12 and U13 shift registers. The output from U12 at pin 10 is fed to U10 and U11, and so on to U9 and U8 to complete the data load and forming the serial-to-parallel conversion of synthesizer data into the data registers. The data registers U8 through U14 hold the data for the synthesizer frequency, the U8 register holding the 4-bit BCD data for the 1 Hz digit and each register the next decade so the U9 register holds the 10 Hz data and so on to the U14 register which holds the 1 MHz and 10 MHz data.

(a) If the front panel RF frequency is set to 10.426800 MHz then the actual loaded data is 39.255 MHz above this frequency which is 49.680800. The first IF frequency is 40.455 MHz so we can see that a further offset of 1.2 MHz less than the main LO frequency of 50.881800 is introduced by the microcomputer into the serial data stream sent to A7. This is accounted for in the actual mathematical process in the first and second accumulator circuitry, which replaces this offset before generating the final VCO control voltage to the Local Oscillator.

(2) Accumulator operation. The data loaded into the registers U8 through U12 is fed in 4 parallel boards under control of the ring counter U5 during the first half cycle of the tuning as discussed in the tuning section to the Full NBCD Adder U15. As the accumulation proceeds, the accumulating sum is passed from the sum outputs of U15 to the 4-bit wide latch U18. The Carry Out signal from U15 is stored in U18 and is clocked out to U7A and then under control of U7C from the tuning circuits through U4C back into the Carry-In port of U15 deriving the first accumulation the outputs from U18 will be propagated through into the 4 stage shift registers contained in U20 and U21. U20 and U21 are 18 stage registers divided each into 2 four stage registers and 2 five stage registers. The four outputs from U18 are fed into the 4-stage registers in each half of each of U20 and U21 and then the output of these 4-stage registers is fed back to the 5-stage register in each half of U20 and U21. At the end of the first accumulation the data at the output of the 4-stage register appears at the input to the tri-state 4-bit buffer U2A.

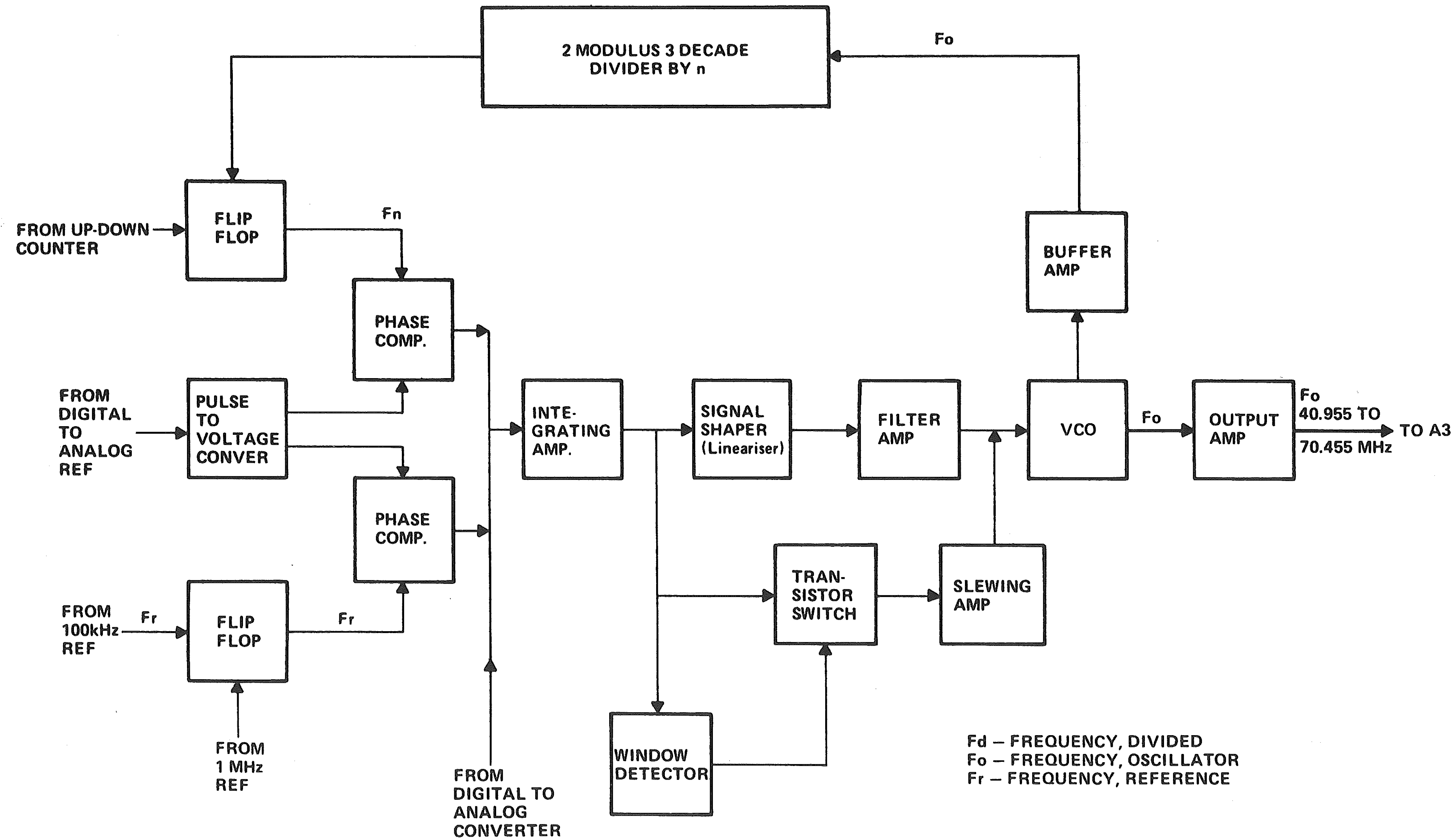
(a) As the second accumulation begins U2A is enabled, under control of U4A, and the data at its inputs is transferred to the B inputs of U15 the NBCD Adder. During the five clock periods of the second accumulation the data in U20 and U21 is shifted back to the B inputs of U15. During this period, the data in U8 through U12 is held as the tri-state output enable of these registers is not enabled ensuring the results of the first accumulation is added again in the second accumulation. At the end of the second accumulation the results of the first accumulation will be propagated through the 5-stage register in each half of U20 and U21 and will appear at the inputs DØ through D3 of the 4 x 4 multiport register U22, and at the A1 through A8 inputs to U15. If no new data is loaded into U8 through U12 from the serial input data stream, then the two cycles of accumulation will continue; first accumulating the contents of U8 through U12 on one half cycle with the data at A1 through A8 in U15, and on the second half cycle adding the results from the first accumulation back into the B inputs of U15. Temporary storage for the results of each accumulation is provided by U18, U20 and U21.

(b) If the result of adding numbers in U15 is a terminal count, the adder will produce a Carry-Out pulse at U15 pin 6 and reset to zero and start counting again. In a real situation this process is on going and the adder is continually providing Carry-Out pulses. (See Fig. 5-12, line B.) This Carry-Out pulse is fed to U6 to be reclocked. The reclocked output at U6 pin 7 is routed through U1C to a further adder U17. The Carry-Out is also clocked by U19A so that if it occurs on one edge of the accumulating half cycle controlled from U4B, it will appear at the Q output of U19A and after reclocking in U6 through the fifth latch it is applied to the Carry



UK and US Patents have been obtained covering the synthesizer circuits described on this page as follows: US Patent No. 4,204,174 Phase Locked Loop Variable Frequency Generator and US Patent No. 3,555,446 Frequency Synthesizer.

Figure 5-10. First Local Oscillator Digital Circuits Functional Block Diagram



UK and US Patents have been obtained covering the synthesizer circuits described on this page as follows: US Patent No. 4,204,174 Phase Locked Loop Variable Frequency Generator and US Patent No. 3,555,446 Frequency Synthesizer.

Figure 5-11. First Local Oscillator Analog Circuits Functional Block Diagram input of the 4-bit Full Adder U17. (See Fig. 5-13, line C.) The Adder U17 continually updates, by addition, based on the Carry Out information from U15, the 100 kHz frequency information, provided by the input storage register U13. The addition in this adder is continuous so that the outputs at U17 pins 10 through 13 are constantly changing to provide the averaging action previously discussed.

(3) DAC Control. U22 the 4 x 4 multiport register provides storage for the results of the constant accumulations and provides the information to the digital-to-analog converter U23. U19B divides the accumulator control signal by two so that all four registers in U22 can be loaded. The read cycles to these registers are controlled by the RØA, RØB, R1A and R1B inputs of U22. The RØA and RØB inputs are fixed and the R1A and R1B inputs are controlled by the output of U19B so that during two accumulations R1 is loaded, each register RØ and R1 consisting of two 4-bit data storage areas. The data stored is that which appears at the data inputs of U22, DØ through D3. This stored information is transferred to the register A outputs and register B outputs when W Enable is high and either WØ is high transferring RØA and RØB contents or W1 is high transferring the contents of R1A and R1B.

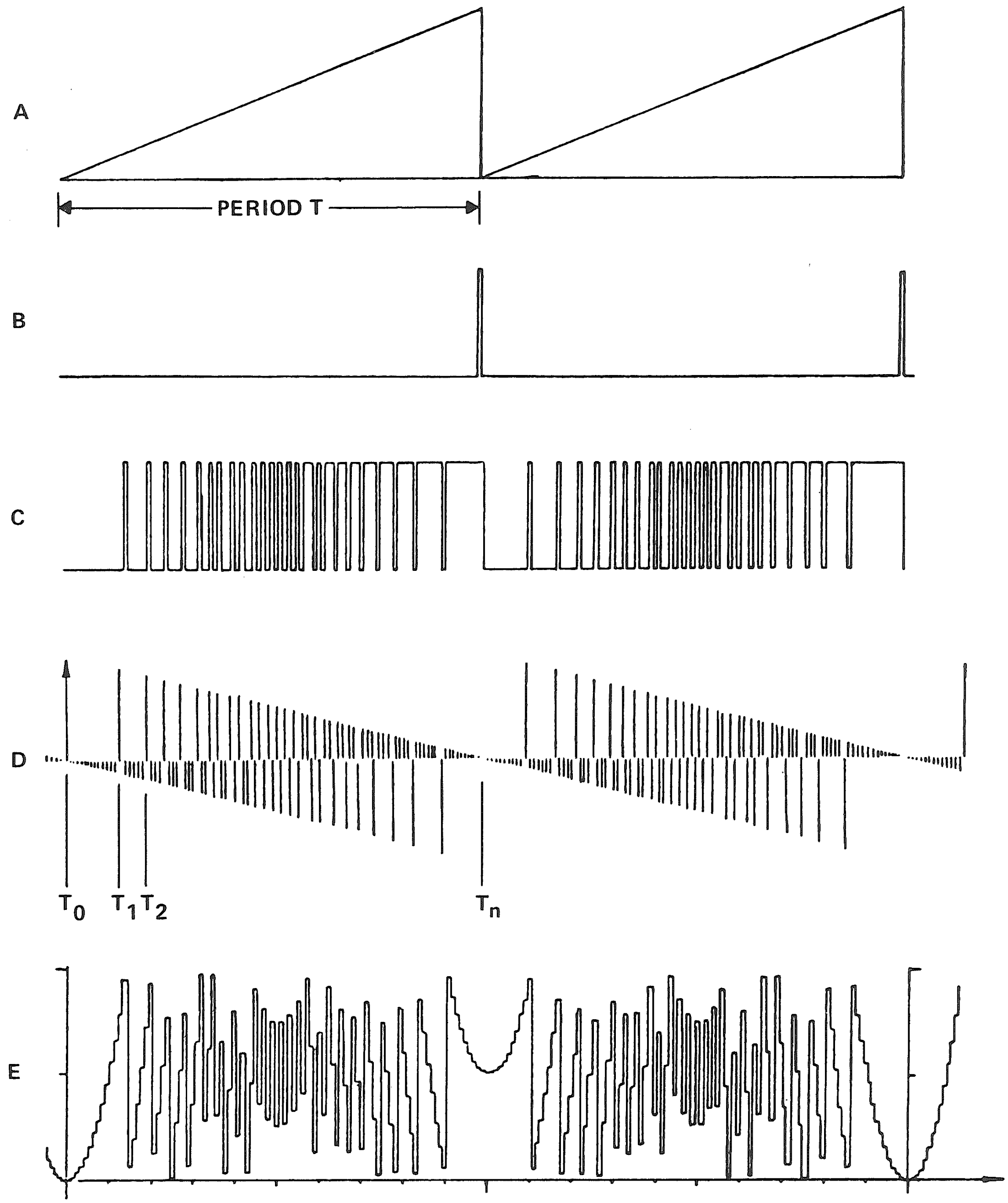
(a) The digital-to-analog converter provides an output based on the changing data at its inputs as a voltage ramp whose amplitude and DC offset is modified by the adjustment of R5. The D/A also provides a reference source for the pulse to voltage converter U33B. NOTE: The pulses demonstrated in Fig. 5-12 can be reproduced in circuit if the RF front panel frequency is set to 1.046000 MHz. This ensures that the accumulations start from a zero condition. B will then be at TP3, C at TP4 and E at U23, pin 2 (the D/A output).

(4) Oscillator Control. Figure 5-11 shows a simplified block diagram of the oscillator control circuits.

(a) Main Division. The BCD data outputs for 100 kHz, 1 MHz and 10 MHz provided by U17 and U14 are applied to a 2-modulus, 3-decade divider consisting of U27, U29, U30 and U31. This form of division ensures that by using a 2-modulus high speed control device U27 that can divide by 10 or 11 under control of its M1 and M2 input control can divide a high frequency input by an integer value. The terminal count from U29 is applied inverted by Q5 to this control input of U27. The resultant divided signal at pin 9 of U29, U30 and U31 is applied to a TTL to ECL converter network consisting of R30, R31 and CR7 to a flip-flop U28A. This flip-flop reclocks the divided output under control of the clock signal on U28A pin 6 from the ECL output U27 pin 8, and then applied to one side of the phase comparator from its quadrature outputs on pins 2 and 3.

(b) Phase Comparator and Pulse-to-Voltage Converter. The phase comparator reference is derived from the 100 kHz signal from U5 pin 12, reclocked against the 1 MHz reference in U26A. The reference output at U26A is applied to the other side of the phase comparator consisting of U28B, U26B and U32. The ECL comparator provides phase comparator outputs at TP7 and TP8. The variable input from U28A pin 3 is applied to a pulse-width detector consisting of CR9, CR10, Q6 and U33B. As the pulse width changes as the frequency varies from 40.455 MHz to 70.454999 MHz the voltage at the emitter of Q6 varies continuously and linearly over a range of approximately 1 volt. The DC offset of this voltage is determined by the D/A ref from U23. U33A and Q8 form one-half of a current source to CR12 and CR14 and Q7 and Q9 from the bottom half of this current drive through CR13 and CR15. Phase compared outputs at TP7 and TP8 are fed into the diode network formed by CR12, CR13, CR14 and CR15 and an output from this pulse-to-current converter is fed to R60.

(c) VCO and Analog Control Circuitry. The current output of the phase comparator is combined with the voltage ramp from the D/A through C80. This combined signal is



UK and US Patents have been obtained covering the synthesizer circuits described on this page as follows: US Patent No. 4,204,174 Phase Locked Loop Variable Frequency Generator and US Patent No. 3,555,446 Frequency Synthesizer.

Figure 5-12. Detailed Timing Diagram

then applied to an integrating amplifier U35. In normal operation, the output of U35 is sent to a signal linearizing/inverter circuit U37A and to the out-of-lock window detector comprising U34C and U34D. This is described in more detail in the speed-up and out-of-lock circuit operation. The output of U37A at TP10 is a DC voltage that can vary from a high voltage up to 18 volts and a low voltage equal to 1 volt, it will be high voltage when the selected frequency is at 29.999 MHz and low when the system requires 0.5 MHz. This DC voltage is then passed through U37B which along with its associated resistors and capacitors forms a low-pass filter. This output is then buffered from the VCO by 120K resistor R88 between TP11 and TP12. A further lead-lag network is then in the VCO control line between TP12 and ground formed by R92, R93, R94 and C98. This voltage is then applied to the VCO control varactors CR3 and CR4 through R85 and L4. A voltage applied to CR3 and CR4 will vary the capacitance across the main VCO coil L5 and thus vary the frequency generated. Q1 is the main LO active device and an output from its drain is capacitively coupled to a buffer amplifier of the cascade type formed by Q12 and Q13. The output of this feeds the 2-modulus divider controller U27. A further output from the oscillator coil is tapped off and provides the main LO output through Q2 and Q3 with step down transformer T1.

(d) Speed-Up and Out-of-Lock Operation. When a large step of frequency is introduced on the front panel or from remote the window detector U34C and U34D comparators, compares the inputs on pins 9 and 10 from the VCO control circuitry with fixed high and low references on pins 11 and 8. If the voltage goes higher or lower (frequency step up or down) than these references a pulse will appear at the comparator outputs on pins 13 and 14. This pulse is applied through an RC network to a voltage converter consisting of U34B and CR19 and CR20. This voltage offset pulse is then used to drive three switches U36B, U36C and U36D. These switches by-pass the lowpass filter U37B and increase the integrating bandwidth of U35 and one switch, provides a feed forward from TP10 to the positive input of U40. U40 provides an integrated drive to push-pull drivers Q10 and Q11, the action of these drivers is to high-speed charge or discharge C98 through R91, C97 and R94. When the control voltage is at approximately the correct voltage for the frequency selected this circuit becomes operative. U34A provides the Out-of-Lock signal for feeding to the A9 receiver control board and then to A6A2 for processing. If a pulse or a constant low level is applied to pin 6 of U34A then its output will go low indicating OOL.

5-16. SECOND LO AND BFO GENERATOR A8. The second local oscillator and beat frequency oscillator circuit card assembly contains the circuitry for these two oscillators. An internal/external frequency reference circuit is also contained on this circuit card. The second local oscillator develops the fixed 40 MHz signals for the second mixer that in turn provides the 455 kHz second IF signal. The BFO is a variable oscillator that provides both the 455 kHz second IF signal and the basic 455 kHz beat frequency for sideband and CW modes of operation. The oscillator, through receiver control, may be either set at 455 kHz or varied plus or minus 8 kHz either side of its basic frequency for CW operation. The internal/external frequency reference circuit provides a reference frequency for both oscillators phase lock loops as well as the first LO contained on A7. In addition, the circuit includes an internal temperature controlled crystal oscillator which supplies a selectable 1 MHz, 5 MHz or 10 MHz reference frequency output at the rear panel. An external reference frequency can be used in place of the internal reference. The circuit description for the internal/external reference, the second LO and BFO are described under their respective headings with functional block diagrams shown in Figures 5-13 and 5-15. Schematic diagrams of these circuits are shown in Figure 8-11.

a. <u>Internal/External Reference Frequency.</u> The A8 circuit card contains circuitry that permits either an internal or external reference frequency. This reference frequency is required for the operation of all three oscillator synthesizers. A reference in/out connector and switch on the rear panel in addition to linkage on the A8 circuit card provide for the selection of either internal or external frequency and for selecting the proper divide by N frequency for the phase comparator.

(1) Internal Mode. A 5 MHz crystal oscillator Y1, located on A8 is used as the internal reference frequency. With the rear panel REF INT/EXT switch in the INT position, the base of Q1 is grounded through R7 which turns voltage regulator U1 on. The voltage from this regulator enables the temperature controlled crystal oscillator. Approximately 30 minutes are required for maximum stability. The oscillator output is coupled through capacitor C5 to the base of transistor switch Q5. With the ground applied through the INT/EXT switch, the base of Q5 is held high through inverter U2A and diode CR3 while the base of transistor switch Q4 is held low through diode CR2. Transistor Q5 conducts, transferring the 5 MHz signal through a TTL square wave shaper Q6 to one clock input of the phase comparator. See paragraph b (3). The 20 MHz voltage controlled oscillator, described in paragraph (b), is stabilized through the use of this reference frequency. The 20 MHz output of the oscillator is divided by three dividers (two ÷ 2, U7A and U7B and a ÷ 10, U6). The two dividers (÷ 2) are contained in a single dual D flip-flop. The clock signal (20 MHz) is applied to the clock input of U7A. With the $\overline{Q}$ output connected to the D input, the Q output provides the 10 MHz reference. The 10 MHz is also connected to the clock input of the second flip-flop and to the divide by 10 circuit. The second flip-flops Q output provides the 5 MHz reference signal. The divide by 10 circuit is a two stage divider (÷ 2 and ÷ 5). The 10 MHz drives the clock input for the divide by 5 at B input pin 1. The output of this divider (QD pin 11) is connected back to the clock of the second divider (÷ 2) at A input pin 14. Dividing by 5 first then by 2 provides a more symmetrical 1 MHz reference. The 1 MHz signal is output from the divider (÷ 2) at QA output pin 12. The 1 MHz, 5 MHz and 10 MHz frequencies derived from these dividers are available for reference through data select switches U4 and U5. The 1 MHz reference is routed directly to the BFO synthesizer and to the first local oscillator synthesizer through NAND gate U11C and connector J2. One of the three frequencies will be selected by data select U5 and routed to rear panel connector J7. Either one of the three frequencies may be selected by proper connection of links LK1 and LK2. In this internal mode, data select C of both U4 and U5 is held low through the INT/EXT switch. Linking LK1 makes data select A low which outputs D0 input of both U4 and U5 to their respective Y outputs. For U4 this is 5 MHz, for U5 it is 10 MHz. When only LK2 is linked data select A will be high and B low which connects both D1 inputs to their respective Y outputs (U4-5 MHz, U5-5 MHz). When both LK1 and LK2 is linked both data select A and B are held low which outputs D0 of both U4 and U5 (U4-5 MHz, U5-1 MHz). As noted in this internal mode, U4 always selects the 5 MHz. It is then routed to the phase comparator as the oscillator reference signal. The output frequency selected by U5 is routed through resistor R13 to buffer amplifier stages Q3 and Q2. These stages provide for output into 50 ohms through a high pass filter, L1, C6 and C7, and connector J7 on the rear panel. The high pass filter also provides filtering for reference frequencies applied externally through J7 while resistors R8 and R9 provide a 50 ohm impedance to the incoming reference frequency.

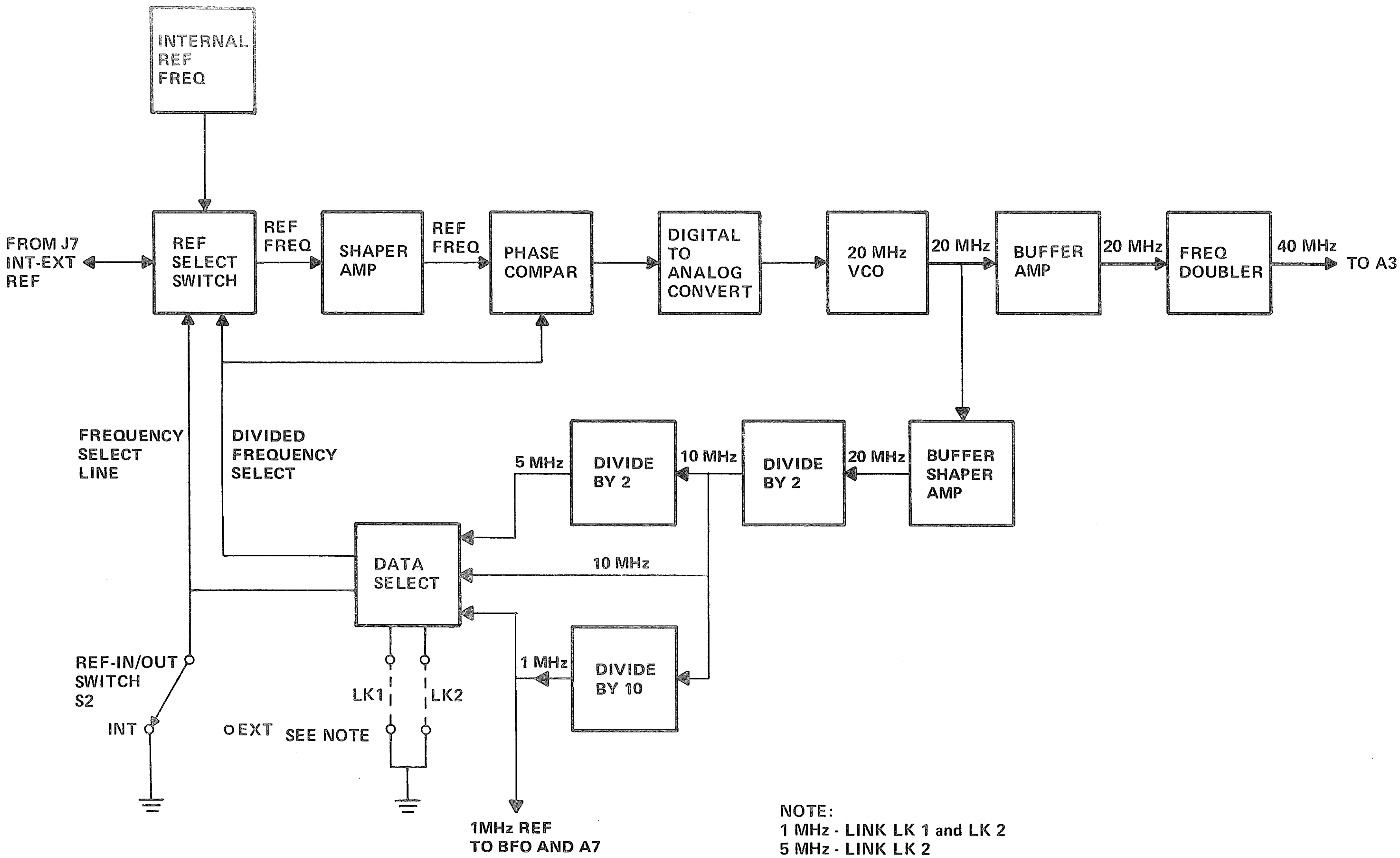
(2) External Mode. In this mode of operation the INT/EXT switch is set to EXT and this line goes high from the +5 volts through resistor R78. This causes transistor Q1 to turn voltage regulator U1 off which in turn turns off the internal crystal oscillator Y1. When an external oscillator is connected to connector J7 on the rear panel, the input is routed through the high pass filter, and capacitor C8 to the base of transistor switch Q4. The input of NOR gate U2A is now high which in turn keeps the base of Q5 low through diode CR3. Transistor Q4, whose base is no longer low, conducts which applies the external reference through the TTL shaper to the same clock input of the phase comparator that the 5 MHz reference was applied in the internal mode. The appropriate reference frequency for application to the second clock input to the phase comparator can be selected through LK1 and LK2 as in the internal mode; however, data select C is now high. Linking LK1 selects D6 (10 MHz), LK2 selects D5 (5 MHz) or both LK1 and LK2 select D4 (1 MHz). The D0, D1, and D2 inputs to U5 cannot be selected when data select C is high (external mode) and no output appears on the Y output of U5.

b. Second Local Oscillator. Figure 5-13 shows a simplified functional block diagram of the second local oscillator. The circuit consists mainly of a crystal referenced, voltage controlled oscillator, a frequency doubler output circuit and a phase lock loop. The phase lock loop includes amplifiers, an ECL to TTL buffer, three frequency dividers (two ÷2 and a ÷10), reference frequency select circuit, a phase comparator and a digital to analog converter. The three dividers are used to provide a choice of reference frequencies for internal or external reference. These circuits are described in Paragraph 5-16 a.

(1) Phase Lock Loop. The 20 MHz oscillator frequency is kept on frequency through a phase locked loop (See Figure 5-9). The oscillator output is routed through a divide by N circuit that provides an oscillator reference frequency. This divided oscillator frequency is coupled to the second clock input of a phase comparator. The phase comparator, described in Paragraph (3), detects any phase shift between the oscillator frequency and a reference frequency also connected to the phase comparator. The phase comparator then changes the digital to analog converter output voltage which is connected to the oscillator varactor and crystal. This then causes the oscillator frequency to change. This loop action will continue until the oscillator frequency is brought into phase (same frequency) with the reference frequency.

(2) Voltage Controlled Oscillator. The 20 MHz oscillator consists of an ECL OR gate U22D, 20 MHz crystal Y2, varactor CR4, resistors R47, R48, R49 and R50 and capacitors C34 through C38. Oscillation frequency is derived from the parallel combination of crystal Y2 in series with C37 and with varactor CR4 in series with C34. The dc voltage applied at the junction of CR4 and Y2 controls the reactance of the parallel circuit, mainly through CR4. This dc voltage, controlled through the phase lock loop described in Paragraph (1) compensates for any frequency shift of the oscillator. The oscillator output is coupled to two buffer amplifiers U22A and U22B. Buffer U22A is used to drive a TTL shaper buffer amplifier, Q10, which shapes the oscillator output into a square wave for input to the divider. These circuits are described in Paragraph a . Buffer U22B drives a frequency doubler circuit, Q11, and associated components. This tuned circuit selects the 40 MHz component of the signal and outputs it through J3 to circuit card A3 as the second oscillator frequency.

(3) Phase Comparator and Digital to Analog Converter. The phase comparator is used to detect the phase shift between the reference frequency and the oscillator frequency and to apply control to the digital to analog converter in relation to that phase shift. The comparator consists of dual flip-flop U3A and U3B and NAND gate U2B. Flip-flop U3A is clocked from the reference frequency while U3B is clocked from the divided oscillator frequency. The D inputs to both flip-flops are held high through the +5 volts. When both Q outputs are high the output of NAND gate U2B goes low, resetting both flip-flops with a delay through R32 and C20. Thus when the positive edge of a clock signal clocks a flip-flop, Q goes high while $\overline{Q}$ goes low. If the two clock signals to the flip-flops are in phase, the $\overline{Q}$ outputs then will go high from the reset action through NAND gate U2B, initiated from the leading edge of both clock pulses. The $\overline{Q}$ outputs will remain high through the on-off period of that particular clock pulse. Exept for a small delay time introduced by the flip-flops the $\overline{Q}$ outputs will be high most of the time when the two clock signals are in phase. (See Figure 5-14.) When the oscillator frequency leads the reference signal (frequency high), the $\overline{Q}$ output of U3B remains on less than the $\overline{Q}$ output of U3A because the leading pulse sets back to Q on U3B before the lagging pulse of the reference signal sets back to Q on U3A. The reverse of this is true when the oscillator frequency lags the reference signal (frequency low). The two $\overline{Q}$ outputs of the phase comparator are coupled to a digital to analog converter which consists of transistors Q7, Q8 and Q9, resistors R33 through R39 and capacitors C24 through C26. The $\overline{Q}$ output of reference flip-flop U3A is connected to the emitter of Q7 through R33 while the $\overline{Q}$ output of the oscillator flip-flop U3B is connected to the emitter of Q9 through R34. When the oscillator and reference signal are in phase, the two outputs are the same and transistors Q7 and Q9



NOTE:
1 MHz - LINK LK 1 and LK 2
5 MHz - LINK LK 2
10 MHz - LINK LK 1

UK and US Patents have been obtained covering the synthesizer circuits described on this page as follows: US Patent No. 4,204,174 Phase Locked Loop Variable Frequency Generator and US Patent No. 3,555,446 Frequency Synthesizer.

Figure 5-13. Second Local Oscillator Functional Block Diagram

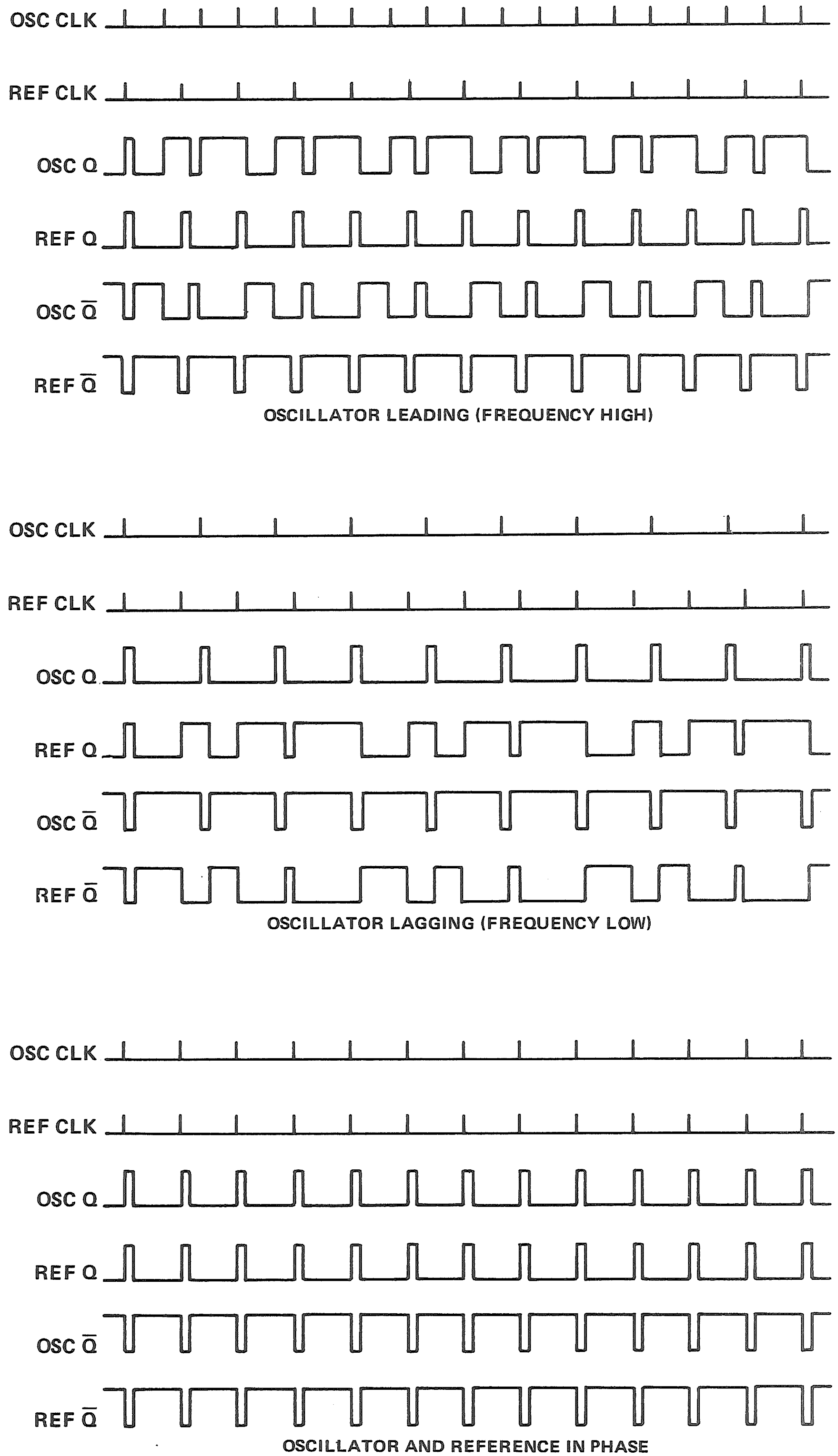


Figure 5-14. Waveform Diagram: Phase Comparator

conduct at a rate dependent on the amplitude and time period of the pulse. With the amplitude always constant, the amount of conduction then depends only on the time period. When the pulse goes high, the emitters of Q7 and Q9 go more positive causing them to conduct less and when the pulse goes low, they conduct more. The voltage output at the common collectors of Q8 and Q9 would tend to follow this rise and fall in the pulse; however, the inverted signal at the base of Q8 also causes it to conduct less when the pulse is high and more when the pulse goes low. This action converts the pulse signals into a dc level sawtooth waveform at the Q8-Q9 common collectors. The low pass filter, C25, C26 and R39 smooths this waveform and dampens sudden changes caused from changes in the phase comparator pulse rates and in turn stabilizes the phase lock loop. When oscillator frequency increases, the pulse rate increases at Q7 and decreases at Q9, causing a reduction of the dc level output. When oscillator frequency decreases the reverse action takes place. This analog dc output is coupled through R47 to the oscillator for frequency control.

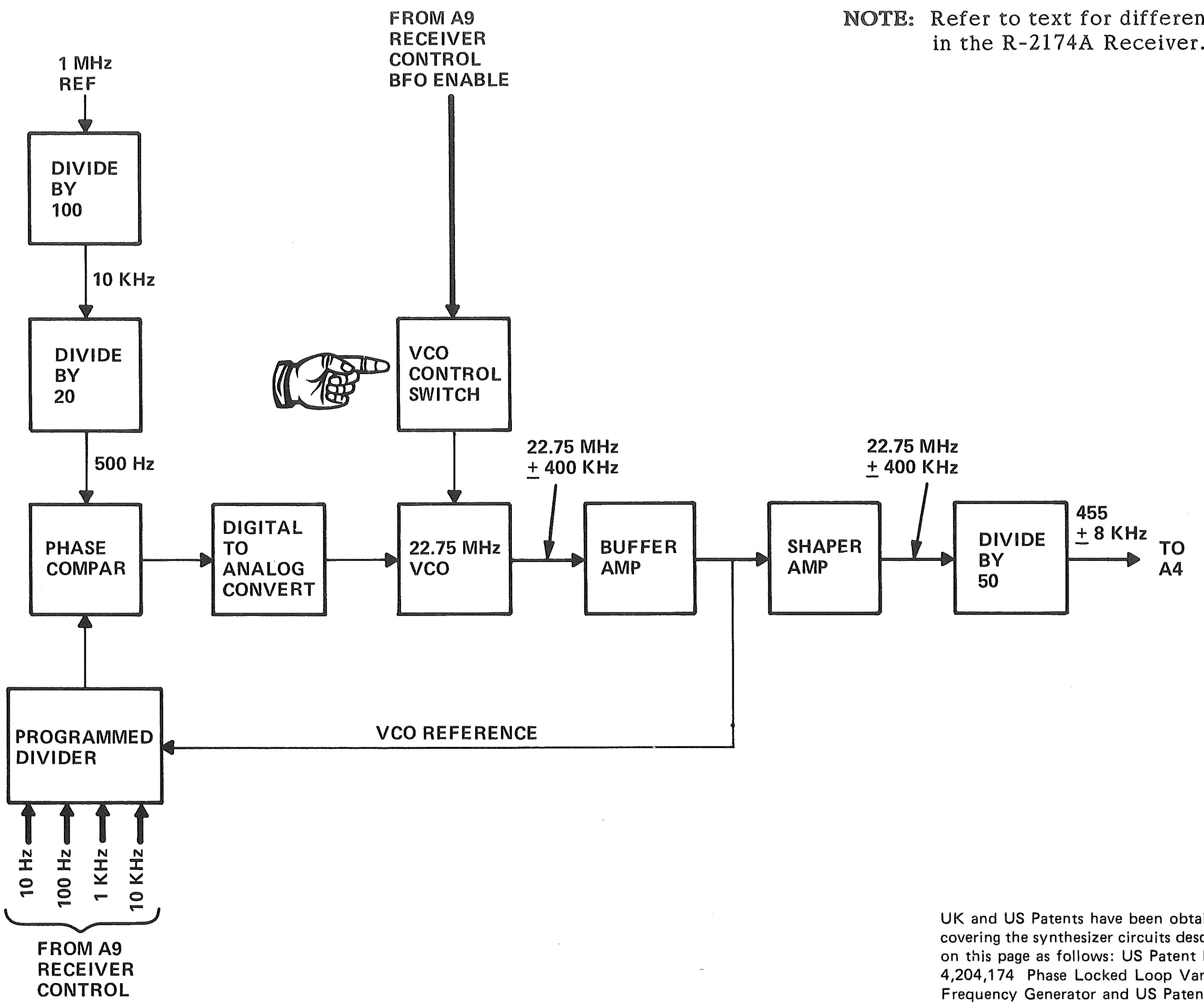
(4) Out of Lock Detector. The out of lock detector consists of NAND gate U2C, resistors R43 and R44 and capacitors C29 and C31. The NAND gate output is held low (phase loop in lock) by the $\overline{Q}$ outputs of the phase comparator. The resistor capacitor combinations R43-C29 and R44-C31 integrate the square wave signal to provide a constant high on the two NAND gate inputs. If either or both of the two $\overline{Q}$ outputs from the phase comparator remains low the output of the NAND gate will go high. The output from this circuit is routed to A9 front panel control for processing.

c. Beat Frequency Oscillator (BFO). Figure 5-15 is a simplified block diagram of the beat frequency oscillator. This circuit provides the variable 455 kHz BFO for Receiver CW and sideband operation. The BFO is varied plus or minus 8 kHz through Receiver control. The oscillator operates in a phase locked loop which consists of a voltage controlled oscillator (VCO), a buffer amplifier, a programmed divider, a phase comparator and a digital to analog converter. A divide by 2000 circuit is included to provide a 500 Hz reference signal for the phase comparator. The VCO operates at a center frequency of 22.75 MHz which is 50 times the BFO center frequency of 455 kHz. The oscillator output is routed through a buffer amplifier, TTL shaper, divide by 50 circuit and filter to provide the 455 kHz BFO to the A4 circuit card. An out of lock circuit cuit is also included to detect any out of lock condition of the phase lock loop.

(1) Phase Lock Loop. The phase lock loop for the BFO oscillator functions in the same way as the circuit described for the second local oscillator except the divide by N is made variable through BFO input data to the divide by N circuit.

(2) Voltage Controlled Oscillator. The VCO consists of field effect transistor Q18, opto isolator U21, coils L4 and L5, resistors R66 and R67, capacitors C52 through C56 and C59 and varactors CR6 and CR7. The capacitive reactance of the two varactors in conjunctions with L4 determines the frequency at which the circuit will oscillate. Since varactors change capacitance in relation to the level of the dc voltage applied, the frequency of the oscillator is controlled from the output of the digital to analog converter that is applied to varactors CR6 and CR7 through coil L3. Opto isolator U21, connected to the source of Q18 through resistor R67, provides for on-off control of the oscillator by isolated control of the oscillator source bias. When BFO is enabled in the CW and sideband modes, U21 is enabled through pin 2 which in turn completes the bias path for Q18 through R67. The output of the oscillator is coupled through capacitor C57 to the gate of field effect transistor Q19 which acts as a buffer amplifier between the oscillator and two output circuits. One output of the buffer amplifier provides the oscillator reference frequency through capacitor C72 to the programmed dividers. This circuit is described in Paragraph (3). The second output is coupled through capacitor C60 to a shaper circuit, Q20, R72, R73, R74 and C61. This circuit shapes the waveform into a square-wave for the TTL logic of the divide by circuit U20. The dual decade counter U20 is externally strapped to provide a division of 50 on its

NOTE: Refer to text for differences in the R-2174A Receiver.



UK and US Patents have been obtained covering the synthesizer circuits described on this page as follows: US Patent No. 4,204,174 Phase Locked Loop Variable Frequency Generator and US Patent No. 3,555,446 Frequency Synthesizer.

Figure 5-15. BFO Functional Block Diagram

QD output, pin 9. The variable 22.35 to 23.15 MHz oscillator signal is reduced in frequency by the division of 50 which provides the 447 to 463 kHz BFO. This output is filtered through the filter network consisting of C63, C64, C65,L6, R75, R76 and R77. This filter shapes the digital waveform from U20 into an approximate sine wave signal before being routed to circuit card A4 through connector J4.

(2.1) In the R-2174A version the enable signal is routed directly through R67 to the source of Q18 rather than being routed through opto-isolator U21. Opto-isolator U21 is not used in the R-2174A.

(3) Programmed Dividers. The programmed dividers determine the divide by N number by which the oscillator frequency will be divided for a variable reference to the phase comparator. The program dividers consist of presettable BCD decade counters U14 through U18, divide by 10 or 11 2-modules controller U19, NOR gates U12A through U12D and AND gates U13A through U13C. The program divider has two reference inputs; the oscillator frequency coupled through C72 to the V reference and clock inputs of U19 at pins 15 and 16 and the BFO data control inputs to U15 through U18. It is the BFO data inputs in conjunction with U19 that sets the divide by N number for dividing the VCO frequency. To divide the 22.75 MHz to 500 Hz, for the second clock input to the phase comparator, would require a division of 45500. The five decade counters are externally strapped to count down from a maximum count of 100000 (99999 + 1). The actual data then that would be set on the BFO inputs would be 100000 – 45500 = 54500; however due to gating restrictions between the decade counters the actual number set at the BCD inputs is 54509 at center frequency (455 kHz). The BFO is adjustable plus or minus 8 kHz so that the swing in the BCD inputs must be from 53709 (54509 – 800) to 55309 (54509 + 800) with 54509 as center. At center frequency counter U18 receives the 10 Hz BCD digits on its parallel inputs P0 through P3 with P0 and P3 ($2^0 + 2^4 = 9$) high. Counter U17 receives the 100 Hz digits with all inputs low (0), U16 receives the 1 kHz digits with P0 and P2 ($2^0 + 2^2 = 5$) high, and U15 receives the 10 kHz digits with only P2 ($2^2 = 4$) high. Counter U14 is strapped P0 and P2 ($2^0 + 2^2 = 5$) to the +5 volts (high) and P1 and P3 to ground (low). This supplies the 100 kHz digit which is always 5. Counter U15 receives only the 2^0, 2^1 and 2^2 BCD digits since the 10 kHz swing is never greater than 7. The counter is a two modulus divide by 10 or 11 controller and will divide by 10 or 11 for different periods in the clock signal. The TC output pin 15 of U18 coupled to the M1-M2 inputs of U19 determine the periods at which it will divide with either 10 or 11. NOR gate U12C ensures that the count enable input of U18 goes low when TC goes high. This assures that the TC output will be retained long enough for action on the M1-M2 inputs of U19. The QTTL output (pin 11) is used to clock the decade counters U14 through U18 and as a reclocking source for NOR gate U12A. Four control inputs, parallel enable (PE), count enable parallel (CEP), count enable trickle (CET) and reset (R) select the counters mode of operation. The R and CET of all counters is held high through the +5 volts connected to all counter CET and R inputs. The CEP input of counter U17 (100 Hz) is also held high from the same +5 volts since this counter does not receive a carry out from previous counters. The CEP of counter U16 is high only when the TC output of U17 is high, the CEP of U15 is high only when the TC output of both C16 and C17 through AND gate U13A are high and the CEP input of U14 is high only when the TC output of both U15 and U16 through AND gate U13B are high. This AND gating of the TC outputs help prevent extra pulses from occurring that are caused from delays in the counters. The PE of all counters are alternately low and high as the TC output to inverter U12B is alternately high and low. With the R and CET of all counters held high (counter resets when R is low) the count mode is enabled when CEP and PE goes high. When PE goes low the counters will synchronously load the data from the BFO inputs into the counters with the count occurring each 500 Hz. The counters output on TC only when PE is held high; however when CEP is held low the TC output will be retained until the next clock pulse. The TC output of the programmed dividers is connected to one input of a two input NOR gate U12A. The clock signal is connected to the second input so that any unwanted pulses, created by delay in the counters and not in sequence with the clock pulse will be rejected. The output of U12A is routed through inverter U12D to one clock input of the phase comparator as the oscillator reference frequency.

(4) Reference Frequency. The 1 MHz reference frequency supplied from internal/external reference circuits is divided by 2000 to provide a 500 Hz reference frequency to the phase comparator. This division of 2000 is accomplished with two dual decade counters U8 and U9. Counter U8 provides a division by 100 while counter U9 provides division by 20. Each counter has two divide by 2 circuits and two divide by 5 circuits and are externally strapped to provide the divisions by 100 and 20. The division by 100 is accomplished by using all four dividers in the order shown ($\div 2$ = 500 kHz, $\div 5$ = 100 kHz, $\div 5$ = 20 kHz and $\div 2$ = 10 kHz). The divide by 20 is accomplished in the same manner except its input is the 10 kHz output of the $\div 100$ and the second $\div 5$ is bypassed ($\div 2$ = 5 kHz, $\div 5$ = 1 kHz, and $\div 2$ = 500 Hz). The resultant 500 Hz output is coupled to the clock input of D flip-flop U10A. This flip-flop is contained in a dual flip-flop package which together with NOR gate U11A make up the phase comparator.

(5) Phase Comparator and Digital to Analog Converter. As described in Paragraph (4), the 500 Hz reference frequency is connected to flip-flop U10A. The second flip-flop U10B receives its clock signal from the programmed dividers. The D inputs of both flip-flops are tied to the +5 volts (logic 1) while both Q outputs are connected through 2 input AND gate U11A and resistor R83 to the reset of both flip-flops. Both flip-flops will reset each time that both Q's go high, causing a logic 0 at the resets of both flip-flops. The clock input signal to U10A (reference) consists of positive going pulses while the signal from the programmed divider (oscillator reference) also contains positive going pulses and is connected to the clock input of U10B. Each flip-flop triggers Q on (high) the positive going pulse of its respective clock signal and at the same time triggers $\overline{Q}$ to zero (low). Previously as described, when both Q outputs are high the output from AND gate U11A is low clearing both flip-flops through R83. This resets the Q outputs to low and the $\overline{Q}$ outputs to high. Refer to Figure 5-14. The two $\overline{Q}$ outputs are connected to the digital to analog converter which consists of transistors Q15, Q16 and Q17 and their associated components. This circuit operates in the same manner as the digital to analog converter described in Paragraph b (3) except that adjustments in the BFO frequency provide a different setting of the dc control voltage. This causes the VCO to change frequency in relation to the BFO setting.

(6) Out of Lock Detector. The out of lock detector consists of NAND gate U11D, resistors R57, R58 and R84 and capacitors C83 and C86. This circuit operates in the same manner as the second local oscillator out of lock circuit described in Paragraph b (4).

5-17. **FRONT PANEL AND RECEIVER CONTROL A9.** The front panel receiver control circuit card A9 provides for the in and out flow of receiver control data, both from local (front panel) and remote locations. The front panel contains controls and indicators for local operation of the Receiver which includes: two - sixteen keypad switch sets, a tuning knob, two Liquid Crystal Displays (LCD), a fault indicator, an IF and AF GAIN control, two audio line level controls, an audio phones jack and a POWER-ON switch. All of these controls, except POWER-ON switch S1, are interfaced to receiver circuits through the A9 circuit card. The IF and AF GAIN controls, two audio level controls and phones jack are routed directly through the A9 circuit card to their respective receiver functions. The keypads, tuning encoder, LCD's and fault indicator connect through various interface circuits on the A9 circuit card to the microprocessor (A6A2). The data is processed by the microcomputer and routed back through interface circuits (A9) to various receiver functions (A4, A5, A7 and A8). Receiver control data entered from a remote location is routed through interface circuits (A6A1) to the microprocessor (A6A2). This data is processed and routed through A9 in the same way as front panel data. Figure 5-16 shows a functional block diagram while the schematic diagram is shown on three sheets in Figure 8-12.

a. Front Panel Switches. Two sets of switch panels, each containing 16 pushbutton switches, are used to enter Receiver control data from the front panel. Switch panel 1 is used for receiver tuning, BFO tuning and for selecting remote or local control. Switch panel 2 is used to select receiver mode, AGC mode, bandwidth and RF/AF meter indication. Each pushbutton

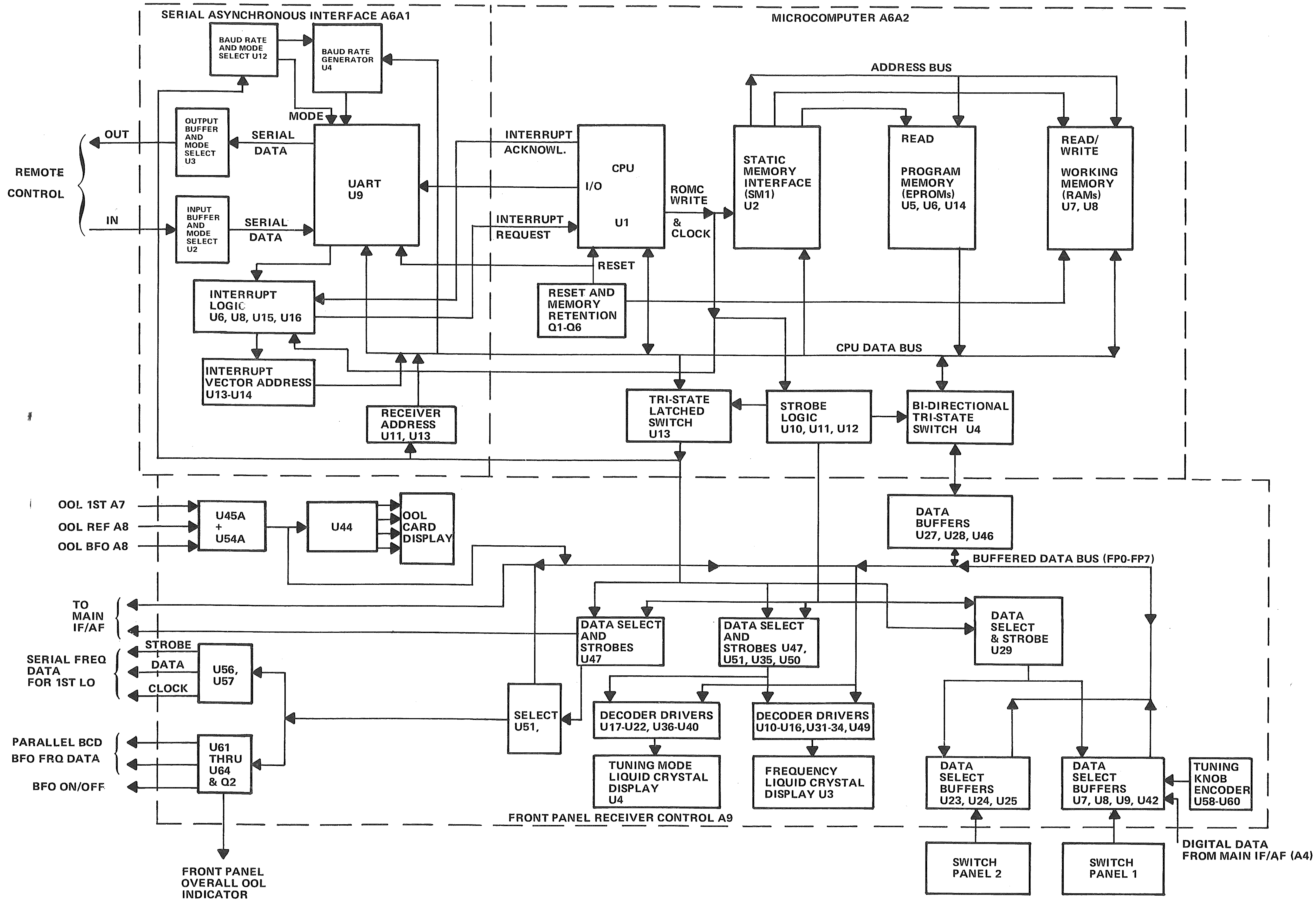


Figure 5-16. Front Panel Control, Block Diagram

switch is a single pole, single throw switch with normally open momentary contacts. One contact of each switch is commonly connected to ground within each keypad set. The other contact of each switch is connected to an input of six hex buffers U7, U8, U9, U23, U24 and U25 (two inputs of U8 and U24 are unused) and to +5 volts through a 10K ohm resistor supplied through resistor array U1, U2, U5 and U6. When any particular switch is open (not pushed), its input to the buffer is held high through the 10K ohm resistor to the +5 volts. When the switch is closed (pushed), the input line to the buffer goes low. The high or low condition of any switch is passed through the respective buffers to the data bus when that particular buffer is enabled from the address multiplexer U29. The 32 outputs (four are unused) of the six hex buffers are strapped to the 8-line data bus in groups of eight with each group controlled from a separate address enable signal from U29. This assures that the status of two or more switches will not be transferred through the buffers to the same data line at the same time. The enable signals from U29 are controlled from in/out read and address control signals generated by the microprocessor in order to regularly scan the switch pads for new data. Data on these lines are transferred to the microprocessor as described in Paragraph e.

b. Tuning Encoder. The tuning encoder, operated from the front panel tuning knob, is used to adjust, in fine frequency increments, either Receiver frequency or BFO frequency. Pushbuttons, on the right keypad, select the mode of the tuning encoder and the rate at which frequency data may be entered. The TUNE RATE pushbutton selects one of three rates of change for main Receiver frequency that the tuning encoder will respond; fine (1 Hz increments), slow (30 Hz increments) and fast (1 kHz increments). The BFO pushbutton selects BFO frequency tuning in one rate only (10 Hz increments). The LOCK pushbutton disables the encoder while the TUNE RATE or BFO pushbutton enables the encoder from a locked condition. The tuning encoder consists of a 25 segmented disk operating in conjunction with two offset reflective object sensors U59 and U60 with the sensors being mounted on the A9 circuit card. The light from the sensor is reflected from the alternately reflective and non-reflective segments of the disk to the detectors as the disk is rotated. This produces two pulse waveforms (see Figure 5-17). The two detectors are physically positioned, in relation to the disk segments, so that the one waveform either leads or lags the other by 90 degrees. Clockwise rotation of the tuning knob causes the output of U59 to lead that of U60 causing frequency entered to increase. Counter-clockwise rotation causes the waveform of U60 to lead that of U59 causing frequency to decrease. The outputs of the object sensors are coupled, through resistors R16 and R17, to a comparator U58A and U58B. The two inputs to this circuit are compared to a fixed dc voltage input to the comparator from resistor combinations (R8 and R10 for U58A and R9 and R11 for U58B) which control the comparator switching point. The square wave outputs of the comparator are routed to buffer U42B. This data buffer is enabled, from multiplexer U29, in program sequence to transfer the encoder data to data lines FP0 and FP1 for processing as described in Paragraph e.

c. Audio and IF. Audio and IF controls and an audio phones jack are contained on the front panel for control and monitoring of these functions. Control and audio to and from these components are routed through the A9 circuit card from the A4 circuit card with no connection to the in-out digital control hardware on A9. A complete description of their function can be found in Paragraph 5-13.

d. Liquid Crystal Displays. Two Liquid Crystal Displays (LCD) are contained on the front panel for displaying Receiver status. Receiver frequency and BFO frequency are displayed on LCD U3 while Receiver mode, AGC mode, tuning mode, remote/local mode, bandwidth and AF/RF metering are displayed on LCD U4. The 8-line data bus is routed directly to ten 4-line LCD drivers (U19-U22, U36-U40 and U49) and to thirteen BCD to seven segment decoder/drivers (U10-U18 and U31-U34). The ten line drivers provide decoding and drive for all annunciator

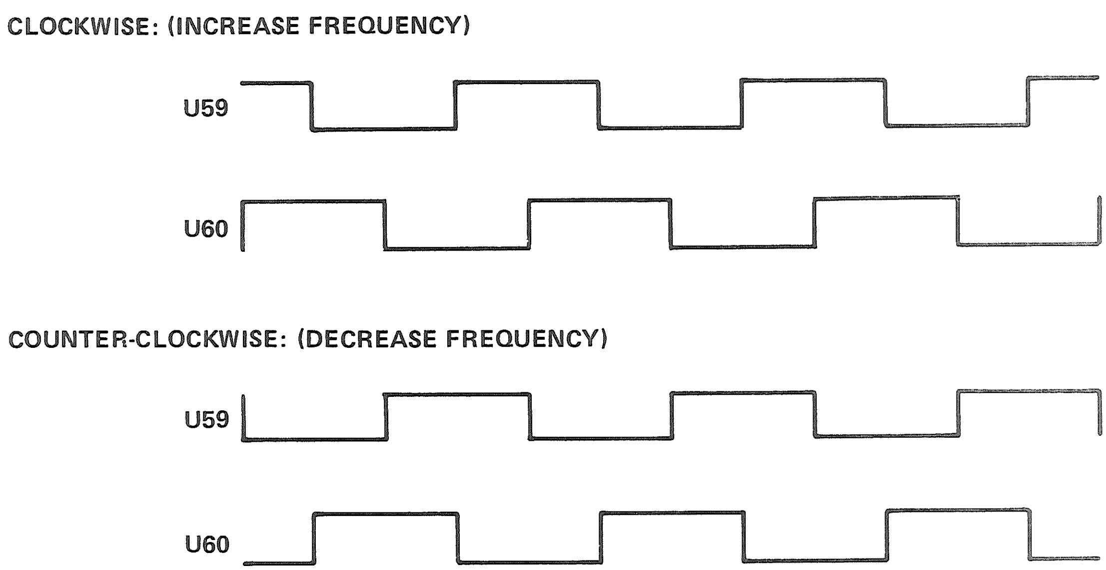


Figure 5-17. Encoder Output Signals

displays while the thirteen 7-segment drivers provide decoding and drive for all numerical displays. Multivibrator U26, timed by R1 and C8, provides a 100 Hz signal to the DF (display frequency) inputs of the line drivers, the BP (backplane) inputs of the 7-segment drivers and the two LCD's. This signal is used to drive the LCD's display. (NOTE: LCD displays operate from low frequency square wave pulse trains. The contrast of the display being a function of the frequency.) Timing to the line drivers is provided by strobe signals from BCD to decimal decoder U50 while the 7-segment drivers receive timing from 4-bit latch and decoder U35. These two decoders receive their input from binary counter U51. The clock pulse (CP) for U51 is derived from three strobes S7, S11 and S15 combined by NOR gate U48A. Decoder U35 is controlled by inversion of strobe S7 through U48B while U50 is timed by strobe S15 through inverter U56. When a strobe signal in program time enables a line driver or 7-segment driver, the data at its input port is latched into the driver. The 100 Hz signal on the DF or BP input of the drivers is applied to the display segments and is inverted or not inverted through control of the data input to each driver. This in turn controls whether the segment is turned on or off. Any segment of an LCD is turned on by a 180 degree difference of phase between segment input and the main backplane drive to the LCD (see Figure 5-18). To turn the display segment off the phase difference between these two signals must be zero degrees; that is, the two signals must be in phase (see Figure 5-18).

e. Circuit Card A9. Receiver Control Circuit Card A9 routes data, entered at the front panel, to the microprocessor bus and routes processed data from A6A2 to various Receiver functions on A4, A5, A7 and A8 circuit cards. This data flow in the data bus IOD0 through IOD7 is controlled by read, write and address controls (IOC0 through IOC7) signals from the microprocessor. All data entered from the front panel except audio and IF functions described in Paragraph c, is transferred to the microprocessor for processing, then routed back through A9 to various Receiver functions. Data entered from a remote location is routed to the microprocessor, then the processed data is routed to various Receiver functions through A9 in the same manner as processed front panel data.

(1) Data In/Out Control. Data flow between the A9 circuit card and the microprocessor is via their respective 8 bi-directional data lines. The flow of data from A9 to A6A2 and vice versa is buffered and controlled by U27, U28 and U46. The bi-directional switches U27 and U28 are configured to transfer data from A9 to A6A2 when enabled in a READ cycle via inverter U56. The tri-state, 8-bit latch U46 is used to transfer data from A6A2 to A9 during a WRITE cycle under the control of the WSTB signal. Control signals (IOC0 through IOC3) from the microprocessor are used to generate strobe signals through 4-bit latch to 16-line decoder, U47. The strobe signals are timed through the WSTB signal to the strobe input of U47 and from multivibrator U55A and U55B. The multivibrator, controlled from the WSTB signal and inverted IOC5 signal through NOR gate U48, provides timing to the inhibit input of U47. The strobe signals (U47 outputs) are then latched in proper timed sequence and are used to time latches, decoders, gates, etc., that in turn control data flow to various Receiver control functions or displays. The data flow through these components and the strobe signal functions are described in the various Receiver functions that follow.

(2) Receiver Frequency. Processed Receiver frequency data from the microprocessor is routed through data line FPO to one input of two input AND gate U57A. The second input to the AND gate comes from the Q0 output of decoder U64 which receives its input from presettable binary counter U51. Strobes S5 and S7, S11 and S15 through NOR gate U48 time U51, strobe S11 through inverter U56 time U64. The frequency data in proper timed sequence is serially routed through AND gate U57A to the A7 circuit card. Strobe signal S12 and the Q0 output of U64 are connected to two input AND gate U57B whose output is routed to A7 as a clock signal for circuits on that card. The Q0 output of U64 is also routed to A7 through inverter U56 as a strobe signal to those same circuits. These circuits on the A7 circuit card further process

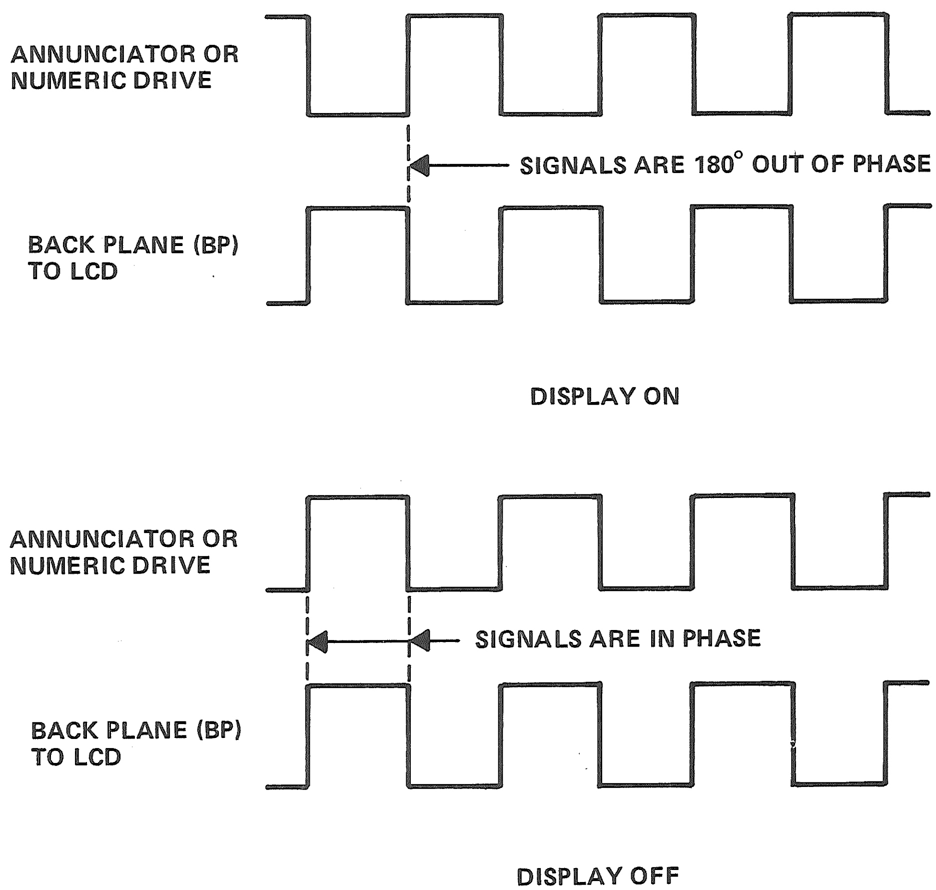


Figure 5-18. Liquid Crystal Display Control Signals.

the serial frequency data in conjunction with the clock and strobe signals, and adjust the oscillator frequency as first directed from the front panel or remote location.

(3) BFO Frequency. BFO frequency data after being processed by the microprocessor (A6A2) is routed through data lines FP0, FP1 and FP3 to the same binary counter (U51) as the Receiver frequency data. Outputs (Q1, Q2 and Q3) of the binary counter are connected to the three binary inputs of four 8-bit addressable latches U61 through U64. These latches supply the BCD inputs to a programmed divider circuit on the A8 circuit card for BFO frequency control. Timing for the latches is supplied by strobe S11 through inverter U56. The Q4 output of latch U61 provides a signal through transistor Q2 that enables the BFO synthesizer on A8 in CW and SSB/ISB modes.

(4) Circuit Card A4 Functions. All eight data lines along with six strobe signals are routed to control circuits on the A4 circuit card for control of various Receiver functions operating on this circuit card. The control circuits (located on A4) are a direct function of the A9 interface circuits; therefore, a description of their operation is included in this paragraph. All references to components in this paragraph (unless otherwise noted) refer to components on the A4 circuit card. Refer to Figure 8-5 for the schematic diagram of this circuit card. The eight data lines of A9 are routed to 2-level translators (U3 and U5) on the A4 circuit card. Six strobe signals (STB10 through STB15) are also routed to A4 with strobes STB12 through STB15 connected to the input of level translator U16. These level translators provide a new voltage level to the incoming data for operation of circuits on the A4 card. The strobe outputs from translator U16 are used to clock data latches U2, U4, U13, U15 and U23, the digital-to-analog converter U21, and the crosspoint switch U25. The data bus output from translators U3 and U5 is routed to these components and applied to the various A4 functions as directed by the strobe signals. Data latch U2 is used to select the bandpass filters, but through BCD to 1 of 10 decoder U1. This decoder has only one output high at a time as directed by the BCD input. This allows selection of filter slots FL2 through FL7 in accordance with the three digit BCD on the data line as clocked by strobe 12 on the clock input of U2. The Q4 output of U2 is routed directly to the diode switch of FL1 which is used to select that filter slot at the appropriate program time. Data through data latch U4 is used to control the RF switch that selects between BFO and the IF signal for input to the limiting amplifier and FM detector and D flip-flop U9A. This flip-flop controls the AGC dump line. Data latch U4 is also timed by strobe 12. Data through data latches U13 and U15 control switches in the AGC circuits for various AGC modes. These latches are timed through strobe 13. The output of data latch U23, timed by strobe 15, controls the detector select switch U19A, an audio filter level control switch U19B and an AF meter audio select switch U19C. All eight data lines are connected to the digital-to-analog converter for digital control of its analog output. This unit is timed through strobe 14 and is used to provide analog-to-digital conversion of the DIV AGC line and audio line by peak detector U22A using a successive approximation technique. The digital information gathered by the microprocessor is used for front panel metering. Five data lines are routed to crosspoint switch U25 which is timed by strobe S15. The audio function of the crosspoint switch along with other A4 functions controlled through A9 are described under the A4 circuit card in Paragraph 5-13.

(5) Circuit Card A5 Functions. Two data latches on the A5 circuit card are used to control AGC circuit functions on this circuit card. The two latches U7 and U8 have A5 reference designators and are shown on the A5 schematic diagram in Figure 8-6. The 8-line data bus from translators (described in Paragraph 4) on the A4 circuit card are routed to the data latches with strobe 10 timing both latches through transistor Q6, also located on A5. The data output from the latches is used to control the AGC circuits described under the A5 circuit card in Paragraph 5-14.

(6) Out of Lock (OOL) Functions. Three out of lock circuits, that monitor the

condition of the phase lock loops of the three oscillators, drive OOL indicators on the A9 circuit card and supply their output data to the microprocessor. This data is routed through circuits on the A9 card that drive a fault indicator on the front panel and also a fault indicating circuit that provides a TTL level related to the FAULT condition to connector J3 on the rear panel via A4 circuit card. The three OOL circuit outputs from the three oscillator phase lock loops are connected to the S inputs of dual D flip-flops U45 and U54. These flip-flops are clocked from address multiplexer U29. With the data and reset inputs tied to ground (low) and the S inputs low (phase lock loop in lock) the Q outputs of the flip-flops will be low. If an S input goes high (out of lock) its Q output will go high causing a low through its respective inverter U44A, U44B or U53A. This in turn will enable the applicable LED indicator DS1, DS2 or DS3. These LED indicators are located on the A9 circuit card for accurate determination of the OOL circuit. The Q outputs of the flip-flops are also connected to the inputs of buffer U43 which is also timed by multiplexer U29. The buffer, in program sequence, outputs the status of the OOL circuits on the data bus which is then routed to the microprocessor. The processed FAULT data is routed through binary counter U51 and decoders U63 and U64. The Q5 (FAULT) output of decoder U63 is routed through inverter U52B to the rear panel while the Q5 (FAULT) output of U64 drives the front panel fault indicator through inverter U52A.

(7) AF/RF Meter Comparator Functions. The main RF, ISB RF, and AF comparator circuits along with an ISB fitted circuit from the A4 circuit card are connected to four inputs of non-inverting buffer U42A. The inputs are strapped to +5 volts through 22K ohm resistors in resistor array U41. When the optional A5 circuit card is installed, input I1 is strapped low through a grounding circuit on that card. The three comparator input (I2, I3 and I4) levels depend on the comparator outputs. Buffer U42A is timed from multiplexer U29 and in program sequence transfers the comparator data as used by A6A2 in a successive approximation technique to generate a bar graph for front panel display to data lines FP0, FP1 and FP2 and the ISB fitted status to data line FP4.

(8) Power Supply Distribution. The A9 circuit card provides a distribution path for dc power, generated from the A10 power supply module, directly to circuit cards A4, A6A2, A7 and A8. This dc power through A9 is further distributed through the A4 circuit card to the optional A5 circuit card and through A6A2 circuit card to optional A6A1 circuit card. The +15 volts dc is also routed to the front panel for operation of the LCD back lighting. The distribution of this dc power is as shown below.

DC Power	From A10 To A9J4 Pin Numbers	Output To A4 from A9J5 Pin Numbers	A6A2 from A9W1 Pin Numbers	A7 from A9J6 Pin Numbers	A8 from A9J7 Pin Numbers
+5 Volts	3, 4, 7 and 8	1	23 and 24	20	26
+5 Volts (unregulated)	9 and 10		15 and 16	15 and 16	
+15 Volts	13, 15, 19, 21 and 22	2 and 4	19 and 20	17 and 18	24
+15 Volts (unregulated)	5 and 6	8			
−15 Volts	18 and 20	6	21 and 22	14	22
+20 Volts	1 and 2				

5-18. **MICROCOMPUTER BOARD A6A2.** A functional description of the microcomputer board A6A2 is given in Paragraph 5-6 with a functional block diagram shown in Figure 5-20.

a. As shown on the electrical schematic diagram, Figure 8-9, the microcomputer board A6A2 makes use of a type 3850 CPU (U1). The 3850 CPU is from the Fairchild F8 microcomputer component family. A detailed description of the microcomputer family operation, including timing and instruction set, is given in the F8 Users Guide. This guide is available from the Fairchild Camera and Instrument Corporation, Mountain View, California.

b. The CPU (U1) controls Receiver operation by reading the operating program and routing data and control signals throughout the Receiver based on the procedures and algorithms of this program. The CPU 8-bit data word bi-directional ports (DB0-DB7) connect to an 8-line data bus. This bus is common to major Receiver control circuitry (directly or through buffers) and is the primary means of communication between the CPU and other parts of the Receiver.

c. The CPU clock is provided by the 2.0 MHz crystal Y1 which is connected across pins 38 and 39 of the CPU. The Φ and Write pulse outputs (shown in Figure 5-19) are clock outputs which provide timing drive for all microcomputer circuitry. The ROMC-0-4 outputs from the CPU connect to other circuits in the Receiver and identify operations which these circuits must perform during any instruction cycle. Interrupt requests are received through the /INT REQ port while the acknowledgement that the CPU will respond to the interrupt requests is routed through the /ICB port. The Input/Output (I/O) ports 00-07 and 10-17 are ports through which the CPU communicates with logic external to the microprocessor. Here, seven of these ports are used and are connected to the serial asynchronous interface module A6A1 (when it is installed in the Receiver).

d. Figure 5-20 is a functional block diagram of the CPU. The inputs and outputs, described previously, are shown as well as the basic functions performed by the CPU. The CPU performs instructions which are obtained from the control program contained in the program memory (EPROMs, U5, U6 and U14). These instructions are routed to the instruction register of the CPU and then carried out during instruction cycles. The control unit logic of the CPU sends out the ROMC signals to other parts of the Receiver during each instruction cycle. These specify the functions to be performed for each instruction. There are four or six clock periods (Figure 5-19) in an instruction cycle (dependent upon the number of 8-bit instruction words required), which are determined by the ROMC signals generated by the CPU. The CPU performs computations, when required by the program, in its ALU (Arithmetic Logic Unit) making use of the accumulator, status register and scratch pad memory registers. The ISAR (Information Storage Address Register) is the address register for the scratch pad memory.

e. The CPU receives and follows the program (sequence of instructions) which is stored in the erasable/programmable read only memory (EPROMs) contained in U5, U6 and U14 (Figure 8-9). These are type 2716 EPROMs. Each of these units contains 2K 8-bit words for a total of 6K 8-bit words of programmable memory. The CPU also uses the temporary Random Access Memory (RAMs) contained in U7 and U8. These are type 5101L RAMs and provide 256 8-bit words of working memory (temporary data storage). U7 provides 4 bits of each 8-bit word and U8 provides the remaining 4 bits of each word.

f. The memories are addressed by the CPU through U2, the Static Memory Interface (SMI) type 3853 (Figure 8-9). The CPU sends the ROMC-0-4, Write and Φ signals to the SMI. The SMI, in timed sequence, recognizes the ROMC-0-4 code for a memory access operation, and addresses the appropriate memory, program (EPROM) or working (RAM), over the address bus A0-A10. The SMI (U2) address outputs A11 and A12, through decoders U3A and U3B are also

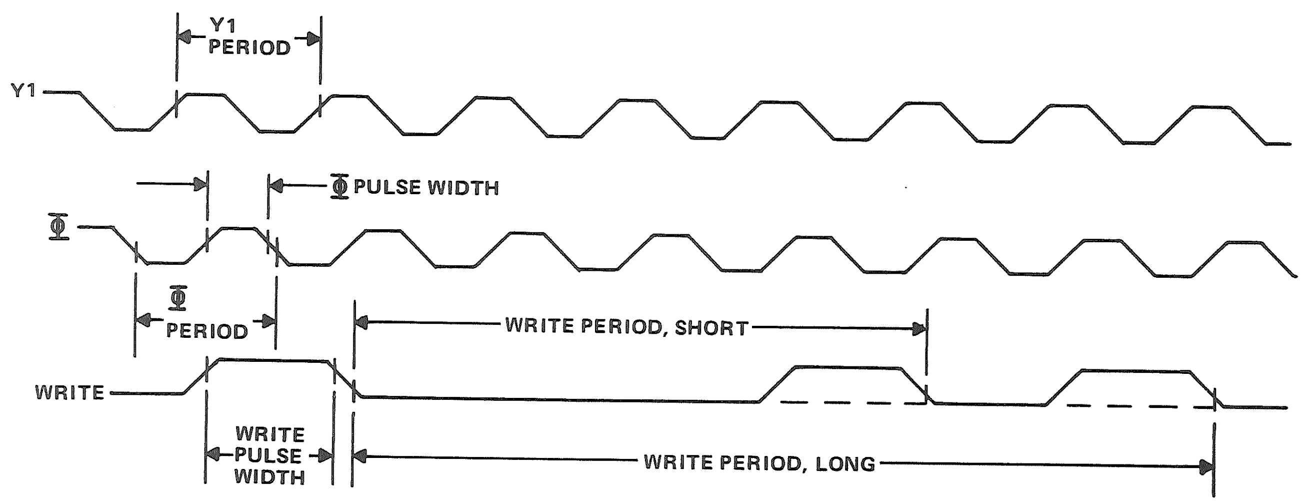


Figure 5-19. Central Processor Unit Timing Signal Diagram

used in addressing by enabling the appropriate memory chip U5-U8 and U14. Directed by the ROMC-0-4 code and write signals from the CPU, the SMI also directs reading or writing through its CPU READ and /MEM W outputs. Thus, the memory units (when addressed and directed place data on the CPU data bus or accept data from the CPU data bus (DB0-DB7). The EPROMs place 8-bit instruction words on the bus and the RAMs supply data to or read data from the bus when addressed and directed by the CPU under program control.

g. Figure 5-21 is a functional block diagram of the System Memory Interface (SMI). The inputs and outputs, described previously, are shown. The SMI contains the program counter which contains the program memory address (at which instructions are located) and the data counters which contain the working memory (RAM) addresses. The program counter is either incremented as each instruction in the program is executed or new addresses are inserted by the program or by the interrupt address vector. The working memory addresses are generated by the program. The SMI also contains a timer which is used to generate internal interrupts for initiating program sub-routines at required times during the program cycle.

h. As described previously, the CPU (under program control) writes and reads data to and from the front panel controls and displays and the Receiver circuitry. This data consists of front panel control settings, display readouts and Receiver circuit control and status signals in the form of 8-bit digital words. The CPU data bus (D00-D07) connects to these units via the tri-state bi-directional switch U4 (Figure 8-9) and then through the bi-directional data bus (IOD0-IOD7). The direction of data flow and timing of switch openings are controlled through pins 1 and 19 of U4. Signals to these pins are generated by the strobe logic gates U10-U12 and the Q7 output from the tri-state latched switch U13 at the appropriate times in the program. The strobe logic inputs consist of the ROMC-0-4 and write signals. Thus, at appropriate program times, the CPU data bus connects through U4 and through pins 1-8 of connector J2 to the front panel and Receiver control circuitry. Also, outputs /IO READ and /WSTB from pins 25 and 27 of J1 go to the front panel and Receiver control circuitry to direct reading or writing data from or to the bus at the appropriate times in the program. The U13 latched outputs (IOC0-IOC7) provide the programmed codes for the selection (or addressing) of the various elements in the front panel and Receiver control circuitry (to accept or supply data from or to the common data bus) at appropriate times in the program. These addresses (IOC0-IOC7) are latched into the U13 outputs from the CPU data bus (D00-D07) at the proper times in the program through the U13 OE (output enable) and CP clock inputs. The OE and CP inputs are generated by the ROMC-0-4 and write outputs from the CPU through gates U10 and U12.

i. As described previously, the CPU also receives and sends data from and to the Serial Asynchronous Interface modules (A6A1) via the data bus. This data consists of commands and Receiver settings to the CPU and Receiver status to the remote controller in the form of 8-bit digital words. Connections between these units are made through connector J2. The data bus to the Serial Asynchronous Interface module is labeled PB0-PB7. The microcomputer receives the interrupt request (/INT REQ) signal from the Serial Asynchronous Interface module. The CPU also sends the WRITE, Φ timing signal, strobe logic outputs /IO READ and /WSTB, the tri-state latched outputs IOC0-IOC7, the ROMC-0-4 outputs, the CPU 00-07 and 10-17 outputs and the interrupt acknowledge /ICB signal. These signals are used to direct operations of the interface module and to synchronize operations between the CPU and the remote controller, as will be described later.

j. The reset and memory retention system is composed of stages Q1 through Q7, the 2.0 volt internal power source BT1, R9, CR3 and C16, and the battery charging circuitry, CR6, R9. At Power On, the +5 volt unregulated line (from pins 15 and 16 of J1) switches Q1 and Q2, bringing the /RESET line high. Also at Power On /RESET turns Q4 and Q5 on, C15 is charged,

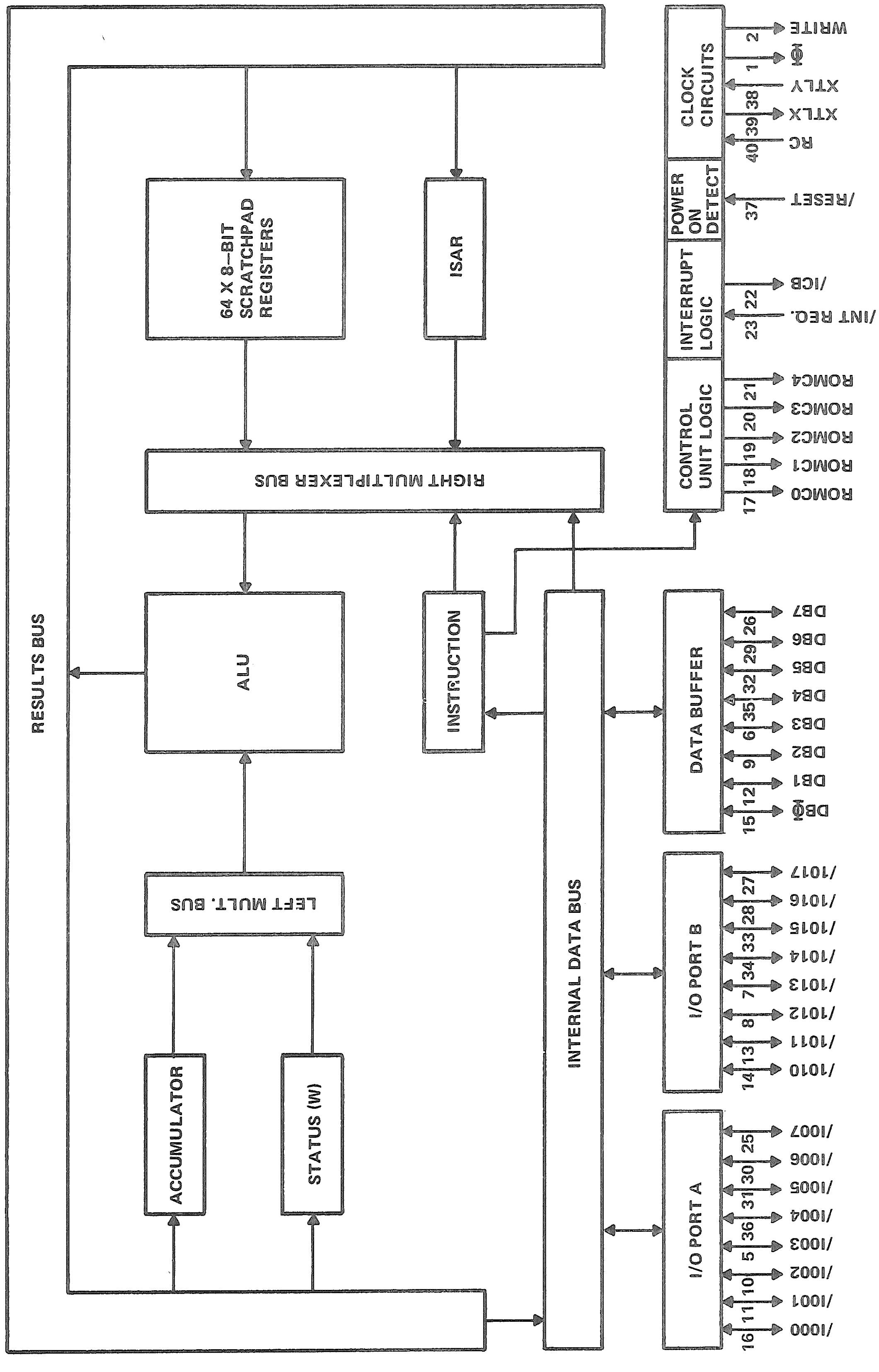


Figure 5-20. Central Processor Unit Functional Block Diagram

the gate of Q6 is taken negative and CE2 of the RAMs (U7 and U8) is asserted. This activates the RAMs in their normal operating, higher power drain, mode. Also, the gate of Q7 goes negative taking the low off the CPU RESET. The CPU now starts the initialization process. During the turn on cycle the +12V through R8 quickly turns on Q3, charging C16, which supplies Vcc to the RAMs. CR2 limits the voltage to Vcc while R11 limits the current. CR3 is back biased and the +5 volt supply through CR6 and R9 charges the internal battery BT1.

k. The Schmidt trigger, Q1 and Q2, detects voltage variations in the +5 volt unregulated line. The collector of Q2 will go to ground when the power supply +5 volt unregulated line decreases (such as at power turn off or failure) past the trigger levels set by CR1 and R2-R5-R6. When this occurs, the /RESET line goes low. Also, the voltage at D of Q7 going low, instructs the CPU to come to a stop at the end of the next execution cycle. At power down, Q3 will stop conducting. Initially, the voltage across C16 still supplies sufficient VDD voltage to the RAMs for the CPU to complete its cycle. When the voltage across C16 falls to approximately 2.4 volts the internal battery BT1, through R9 and CR3 supplies the memory retention power to the RAMs. The voltage out at D of Q6, now low, sets the RAMs at their lower power drain memory retention mode. The battery leakage is greater than the retention memory current drawn by the RAMs; therefore, several months of memory retention is available.

l. As indicated in Figure 8-9, the CPU may receive an interrupt request (/INT REQ) into its pin 23 from the SMI (internal interrupt) or from the Remote Controller Serial Asynchronous Interface (when used) through J2. During an interrupt routine, the CPU will assert its /ICB output (from pin 22), thus not accepting any further interrupts until it has completed the routine. When a Remote Controller Serial Asynchronous Interface is not used, with no J2 connection and with LINK 1 installed (see Figure 8-9), the /ICB output from the CPU connects directly to the /PRI IN input of the SMI. This prevents an internal interrupt from being generated by the SMI until any previously accepted interrupt has been serviced by the CPU. When a Remote Controller Serial Asynchronous Interface is used with the interface connected to J2 and LINK 1 removed, the /ICB output goes directly to the Serial Asynchronous Interface circuitry. As will be described in more detail later, this prevents the interface from generating an external interrupt until any previously accepted interrupt has been serviced by the CPU. In addition, the PRI input (into pin 24 of J2) from the Serial Asynchronous Interface goes to the /PRI IN of the SMI. The Serial Asynchronous Interface is waiting to request an interrupt. Thus, the SMI cannot generate an internal interrupt while either of these conditions exist. It will be noted that the DR and TBRE outputs from the UART (in the Serial Asynchronous Interface, see Figure 8-8) are sent out through connector P1, pins 37 and 36, to the CPU I/O terminals 11 and 10. These are used by the microcomputer to determine whether the interrupt request was for a receive or transmit routine.

m. The error outputs from the UART; PE (parity error), OE (overload error) and FE (framing error) are sent to the CPU I/O ports 14, 13 and 12 through connector P1 pins 5, 43 and 42.

5-19. SERIAL ASYNCHRONOUS INTERFACE MODULE A6A1. A functional description of the Serial Asynchronous Interface Module is given in Paragraph 5-6 in conjunction with the functional block diagrams, Figure 5-16.

a. Figure 8-8 is the electrical schematic diagram of the Serial Asynchronous Interface Module A6A1. This module interfaces an external remote controller (when used) through a serial data line to the microcomputer through an 8-bit data bus. The Universal Asynchronous Receiver transmitter, UART (U9), provides the interface between the serial data lines to and from the remote controller and the microcomputer parallel data bus (PB0-PB7).

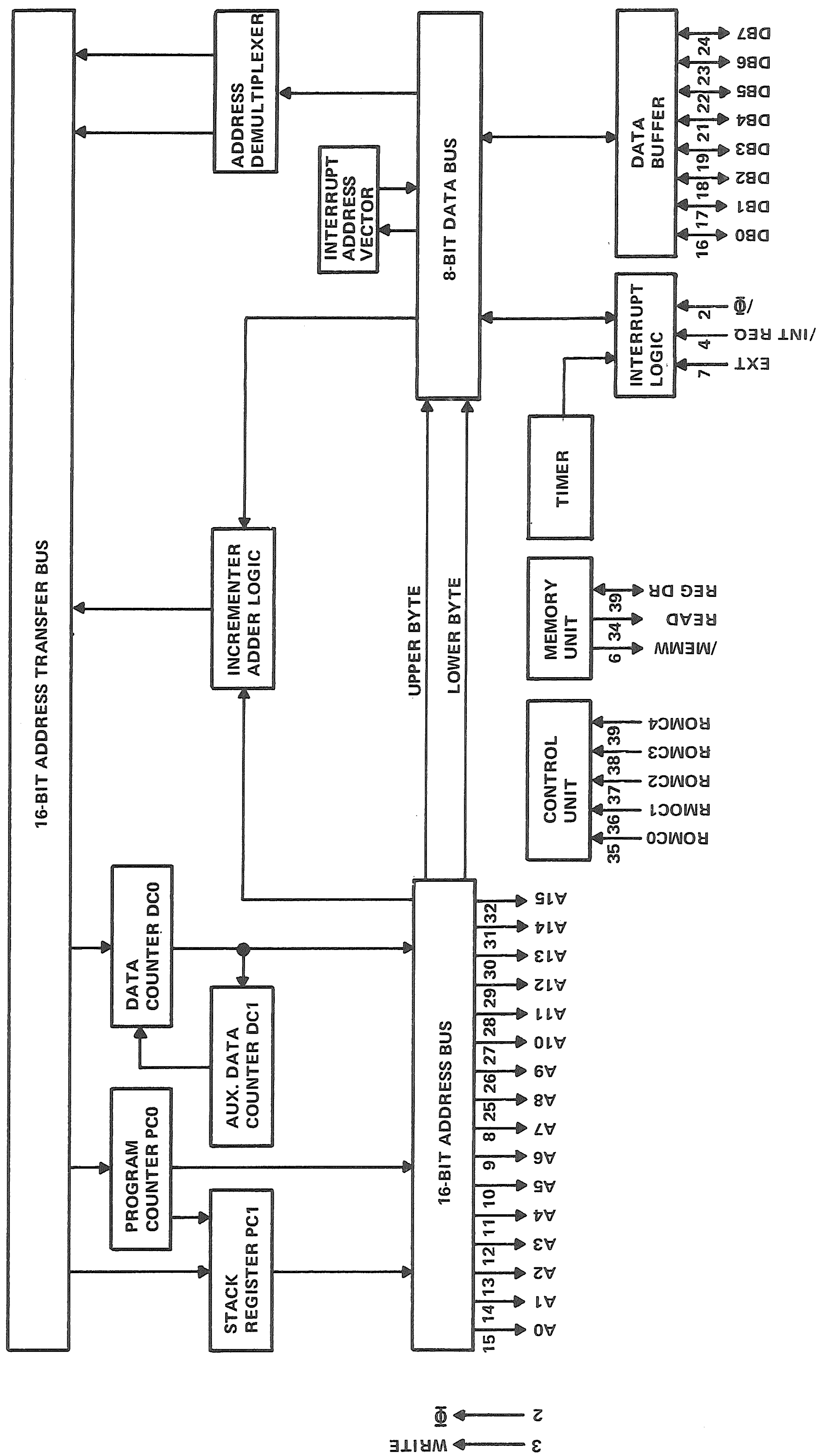


Figure 5-21. System Memory Interface Functional Block Diagram

b. The UART contains a transmit and a receive station. A block diagram for each of these sections is shown in Figures 5-22 and 5-23. The receive section converts the incoming serial stream (from the remote controller into the pin 20 RR1 input) to 8-bit parallel words and places them on the microcomputer bus through output pins 5 through 12. The transmit section, when directed by the microcomputer (through pin 23, data strobe TBRL) takes the 8-bit parallel words from the microcomputer data bus (through pins 26-33) and puts them in a serial format for serial transmission to the remote controller (through pin 25). The serial format, as described previously in Paragraph 4-6, is an 11-bit word containing one start bit, the 7-bit ASCII Code data word, a parity bit followed by two stop bits. Coding for the data word is described in Paragraph 4-6. The UART parallel inputs and outputs are tied together and onto the common microcomputer data bus (Figure 8-8). The UART Receiver inputs and outputs are tri-state, with only inputs or outputs activated at one time.

c. The UART is initialized by the /RESET line from the microcomputer, through pin 2 of connector P1 and inverter U6A, into its MR (pin 21) input. Transmit and receive clock signals, TRC and RRC (pins 40 and 17), which determine the rate of data transfer, are supplied by the programmable Baud Rate generator U4. This generator divides the frequency of crystal, Y1, down to the programmed transmit and receive clock rates. Both the receive and transmit clock rates are set at 16 times the baud rate. The frequency generated by U4 is obtained from the data bus, upon initialization by the microcomputer program from information supplied by the configuration set on the rear panel cover into its input RA-RD and TA-TD. This data is strobed into U4 by the strobing signal from output VO (pin 14) of decoder U19. This decoder is driven by microcomputer address and strobing signals IOC0-IOC1, IO READ and /WSTB.

d. As indicated by Table III on the A6A1 schematic diagram the baud rate is set by connecting the appropriate A6A1W1J1 external connector terminals W, X, Y and Z to common. Terminals not connected to common will have +5V connected through U1. These terminals connect to inputs of tri-state buffer U12. The inputs are strobed onto the data bus (to go to the baud generator inputs, at the appropriate times), by the strobe signal out of X1 (pin 4) of decoder U19. The baud rate is set to match that of the Remote controller. Table 2-7 gives information for setting the baud rate.

e. Also strobed, upon initialization, from output Y1 of decoder U19 is the CRL (pin 34) input to the UART. This loads the UART control register with the EPE, CLS1, CLS2, SBS and P1 inputs at that time. This sets whether parity is used (P1) odd or even parity (EPE), number of bits in a data word (CL1, CL2) and number of stop bits (SBS) used. As described previously, the word length is fixed at 8 and the number of stop bits is fixed at 2. Table I on the schematic shows that the parity (ON or OFF) and even or odd parity are set through terminals U and V of external connector A6A1W1J1. These are also set by connecting the appropriate terminals to common ground. The unconnected terminals will have +5V connected through U1. These terminals also connect to tri-state buffer U12 and are strobed on to the data bus (and to P1 and EPE) at the appropriate time by the strobe signal out of X2 (pin 4) of decoder U19.

f. The Receiver number for remote addressing is selected by connecting the appropriate terminals K, L, M, N, P, R, S, T of connector A6A1W1J1 (See Table I on schematic) to common. This setting through tri-state buffers U11 and U13B and Pull-up resistors U10 and U1 is strobed onto the data bus, for readout by the microprocessor, by the strobe from X1 (pin 3) of decoder U19.

g. Receiving Data – Figure 5-23 is a block diagram of the receive station of the UART. When data is received from the remote controller, it comes through the external connector A6A1W1J1 to Receiver U2. Receiver U2 yields signals that are compatible to the receiver

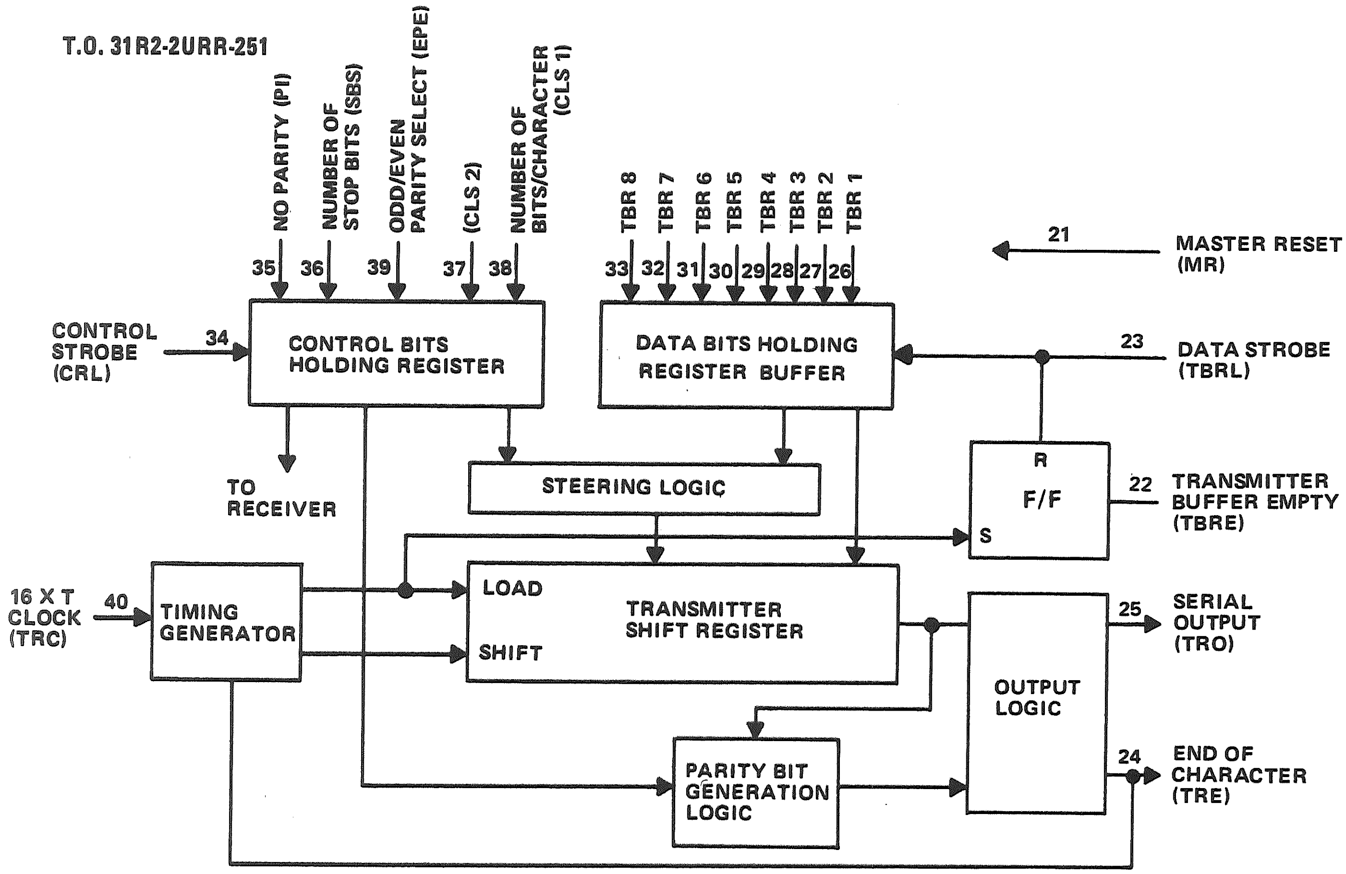


Figure 5-22. UART Transmitter Functional Block Diagram

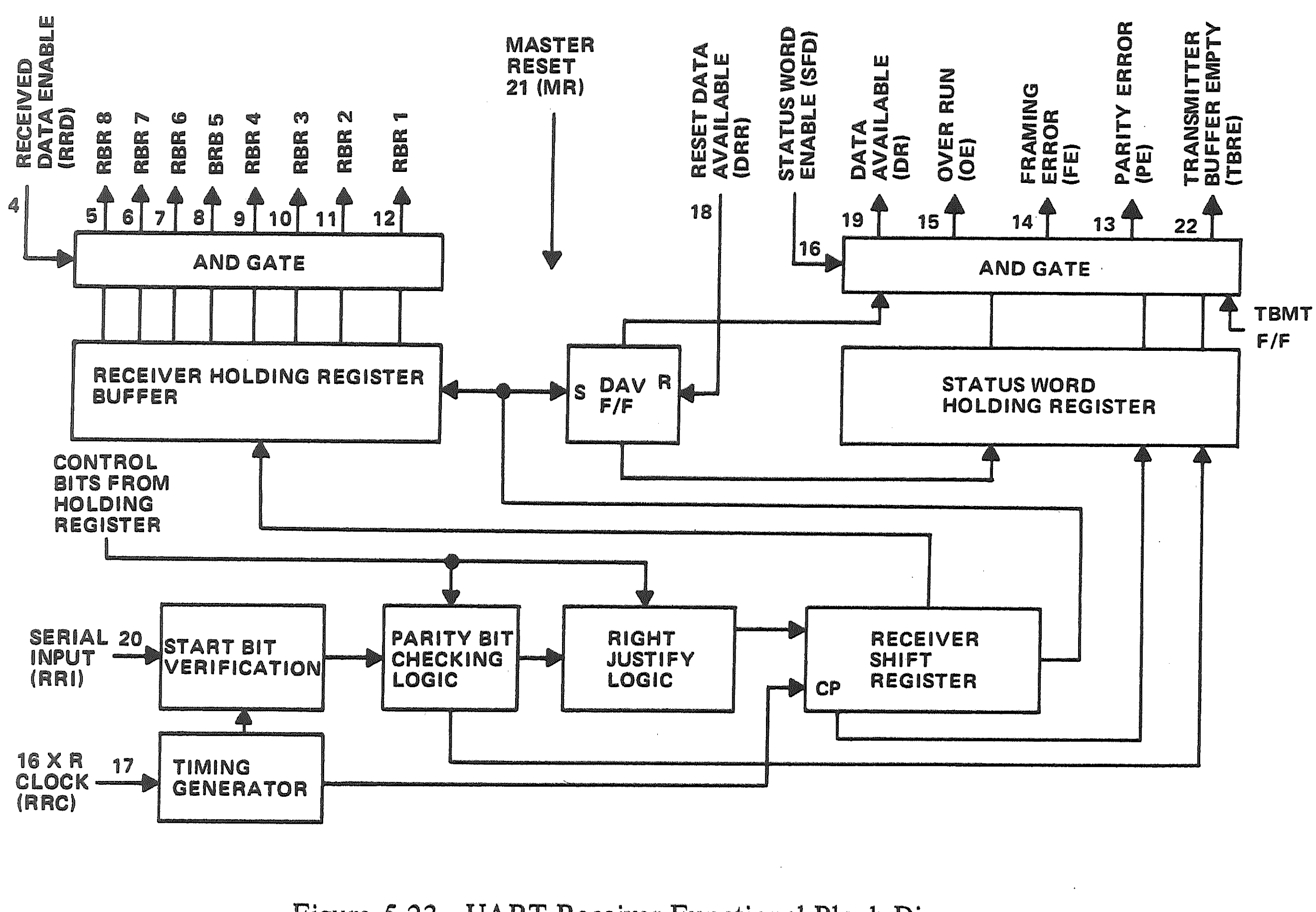


Figure 5-23. UART Receiver Functional Block Diagram

circuits of the UART (U9) through its RR1 input (pin 20). The UART Receiver section converts the incoming serial data stream from the remote controller to 8-bit parallel words and places them on the microcomputer bus (PB0 through PB7) through outputs RBR1 through RBR8. The serial format, as described previously in Paragraph 4-6, is an 11-bit word containing a start bit, a 7-bit ASCII code, a parity bit followed by two stop bits. Instruction word codes are also described in Chapter 4. When data is available from the remote controller, an interrupt request is made by asserting the DR output, indicating data is available to the microcomputer. The DR output will go through gate U8A, if not inhibited by computer outputs 00 and 01 (microcomputer not accepting these interrupts), and then through gate U8B, at the correct time (ROMC inputs through U17A, U6C, U16B-D, and U17B) to drive flip-flop U16A. The outputs of this flip-flop drive one of the two inputs to each of gates U15B and U15C. The other input to these gates is the inverted /ICB signal from the microcomputer. If the CPU is currently blocking, thus ignoring interrupt requests, /ICB will be high. Under this condition U15B and C gates are inhibited. When /ICB is not high (microcomputer accepting interrupts), gates U15B and C are enabled. The output from U15B, through switch U14B, sends the /INT REQ to the microcomputer (through pin 27 of P1) to initiate an interrupt. The microprocessor will orderly stop its normal Receiver monitoring functions as directed by the control program (from EPROM) and start the interrupt routine to accept data from the remote controller.

h. During the interrupt routine the microcomputer asserts its /ICB output, thus not accepting any further interrupts until it has completed the routine. It will be noted that the DR output from the UART are routed through connector P1, pin 37 to the microprocessor I/O terminal 11. This input enables the microcomputer to determine that the interrupt request was for a receive routine.

i. Transmitting data – Figure 5-22 is a block diagram of the transmit section of the UART. When the remote controller has requested data (status) and the transmit buffers of the UART are empty, so that it can accept data from the microcomputer for transmission to the remote controller, the TBRE output is asserted. The TBRE signal will go through gate U8A, if it is not inhibited by microcomputer outputs 00 and 01 (microcomputer not accepting interrupts), and then through gate U8B, at the correct time (ROMC inputs through U17A, U6C, U16B-D and U17B) to drive flip-flop U16A. The outputs of these flip-flops drive one of the two inputs to each of gates U15B and U15C. The other input to these gates is the inverted /ICB signal from the microcomputer. When the CPU in the microcomputer is busy and ignoring interrupt requests, /ICB will be high. Under this condition U15B and C gates are inhibited. When /ICB is not high these gates (U15B and C) are enabled and the /PRI output from U15C is output through pin 24 of P1. The output from U15B, through switch U14B, sends the /INT REQ to the microcomputer (through pin 27 of P1) to initiate an interrupt. The microprocessor will orderly stop its present program and start the interrupt routine to send Receiver status to the remote controller. During the transmit interrupt routine the microcomputer asserts its /ICB output, and will not accept any further interrupts until it has sent the status data to the remote controller. The TBRE output from the UART is routed through connector P1 pin 36 to the microcomputer I/O terminal 10 to identify the interrupt as a transmit routine. The serial output from the UART is output TR0 (pin 25) and is routed through line driver U3 to the remote controller through external connector A6A1W1J1.

j. Connections between the serial asynchronous interface module and the remote controller may be selected to accommodate signals compatible with MIL-188C/RS-232C, RS-423 and RS-422. The selection is made by connecting the remote controller to the interface external connector A6A1W1J1 in accordance with Table II (shown on the schematic) and using the links (on the Serial Asynchronous Interface module) in accordance with Table IV (shown on the schematic).

k. The interrupt circuitry on the A6A1 module not only generates the interrupt request, but it also provides the microcomputer with the interrupt vector. This is the program memory address at which the interrupt routine starts. A specific sequence of ROMC signals (put out when the CPU expects the interrupt vector address) is detected by gates U15D, U15A and flip-flops U16C, U16D and U16A. When these signals are received, gate U15A enables switches U13A and U14A to output the interrupt vector on the data bus to be read by the microprocessor.

5-20. **POWER SUPPLY, A10.** The Receiver contains a power supply module that provides the power required for operation of the Receiver. Refer to schematic diagram, Figure 8-13. The module operates from an ac line input, steps down the voltage, rectifies the ac, filters and regulates the various divided voltages. The unit contains a circuit card switch which provides for switching the transformer input for 100, 120, 220 or 240 volts ±10% operation from the input power line. This line frequency can be between 43 and 420 Hz and is controlled through the POWER-ON toggle switch located on the front panel. The input power is also fused through F1, located on the rear panel for easy access. The 100 or 120 volt input must be fused differently than the 220 or 240 volt input. The alternate fuse is contained in a fuse holder located inside the power supply.

a. DC Power Output. The secondary of transformer T1 contains three separate windings that provide the six different dc outputs for Receiver operation. These six dc outputs, along with their tolerances are listed below:

+20 ±1 volt
+15 ±0.5 volt
+15 volts unregulated (nominally +22 volts)
−15 ±0.5 volt
+5 +0.5 −0.2 volts
+5 volts unregulated (nominally +10 volts)

(1) Conventional bridge rectifiers CR1, CR2 and CR3 provide ac to dc rectification while capacitors C1, C4, C7 and C10 provide filtering and to smooth the pulsating dc. Capacitors C1 through C9 are connected adjacent to the three voltage regulators to suppress possible oscillations. The rectified and filtered dc from one winding 12 to 13 of the transformer is coupled to dc regulator A10A2, which provides the regulated +20 volts to pins 1 and 14 of A10J3. Winding 6 to 8 provides the +15 volts unregulated to pins 3 and 16, the +15 volts regulated through regulator U2 to pins 7, 8, 10, 11 and 24 and the −15 volts regulated through regulator U3 to pins 22 and 23. Winding 9 to 11 provides the +5 volts unregulated to pins 5 and 18 and the +5 volts regulated through regulator U1 to pins 2, 4, 15 and 17 of A10J3. The six dc outputs from A10J3 are routed to various applications throughout the receiver circuitry.

SECTION III. FUNCTIONAL OPERATION OF MECHANICAL ASSEMBLIES

5-21. **TUNING ENCODER.** This section contains a description of the mechanical operation of the tuning encoder. The encoder provides a means of selecting either the BFO or reception frequency through the tuning knob located on the front panel. The tuning knob controls the operation of the optical encoder while keypad switches select the mode (BFO or reception) and the tune rate (fast, slow, and fine).

a. The key components of the encoder are a four inch mirror segmented disk and two offset reflective object sensors. One side of the four inch diameter disk is coated with a non-reflective black finish with mirrored surfaces 7.2 degrees wide and placed each 7.2° around the outer radius of the disk. This provides 25 equally spaced mirrored and black segments approximately ½ inch long that are placed between 1.4 and 1.9 inches on the outer radius of the disk.

The disk is mounted on a shaft that holds the disk to the rear of circuit card A9. The shaft extends through a bushing to the front of the front panel with the tuning knob attached to that end. This mechanical arrangement provides for a one to one turning ratio between the knob and disk and is so designed to provide easy spin operation.

b. The two object sensors, U59 and U60, are mounted on circuit card A9, and are placed so that they are adjacent to the segmented surfaces of the disk. When the disk is rotated, the non-reflective black segments of the disk absorb the light emitted by the sensors while the mirrored segments reflect the light back to the sensors. This produces two pulse waveforms whose frequency depends on the rate at which the disk is rotated. The two object sensors are also positioned in relation to the disk segments and to each other so that the waveforms are either leading or lagging each other by 90 degrees (refer to Figure 5-17). The direction of rotation determines which waveform leads the other. A complete description of the electronic operation of the Encoder is described in Paragraph 5-17b while maintenance procedures are presented in Chapter 6.

CHAPTER 6
MAINTENANCE

6-1. **INTRODUCTION.** This chapter contains the organizational and intermediate level maintenance procedures for the R-2174(P)/URR Radio Receiver. The information is intended to aid the technician in maintaining the overall performance and general appearance of the unit. Maintenance information is presented in three main sections: Section I contains the organizational and intermediate maintenance which includes preventive maintenance, operational checks and performance test tables. Section II, Special Maintenance, presents the instructions for maintaining the encoder and other items on the front panel assembly. Section III includes the intermediate level performance tests.

6-2. **MAINTENANCE REQUIREMENTS.** Organizational level maintenance includes inspections, operational checks, faulty circuit card isolation using BITE (Built-In Test Equipment) and minor repairs to the overall Receiver. Intermediate level maintenance includes additional faulty circuit card isolation using the test equipment listed in Table 6-1, the performance test procedures, Table 6-3, and special maintenance instructions. When discrepancies or malfunctions are encountered that require extensive dismantling, or isolating failures to individual components, the unit should be returned to the Technical Repair Center. Circuit Cards should also be sent to the Technical Repair Center for repair and alignment. Maintenance of the Receiver should be performed only by technicians with proper training in electronic theory and maintenance including digital and RF circuitry. In addition, the technician should be familiar with the information included in Chapters 1 through 5 of this manual and with any options installed in the particular Receiver to be serviced.

SECTION I. ORGANIZATIONAL AND INTERMEDIATE MAINTENANCE

6-3. **GENERAL.** Section I provides the information required to periodically check the general appearance, operational checks of the Receiver and for fault isolation when malfunctions occur. The preventive maintenance procedures call for inspections, cleaning and repairing damaged or deteriorated components and for periodic operational checks. BITE and performance tests check the overall unit performance and for isolating malfunctions to a particular module or circuit card. The procedures should be performed periodically as called for and a maintenance log kept of each performance accomplished, discrepancy found and correction made. Paragraph 6-7 covers Organizational Level Maintenance, Paragraphs 6-8, 6-9, and 6-10 cover Intermediate Level Maintenance.

WARNING

6-4. **SAFETY PRECAUTIONS.** Observe all safety regulations. Do not make connections or replace modules or circuit cards with the ac line cord plugged in. Dangerous potentials may exist with all power removed due to charges retained by capacitors.

6-5. **MAINTENANCE SUPPORT EQUIPMENT.** Table 6-1 lists the equipment required for intermediate level maintenance procedures. This table includes the manufacturer's model or type number and operating characteristics of the equipment. Equivalent units may be substituted when necessary.

TABLE 6-1. MAINTENANCE SUPPORT EQUIPMENT

Item	Equipment Identification (or equiv.)	Characteristics
1.	Digital Voltmeter, Fluke 8040A-01	Range: 0 to 150 Vac and dc 0 to 1 A ac and dc Display: 3½ digits Accuracy: ±2 L.S. digit
2.	Oscilloscope, Dual Trace, Portable AN/USM-425(v)1, Tektronix 465M	Sensitivity: 5mV/div. Frequency: dc to 100 MHz
3.	Spectrum Analyzer, Tektronix 4960PT3T	Frequency Range: 0 kHz to 110 MHz Frequency Bandwidth: 10Hz-300Hz
4.	HI-Impedance Probe, Spectrum Analyzer Hewlett Packard HP1121A	Frequency Response: ±0.5dB from 0.1 to 110MHz ±3dB from 1KHz to >500 MHz Input Impedance: 100K ohms shunt capacity of 3 pF@100MHz with 10:1 divider, 1M ohm with 1 pF@100MHz
5.	SG-1093/U AM/FM Signal Generator, Hewlett Packard 8640B-003	Frequency Range: 500kHz to 100MHz Accuracy: ±0.5% of dial setting Stability: 10 parts in 10^6 Output Level Range: -140dBm to + 20dBm Modulation: AM -0 to 100% FM ±150kHz @ 30MHz Output Impedance: 50 ohms
6.	X10 Oscilloscope Probe, Tektronix 010-6105-03	Tip Impedance: 10 Megohms, 13.5 pF
7.	BOONTON Model 92E RF Millivoltmeter with 50 ohm Probe Adapter NSN 6625-01-183-8124, P/N 92E.	VOLTAGE RATING: 100.0 AC Minimum 240.0 AC Maximum FREQUENCY RATING: 50.0 HZ Minimum 400.0 HZ Maximum

6-6. PREVENTIVE MAINTENANCE. Preventive maintenance for the receiver consists of routine maintenance tasks and checks necessary to detect potential malfunction or failure of components. In addition, preventive maintenance defines the necessary cleaning, operational checks and minor calibration required to maintain operational performance standards.

a. Cleaning. The Receiver should be inspected each 336 days, or prior to operation if the unit has been inoperative for an extended period, for cleanliness and good general appearance.

CAUTION

Use only approved solvents throughout the cleaning procedures. Do not use abrasive or other chemical cleaning agents containing benzene, toluene, zylene, acetone or other chemicals that can damage paint, circuit cards, electrical components and plastics used in the Receiver.

(1) Remove dust, dirt and other foreign matter from the front and rear panels with a soft brush or cloth. Make sure heat sinks are free of dirt and foreign matter.

(2) Inspect the top and bottom covers. Ventilation holes must be kept free of dust and dirt. Refer to Paragraph 6-12d and remove the covers, clean with a soft brush or compressed air.

WARNING

Compressed air used for cleaning can create airborne particles that may enter the eyes. Pressure shall not exceed 30 PSIG and wearing of goggles is required.

CAUTION

Do not use bristle brushes or cloths to clean circuit cards. This material may create static electricity which can damage CMOS integrated circuits.

(3) Inspect the interior for dust and dirt collection and for corrosion of solder joints, connections, circuit cards, etc. Use low pressure compressed air to remove dust and other loose matter. Use an approved corrosion solvent to remove corrosion and crystalization.

WARNING

The filter capacitors used in the power supply will retain an electrical charge after power is removed. The capacitors should be discharged slowly by shorting the terminals through a protected resistive device.

(4) Remove the power supply cover and after discharging filter capacitors inspect and clean in the same manner as described in step (3).

(5) Inspect the encoder disk for scratches, dirt, fingerprints and corrosion. The mirrored surfaces should be especially clean. Clean with a soft cloth and cleaner-solvent.

b. Damage Inspection. Inspect the Receiver every 336 days, or prior to operation if the unit has been out of operation for an extended period, for internal and external damage.

(1) Inspect knobs, heat sinks, switches and controls for damage, tightness, freedom to operate, etc. Replace damaged items as required.

(2) Inspect front and rear panels for missing screws, paint scratches and general appearance. Replace missing screws and touch up paint with matching finish as required.

(3) Inspect the LCD edge-lighting lamps, keypads and FAULT indicator. Refer to Section II if replacement of these components are required. Edge Lighting Lamps may be disconnected (W1P1) in radios that are operated in well lighted work areas, this greatly extending their usable life.

(4) To inspect the interior of the receiver, remove the top and bottom covers as described in Paragraph 6-12d. Inspect internal circuit boards and components for signs of excessive heat corrosion damaged circuits, loose connections or other signs of damage.

(5) Inspect the encoder assembly for freedom of operation and general appearance. Encoder should operate and spin freely when operated with encoder knob on the front panel. Encoder disk should be tight on the shaft and free from wobble as it is rotated. Refer to Section II for encoder repair.

(6) Inspect all connectors for bent or broken pins, damaged shells and corrosion. Clean corrosion with an approved solvent. Replace damaged connectors as required.

(7) Inspect the fuse and circuit card switch in the power supply located on the rear panel. Make sure the fuse is not blown or the circuit card damaged. Replace as necessary.

(8) Inspect cables for frayed insulation, damaged conductors or connectors. Repair or replace as required.

(9) Inspect the nickle cadmium battery BTI located on circuit card A6A2. The battery should be replaced if there is any sign of damage, corrosion or leakage of electrolyte.

c. Lubrication. No lubrication is required for the Receiver.

d. Operational Checks. The operational check as outlined in Paragraph 6-7 should be performed monthly to determine that the overall performance of the Receiver is satisfactory. Any sub-standard conditions found through the performance tests should be corrected before placing the unit in normal operation. If discrepancies or malfunctions cannot be corrected, then the fault isolation procedures in Paragraph 6-8 should be performed to isolate the malfunction to a circuit card.

6-7. OPERATIONAL CHECK AND FAULT ISOLATION. Operational checkout of the Receiver must include a symptom/diagnostic analysis to augment the results of BITE test procedures. Since BITE is not a panacea for all electromechanical problems, a degree of interpretation by maintenance personnel is necessary. The analysis must include the conditions that preceded the use of BITE as well as those during and following its use. Interpretations will, with a probability of greater than 90%, verify the Receiver operation or isolate a Receiver malfunction to a specific board. Both Verification and fault isolation depend upon careful observation of all symptoms starting with the initial step of energizing the Receiver.

Further, for fault isolation, certain assumptions must be made in order to facilitate an intelligent assessment. These assumptions are: (1) the previous configuration of the Receiver is correct, i.e., filter complement installed correctly, system interfaces properly connected; (2) the Receiver was properly installed in an operational position (station); (3) the Receiver was functioning correctly prior to the occurrence of the fault; and (4) all connections, connectors, cables and components were checked for correct placement, continuity and tightness.

a. Initial Check. The following procedures detail verification and fault isolation.

(1) Verify that the printed circuit switch in A10J1 on Receiver rear panel matches available line voltage (100, 120, 220, or 240 Volts ac ±10% at 43 to 420 Hz) and that the proper fuse is inserted. Ensure the correct fuse is installed: 100/120 VAC operation = 1 Amp. or 220/240 VAC operation = 1/2 Amp.

(2) Make sure that the REF IN/OUT switch, S2 on rear panel, is set to the INT position.

(3) Energize receiver by turning POWER ON switch to "ON" position. Check FAULT indicator, if on, refer to paragraph 6-8 and correct fault before proceeding.

(4) Observe edge lighting and Liquid Crystal Displays (LCD's). When edge lighting is present and LCD displays contain data, the Power Supply (A10) is working properly.

(a) If edge lighting is not present, the +15 volts from the A10 power supply is malfunctioning. Check this voltage through to A10 and correct the malfunction.

(b) If edge lighting is present and frequency display contains mostly zeros, and no mode indication is present, either the wafer does not match available line voltage, the A10 module is faulty or the A6A2 Microcomputer Assembly is faulty and should be replaced.

NOTE

Once steps (1) through (4) have been successfully accomplished, it can be assumed with 60% confidence that both the A6A2 Microcomputer and the A9 Front Panel Assemblies are functional. To increase the confidence factor, perform steps (5) and (6).

(5) Depress the front panel LOCAL/REMOTE pushbutton switch. The LCD display should indicate a change in Receiver control from no display to REMOTE or vice versa. Repeated pressing of the LOCAL/REMOTE pushbutton switch should alternate the display between no display and REMOTE indications.

(a) If the Receiver indicates that it is in the REMOTE mode, and depressing the LOCAL/REMOTE pushbutton does not change the display, either the A6A2 Microcomputer Assembly or the A9 Front Panel Assembly is faulty and must be replaced.

(b) If the Receiver display does not indicate that it is in REMOTE, further isolation is possible. Depress the METER RF/AF pushbutton switch. The meter display should change correspondingly. If it does change, the REMOTE/LOCAL pushbutton switch is probably bad and the A9 Front Panel Assembly should be replaced. If the meter display does not change, initialize the Receiver by depressing the LOCK and AM pushbuttons in that order, then release in the opposite order that they were pressed. Allow the Receiver to initialize (approximately one minute). Once again attempt to change from LOCAL to REMOTE and back; and from RF to AF meter indications. If the display still will not change, the fault is probably on the A6A2 Microcomputer Assembly which should be replaced.

(6) Ensure that the Receiver is under LOCAL control (indicated by absence of REMOTE in LCD display). Depress the ENTER pushbutton switch momentarily, followed by numerals 12345678. These numerals should appear as 12.345678 on the frequency LCD. If this display is correct, then a confidence factor of 99% can be assumed regarding the total reliability of the A6A2 Assembly and a confidence factor of 60% for the A9 Assembly.

(7) Ensure that the Receiver is under LOCAL control. If MAN is not displayed in LCD, momentarily depress the MAN pushbutton on the front panel to achieve Manual IF gain control. Once MAN is visible on the LCD, ensure that SHORT, MED, or LONG are not present in the display. If any of these three indications are present, momentarily depress the corresponding SHORT, MED, or LONG pushbutton on the front panel to remove the indication from the display.

(8) When set up correctly, only the MAN display should be present in the LCD. Also, ensure that the meter indication is set for RF level. Once this condition has been attained, slowly rotate the IF GAIN potentiometer on the front panel from the full clockwise to full counter-clockwise positions and back again while observing the RF level meter display in the LCD. The RF level display should range from zero (no indication) to full scale and back again to zero. If this range is not attainable, then either the A4 Main IF Assembly (60% probability) or the A9 Front Panel Assembly (40% probability) is at fault and should be replaced.

NOTE

Failure to attain the desired range definitely indicates that proceeding with the BITE checks is useless until the problem is corrected. On the other hand, full range indication demonstrates that the A4 Main IF measurement system used by BITE is functional and BITE checks will yield useful results.

b. BITE Check. Steps (1) through (8) in Paragraph a must be successful before BITE testing can be effectively applied.

(1) Press the LOCK pushbutton and while still holding, press the AM pushbutton then release them in the opposite order they were pressed. The Receiver will enter its BITE check mode as indicated by (a) the appearance of REMOTE in the LCD display; (b) the rapidly changing frequencies, modes, and LCD displays on the front panel, and (c) the presence of rapidly changing AF tones and sounds (if AF is being monitored). BITE performs checkout procedures on the following assemblies:

A2 – First Mixer
A3 – Second Mixer
A4 – Main IF/AF
A5 – (If installed) - ISB
A6A2 – (Memory portion) - Microcomputer
A7 – First and Third LO Synthesizers
A8 – Second LO Synthesizer
IF Bandwidth Filters

NOTE

By observing the frequency display LCD, it is possible to isolate a fault to the board level by noting BITE error code(s) which appear in that display.

(2) If an error code does appear in the frequency LCD (a two-digit number) refer to Table 6-2, BITE Error Code Identification. If more than one board is identified as a suspected fault, depress and hold the LOCK then the CW pushbuttons, then release in the opposite order. Observe the display. A subsequent number will appear which, when considered along with the number which first appeared should identify the faulty board.

NOTE

When boards A4 and A7 are indicated to be defective, they should be replaced only at the intermediate maintenance level.

(3) Replace the faulty board and repeat steps 1 through 3 until no further faults are indicated by BITE. (This will be indicated by the exit from REMOTE and the return of the Receiver to its pre-BITE status.

(4) Successful completion of Paragraphs a and b verify the operational readiness status of all boards except: A1 Lowpass Filter, A6A1 Remote Interface, and the audio portions of A4 Main IF/AF and A5 ISB (if installed).

TABLE 6-2. BITE ERROR CODE IDENTIFICATION

Displayed Error	Description	Probable Fault
01	First Local Oscillator synthesizer not locked after 100 millisecond delay from 500 kHz step change.	A7
02	Second Local Oscillator (Reference) synthesizer not locked.	A8
03	First Local Oscillator synthesizer does not break lock to enter fast sampling mode on 500 kHz step change.	A7
04	Third Local Oscillator synthesizer not locked after 100 millisecond delay from 500 kHz step change.	A8
05	Third Local Oscillator synthesizer not locked after 100 millisecond delay from 500 kHz and 500 Hz step change, respectively. 03 and 05 indicates A7 faults; 04 & 05 by itself indicates A8 fault.	A8, A7
06	Filter slot one contains a symmetrical filter, but there is/are SSB filter(s) also in the system.	Wrong or bad filter.
07	Filter slot one contains an upper sideband filter. ISB operation, if installed, will be impaired.	Wrong or bad filter.
08	No USB filter has been found in the system, and filter slot one does not contain a symmetrical filter.	Wrong or bad filter.
09	Too many symmetrical filters installed in the system.	Check filters installed.
10	Not used.	
11	No LSB filter has been found in the system and filter slot one does not contain a symmetrical filter.	Wrong or bad filter.
12	No symmetrical filters have been found in the system.	Wrong or bad filter.
13	Filter slot one does not contain a lower sideband filter, but ISB is installed. If ISB is installed and no 13 error, A5 is functional.	Wrong or bad filter.
14	Random access memory test failure: Data written to memory different from data read back.	A6A2
15	Either no filters are installed in the system, or the synthesizer signal strength is out of range prescribed for BITE. NOTE: If no 15 error, A2, A3, and A4 are fully functional.	A2
16	Filter slot one contains no filter.	Wrong or bad filter.

TABLE 6-2. BITE ERROR CODE IDENTIFICATION (Cont.)

Displayed Error	Description	Probable Fault
17	Two or more LSB filters have been found in the system.	Wrong or bad filter.
18	Two or more USB filters have been found in the system.	Wrong or bad filters.
19	Although a lower sideband filter has been found in this system, it is not installed in filter slot one. ISB operation, if installed, will be impaired.	Wrong or bad filters.
20	Not used.	
21	Filter in filter slot one is skewed from the IF center frequency.	*Wrong or bad filter.
22	Filter in filter slot two is skewed from the IF center frequency.	*Wrong or bad filter.
23	Filter in filter slot three is skewed from the IF center frequency.	*Wrong or bad filter.
24	Filter in filter slot four is skewed from the IF center frequency.	*Wrong or bad filter.
25	Filter in filter slot five is skewed from the IF center frequency.	*Wrong or bad filter.
26	Filter in filter slot six is skewed from the IF center frequency.	*Wrong or bad filter.
27	Filter in filter slot seven is skewed from the IF center frequency.	*Wrong or bad filter.
28	Not used.	
29	Not used.	
30	Not used.	
	NOTE: 31 through 37; 80% probability of bad filter; 30% probability A4 board.	
31	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot one.	Bad filter, A4
32	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot two.	Bad filter, A4

TABLE 6-2. BITE ERROR CODE IDENTIFICATION (Cont.)

Display Error	Description	Probable Fault
33	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot three.	Bad filter, A4
34	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot four.	Bad filter, A4
35	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot five.	Bad filter, A4
36	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot six.	Bad filter, A4
37	BITE frequency sweep underflowed while attempting to measure bandwidth of filter installed in filter slot seven.	Bad filter, A4

*Synthesizers off frequency or wrong or bad filters.

c. A1 Low Pass Filter Check.

(1) Connect a coaxial cable (i.e. RG 223/U) between Reference IN/OUT connector J7 and RF IN connector J1. Ensure that S2 is in the INTERNAL position. Set the receiver controls as follows:

MODE:	CW
AGC:	Short
BFO:	+1.00 kHz
FILTER:	Nearest 3.2 kHz

(2) Using the Frequency Keypad, enter the following frequencies in order, noting that as each frequency is selected, a 1 kHz tone is present at the audio output jack; 01.000000, 05.000000, 10.000000 and 25.000000 MHz.

(3) Should the audio tone not be heard at any of the above frequencies, the A1 Filter Assembly is possibly defective, and should be replaced.

d. A4 Main IF/AF (AF Section) Check.

(1) Connect J7 to J1 as described in paragraph c. Using pushbutton frequency entry, set receiver to 01.000000 MHz. Select CW, BFO +1.00 kHz, and 3.2 kHz (or nearest) bandpass filter. Ensure that the AF GAIN Control has been advanced at least one third clockwise from the fully counter-clockwise position. If the A4 board audio circuitry is operative, a 1 kHz tone will be heard at the phone jack on the front panel. Place the AF/RF meter in the AF mode. Using a screwdriver rotate the MAIN LINE LEVEL control, and note that the AF meter varies from −10 dBm to greater than 0 dBm. This last step will check the operation of the A4 line amplifier.

e. A5 ISB (AF Section) Check (If Installed).

(1) Connect J7 to J1 as described in paragraph c. Using pushbutton frequency entry, set receiver to 01.001000 MHz. Select ISB/L from the Mode panel. Ensure that the AF

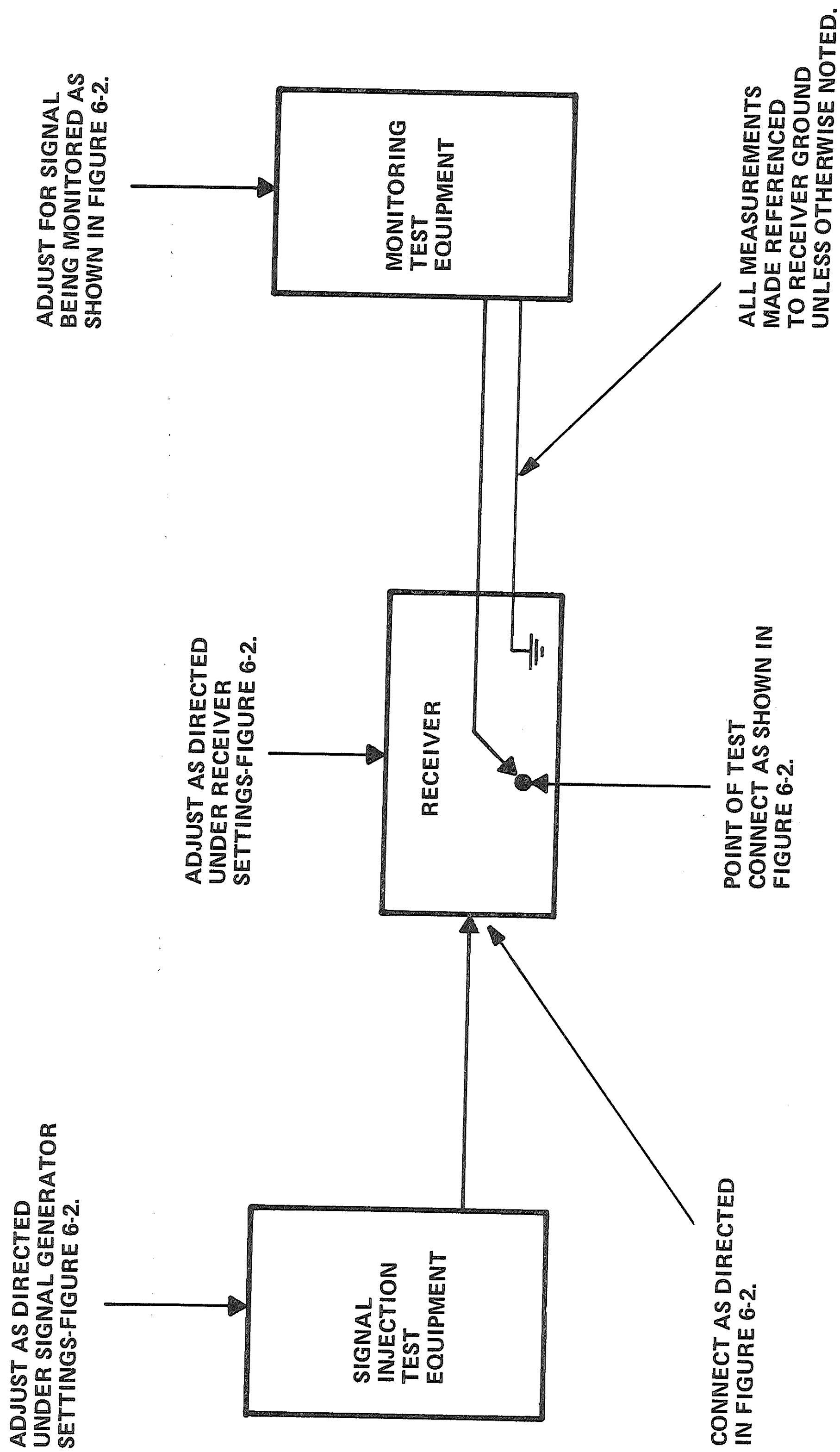
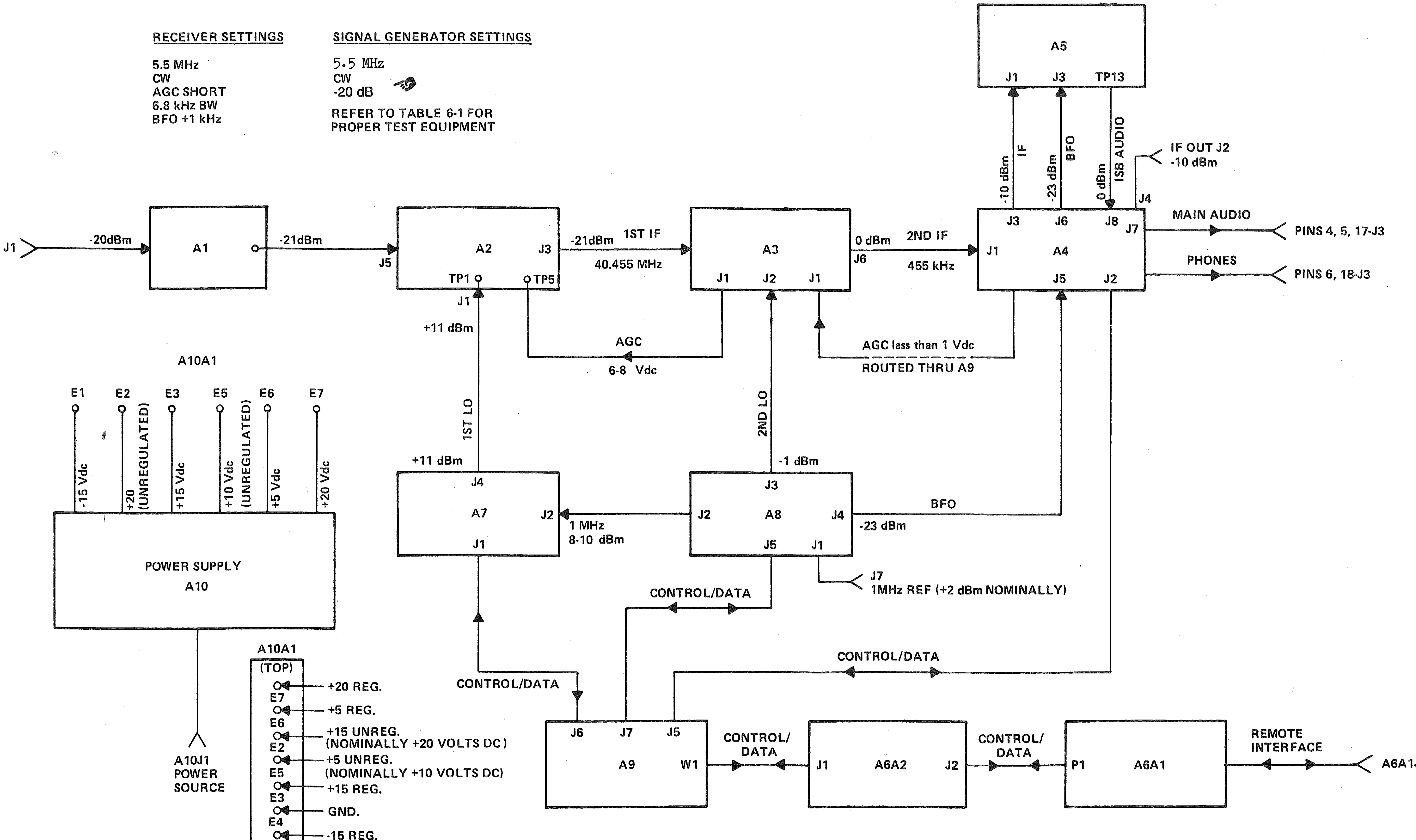


Figure 6-1. Fault Isolation, Equipment Functions



NOTE: ALL REGULATED VOLTAGES ARE ±5%

Figure 6-2. Typical Signal Levels R-2174 (P)/URR HF Radio Receiver

GAIN control has been advanced at least one-third clockwise rotation from the fully off position. If the A5 board is operative, a 1 kHz tone will be heard at the phone jack on the front panel. Place the RF/AF meter in the AF mode. Using a screwdriver rotate the I-LSB LINE LEVEL control and note that the AF meter varies −10 dBm to greater than 0 dBm. This last step will check the operation of the ISB line amplifier.

6-8. **BOARD LEVEL FAULT ISOLATION. (Intermediate Level Only)** Figure 6-1 shows equipment connection methods while Figure 6-2 shows signal flow between individual circuit cards, and the jacks and/or test points for measuring signal values. This information, along with the BITE check detailed in Paragraph 6-7 and the Performance Test Tables detailed in Paragraph 6-9 should be used in isolating malfunctions to the board level. Receiver settings, signal generator settings, and connector pin location diagrams are shown as part of Figure 6-2. The following procedures should be used to perform signal level tests:

a. Set signal generator outputs as specified in Figure 6-2.

b. Set receiver front panel controls as specified in Figure 6-2.

c. Measure values indicated at each jack or test point using the test equipment shown in Table 6-3.

d. Tolerances are: ±3 dBm; ±0.5 volts.

e. Once a fault has been isolated, the faulty circuit card should be replaced in accordance with the Receiver assembly and disassembly procedures detailed in Paragraph 6-12; and Receiver proper operation verified. Verification is accomplished by performing BITE check (paragraph 6-7) and Performance Tests in Section III.

6-9. **PERFORMANCE TEST TABLES. (Intermediate Level Only)** Table 6-3 lists the signal values present at the test points and significant points of measurement in the Receiver. Unless otherwise stated, the measurements were made with the Receiver set as described in subparagraph b and c. For convenience the circuit cards are grouped in the Table as they are in the Receiver.

a. Test Equipment Required. The test equipment required for the performance test includes the signal generator, item 5; spectrum analyzer, item 3; oscilloscope, item 2; digital multimeter, item 1, of Table 6-1 which lists the recommended test equipment and its performance specifications.

b. Maximum Gain Test Set-Up. The Receiver to be tested should be placed on a convenient work bench. The top and bottom covers of the Receiver and the individual module covers should be removed to gain access to the test points. Set the signal generator to produce a 5.5 MHz signal at an output level of −50 dBm. Connect the signal generator output to the RF INPUT on the Receiver (rear panel connector J1). Tune the Receiver frequency to 5.5 MHz. Select the CW operating mode and adjust the BFO to provide a +1.00 kHz offset. Select an IF filter as close as possible to 3.2 kHz bandwidth. Set the AGC to the MAN operating mode and IF GAIN control to maximum clockwise position. Ensure Receiver is operating from own internal reference. Set switch S2, on rear panel to INT position.

c. AGC Test Set-Up. All procedures for AGC test set-up are the same as paragraph b. except set AGC to SHORT operating mode.

TABLE 6-3. PERFORMANCE TEST TABLE

Step	Connection of Test Equipment		Point of Test	Control Settings	Performance Standards
			FIRST MIXER, CIRCUIT CARD ASSEMBLY A2		
1	Spectrum Analyzer		A2TP1	As described in	+6 dBm, ±3 dB 45.955 MHz
2	with High Z Probe		A2TP2	Paragraph 6-9b	+5 dBm, ±3 dB 45.955 MHz
3	Center Frequency:	45.955 MHz	A2TP3		+8 dBm, 45.955 MHz
4	Output Level:	+10 dBm	A2E1		−51 dBm, ±3 dB 5.5.MHz
5	Input Attenuator:	20 dB	A2E3		−51 dBm, ±3 dB 5.5. MHz
6	Log Reference Level:	10 dBm, 10 dB/log	A2E8		−51 dBm, ±3 dB 40.455 MHz
	Bandwidth:	300 kHz			
	Scanwidth:	1 MHz/Div			
7	Digital Multimeter		A2TP4	As described in	0.57 ±0.05 Volts dc
8			A2TP5	Paragraph 6-9b	+11.6±0.15 Volts dc
			SECOND MIXER, CIRCUIT CARD ASSEMBLY A3		
9	Spectrum Analyzer		A3E1	As described in	−55 dBm, ±3 dB 40.455 MHz
10	with High Z Probe		A3E3	Paragraph 6-9b	−50 dBm, ±3 dB 40.455 MHz
11	Center Frequency:	40.455 MHz	A3TP1		−34 dBm, ±3 dB 40.455 MHz
12	Output Level:	−50 dBm	A3TP2		−25 dBm, ±3 dB 455 kHz
14	Input Attenuator:	10 dB	A3TP3		−18 dBm, ±3 dB 455 kHz
15	Log Reference Level:	0 dB, 10dB/log			0 dBm, ±3 dB 455 kHz
	Bandwidth:	300 kHz			
	Scanwidth:	1 MHz/Div			
	Scan Time:	20 Msec/Div			
	Video Filter:	10 kHz			
			FIRST LO SYNTHESIZER, CIRCUIT CARD ASSEMBLY A7		
16	Digital Multimeter		A7TP1	As described in	+5 ±0.2 Volts, dc
17			A7TP5	Paragraph 6-9b.	+5.2 ±0.05 Volts, dc
18			A7TP2	Reset Receiver to CW	Ground
19	Oscilloscope		A7TP3	mode (if necessary).	4 Volt p-p random digital signal
20	with X10 Probe		A7TP3		4 Volt p-p random digital signal
21			A7TP4		4 Volt p-p random digital signal
22			A7TP6		5 Volt negative going pulses, 100 kHz
23			A7TP7		1 Volt narrow pulse, pos. going 100 kHz
24			A7TP8		1 Volt narrow pulse, negative going 100 kHz
25	Digital Multimeter		A7TP9		+8.1 ±0.5 Volts, dc
			A7TP9		+8.1 ±0.5 Volts, dc
26			A7TP10		+5.2 ±0.5 Volts, dc
27			A7TP11		+5.2 ±0.5 Volts, dc
28			A7TP12		+5.2 ±0.5 Volts, dc
29			A7TP13		+0.2 ±0.1 Volts, dc
			SECOND LO/BFO SYNTHESIZER, CIRCUIT CARD ASSEMBLY A8		
30	Oscilloscope with		A8TP10	As described in	4 Volts p-p, 5 MHz
31	X10 Probe		A8TP1	Paragraph 6-9b	5 Volts p-p, 5 MHz
32			A8TP2		4 Volts p-p, 5 MHz
33			A8TP3		4 Volt Negative going pulse, 5 MHz
34			A8TP4		4 Volt Negative going pulse, 5 MHz
35	Digital Multimeter		A8TP5		3.2 to 7.5 Volts dc
36			A8TP11		0.4 Volts dc maximum
37			A8TP12		0.4 Volts dc maximum
38	Oscilloscope with		A8TP6		5 Volt Negative going pulses, 500 Hz
39	X10 Probe		A8TP7		5 Volt Negative going pulses, 500 Hz
40	Digital Multimeter		A8TP8		3.2 to 7.5 Volts dc

TABLE 6-3. PERFORMANCE TEST TABLE (Cont.)

Step	Connection of Test Equipment		Point of Test	Control Settings	Performance Standards
41	X10 Probe.		A8TP9		0.25 Volts p-p minimum, 22.70 MHz
	MAIN IF/AF, CIRCUIT CARD ASSEMBLY A4				
42	Spectrum Analyzer with High Z Probe		A4TP1	As described in Paragraph 6-9c	−38 dBm, ±3 dB, 455 kHz
43	Center Frequency:	455 kHz	A4TP2		−38 dBm, ±3 dB, 455 kHz
44	Output Level:	−50 dBm	A4TP6		0 dBm, ±3 dB, 455 kHz
45	Input Attenuator:	10 dB	A4TP7		0 dBm, ±3 dB, 455 kHz
	Log Reference Level:	0dB, 10dB/log			
	Bandwidth:	1200 Hz			
	Scanwidth:	0.5 kHz/div			
	Scan Time:	.5 Seconds			
	Video Filter:	100 Hz			
46	Digital Multimeter		A4TP3		+0,9 ±0.05 Volts dc
47			A4TP4		+12.7 ±0.3 Volts dc
48			A4TP5		+0.9 ±0.05 Volts dc
49			A4TP8		+6.8 ±0.3 Volts dc
50			A4TP9		+6.8 ±0.3 Volts dc
51			A4TP10		+0.6 ±0.04 Volts dc
52			A4TP11		+5.7 ±0.8 Volts dc
53			A4TP14		+6.5 ±0.8 Volts dc
54	Oscilloscope with		A4TP13		1.5 Volts P-P, 454 kHz
55	X10 Probe		A4TP15		1.4 Volts P-P, 1 kHz (with high freq.
56			A4TP16	LINE and AF	1.4 Volts P-P, 1 kHz component)
57			A4TP17	GAIN controls max clockwise	1.2 Volts P-P, 1 kHz sinewave
	ISB IF/AF, CIRCUIT CARD ASSEMBLY A5 (If Installed - Optional)				
58	Spectrum Analyzer with High Z Probe		A5TP1	As described in Paragraph 6-9c; except that the Receiver must be set to the ISB mode and generator set to 5.4982 MHz.	−38 dBm, 456.8 kHz
59	Center Frequency:	455 kHz	A5TP2		−38 dBm, 455 kHz
60	Output Level:	−54 dBm	A5TP6		0 dBm, 455 kHz
61	Input Attenuator:	10 dB	A5TP7		0 dBm, 455 kHz
	Log Reference Level:	0dB, 10dB/log			
	Bandwidth:	3kHz/Div			
	Scanwidth:	20kHz/Div			
	Scan Time:	.5 Seconds			
	Video Filter:	100 Hz			
62	Digital Multimeter		A5TP4		+0.9 Volts dc ±0.05
63			A5TP5		+12.7 Volts dc ±0.3
64			A5TP8		+6.8 Volts dc ±0.3
65			A5TP9		+6.8 Volts dc ±0.3
66	Oscilloscope with X10 Probe		A5TP10		1.5 Volts p-p. 454 kHz
67			A4TP13		1.4 Volts p-p, 1 kHz
68			A5TP11		No level present
69			A5TP12	I-LSB LINE control max. clockwise	1.4 Volts p-p, 1 kHz

6-10. FAULT CORRECTION. When a fault or malfunction is traced to a particular module or circuit card it should be replaced with a known functional module or circuit card. To replace the faulty unit refer to paragraph 6-11.

6-10.1. **FREQUENCY ALIGNMENT PROCEDURES.** R-217/(P)/UPR Frequency Alignment Procedure:

a. A HP-8660C signal generator, 400B audio meter, HP-5328A frequency counter, and a HP 11005A bridging transformer are required to accomplish this task.

(1) Disconnect antenna cable from JL, RF IN on the rear panel of the Receiver and connect equipment as shown in Figure 6-2.1.

(2) Turn on Receiver and tune to 28.9999 MHz, select USB mode and AGC SHORT.

NOTE

For the following procedure, a 1 kHz frequency setting will be used if an offset sideband filter is utilized; a 1.8 kHz frequency setting will be used if symmetrical or center-tuned filters are utilized.

(3) Turn signal generator RF switch on and adjust RF output frequency for a frequency 1 kHz higher than the Receiver frequency at a level of -60 dBm and no modulation.

(4) On the Receiver, set AF gain control to obtain a 0 dBm reading on the audio meter.

(5) Observe that the audio output is 1000 Hz ±10 Hz ort 1800 Hz ±10 Hz depending on the frequency setting used.

(6) If step (5) is out of tolerance, adjust the A8 5 MHz reference oscillator for a 1 kHz or 1.8 kHz audio output depending on the frequency setting.

(7) Disconnect cable from receiver phones jack and connect to J7, REF IN/OUT on rear panel of the Receiver.

(8) Observe that the reference oscillator output is 1 MHz ±1 Hz.

(9) If the Receiver meets the standards in this procedure, disconnect all test equipment and restore the Receiver to normal service. If the Receiver meets the standards in this procedure, disconnect all test equipment and restore the Receiver to normal service.

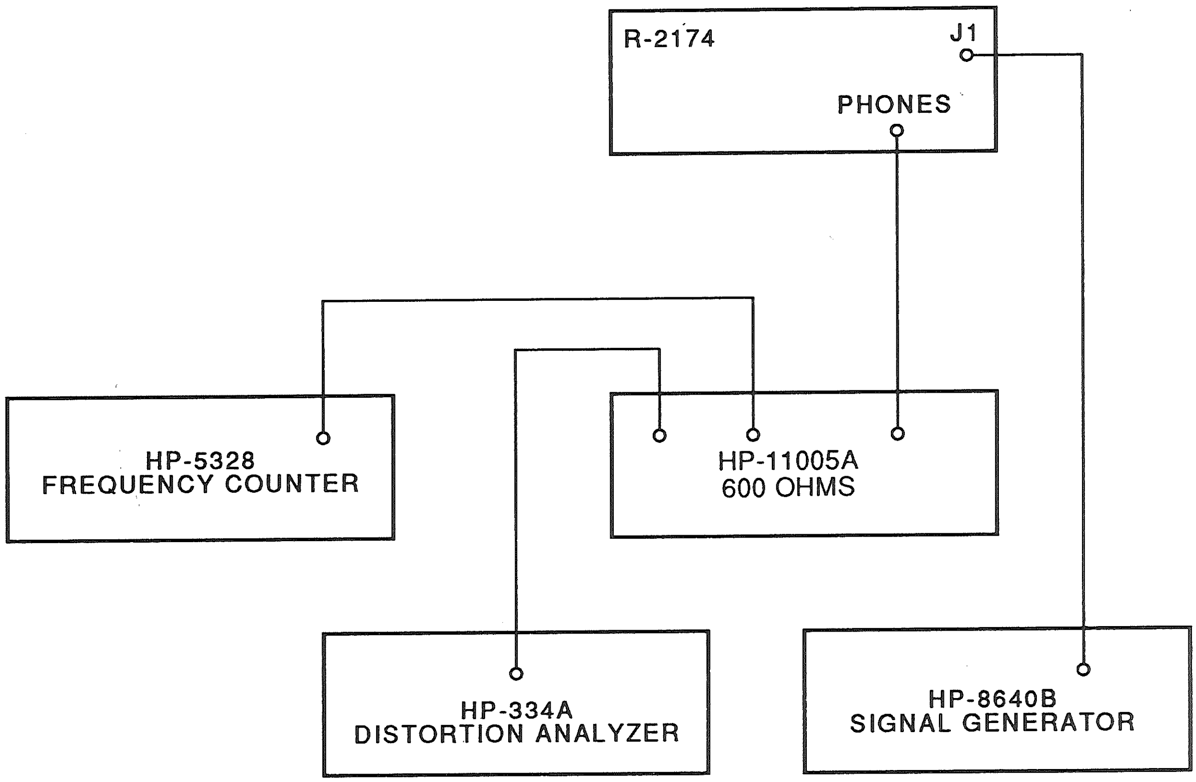


Figure 6-2.1. R-2174 Configuration

6-10.2. RECEIVER SENSITIVITY ALIGNMENT

a. A HP 8640B signal generator, Fluke 8600A multimeter and a 403B audio meter is required to accomplish this task.

b. Disconnect antenna cable JI (RF IN) on the rear panel of the Receiver and connect the output of the signal generator.

c. Turn the Receiver on and tune it to 15.000 MHz, select AM mode, AGC SHORT and 6.8 kHz bandwidth or nearest bandwidth.

d. Turn signal generator RF switch on and adjust output frequency to 15.000 MHz, level to -50 dBm and AM modulation to 1 kHz at 30%.

e. Using a DVM, observe A4TP11 for 5.7 ±0.8 VDC, if out of tolerance, adjust A4R105.

f. Using a DVM, observe A4TP14 for 6.5 ±0.8 VDC, if out of tolerance, adjust A4R47.

g. Adjust signal generator output level to -99 dBm.

h. Connect a 403B audio meter to the headphone jack on the Receiver.

i. Adjust the Receiver AF gain for a 0 dB reading on the audio meter.

j. Turn signal generator RF switch off.

k. Observe audio meter for a -10 dB or greater S+N/N ratio; if unable to obtain ratio, adjust A4R39 clockwise until a -10 dB or greater is obtained.

l. Turn signal generator RF switch on and adjust for an output level of -50 dBm.

m. Adjust Receiver AF gain for a 0 dB reading on the audio meter.

n. Using a DVM, observe A4TP11 for 5.7 ±0.8 VDC, if out of tolerance, adjust A4R105.

o. Using a DVM, observe A4TP14 for 6.5 ±0.8 VDC, if out of tolerance, adjust A4R47.

p. Adjust signal generator output level to -99 dBm.

q. Adjust Receiver AF gain for a 0 dB reading on audio meter.

r. Turn signal generator RF switch off.

s. Observe audio meter for a -10 or greater S+N/N ratio. If unable to obtain ratio, repeat steps k through o.

t. Turn signal generator RF switch on and adjust output level to -100 dBm.

u. Adjust Receiver AF gain for 0 dB reading on audio meter.

v. Adjust signal generator output level from -100 dBm to -10 dBm in 10 dB steps, observe audio meter for not more than 6 dB deviation, if out of tolerance repeat steps k through s.

w. Disconnect all test equipment and return equipment to normal operation. Disconnect all test equipment and return equipment to normal operation.

6-11. **RECEIVER DISASSEMBLY, INSPECTION AND REASSEMBLY.** The Receiver is constructed around a full width, rigid die-cast chassis. The two side gussets are attached directly to this chassis with the front and rear panel assemblies attached to the side gussets. This mainframe assembly houses the receiver circuitry that is accessible through top and bottom covers that attach to the mainframe with quick-lock fasteners. The receiver circuitry is constructed on eleven circuit cards or modules which are attached to the mainframe. Refer to Figures 6-3 and 6-4.

a. Disassembly. The disassembly procedures are designed to allow the technician to remove any module or circuit card in the Receiver without performing the whole procedure. To remove a particular circuit card perform the preliminary procedures, remove the applicable top or bottom cover then proceed to the paragraph for that circuit card. Figure 6-3 shows a top view of the receiver with cover removed, while Figure 6-4 shows the bottom view with bottom cover and module covers removed.

b. Inspection. After a module or circuit card has been removed it should be carefully inspected for the following:

(1) Check components for excessive heat, loose connections, corroded leads and other damage.

(2) Check connectors for damaged or bent pins, loose connections, corrosion and other damage.

(3) Check the circuit cards for damaged tracks, excessive heat, corrosion or other signs of deterioration.

c. Reassembly. Before reassembly, make sure that the circuit card or module is functional. Repaired circuit cards should be tested before being installed in the Receiver. Refer to the same paragraph and illustration as used for disassembly. Reassembly instructions follow disassembly for each module or circuit card.

d. Preliminary Procedure. The only tools required for disassembly or reassembly are a flat blade screwdriver and screw starter.

(1) Refer to Chapter 2 and remove the Receiver from its mounting rack and place on a suitable work space.

(2) Refer to Figures 6-3 and 6-4 to determine the cover to be removed for access to the module or circuit card to be removed.

(3) Module A1 and front panel assembly A9 require both covers to be removed, circuit cards A2, A3, A7 and A8 require only the bottom covers removal while A4, A5, A6A1, A6A2 and A10 require only the top cover to be removed.

(4) Position the receiver horizontally so that the cover to be removed is up.

(5) Turn the six quarter-turn fasteners, that secure the cover, counter-clockwise one fourth turn to loosen.

(6) Raise the cover up from the back and at the same time slide toward the back of the Receiver until the cover is free from the groove in the back of the front panel.

(7) Inspect the cover for damage, inspect the quarter-turn fasteners in the covers and their receptacles in the side gussets and rear panel. Make sure that ventilation holes in the covers are free of all foreign matter.

(8) After reassembly of module or circuit card the cover may be reinstalled by aligning the cover on the receiver and sliding into the front panel groove. Tighten the quarter-turn fasteners by turning clockwise while applying downward pressure.

e. Module A1 Removal. Refer to Figures 6-3, 6-4 and 6-5.

(1) Perform the Preliminary Procedure as directed in Paragraph d.

(2) Disconnect SMB connector A1W1P1 from J5 on the Receiver frame.

(3) Disconnect BNC connector A1W1J1 from J1 (the RF IN jack) on the rear panel.

(4) Stand the Receiver on its side.

(5) Working from the bottom of the Receiver, loosen and remove the two screws and hardware from the ends of the A1 module.

CAUTION

Do not allow the A1 module to drop when the screws are removed. Damage to the A1 module or to the Receiver could result from dropping.

(6) Carefully lift out the A1 module from the top of the Receiver.

f. Module A1 Installation. Refer to Figures 6-3, 6-4 and 6-5.

(1) Position the A1 module with the end marked "IN," toward S2 (EXT-INT REF switch).

(2) Install mounting screw with lock washer and flat washer at the "IN" end, ensure that the ground lug on the A1W1J1 cable is placed inside the A1 module between the A1 cover and the threaded mount, and that the mounting screw goes through the lug. Do not tighten.

(3) Install the mounting screw with lock washer and flat washer at the "OUT" end and tighten. Tighten the screw in the "IN" end.

(4) Connect A1W1J1 connector to J1 then connect A1W1P1 to J5.

g. Circuit Card A2 Removal. Refer to Figures 6-4 and 6-6.

(1) Perform the Preliminary Procedure as directed in Paragraph d.

(2) Release the six (6) captive screws which hold down the A2 cover.

(3) Remove the A2 cover.

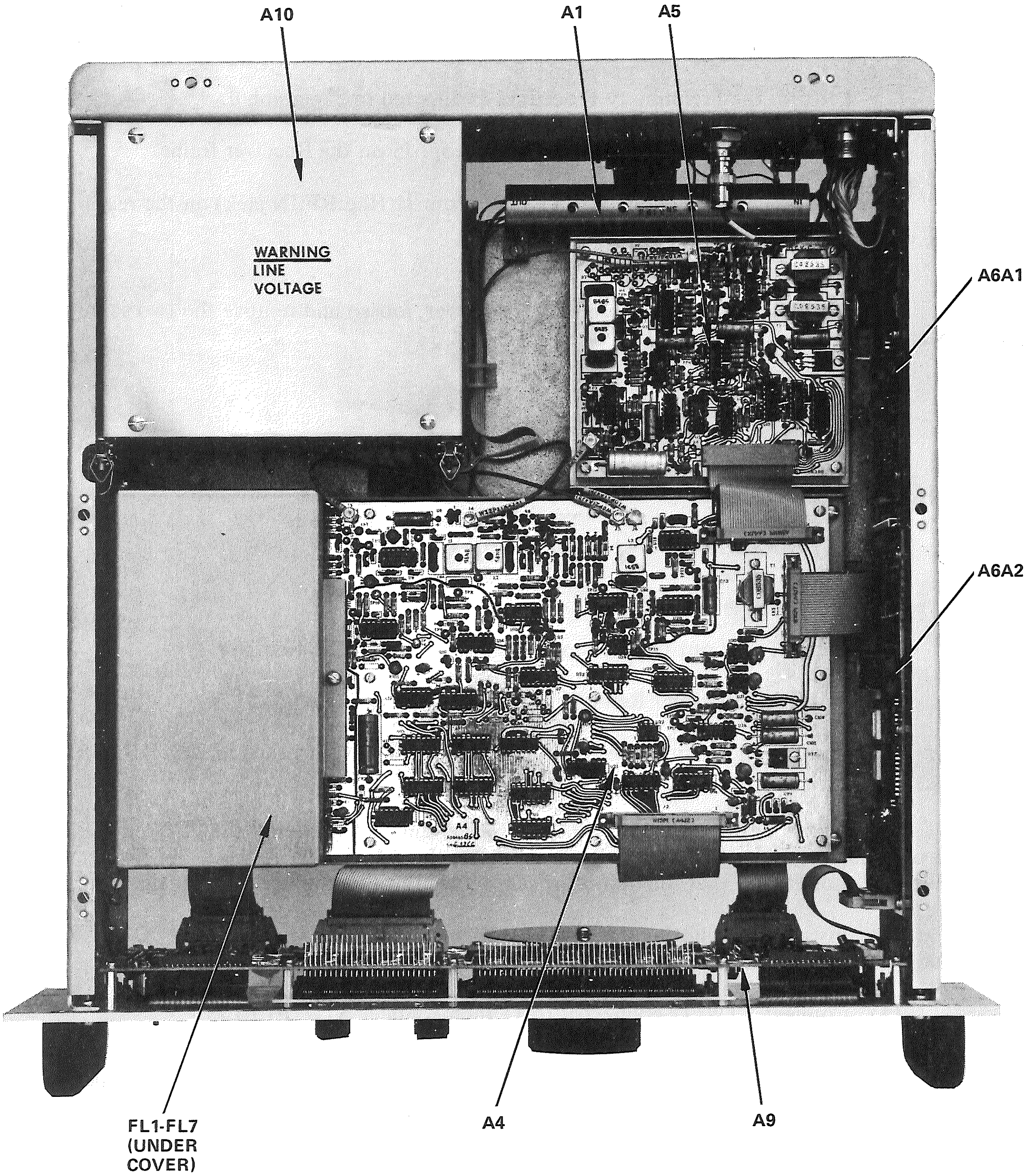


Figure 6-3. Receiver R-2174 (P) URR, Top View, Cover Removed

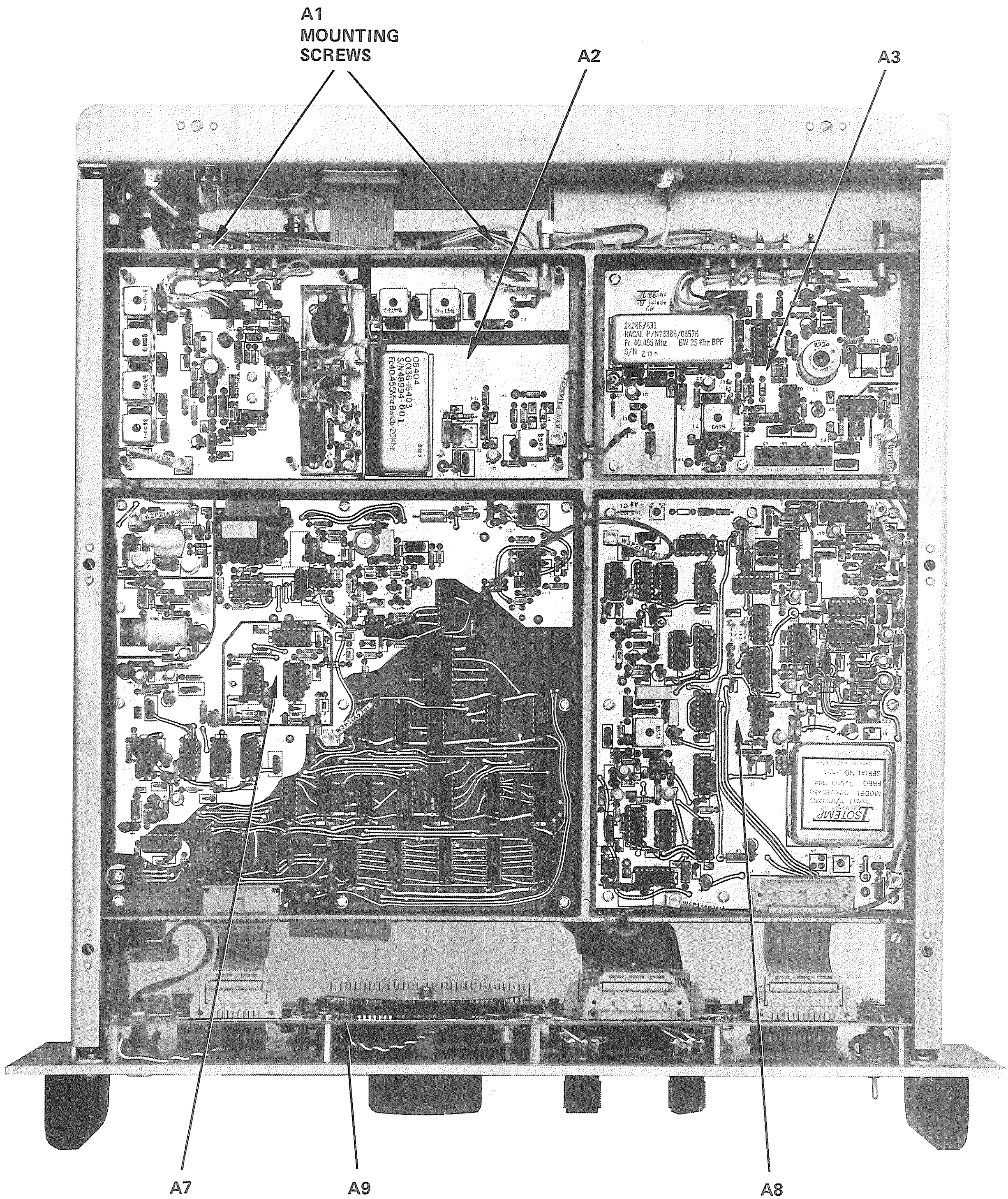


Figure 6-4. Receiver R-2174 (P) URR, Bottom View, Cover Removed

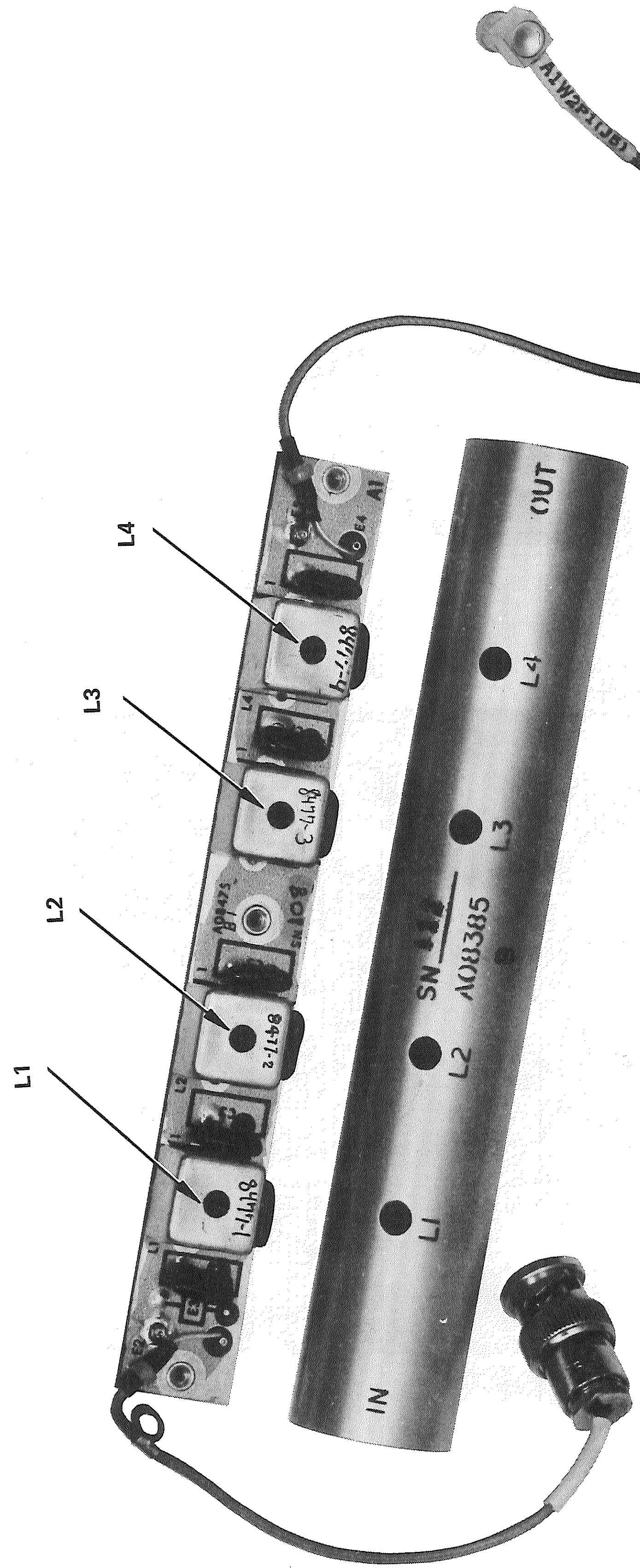


Figure 6-5A. RF Filter Module Assembly A1

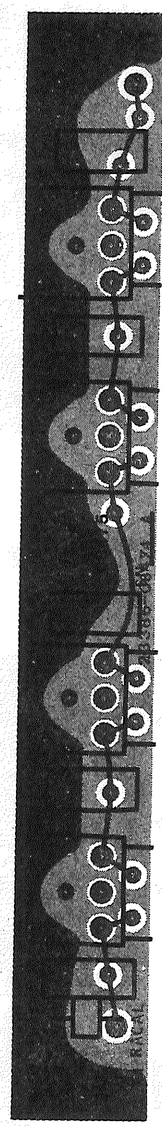


Figure 6-5B. RF Filter A1A1 Printed Circuit

NOTE: Refer to Parts List for differences in the R-2174A Receiver.

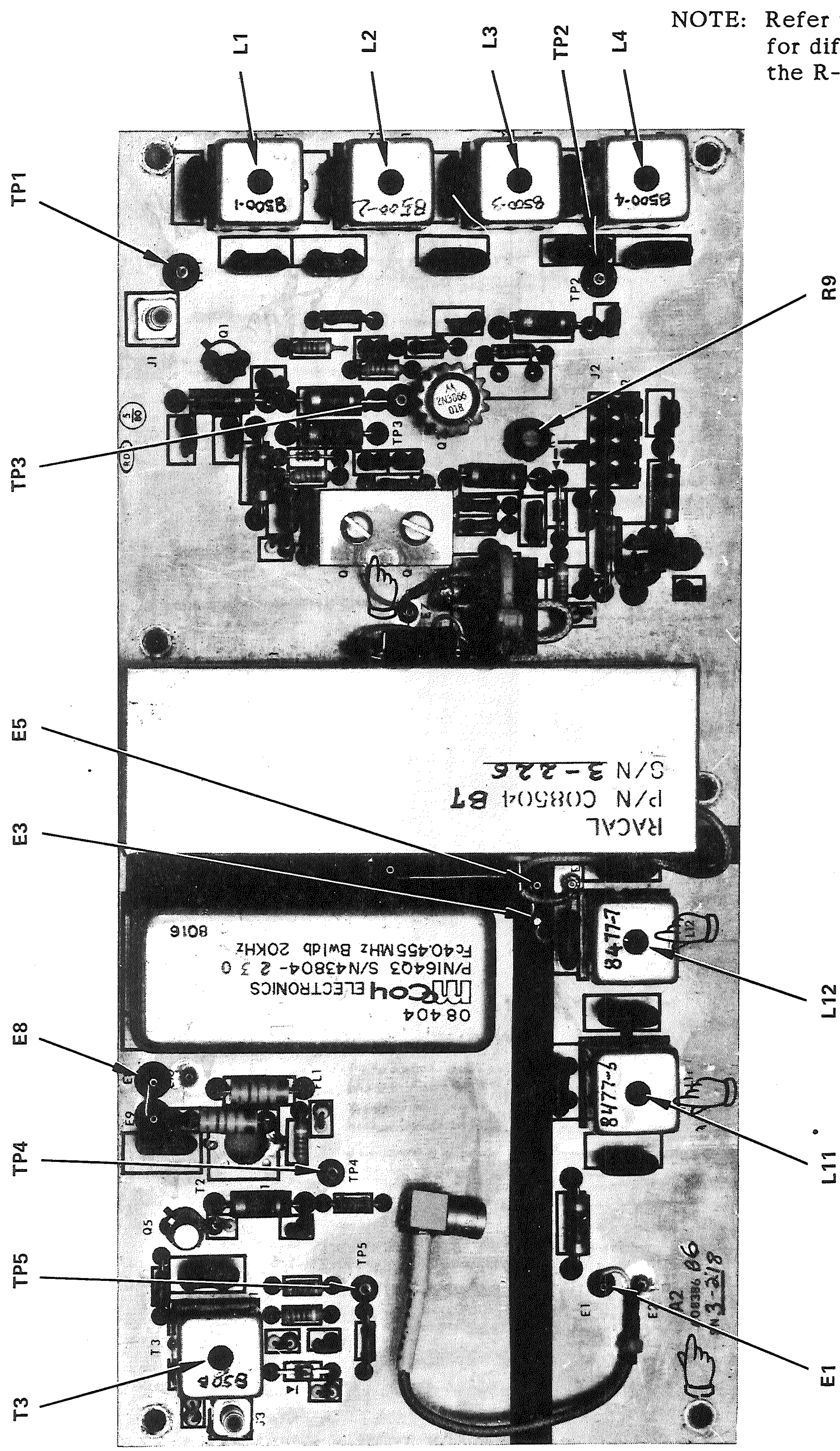


Figure 6-6A. First Mixer Circuit Card Assembly A2

NOTE: Refer to Parts List for differences in the R-2174A Receiver.

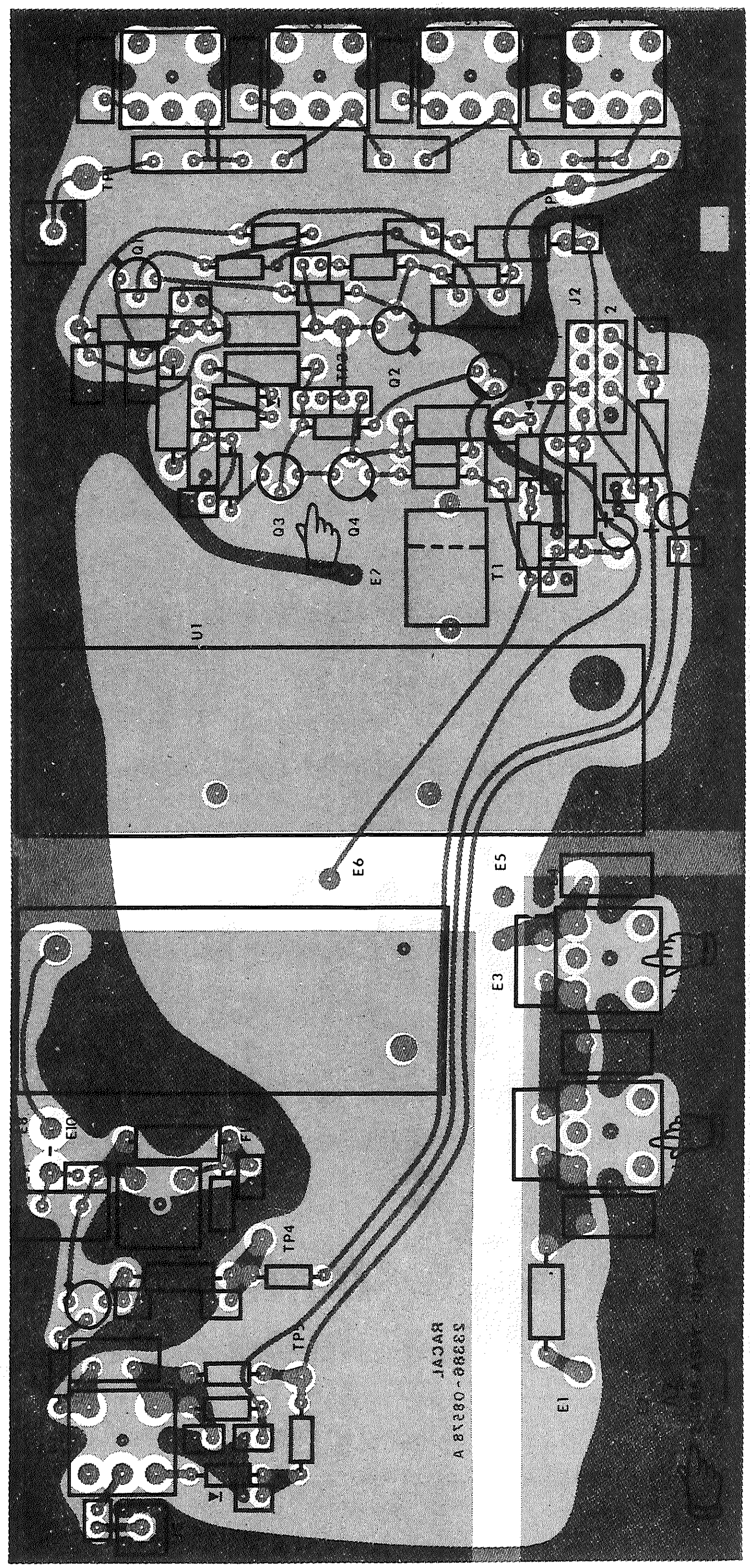


Figure 6-6B. First Mixer A2 Printed Circuit

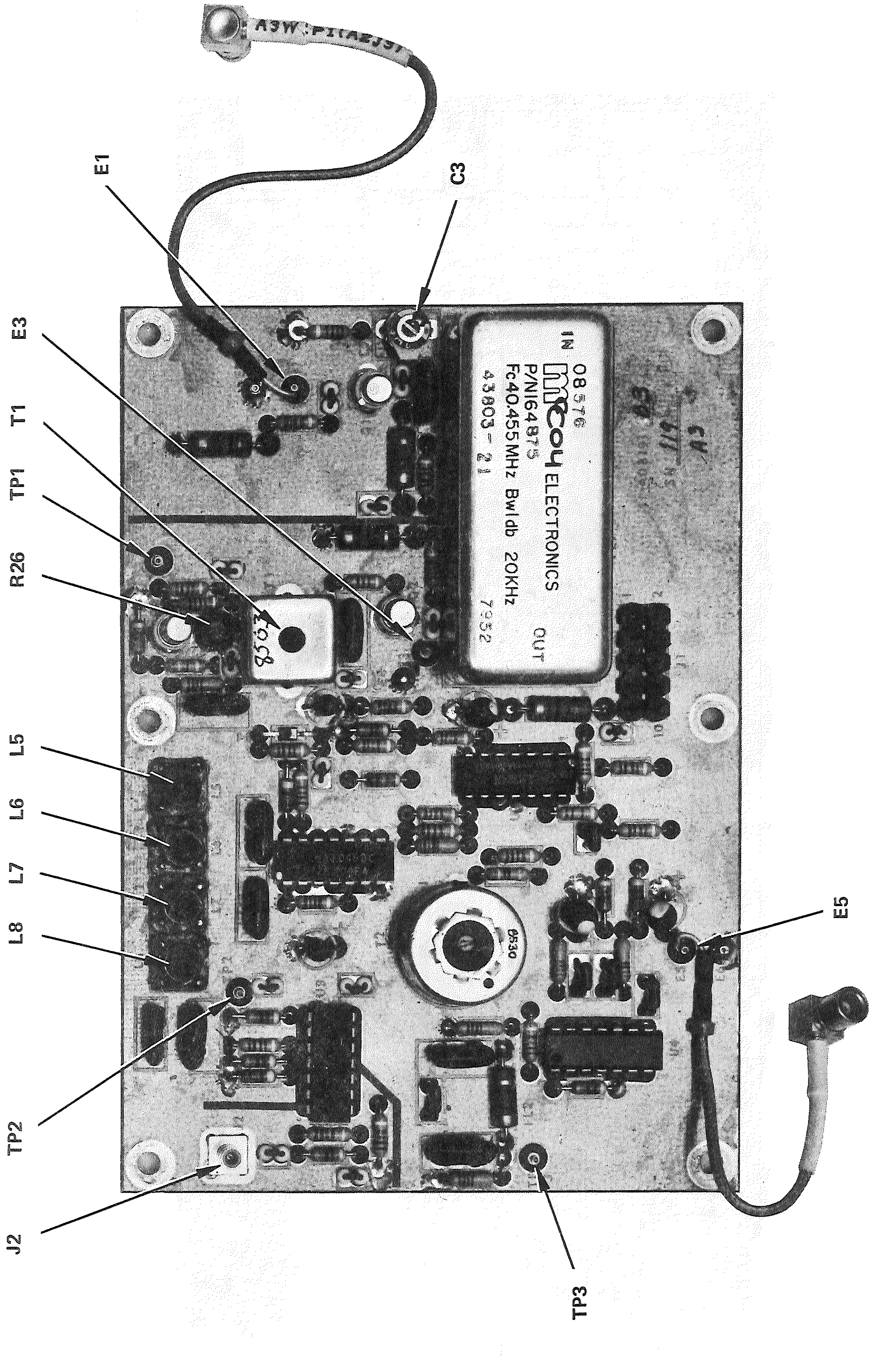


Figure 6-7A. Second Mixer, Circuit Card Assembly A3

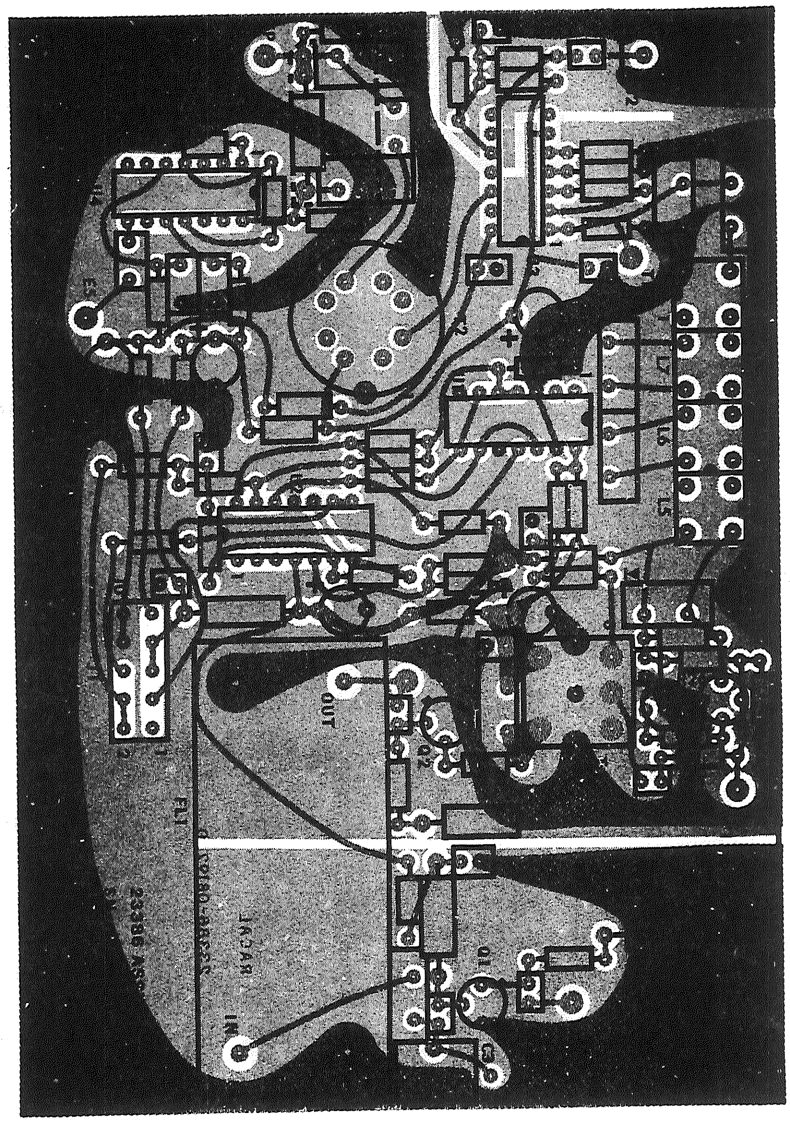


Figure 6-7B. Second Mixer A3 Printed Circuit

(4) Disconnect eight-pin connector W21P1 from A2J2.

(5) Disconnect SMB connector W2P1 from A2J1.

(6) Disconnect SMB connector W1P1 from J5 on the Receiver frame.

(7) Disconnect SMB connector A3W1P1 from A2J3.

(8) Loosen and remove the six (6) standoffs which hold down the A2 circuit card.

(9) Lift out the A2 circuit card, tipping it slightly to avoid bumping it against J5 and the four (4) feed-through capacitors located on the side of the receiver frame.

CAUTION

Bumping J5 or the capacitors may cause damage to the A2 printed circuit track or components.

h. <u>Circuit Card A2 Installation.</u> Refer to Figures 6-4 and 6-6.

(1) Place the A2 circuit card in place by tipping it slightly to avoid bumping it against J5 and the four feed thru capacitors located on the side of the Receiver frame.

(2) Secure the A2 circuit card with the six standoffs and tighten.

(3) Connect SMB connector A3W1P1 to A2J3.

(4) Connect SMB connector W1P1 to J5.

(5) Connect SMB connector W2P1 to A2J1.

(6) Connect eight pin connector W21P1 to A2J2.

(7) Install the A2 circuit card cover and secure with its six captive screws.

i. <u>Circuit Card A3 Removal.</u> Refer to Figures 6-4 and 6-7.

(1) Perform the preliminary procedure as directed in Paragraph d.

(2) Using the pull-tab on the A3 circuit card cover, carefully remove the A3 cover.

(3) Disconnect eight-pin connector W22P1 from A3J1.

(4) Disconnect SMB connector A3W2P1 from J6 on the receiver frame.

(5) Disconnect SMB connector W4P1 from A3J2.

(6) Loosen and remove the six (6) screws,lock washers and flat washers which hold down the A2 circuit card cover.

(7) Remove the A2 cover.

(8) Disconnect SMB connector A3W1P1 from A2J3 on the A2 circuit card.

(9) Loosen and remove the six (6) screws, lock washers and flat washers which hold down the A3 circuit card.

(10) Lift out the A3 circuit card tipping it slightly to avoid bumping the card against J6 and the five (5) feed-through capacitors located on the side of the receiver frame.

CAUTION

Bumping J6 or the capacitors may cause damage to the A3 printed circuit track or components.

j. Circuit Card A3 Installation. Refer to Figures 6-4 and 6-7.

(1) Place the A3 circuit card in place by tipping it slightly to avoid bumping the card against J6 and the five feed-through capacitors on the receiver frame.

(2) Secure the A3 circuit card with six screws, lock washers and flat washers.

(3) Connect SMB connector A3W1P1 to A2J3 on the A2 circuit card. Make sure cable is routed through notch in receiver frame between the A2 and A3 module locations.

(4) Install the A2 circuit card cover with six screws, lock washers and flat washers.

(5) Connect SMB connector W4P1 to A3J2.

(6) Connect SMB connector A3W2P1 to J6 on the Receiver frame.

(7) Connect eight pin connector W22P1 to A3J1.

(8) Carefully install the A3 circuit card cover.

k. Circuit Card A4 Removal. Refer to Figures 6-3 and 6-8.

(1) Perform the preliminary procedures as directed in Paragraph d.

(2) Remove the bandwidth filter cover and bandwidth filters as described in Chapter 2.

(3) Disconnect SMB connector W1P2 from A4J1.

(4) Disconnect SMB connector W11P1 from A4J3.

(5) Disconnect SMB connector W12P1 from A4J4.

(6) Disconnect SMB connector W6P2 from A4J5.

(7) Disconnect SMB connector W10P1 from A4J6.

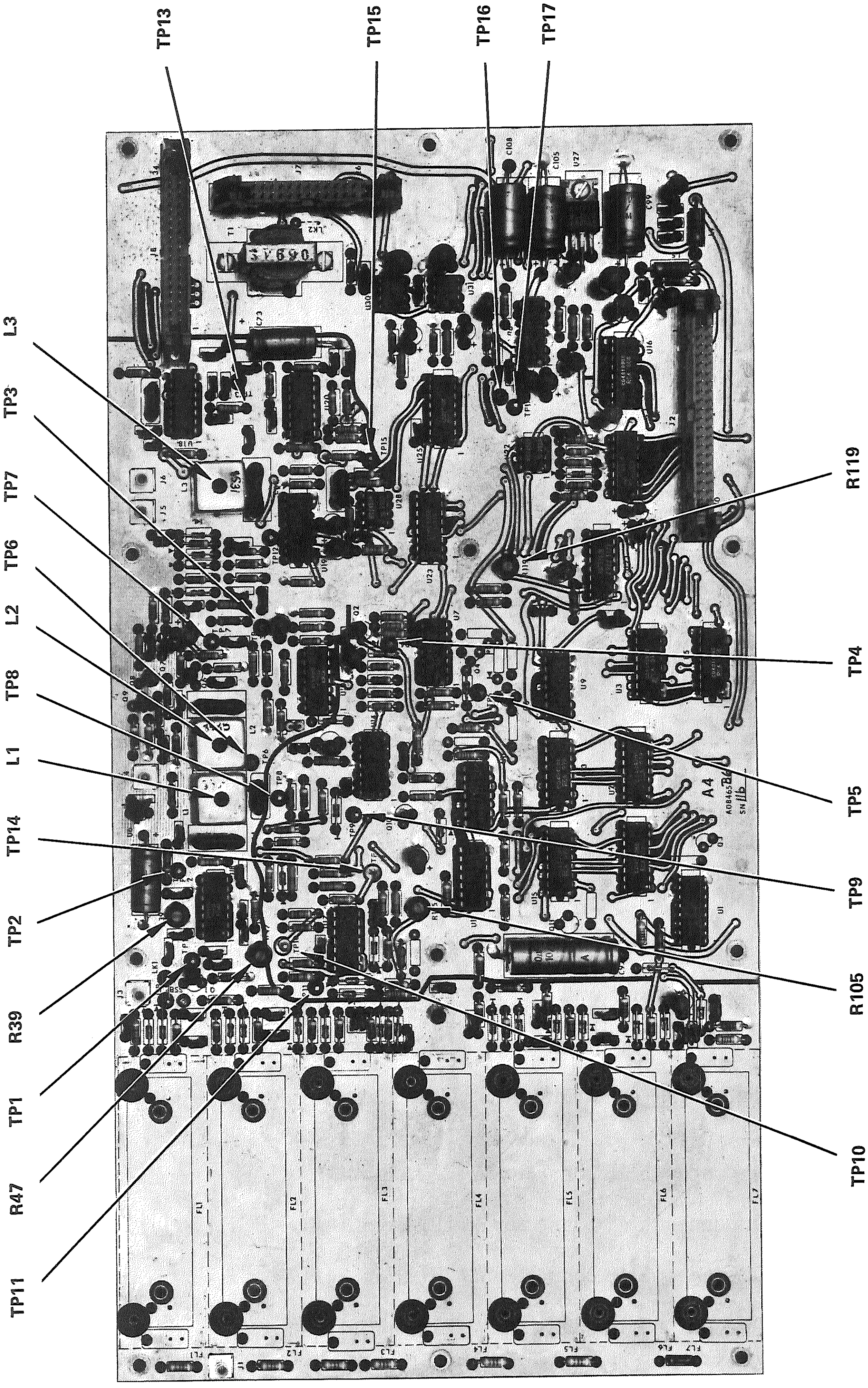


Figure 6-8A. Main IF/AF Circuit Card Assembly A4

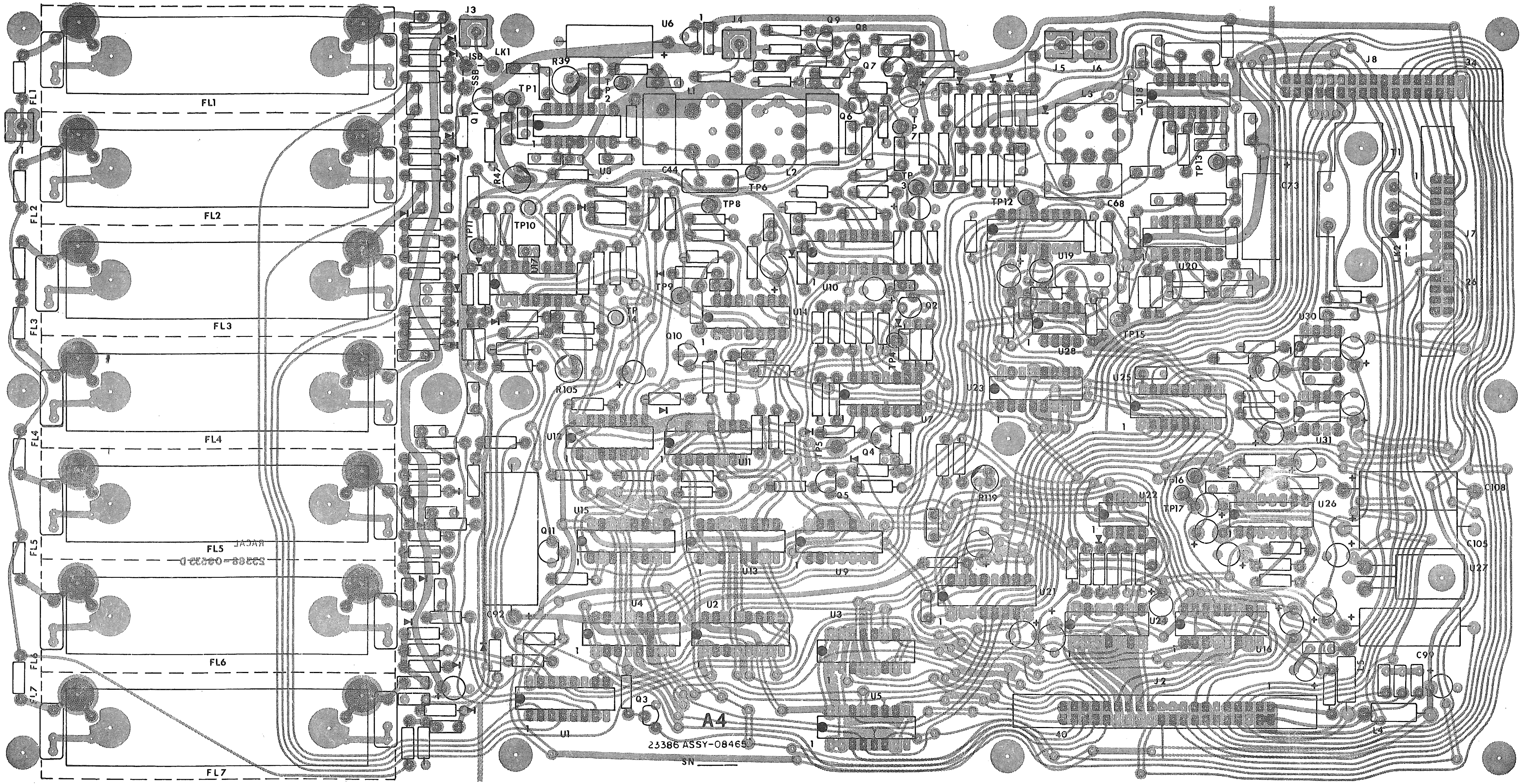


Figure 6-8B. Main IF/AF A4 Printed Circuit

(8) Disconnect ribbon connector A5W1P1 from A4J8.

(9) Disconnect ribbon connector W16P1 from A4J7.

(10) Disconnect ribbon connector W15P1 from A4J2.

(11) Loosen and remove the twelve (12) screws, lock washers and flat washers which hold down the A4 circuit card.

NOTE

The two (2) screws which hold down transformer T1 to the A4 circuit card do not need to be removed to remove the module nor does the screw through U27. Ten (10) hold down screws are located around the A4 module edges, and the two (2) additional screws are located in the middle area of the module.

(12) Lift out the A4 module.

1. Circuit Card A4 Installation. Refer to Figures 6-3 and 6-8.

NOTE

Ensure the A4 card has a jumper connected for either SSB ISB operation from LK1 to the appropriate point.

(1) make sure that cables and connectors are out of the way, then place the A4 circuit card in place and secure with twelve (12) screws, lock washers and flat washers.

(2) Connect ribbon connector W15P1 to A4J2.

(3) Connect ribbon connector W16P1 to A4J7.

(4) Connect ribbon connector A5W1P1 to A4J8.

(5) Connect SMB connector W10P1 to A4J6.

(6) Connect SMB connector W6P2 to A4J5.

(7) Connect SMB connector W12P1 to A4J4.

(8) Connect SMB connector W11P1 to A4J3.

(9) Connect SMB connector W1P2 to A4J1.

(10) Install the bandwidth filters and filter cover as directed in Chapter 2.

m. Circuit Card A5 Removal. Circuit Card A5 is optional and may or may not be installed in the Receiver. Refer to Figures 6-3 and 6-9.

(1) Perform the preliminary procedure as directed in Paragraph d.

(2) Disconnect ribbon connector A5W1P1 from A4J8.

NOTE

The connector disconnects from the A4 module, not the A5 module, and the ribbon cable is part of the A5 module.

(8) Disconnect ribbon connector A5W1P1 from A4J8.

(9) Disconnect ribbon connector W16P1 from A4J7.

(10) Disconnect ribbon connector W15P1 from A4J2.

(11) Loosen and remove the twelve (12) screws, lock washers and flat washers which hold down the A4 circuit card.

NOTE

The two (2) screws which hold down transformer T1 to the A4 circuit card do not need to be removed to remove the module nor does the screw through U27. Ten (10) hold down screws are located around the A4 module edges, and the two (2) additional screws are located in the middle area of the module.

(12) Lift out the A4 module.

(13) Main IF/AF Circuit Card Assembly A4 Alignment Procedure

TEST EQUIPMENT REQUIRED:

RF Signal Generator
Digital Multimeter (DVM)
RF Millivoltmeter (Boonton 92E or equiv.)
Locally mfg. Cable Adapt (for W1P2)

(a) Verify that 4 KHz (or less) symmetrical filter is installed in the Receiver. Turn the Receiver on and initialize it (if necessary) by implementing the Automatic BITE Sequence. Then set the Receiver frequency to 1.5MHz, select the 4KHz (or less) filter, the AGC short mode, and the AM operating mode.

(b) Connect the DVM to TP9 on the A4 Assembly. With no input to the Receiver Antenna input (J1-RFIN), adjust R119 for 10.0 ±.05 VDC indication on the DVM. Connect the RF signal generator to the Receiver Antenna input (J1-RFIN).

(c) Disconnect cable W1P2 from A4J1. Using cable adapter, connect the RF Millivoltmeter to W1P2. Set the RF Signal Generator for an output level of -80 dBm at a frequency of 1.5 MHz. Set R39 at Mid-Range, R47 fully counterclockwise, and R105 fully clockwise.

(d) Select AGC MAN only mode on the Receiver. Set the IF GAIN control for a reading of 8.5 ±0.1 VDC at TP9. The RF millivoltmeter should indicate approximately -20 dBm (-20 to -23 dBm nominal).

(e) Note the exact indication on the RF Millivoltmeter. Adjust R105 for a 1 dBm decrease in this reading.

(f) Reconnect cable W1P2 to A4J1. Set the IF GAIN control to maximum. Select the AGC SHORT mode (cancel MAN mode). Connect the RF Millivoltmeter, using the 50 ohm probe adapter, to J2 (if out) on the rear of the Receiver. Note and retain the RF Millivoltmeter reading as a reference (-10 dBm, +2, -1 dBm nominal).

(g) Set the output of the RF Signal Generator to -113 dBm. Select AGC MAN (cancel SHORT) mode. Adjust R39 for the same reading (+0.5, -0dBm) noted in step 6.

(h) Select AGC SHORT (cancel MAN) mode on the Receiver. Set the output of the RF Signal Generator to -80 dBm. Adjust R47 for a reading of 8.5 ±0.1 VDC at TP9.

(i) Set the output of the RF Signal Generator to -113 dBm. Note the reading on the RF Millivoltmeter. Increase the ouput of the RF Signal Generator to +10 dBm and note the reading on the RF Millivoltmeter. Observe that the readings remain within 2 dBm of each other.

(j) Initiate the automatic BITE Sequence.

(k) Upon successful completion of the BITE, disconnect Test Equipment from the Receiver.

1. Circuit Card A4 Installation. Refer to Figures 6-3 and 6-8.

NOTE

Ensure the A4 card has a jumper connected for either SSB ISB operation from LK1 to the appropriate point.

(1) make sure that cables and connectors are out of the way, then place the A4 circuit card in place and secure with twelve (12) screws, lock washers and flat washers.

(2) Connect ribbon connector W15P1 to A4J2.

(3) Connect ribbon connector W16P1 to A4J7.

(4) Connect ribbon connector A5W1P1 to A4J8.

(5) Connect SMB connector W10P1 to A4J6.

(6) Connect SMB connector W6P2 to A4J5.

(7) Connect SMB connector W12P1 to A4J4.

(8) Connect SMB connector W11P1 to A4J3.

(9) Connect SMB connector W1P2 to A4J1.

(10) Install the bandwidth filters and filter cover as directed in Chapter 2.

m. Circuit Card A5 Removal. Circuit Card A5 is optional and may or may not be installed in the Receiver. Refer to Figures 6-3 and 6-9.

(1) Perform the preliminary procedure as directed in Paragraph d.

(2) Disconnect ribbon connector A5W1P1 from A4J8.

NOTE

The connector disconnects from the A4 module, not the A5 module, and the ribbon cable is part of the A5 module.

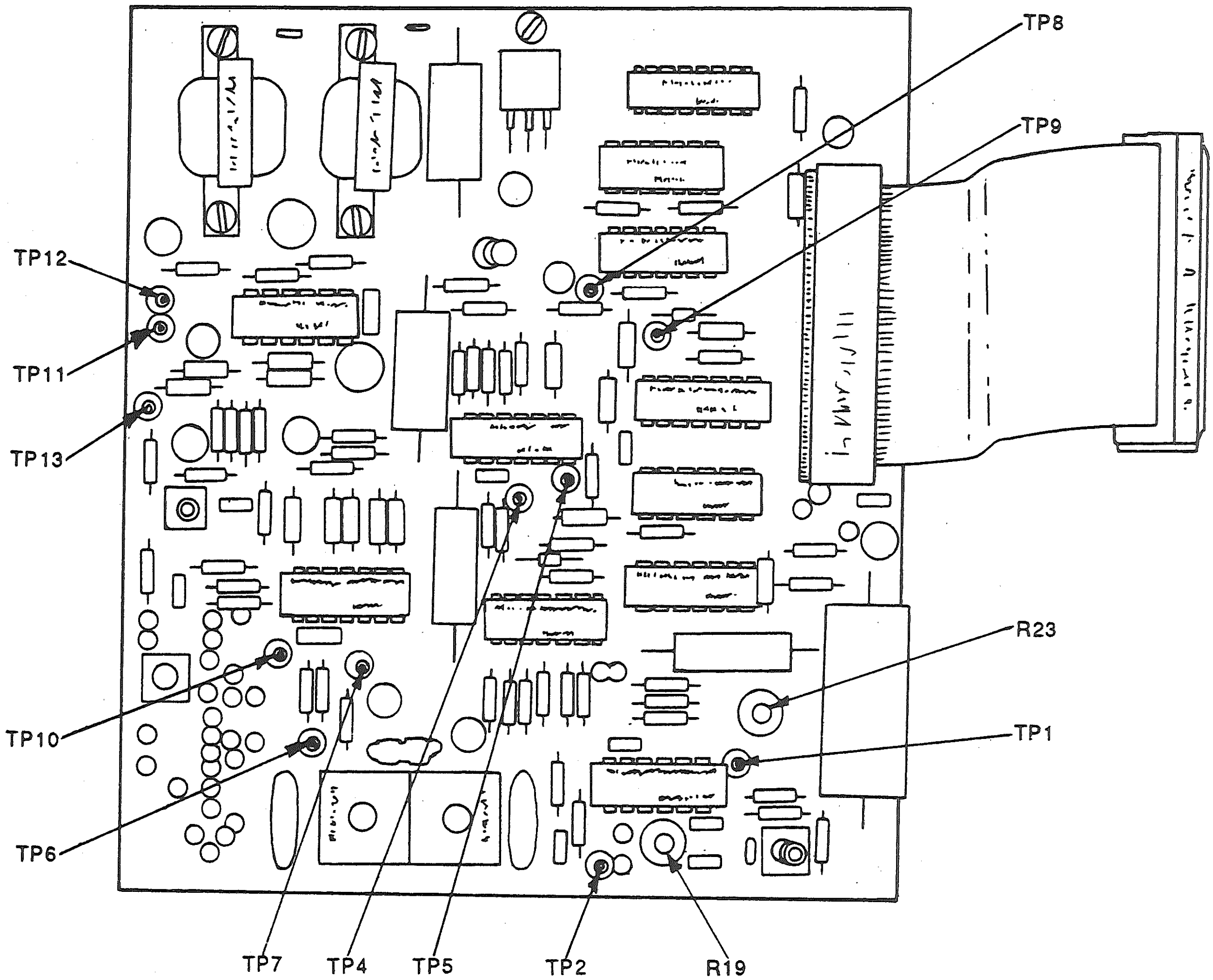


Figure 6-9A. ISB Circuit Card Assembly A5

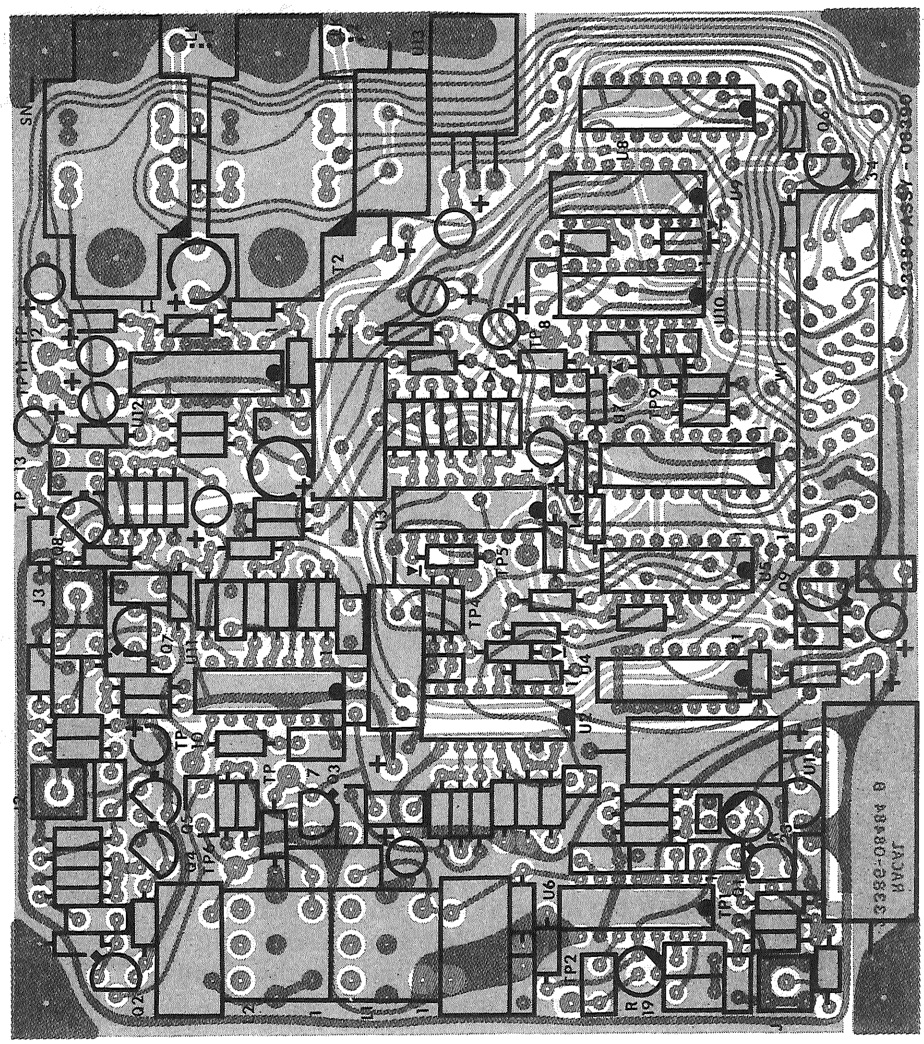


Figure 6-9B. ISB A5 Printed Circuit

(3) Disconnect SMB connector W10P2 from A5J3.

(4) Disconnect SMB connector W11P2 from A5J1.

(5) Loosen and remove the four (4) mounting screws, lock washers and flat washers from the four corners of the A5 module.

(6) Lift out the A5 module.

n. Circuit Card A5 Installation. If optional circuit card A5 is being installed for the first time, refer to Chapter 2 for installation of all associated hardware. Refer to Figures 6-3 and 6-9.

(1) Place the A5 module with the ribbon cable toward the A4 module and secure with four screws, lock washers and flat washers.

(2) Connect SMB connector W11P2 to A5J1.

(3) Connect SMB connector W10P2 to A5J3.

(4) Connect ribbon connector A5W1P1 to A4J8.

o. Module A6 Removal. Module A6 consists of circuit card A6A2 and optional circuit card A6A1 which may or may not be installed in the Receiver. If it is installed the two circuit cards must be removed together. Refer to Figures 6-3, 6-10 and 6-11.

(1) Perform the Preliminary Procedure in Paragraph d.

(2) Disconnect ribbon connector A9W1P2 from A6J1 on circuit card A6A2.

(3) If circuit card A6A1 is not installed, proceed to step (6). If it is installed, proceed with step (4).

(4) Remove two (2) screws, lock washers, and flat washers, from outside the rear panel, that secure A6A1W1J1 to the rear panel.

NOTE

Some Receivers are supplied with a nylon washer between the A6A1 and its middle-top mounting post. If this nylon washer is installed, it must be saved and reinstalled with the circuit card.

(5) Remove three screws, lock washers and flat washers securing the top of A6A1 to the Receiver. Remove the nylon washer, (if present) secured by the center screw, from between the circuit card and mounting post.

(6) Remove three screws, lock washers and flat washers that secure the top of A6A2 to the Receiver.

(7) Carefully lift out both (if A6A1 is installed) circuit cards or A6A2 circuit card. Circuit card A6A1 (if installed) may be separated from A6A2 by pulling the two apart which separates the 50 pin connectors A6P1 from A6J1.

p. Module A6 Installation. If circuit card A6A1 is to be installed in the Receiver it must first be joined with A6A2 and the two then installed together. Refer to Figures 6-3, 6-10 and 6-11.

(1) If A6A1 is to be installed with A6A2,perform steps (2) through (8). If A6A2 is installed alone, perform steps (3), (7) and (8).

(2) Carefully align and mate the 50 pin connectors of A6A1 and A6A2. Apply just enough pressure to bring them snugly together.

(3) Install either the two circuit cards together or the A6A2 circuit card alone by inserting the bottom of the card(s) into the nylon track on the receiver frame. Be sure that screw holes in the circuit card(s) align with screw holes in the receiver standoffs.

CAUTION

If a nylon washer is supplied as part of the hardware kit for A6A1 it must be installed between the Receiver standoff and the center mounting hole of A6A1 to prevent electrical damage from occuring.

(4) Place nylon washer (if supplied) between center mounting hole of circuit card A6A1 and receiver standoff. Insert screw, lock washer and flat washer through circuit card and nylon washer into standoff. Do not tighten screw.

(5) Install the other two (2) screws, lock washers and flat washers into circuit card A6A1. Do not tighten screws.

(6) Install two (2) screws, lock washers and flat washers from rear of rear panel into connector A6A1W1J1 and tighten. Tighten the three (3) screws holding A6A1 circuit card.

(7) Install three (3) screws, lock washers and flat washers through A6A2 mounting holes into the receiver standoffs and tighten screws.

(8) Connect ribbon connector A9W1P2 to A6J1 on circuit card A6A2.

q. Circuit Card A7 Removal. Refer to Figures 6-4 and 6-12.

(1) Perform the preliminary procedure as directed in Paragraph d.

(2) Loosen and remove the single screw and hardware that holds down the A7 cover.

(3) Using pull-tab remove the A7 cover.

(4) Disconnect ribbon connector W13P1 from A7J1.

(5) Disconnect SMB connector W3P1 from A7J2.

(6) Disconnect SMB connector W2P2 from A7J4.

(7) Loosen and remove the eleven (11) screws, lock washers and flat washers and nylon mounting post (from which the A7 cover screw was removed in Step (2) above) which holds down the A7 circuit card.

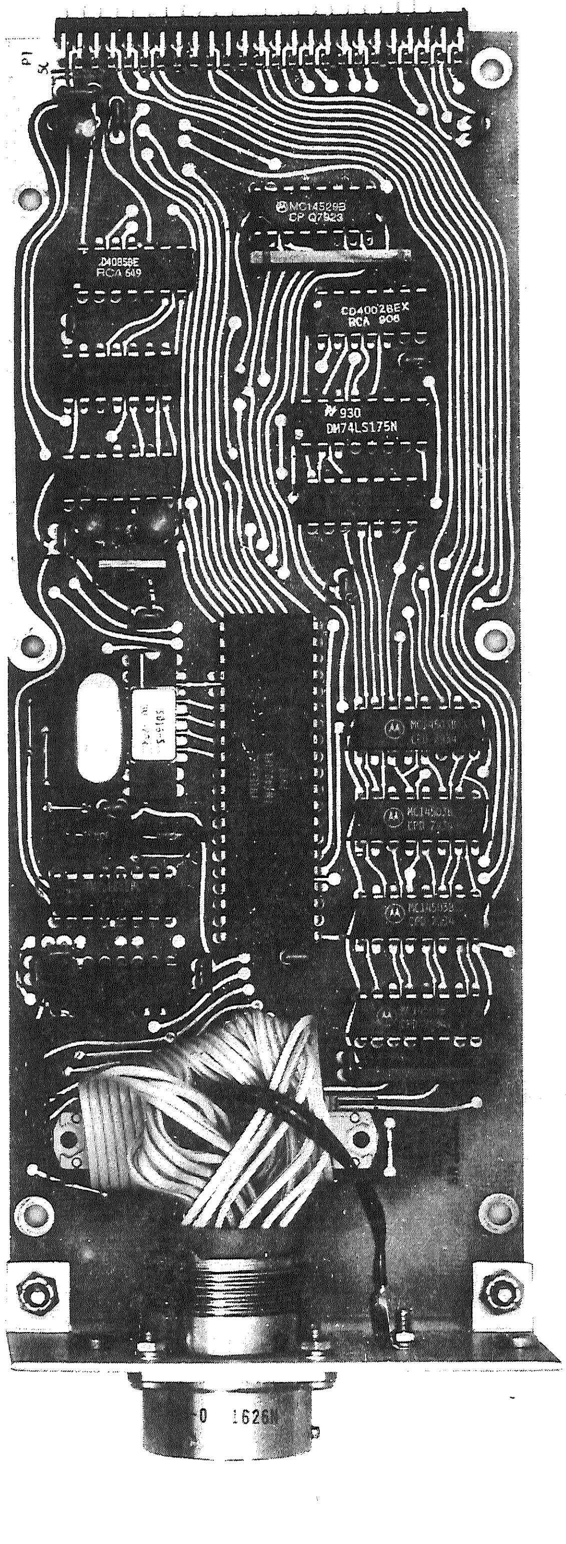


Figure 6-10A. Serial Asynchronous Interface Circuit Card A6A1 Assembly

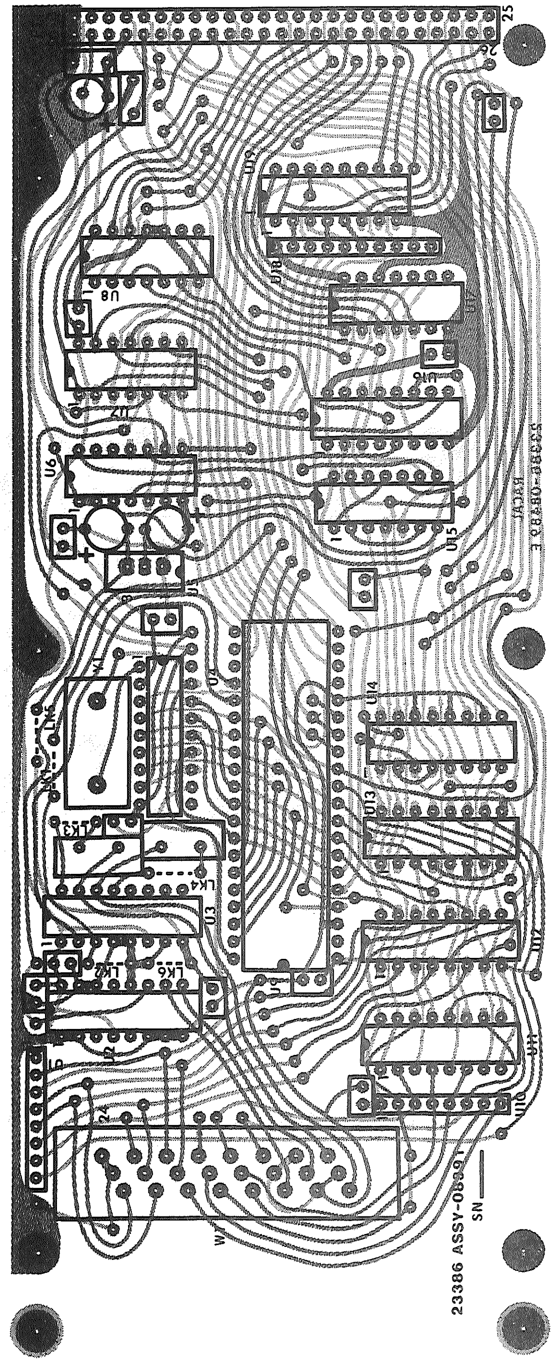


Figure 6-10B. Serial Asynchronous Interface A6A1 Printed Circuit

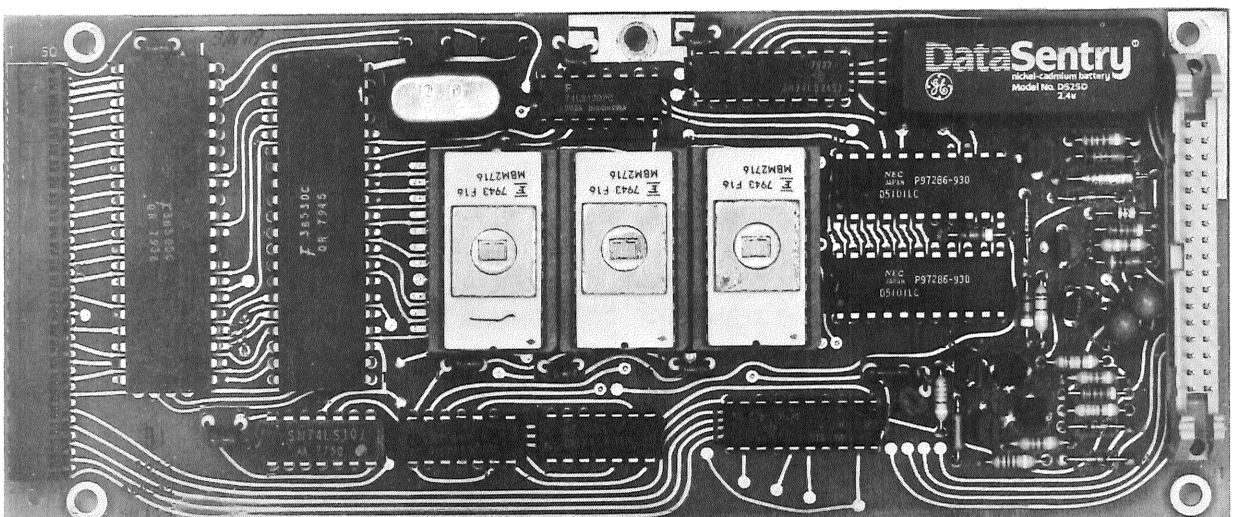


Figure 6-11A. Microcomputer Circuit Card A6A2 Assembly

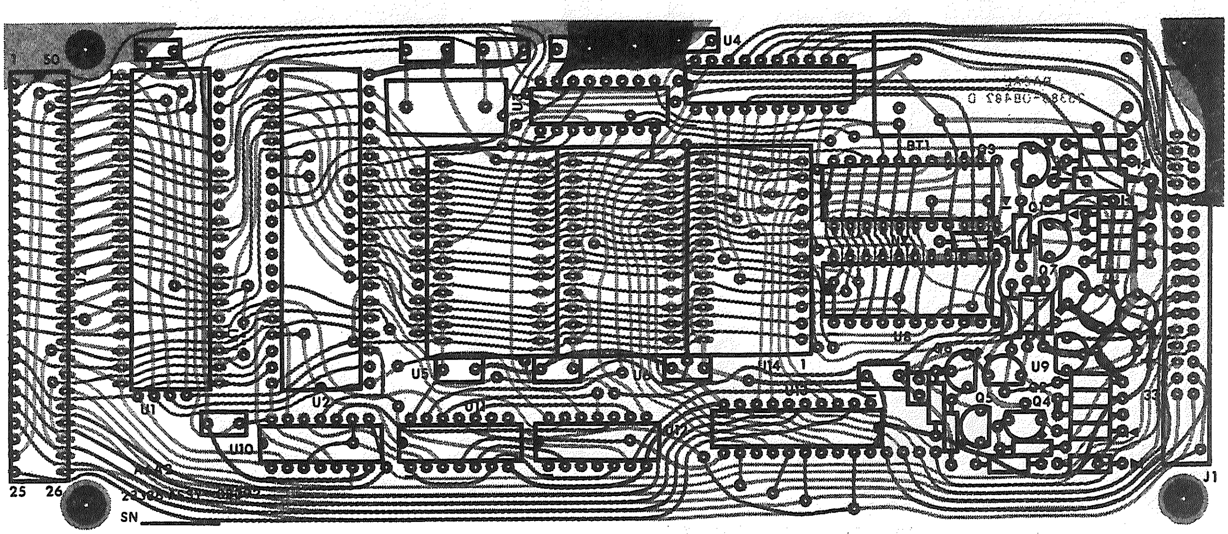


Figure 6-11B. Microcomputer A6A2 Printed Circuit

NOTE: Refer to Parts List for differences in the R-2174A Receiver.

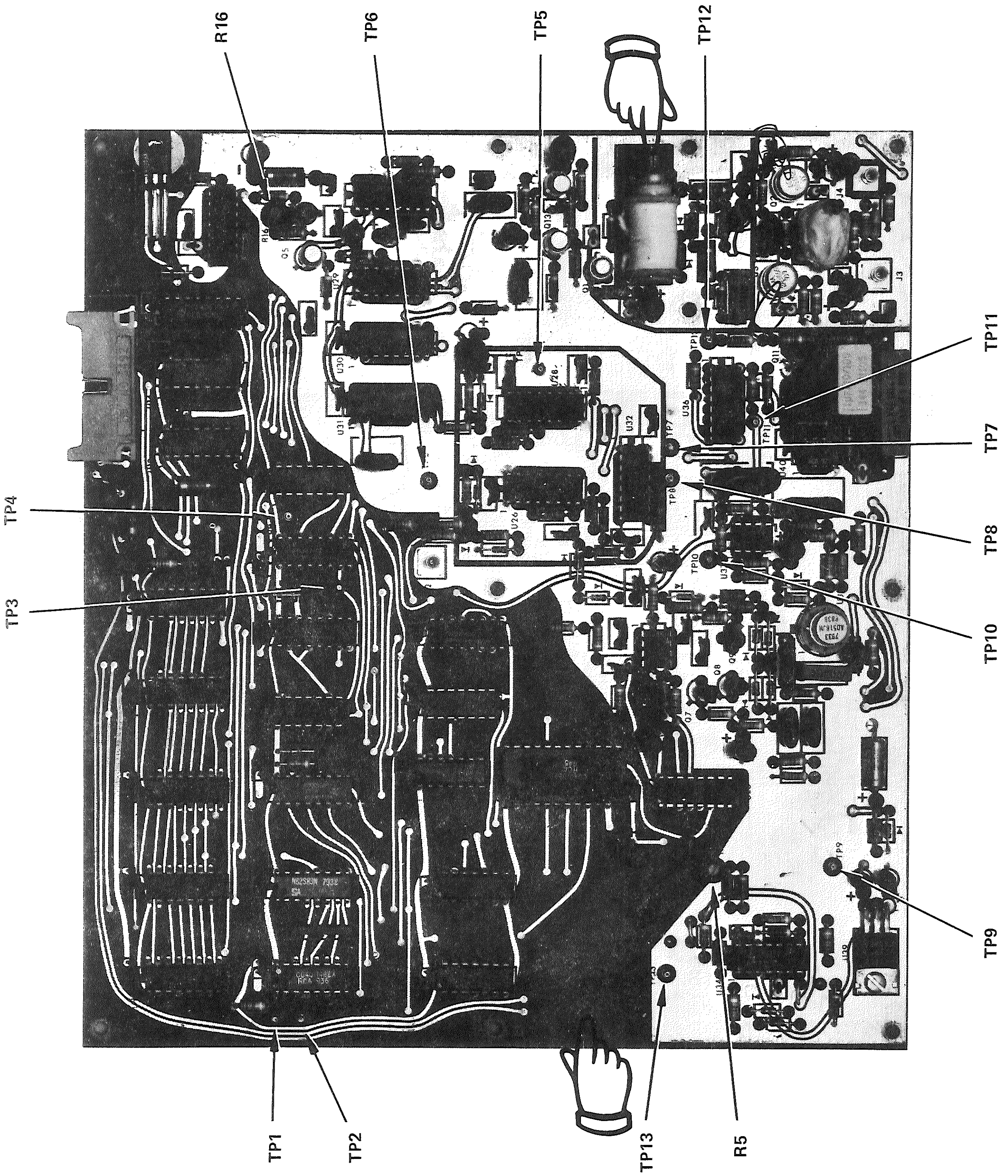


Figure 6-12A. First L.O. Circuit Card Assembly A7

NOTE: Refer to Parts List for differences in the R-2174A Receiver.

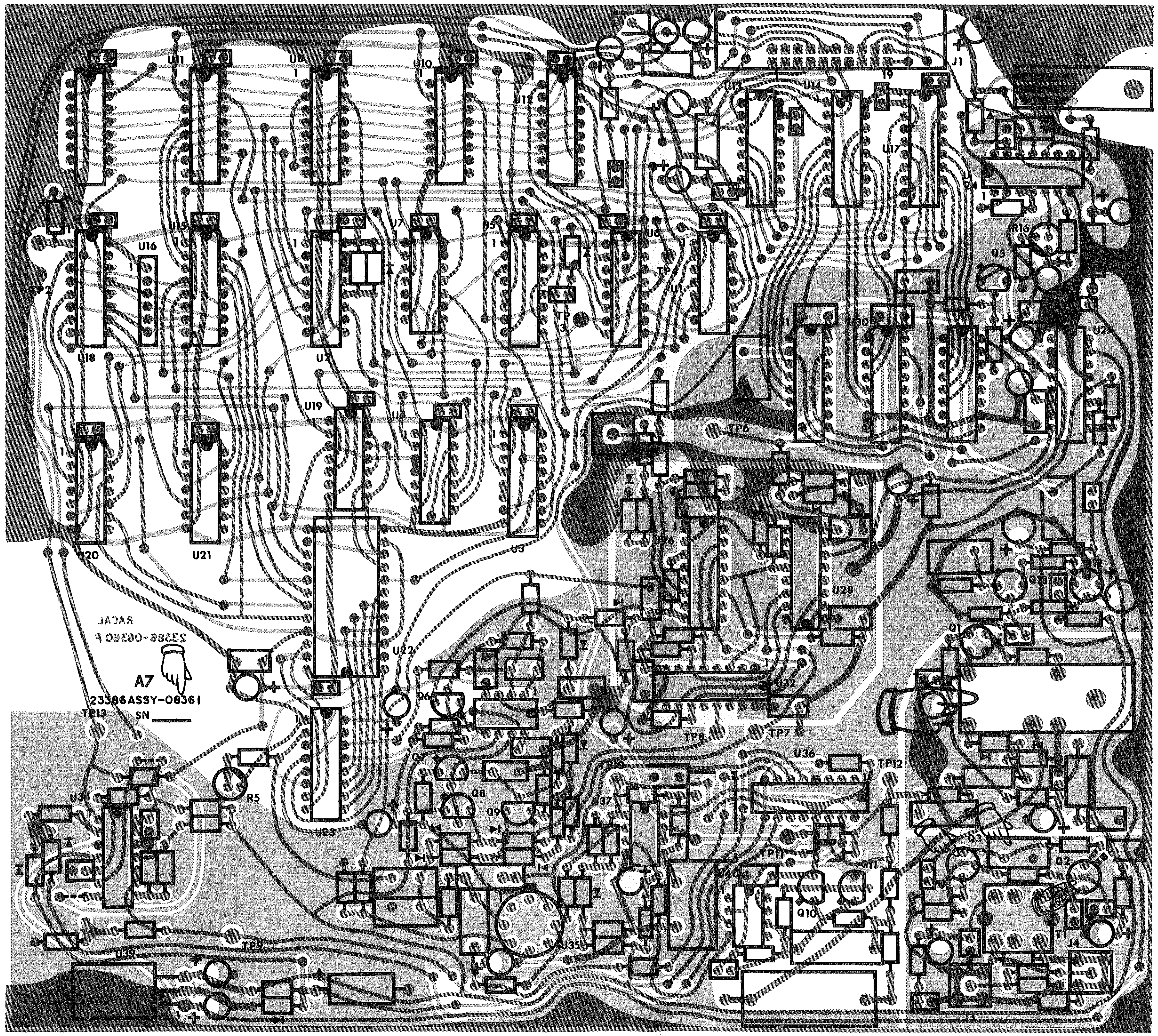


Figure 6-12B. First LO Synthesizer A7 Printed Circuit

NOTE

The screw through A7U39 is not a card holddown screw. The screw through regulator A7Q4 is a module holddown screw. When removing the screw through A7Q4, take care not to lose the mica insulator which fits between A7Q4 and the A7 circuit card.

(8) Lift out the A7 circuit card.

r. Circuit Card A7 Installation. Refer to Figures 6-4 and 6-12.

(1) Place the A7 circuit card in place, with ribbon connector A7J1 located next to chassis cut out, and secure with ten screws, lock washers and flat washers and nylon mounting post.

CAUTION

A mica insulator must be in place between A7Q4 and the circuit card. Do not overtighten the screw that secures A7Q4 or damage may result.

(2) Make sure mica insulator is between A7Q4 and circuit card and secure A7Q4 with screw, lock washer and flat washer. Do not over tighten.

(3) With a voltohm meter, perform a continuity check between the three elements of A7Q4 and receiver chassis. Correct any shorts prior to proceeding.

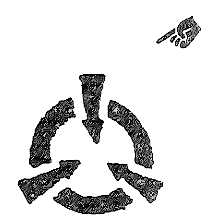
(4) Connect SMB connector W2P2 to A7J4.

(5) Connect SMB connector W3P1 to A7J2.

(6) Connect ribbon connector W12P1 to A7J1.

(7) Carefully install the A7 cover and secure with screw, lock washers and flat washer.

s. Circuit Card A8 Removal. Refer to Figures 6-4 and 6-13.



(1) Perform the Preliminary Procedure as directed in Paragraph d.

(2) Using the pull-tab, remove the A8 cover.

(3) Disconnect ribbon connector W14P1 from A8J5.

(4) Disconnect SMB connector W7P1 from A8J1.

(5) Disconnect SMB connector W6P1 from A8J4.

(6) Disconnect SMB connector W3P2 from A8J2.

(7) Disconnect SMB connector W4P2 from A8J3.

(8) Remove the eight screws, lock washers and flat washers which hold down the A8 circuit card.

(9) Lift out the A8 circuit card.

NOTE: Refer to Parts List for differences in the R-2174A Receiver.

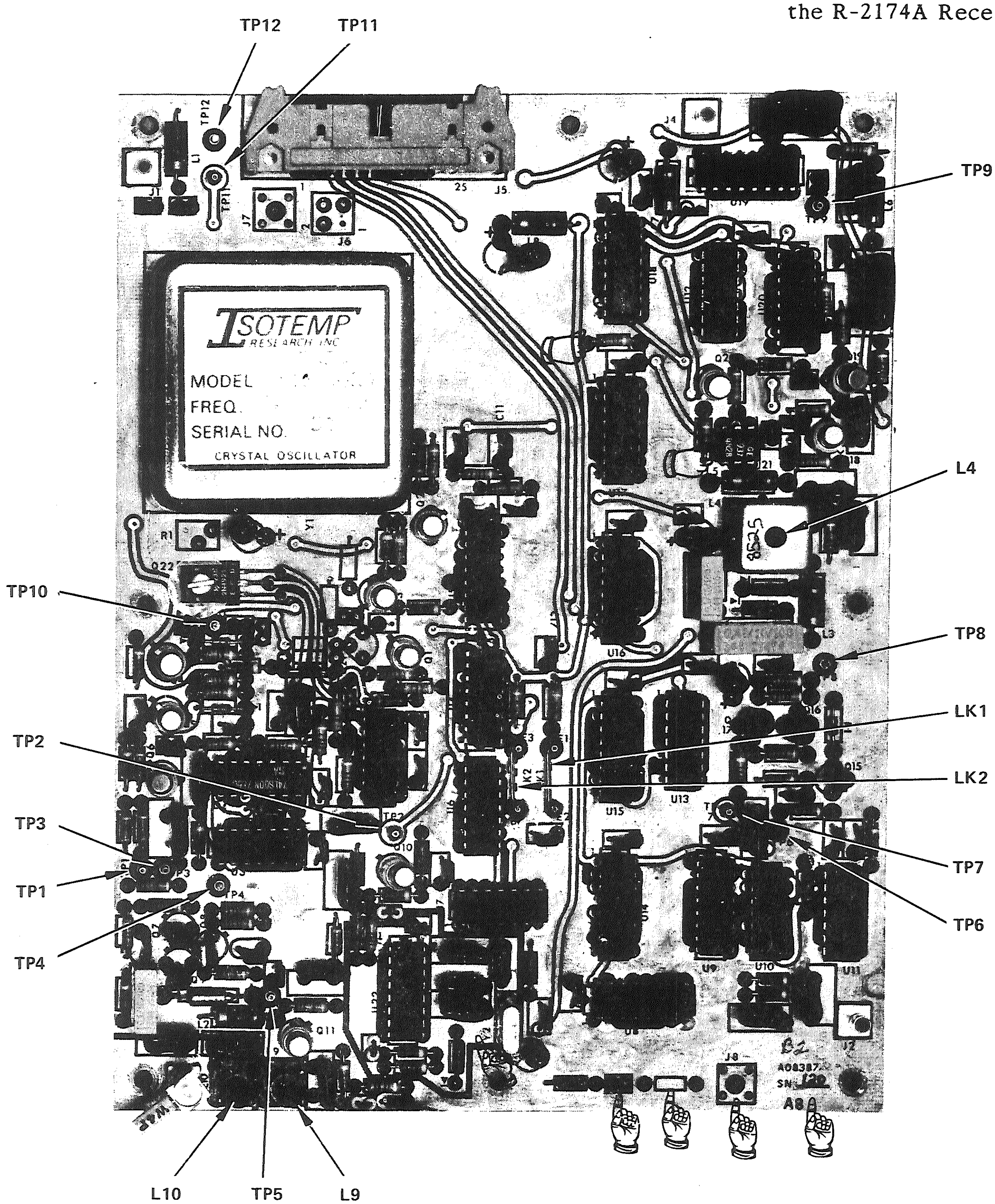


Figure 6-13A. Second LO/BFO Circuit Card Assembly A8

NOTE: Refer to Parts List
for differences in
the R-2174A Receiver.

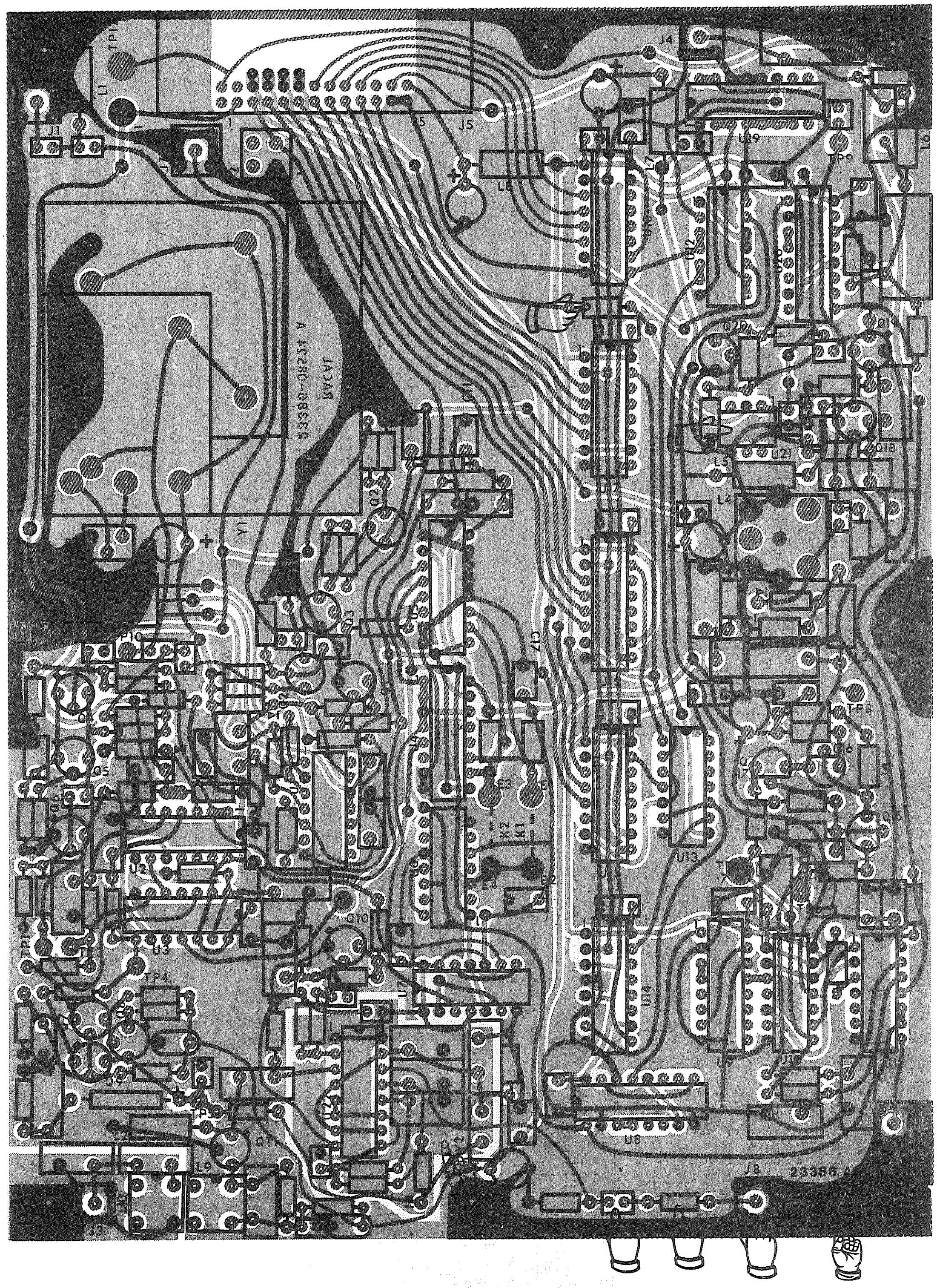


Figure 6-13B. Second LO/BFO Synthesizer A8 Printed Circuit

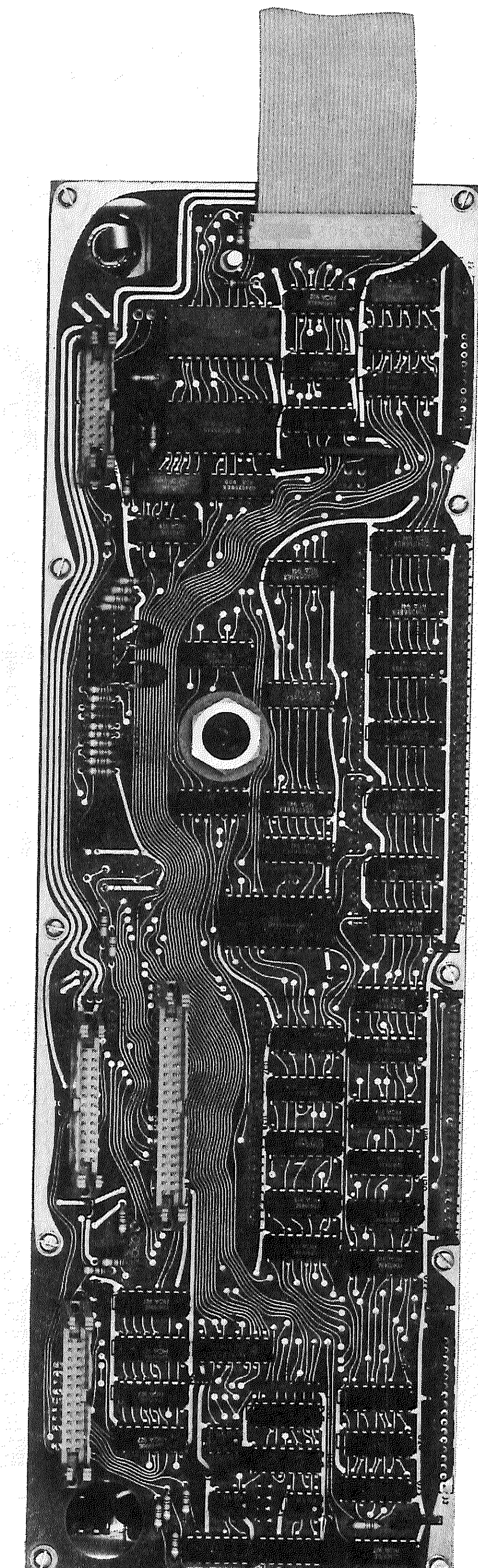


Figure 6-14A. Receiver Control Circuit Card A9 Assembly

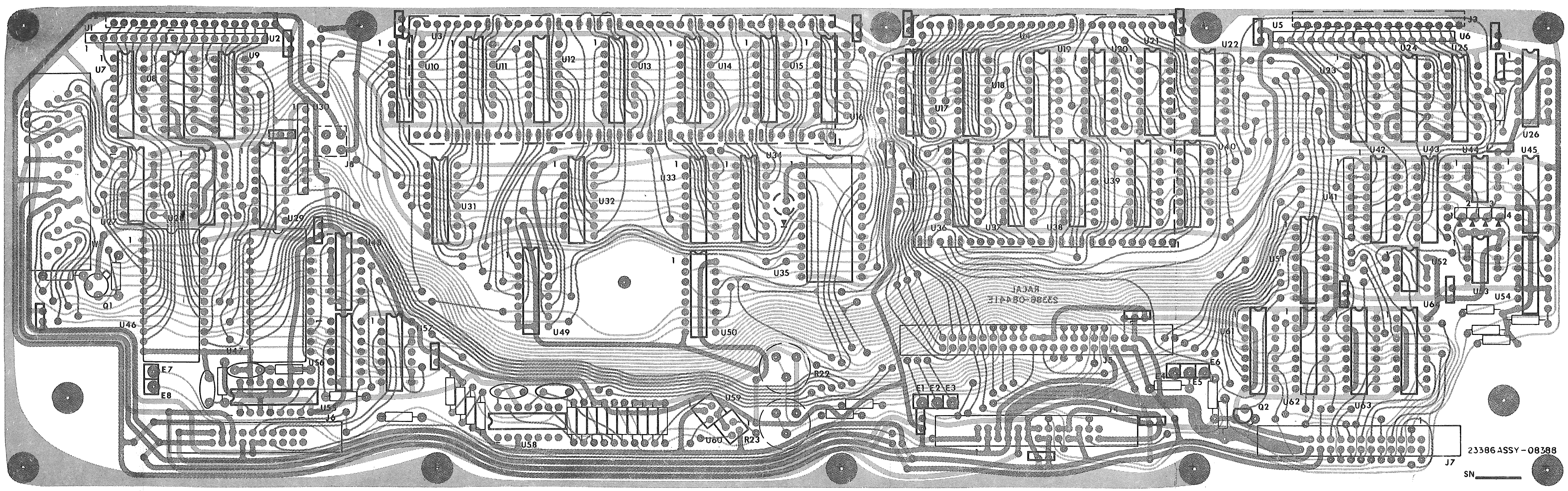


Figure 6-14B. Receiver Control A9 Printed Circuit

NOTE

Inspect the circuit card for proper strapping of the EXT REF at LK1 and LK2 for external reference used. Refer to page 8-47, Figure 8-11.

t. Circuit Card A8 Installation. Refer to Figures 6-4 and 6-13.

(1) Place the A8 circuit card so that ribbon connector J5 is located next to the cutout in the Receiver chassis and secure with eight (8) screws, lock washers and flat washers.

(2) Connect SMB connector W4P2 to A8J3.

(3) Connect SMB connector W3P2 to A8J2.

(4) Connect SMB connector W6P1 to A8J4.

(5) Connect SMB connector W7P1 to A8J1.

(6) Connect ribbon connector W14P1 to A8J5.

(7) Make sure cables entering the A8 compartment are routed through respective cutouts in the Receiver chassis and install the A8 cover.

u. Circuit Card A9 Removal, Inspection and Installation. Circuit card A9 is installed on the front panel assembly which includes the front panel, encoder assembly, keypads, edgelighting, LCD's, and other controls and switches. The disassembly, inspection and reassembly of the front panel assembly must be accomplished in order to remove the A9 circuit card and requires intricate procedures. These procedures are included in Section II of this chapter under special maintenance.

WARNING

The filter capacitors used in the power supply will retain an electrical charge after power is removed. The capacitors should be discharged slowly by shorting the terminals through a protected resistive device.

v. Module A10 Removal. Refer to Figures 6-3 and 6-15.

(1) Perform the preliminary procedure as directed in Paragraph d.

(2) Loosen (counterclockwise) the four (4) 1/4 turn fasteners on the A10 module cover.

(3) Carefully lift out the A10 module cover and discharge filter capacitors.

(4) Loosen three captive screws from the bandwidth filter cover on A4 and remove the cover.

(5) Disengage the locking clips (2 each) on connectors A10J2 and A10J3 located on the outside of the A10 module.

(6) Carefully unplug the connectors from A10J2 and A10J3.

(7) Loosen and remove the five (5) screws, lock washers and flat washers (located on the outside of the rear panel) which hold the back panel of the A10 module to the rear panel of the Receiver. Loosen the four captive screws at the base of the A10 module.

(8) Grasping the sides of the A10 module, slide the module away from the rear panel while lifting the end of the A10 module nearest the bandwidth filters and lift out the A10 module.

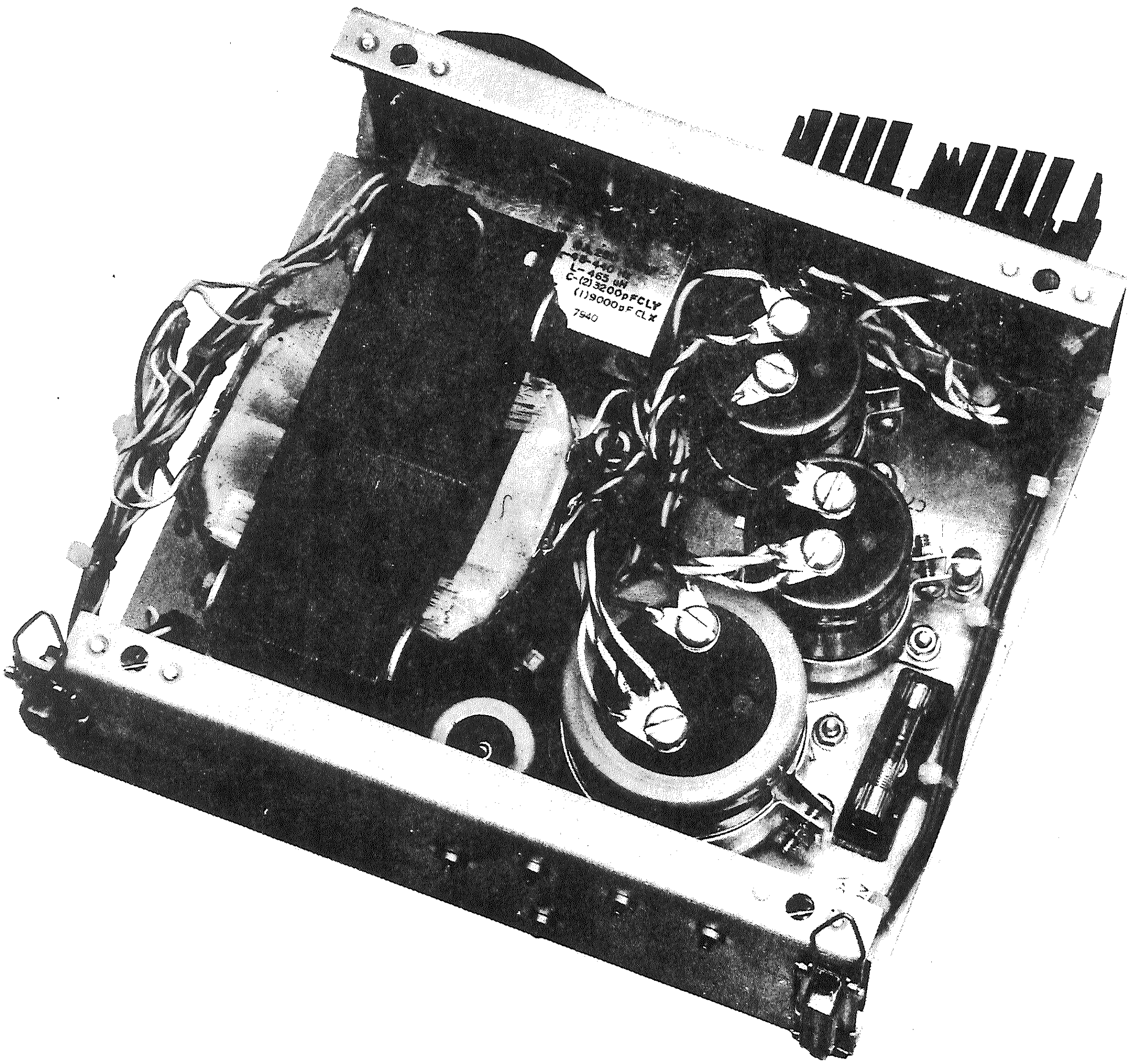


Figure 6-15A. Power Supply Module A10, Top View

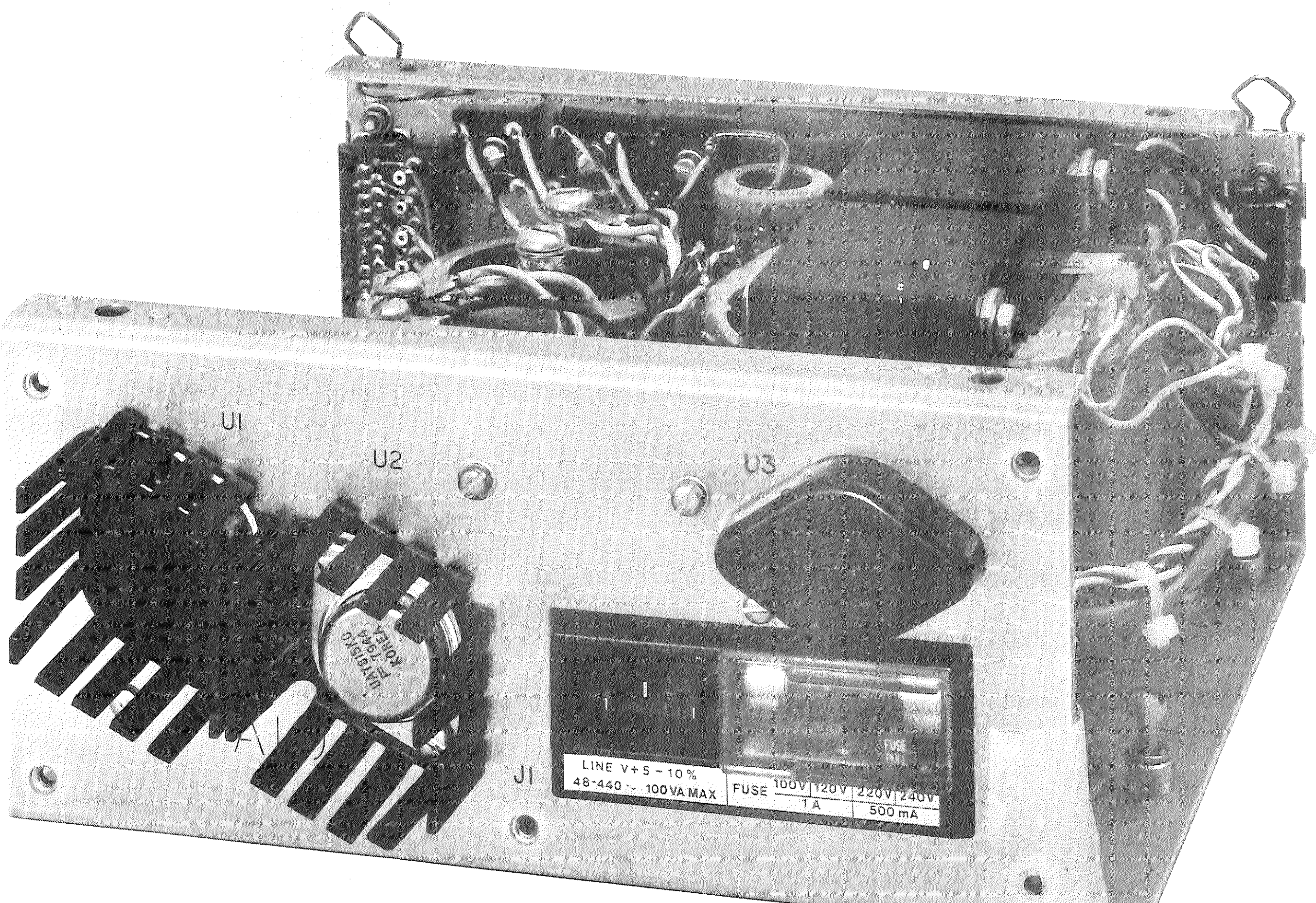


Figure 6-15B. Power Supply Module A10, Rear View

CAUTION

Take care not to crush the A10J2 or A10J3 connectors, the cooling fins on A10U1 or A10U2, or to snag the WP2 wire which connects to A4J1.

WARNING

The filter capacitors used in the power supply will retain an electrical charge after power is removed. The capacitors should be discharged slowly by shorting the terminals through a protected resistive device.

w. Module A10 Installation. Refer to Figures 6-3 and 6-15.

(1) Grasping the sides of the A10 module, keep the end toward the filters tilted upward and slide toward the rear panel.

CAUTION

Take care not to crush the A10J2 or A10J3 connectors, the cooling fins of A10U1 or A10U2 or to snag the WP2 wire which connects to A4J1.

(2) Install the five screws, lock washers and flat washers through the outside of the rear panel into the A10 module. Do not tighten.

(3) Insert the 4 captive screws in the bottom of the A10 module and tighten. Tighten the five screws in the rear panel.

(4) Connect W20P1 to A10J2 and W19P3 to A10J3 and secure with locking clips.

(5) Install the power supply cover and secure with the four one-quarter turn fasteners.

(6) Install the bandpass filter cover on circuit card A4 and secure with its three (3) captive screws.

SECTION II. SPECIAL MAINTENANCE

6-12. GENERAL. Special maintenance instructions are included here to facilitate maintenance at the intermediate level so that the unit does not have to be sent to the Technology Repair Center for these repairs. Included are the disassembly, repair/replacement and reassembly of the front panel assembly.

6-13. FRONT PANEL ASSEMBLY. The front panel assembly contains the A9 circuit card, encoder assembly, keypad switch assemblies S3 and S4 and other mechanically operated controls that can deteriorate during normal use. Refer to Figures 6-16 and 6-17 for illustrations of the encoder and front panel assembly. Since these sub-assemblies are entwined around the A9 circuit card (part of front panel assembly) a procedure for disassembly and reassembly of the complete front panel assembly is presented in step-by-step procedures. These procedures permit the removal of any sub-assembly desired by completing the step-by-step procedures to the point that removes that complete sub-assembly. Inspection, repair and replacement procedures are then presented to properly restore the affected parts. Reassembly instructions provided may then be used to reassemble the front panel assembly.

a. Dismantling and Disassembly.

(1) Remove top and bottom cover plates from the Receiver by loosening six quarter turn fasteners and disengaging each cover from the slot in the front panel by sliding to the rear.

(2) Remove connectors A9W1P1 from A6A2 and W13P2, W15P2, W19P1 and W14P2 from the A9 circuit card.

(3) Remove four 10-32 screws and nylon washers securing the front panel assembly to the gussets of the Receiver and carefully fold the assembly face down.

(4) Remove cable W20P1 connector from the A10 module connector A10J2.

(5) Remove the ribbon cables from A9P2 and A9P3 connectors that connect the keyboard switch assemblies S3 and S4 to the A9 circuit card. Do not attempt to remove the connectors.

(6) Remove the 6-32 screw, lock washer and flat washer from encoder disk, remove the disk, then remove spring washer and flat washer under disk.

(7) Encoder knob, shaft, retainer ring, shim washer and flat washer can now be removed together from front of front panel. Shim washer(s) and flat washer are loose and may be removed from disk end of shaft. Retainer ring may be removed from groove of shaft with retainer ring tool or other suitable device. Encoder knob may be removed from shaft by loosening two allen head screws, accessible through holes in circumference of knob.

(8) Remove knob from each IF and AF gain control by loosening allen head screw in each knob.

(9) Remove 3/8 x 32 hex nut, and internal tooth washer from each IF and AF GAIN control and from PHONES jack.

(10) Remove ½ x 20 hex nut, spring washer, flat washer and nylon washer from encoder spacer-bushing, located on component side of A9 circuit card.

(11) Remove ten 4-40 screws, lock washers and flat washers securing the A9 circuit card and carefully lift the circuit card away from the front panel, making sure the IF and AF GAIN controls and PHONES jack separates from the front panel. If these three items are to be removed from the circuit card their leads must be unsoldered.

(12) Disconnect W1P1 from A9J8 on the A8 circuit card.

(13) From the front of the front panel remove the ½ x 20 hex nut, spring washer and flat washer securing the encoder spacer-bushing to the front panel and remove the bushing.

(14) From the front of the front panel remove the ¼ x 24 hex nut, and internal tooth washer securing the POWER-ON switch S1 to the front panel and remove the switch, solder lug and cable assembly W20. NOTE: Cable W20 includes switch S1.

(15) Remove three (3) 4-40 hex nuts, lock washers and flat washers from the edge lighting assembly and remove the assembly.

(16) Remove five 4-40 hex nuts, lock washers and flat washers from light diffuser plate and lift the plate away from front panel, then lift switch assemblies S3 and S4 away from front panel.

b. Inspection, Repair and or Replacement.

(1) Encoder Assembly.

(a) Inspect the encoder spacer-bushing and encoder shaft for excessive wear or damage. Replace both of these items if excessive wear or damage is present.

(b) Inspect the flat washers,shim washers, spring washer and nylon washer. Spring washer must be able to take up end play in endoder shaft. Replace broken, damaged or worn items.

(c) Inspect the encoder disk for scratches, mars, dents or dirt on the mirrored or black surfaces. Also lay the disk on a flat surface and check for warpage. Replace the disk if it is warped or the mirrored or black surfaces are in any way impaired. Scratches or dark spots on the mirrored surfaces or light spots or scratches on the black areas will affect the encoder operation.

(d) Temporarily assemble the retainer ring, flat washer, shim washer, spacer-bushing (shoulder toward disk end of shaft), flat washer, spring washer, disk, flat washer, lock washer and 6-32 screw on the encoder shaft in the order given. Check the end play of the shaft within the spacer-bushing by holding the spacer-bushing and pushing on each end of the shaft. No end play should be detected when pushing on knob end of shaft, but approximately 0.030 inch of end play will be present when the shaft is pushed from the disk end; however, the spring washer should cause the shaft to return to its original position when released. If end play is too great shaft will float in the bushing and either additional or thicker shim washer must be added. If end play is insufficient shaft will not spin freely in bushing, and less shim is required. Disassemble the unit when correct end play is obtained.

(e) Inspect the encoder knob for damage, replace if necessary.

(2) Controls, POWER-ON Switch and PHONES Jack.

(a) Check the IF and AF GAIN controls for freedom of operation, signs of excessive heat or other damage. Using an ohmmeter check the resistance of each control. The IF GAIN control (R1) should be 50K ohms ±10%. The AF GAIN control (R2) should be 25K ohms ±10%. Replace either or both controls if they are found to be sub-standard.

(b) Inspect the AF and IF GAIN control knobs for any signs of damage, replace as required.

(c) Inspect the PHONES Jack for excessive wear or damage, replace if necessary.

(d) Inspect the POWER-ON switch for freedom of operation, signs of arcing or other damage, replace if necessary.

(3) Keyboard Switch Assemblies S3 and S4.

(a) Visually inspect the switch assemblies for wear, chipping, loss of nomenclature or other physical damage. Switch assemblies are non-repairable and must be replaced if damage has occurred.

(b) Using an ohmmeter with one lead connected to pin 1 (common) of the switch connector and the other lead alternately connected to pins 2 through 17, check the resistance, both with the appropriate key depressed and open. Resistance should be essentially 0 ohms when depressed and infinite ohms when open. If any keys do not show continuity when pressed and open when released, the entire assembly must be replaced.

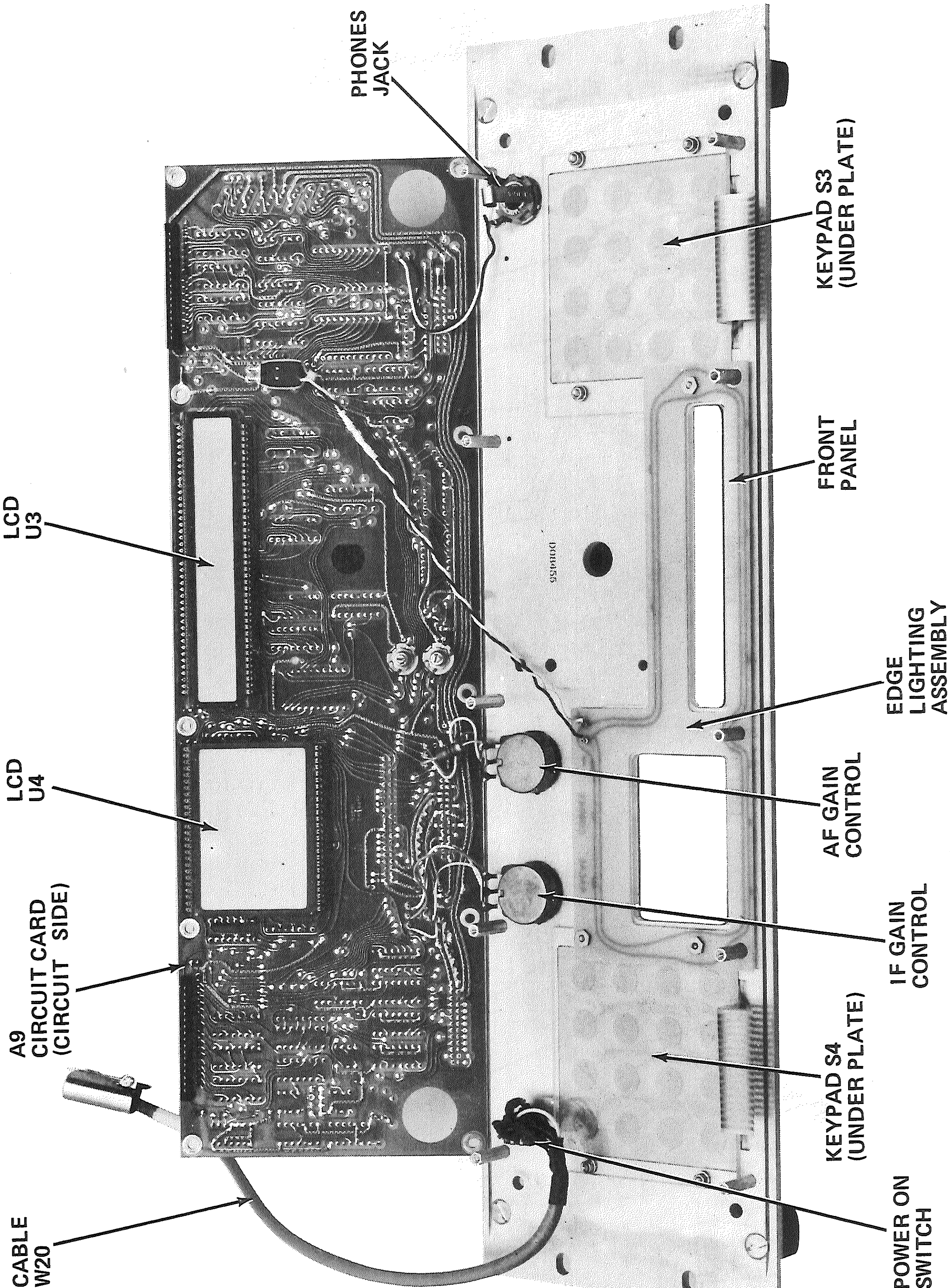


Figure 6-16. Front Panel (Assembly, Partially Disassembled.)

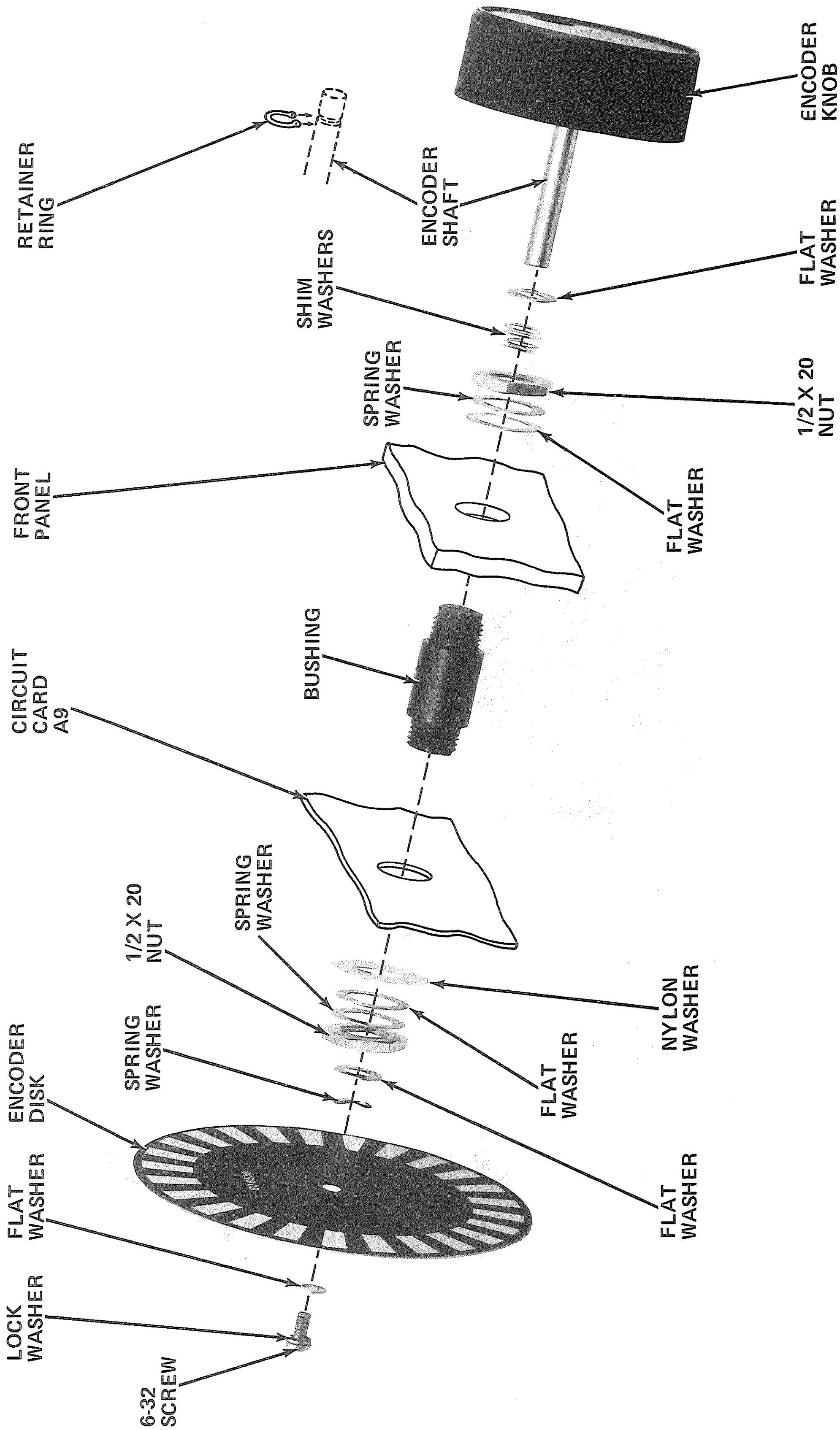


Figure 6-17. Encoder Assembly, Exploded View.

(4) Edge Lighting Assembly.

(a) Visually inspect the assembly for any signs of damage. Also inspect the lead wires and connector W1P1. The assembly is nonrepairable and must be replaced if damage has occurred.

(b) Connect a 15 volt supply through connector W1P1 to the edge lighting. All lamps should illuminate. If any lamps do not illuminate, replace the lamp(s).

(c) Edge Lighting Lamps may be disconnected (W1P1) in radios that are operated in well lighted work areas, thus greatly extending their usable life.

(5) Circuit Card Assembly A9.

(a) Check components for excessive heat, loose connections, corroded leads and other damage.

(b) Check LCDs for looseness or damage to the units.

(c) Check connectors for damaged or bent pins, loose connections, corrosion or other damage.

(d) Check the circuit card for damaged tracks, excessive heat, corrosion or other signs of deterioration.

c. Reassembly.

(1) Install keyboard switch assembly S3 in the opening on the right side (facing front of panel) with keys toward the front and with the ribbon cable extending toward the top of the panel. Place keyboard switch assembly S4 in the opening on the left side (facing the front panel) with keys toward the front and ribbon cable extending toward the top of the panel.

(2) Install light diffuser over studs in front panel so that windows match the openings in front panel. Install five 4-40 hex nuts, lock washers and flat washers.

(3) Install the edge lighting assembly over the studs so that its windows fit the front panel openings. Install three 4-40 hex nuts, lock washers and flat washers. Connect W1P1 to A9J8 on circuit card A9.

(4) Cable W20 has been removed from front panel. Replace as follows: Install solder lug over shank of switch, then install shank through 1/4 inch round hole in left side of front panel. Be sure switch is placed so that ON is toward top of panel. Secure with internal tooth washer and 1/4 x 24 hex nut.

(5) Install the shoulderless end (shoulder toward circuit card A9) of the encoder spacer-bushing through the 1/2 inch round hole located near the center of the front panel. Secure with flat washer, spring washer and 1/2 x 20 hex nut.

(6) If AF or IF GAIN control or PHONES jack leads have been unsoldered they must be resoldered. Refer to schematic diagram in Chapter 8 for proper lead identification. Insert the shaft of these three items into their respective holes in the front panel and place circuit card A9 on the standoffs extending from the back of the front panel. Be sure encoder spacer-bushing is fitted through hole in circuit card. Secure the circuit card with ten flat washers, lock washers and 4-40 screws.

(7) Place the ½ inch nylon washer, flat washer and spring washer over the threads of the spacer-bushing in the order given and secure them with the ½ x 20 hex nut. Tighten only finger tight.

(8) Secure the IF and AF GAIN controls and PHONES jack each with an internal tooth washer and 3/8 x 32 hex nut.

(9) Install the IF and AF GAIN control knobs and secure them by tightening the allen head screw in each knob.

(10) Assemble the retainer ring, flat washer and shim washer on the encoder shaft, in the order given. Install the encoder shaft, from the front of the front panel, through the spacer-bushing. Install flat washer, spring washer, disk (mirror surfaces toward A9 circuit card), flat washer and lock washer in the order given. Secure with 6-32 screw.

(11) Install the encoder knob and secure by tightening two allen head screws in the knob. Inspect the encoder assembly for freedom to spin and for wobble in the disk.

(12) Install the ribbon cables into their respective connectors P2 and P3 located on the A9 circuit card.

(13) Connect connectors W14P2, W19P1, W15P2 and W13P2 to their respective connectors on the A9 circuit card. Connect connector A9W1P1 to its connector on the A6A2 circuit card, connect cable W20P1 connector to A10J2 on the A10 module.

(14) Install the front panel assembly to the gussets of the Receiver with four nylon washers and 10-32 screws.

(15) Install the top and bottom cover plates on the Receiver and secure each cover with six quarter turn fasteners.

CHAPTER 7
ILLUSTRATED PARTS BREAKDOWN

7-1. **INTRODUCTION.** This illustrated parts breakdown (IPB) provides parts information on the R-2174(P)/URR Radio Receiver. The information is presented in four sections in accordance with Specification MIL-M-38807. The four sections include: Section I, Introduction; Section II, Maintenance Parts List (MPL); Section III, Numerical Index; and Section IV, Reference Designation Index. Section I, Introduction, describes the information contained in the IPB, the arrangement of that information and how to use it. Section II, Maintenance Parts List, lists all parts in disassembly sequence along with illustrations that show that sequence. Section III, Numerical Index, lists the same parts contained in Section II but in alpha-numerical sequence. Section IV lists all parts with reference designations in a reference designation sequence.

Section I. INSTALLATION LOGISTICS

7-2. **MODELS COVERED.** The Illustrated Parts Breakdown covers only one model of the R-2174(P)/URR Radio Receiver.

7-3. **PARTS LISTED.** In general, the assemblies and parts installed at the time the end item was manufactured are listed and identified in the manual. When an assembly or part (including vendor items), which is different from the original was installed during the manufacture of later items, series, or blocks, all assemblies and parts are listed (and "Usable on Coded"). However, when the original assembly or part does not have continued application (no spares of replacement), only the preferred assembly or part is listed. Also, when an assembly or part was installed during modification, and the original does not have continued application, only the preferred item is listed. Interchangeable and substitute assemblies and parts, subsequently authorized by the government, are not listed in this manual; such items are identified by information available through the Interchangeable and Substitute (I&S) Data Systems. Refer to TO 00-25-184. When a standard size part can be replaced with an oversize or undersize part, the latter parts, showing sizes, are also listed. Repair parts kits and quick change units are listed when they are available for replacement.

7-4. **SIMILAR ASSEMBLIES.** All assemblies in the R-2174(P)/URR Radio Receiver are sufficiently different to require separate listings for each assembly and are so listed in disassembly sequence.

7-5. **QUICK CHANGE UNITS.** Fifteen Bandpass Crystal Filters are available for plug-in to seven filter slots in the Receiver. All fifteen filters are listed as quick change units while the filters actually installed in the Receiver are left to the discretion of the operator.

7-6. **SYMBOLS AND ABBREVIATIONS.** Table 7-1 lists symbols and abbreviations used throughout the illustrated parts breakdown. The table lists abbreviations, symbols, and reference designators in that order.

MANUFACTURERS CODES. Section II, Maintenance Parts List, lists along with each part number the manufacturer in a five digit code. This number listed under FSCM (Federal Supply Code for Manufacturers) is decoded in Table 7-2. This table lists the code in numerical sequence and defines the name and address of the manufacturer.

TABLE 7-1. SYMBOLS AND ABBREVIATIONS

Symbol or Abbre-viation	Description	Symbol or Abbre-viation	Description
AC	Alternating Current	uh	Micro henry (10^{-6})
AF	Audio Frequency	*	Decal, logo
AM	Amplitude Modulation	#	Number, size
AP	Attaching Part		REFERENCE DESIGNATIONS
BCD	Binary Coded Decimal		
BFO	Beat Frequency Oscillator	A	Printed Circuit Boards
Coax	Coaxial-used with Cable	BT	Battery
DC	Direct Current	C	Capacitor
DPDT	Double Pole-Double Throw	CR	Diode
EPROM	Erasable Programmable Read Only Memory	DS	Indicator
FM	Frequency Modulation	E	Terminal
Hex	Hexagonal	F	Fuse
IF	Intermediate Frequency	FL	Filter
ISB	Independent Side Band	J	Connector, Jack
K ohms	thousand ohms (10^3)	L	Inductor, Choke, or Coil
LO	Local Oscillator	LK	Link
LPF	Low Pass Filter	P	Connector, Plug
meg ohms	million ohms (10^6)	Q	Transistor
pf	Pico farrads (10^{-12})	R	Resistor
RAM	Random Access Memory	S	Switch
ROM	Read Only Memory	T	Transformer
RF	Radio Frequency	U	Integrated Circuit
SMI	System Memory Interface	W	Cable
UART	Universal Asynchronous Receiver Transmitter	XF	Fuse Holder
WVDC	Working Volts, Direct Current	XU	Socket, Integrated Circuit
uf	Micro farrads (10^{-6})		

TABLE 7-2. FEDERAL SUPPLY CODES FOR MANUFACTURERS

FSCM	Name and Address	FSCM	Name and Address
01295	Texas Instruments, Inc. Semiconductor Components Div. Dallas, TX 75222	07263	Fairchild Semiconductor, A Division of Fairchild Camera and Instr. Corp. 464 Ellis St. Mountain View,CA 94040
02735	RCA Corp. Solid State Division Route 202 Somerville, NJ 08876	07374	Optron Corp. 50 Fitch Street New Haven, CT 06515
04222	Aerovox Corp. P.O. Box 867, Aerovox Road Myrtle Beach, SC 29577	07556	Callabro Plastics, Inc. 8738 Westchester Pike Upper Darby, PA 19082
04713	Motorola, Inc. Semiconductor Products Div. 5005 E. McDowell Road Phoenix, AZ 85008	07623	Eck and Kribs Scientific Laboratory Glass Apparatus Inc. 2709 40th Ave. Long Island City, NY 11101
04729	Universal Components Corp. Rock Ave. & Route 22 Green Brook, NJ 08812	08050	Dexter Lock Div. of Kysor Industrial Corp. 1601 Madison Ave SE Grand Rapids, MI 49502
05245	Components Corp. 2857 N. Halstead St. Chicago, IL 60657	08523	Metal Craft Inc. 34 Burgess Wayne, NJ 07470
05820	Wakefield Engineering Inc. Audubon Rd. Wakefield, MA 01880	09922	Burndy Corp. Richards Ave. Norwalk, CT 06852
05972	Loctite Corp. 705 N. Mountain Road Newington, CT 06111	13103	Thermoloy Co. 8717 Diplomacy Row Dallas, TX 75247
06540	Amatom Electronic Hardware Division of Mite Corp. New Rockville, NY	13257	Esna Ltd. 10 Esna Park Drive Markham, Ontario, Canada
06776	RobinsonNugent, Inc. P.O. Box 470 800 E. 8th St. New Albany, IN 47150	14655	Cornell Dubilier Electronics Div. of Federal Pacific Electric Co. Government Contracts Dept. 150 Ave L Newark, NJ 07101
06915	Richco Plastics Co. 5825 N. Tripp Ave. Chicago, IL 60646	16428	Belden Corp. P.O. Box 341 Richmond, IN 47374

TABLE 7-2. FEDERAL SUPPLY CODES FOR MANUFACTURERS (Cont.)

FSCM	Names and Addresses
17069	Circuit Structures Lab. 3200 N. San Fernando Blvd. Burbank, CA 91504
17896	Jermyn Industries Mfg. Div. 712 Montgomery Street San Francisco, CA 94111
18324	Signetics Corp. 811 E. Arques Sunnyvale, CA 94086
22526	Berg Electronics Inc. Youk Expressway New Cumberland, PA 17070
23386	Racal Communications Inc. 5 Research Place Rockville, MD 20850
24355	Analog Devices, Inc. P.O. Box 280, Route 1 Industrial Park Norwood, MA 02062
24446	General Electric Co. 1 River Road Schenectady, NY 12305
27014	National Semiconductor Corp. 2950 San Ysidro Way Santa Clara, CA 95051
27193	Cutler Hammer Inc. Specialty Products Div. 420 N. 27th Street Milwaukee, WI 53216
27440	Industrial Screw Products Co. 2238 Purdue Ave. Los Angeles, CA 90064
28198	Positronic Industries Inc. 1906 S. Stewart Springfield, MO 65804
28480	Hewlett Packard Co. Corporate Hdqtrs. 1501 Page Mill Road Palo Alto, CA 94304
30983	Electra/Midland Corp. A North American Phillips Co. 11468 Sorrento Valley Road San Diego, CA 92121
31148	PMI Corp. 11335 Folsom Blvd. Rancho Cordova, CA 95670
31433	Union Carbide Corp. Material Systems Div. Components Dept. Highway 276 SE Greenville, SC 29606
32293	Intersil Inc. 10900 N. Tantau Ave. Cupertino, CA 95014
32997	Bovins Inc. Trimpot Products Division 1200 Columbia Ave. Riverside, CA 92507
34335	Advanced Micro Devices 901 Thompson Place Sunnyvale, CA 94086
34649	Intel Corp. 365 Middlefield Rd. Mountain View, CA 94040
49956	Raytheon Corp. 141 Spring Street Lexington, MA 02173
50088	Mostek Corp. 1400 Upperfield Drive Carrollton, TX 75006
52072	Circuit Assembly Corp. 3169 Redhill Ave. Costa Mesa, CA 92626
52673	KSW Electronics Corp. South Bedford St. Burlington, MA 01803

TABLE 7-2. FEDERAL SUPPLY CODES FOR MANUFACTURERS (Cont.)

FSCM	Names and Addresses	FSCM	Names and Addresses
52763	Stettner Trush Inc. 67 Albany Street Cazenovia, NY 13035	81349	Military Specifications Promulgated by Military Departments/ Agenices under authority of Defense Standardization Manual 41203-M
52783	Gyrex Corp. 436 E. Gutierrez Santa Barbara, CA 93101	83003	Varo Inc. 800 W. Garland Ave. Garland, TX 75040
53848	Siliconix Inc. 2201 Laurelwood Rd. Santa Clara, CA 95054	83330	Smith Herman H Inc. 812 Snediker Ave. Brooklyn, NY 11207
56289	Sprague Electric Co. North Adams, MA 01247	86797	Rogan Bros. Inc. 8031 N. Monticello Snokie, IL 60076
71400	Bussmann Mfg. Div. of McGraw Edison Co. 2536 W. University Street St. Louis, MO 63107	86928	Seastrom Mfg. Co. Inc. 701 Sonora Ave. Glendale, CA 91201
71468	ITT Cannon Electric 666 E. Dyer Road Santa Ana, CA 92702	91293	Johanson Mfg. Co. P.O. Box 329 Boonton, NJ 07005
71590	Centralab Electronics Division of Globe Union Inc. 5757 N. Green Bay Ave. Milwaukee, WI 53201	91637	Dale Electronics Inc. P.O. Box 609 Columbus, NE 68601
73734	Federal Screw Products Inc. 3917 N. Kenzie Ave. Chicago, IL 60618	91836	Kings Electronics Co. Inc. 40 Marbledale Road Tuckahoe, MY 10707
73743	Fischer Special Mfg. Co. 446 Morgan Street Cincinnati, OH 45206	95987	Weckesser Co. Inc. 4444 West Irving Park Rd. Chicago, IL 60641
75037	Minnesota Mining and Mfg. Co. Electro Products Div. 3M Center St. Paul, MN 55101	96906	Military Standards Promulgated by Military Departments under authority of Defense Standardization Manual 41203-M
75915	Littlefuse Inc. 800 E. Northwest Hwy. Des Plaines, IL 60016	97244	Mallory Metallurgical Co. 3029 E. Washington Street Indianapolis, IN 46206
78912	Garlock Inc. Plastics Div. 602 N. 10th Street Camden, NJ 08101	98291	Sealectro Corp. 225 Hoyt Mamaroneck, NY 10544

7-8. USABLE ON CODES. The Usable On Code column in the Section II parts list is included to show application of parts to different models, configurations, types, etc. of the Radio Receiver. The original R-2174 parts are shown with no code in this column. Differences in the R-2174A version are shown by an A in the Useable On Codes column.

7-9. SOURCE, MAINTENANCE, AND RECOVERABILITY (SMR) CODES. Definitions of applicable source, maintenance, and recoverability (SMR) codes are set forth in TO 00-25-195. These codes for all parts listed are included in the MPL in Section II under the SMR column.

7-10. FINDING PART NUMBER, ILLUSTRATION, DESCRIPTION. The IPB includes part numbers, illustrations of parts, description of parts, reference designations of electrical parts, units per assembly, quantity per end item, codes for manufacturers of each part listed and SMR codes. Figure 7-0 illustrates a technique to aid the technician in locating information in the manual. This illustration shows how a part number can be found through the table of contents and illustrations or how the illustration of a part can be located when a part number is known. When a part number is located in the MPL, its description, units per assembly, SMR and FSCM codes will be in the same line as the part number. If the quantity per end item is desired refer to the part number in the Numerical Index. If only a reference designation is known refer to that Section which lists the Figure and index number for each electrical part in alpha-numerical sequence of reference designations.

SECTION II
MAINTENANCE
PARTS LIST
(MPL)

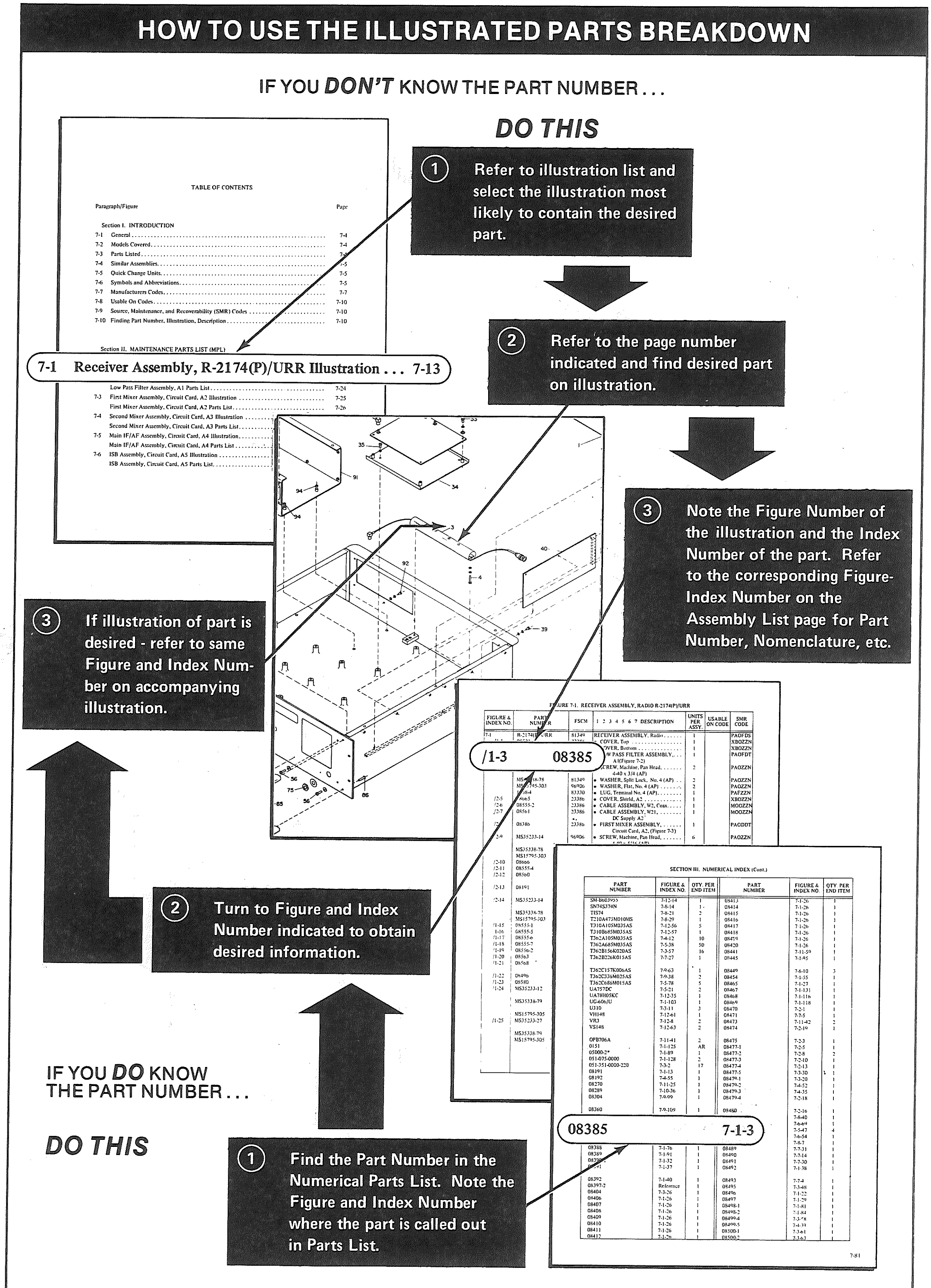
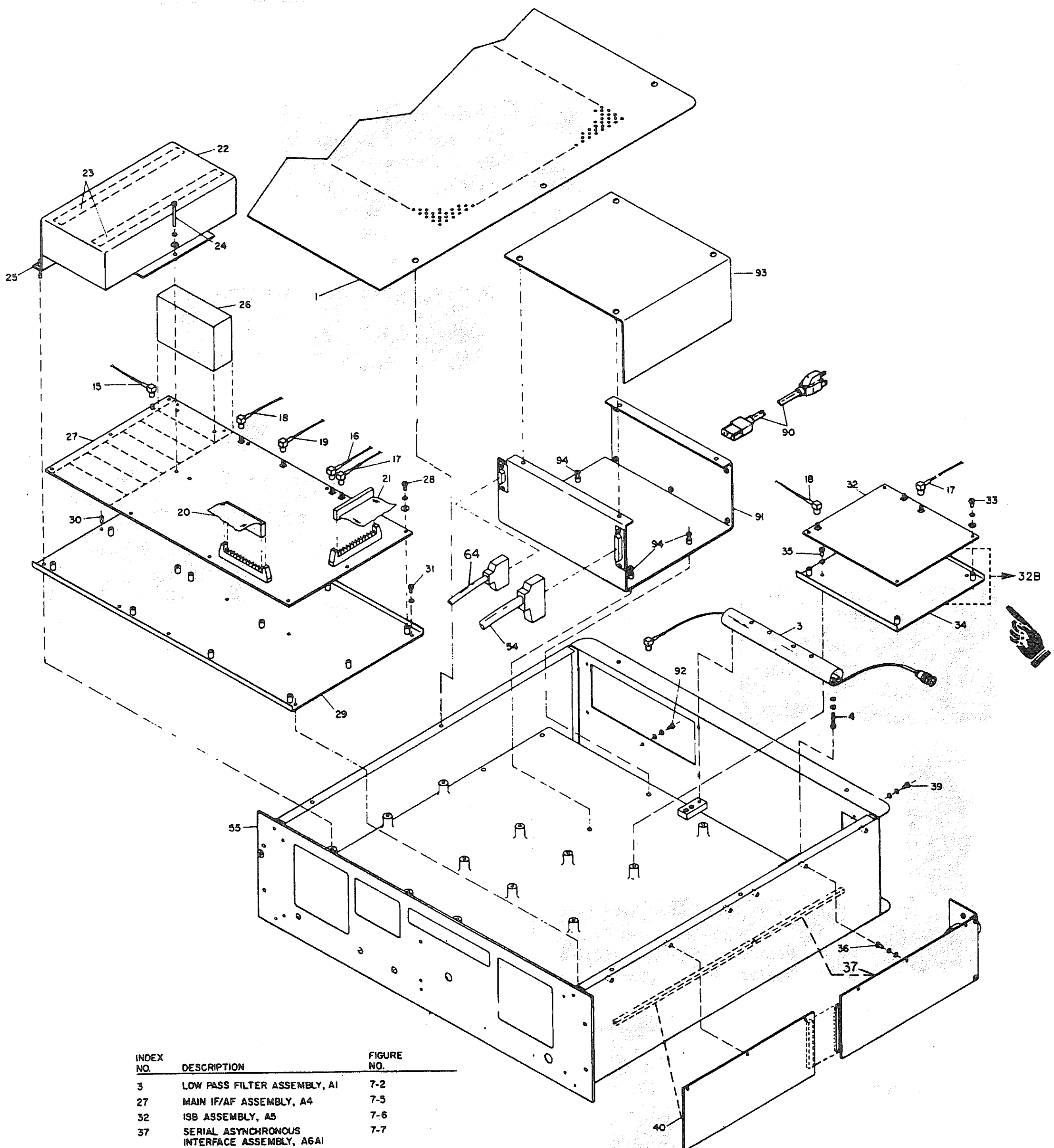


Figure 7-0. Finding Part Number, Illustrated Description



INDEX NO.	DESCRIPTION	FIGURE NO.
3	LOW PASS FILTER ASSEMBLY, A1	7-2
27	MAIN IF/AF ASSEMBLY, A4	7-5
32	ISB ASSEMBLY, A5	7-6
37	SERIAL ASYNCHRONOUS INTERFACE ASSEMBLY, A6A1	7-7
40	MICROCOMPUTER ASSEMBLY, A6A2	7-8
91	POWER SUPPLY ASSEMBLY, A10	7-12

F9312834

Figure 7-1. Receiver Assembly, Radio, R-2174(P)/URR (Sheet 1 of 5)

FIGURE 7-1. RECEIVER ASSEMBLY, RADIO R-2174(P)/URR

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-1	08450 R-2174(P) /URR	81349	R-2174(P)/URR RECEIVER ASSEMBLY, Radio......................	1		PAOFDS V
7-1A	08450-2 R-2174A (P)URR	81349	R-2174A(P)/URR RECEIVER ASSEMBLY, Radio......................	1	A	PAOFDS
/1-1	08521	23386	• COVER, Top...............	1		XBOZZN
/1-3	08385	23386	• LOW PASS FILTER ASSEMBLY, A1 (Figure 7-2)..................	1		PAFLDT
/1-4	MS35233-18	96906	• Screw, Machine, Pan Head, 4-40 x 3-4 (AP)..	2		PAOZZN
	MS35338-78	81349	• WASHER, Splt Lock, No. 4 (AP)................	2		PAOZZN
	MS15795-303	96906	• WASHER, Flat, No. 4 (AP)..................	2		PAOZZN
	1488-4	83330	• LUG, Terminal No. 4 (AP)..................	1		PAFZZN
/1-15	08555-1	23386	• CABLE ASSEMBLY, W1, Coax..................	1		MOOZZN
/1-16	08555-5	23386	• CABLE ASSEMBLY, W6, Coax..................	1		MOOZZN
/1-17	08555-6	23386	• CABLE ASSEMBLY, W10, Coax...................	1		MOOZZN
/1-18	08555-7	23386	• CABLE ASSEMBLY, W11, Coax..................	1		MOOZZN
/1-19	08556-2	23386	• CABLE ASSEMBLY, W12, Coax..................	1		MOOZZN
/1-20	08563	23386	• CABLE ASSEMBLY, W15, Cntrol................	1		MOOZZN
/1-21	08568	23386	• CABLE ASSEMBLY, W16, AF.OUT................	1		MOOZZN
/1-22	08496	23386	• BRACKET, Filter Retaining.............	1		XBOZZN
/1-23	08580	23386	• PAD, Tension.........	2		XA
/1-24	MS35233-12	96906	• SCREW, Machine, Pan Head 6-32 x 1-1/18 (AP).................	1		PAOZZN
	MS35338-79	81349	• WASHER, Splt Lock, No 6 (AP)................	1		PAOZZN
	MS15795-305	81349	• WASHER, Flat, No. 6 (AP)..................	1		PAOZZN
/1-25	MS35233-27	96906	• SCREW, Machine, Pan Head, 6-32 x 5/16 (AP)..................	2		PAOZZN
	MS35338-79	81349	• WASHER, Splt Lock, No. 6 (AP)............	2		PAOZZN
	MS15795-305	81349	• WASHER, Flat, No. (AP)...	2		PAOZZN
/1-26	08406	00136	• FILTER, XTAL, bandpass 0.4 kHz (QCU) Filter No. 1.................	1		PAOZZN

FIGURE 7-1. RECEIVER ASSEMBLY, RADIO R-2174(P)/URR (Cont)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-1 /1-26	08406-10	00136	• FILTER, XTAL, bandpass 0.4 kHz (QCU) Filter No. 1..................	1		PAOZZN
	08407	00136	• FILTER, XTAL, bandpass 1.4 kHz (QCU) Filter No. 2..................	1		PAOZZN
	08407-10	00136	• FILTER, XTAL, bandpass 1.4 kHz (QCU) Filter No. 2..................	1		PAOZZN
	08408	00136	• FILTER, XTAL, bandpass 6.8 kHz (QCU) Filter No. 3..................	1		PAOZZN
	08408-10	00136	• FILTER, XTAL, bandpass 6.8 kHz (QCU) Filter No. 3..................	1		PAOZZN
	08409	00136	• FILTER, XTAL, bandpass 3.2 kHz (QCU) Filter No. 4..................	1		PAOZZN
	08409-10	00136	• FILTER, XTAL, bandpass 3.2 kHz (QCU) Filter No. 4..................	1		PAOZZN
	08410	00136	• FILTER, XTAL, bandpass 3.2 kHz (QCU) Filter No. 5..................	1		PAOZZN
	08410-10	00136	• FILTER, XTAL, bandpass 3.2 kHz (QCU) Filter No. 5..................	1		PAOZZN
	08411	00136	• FILTER, XTAL, bandpass 0.4 kHz (QCU) Filter No. 6..................	1		PAOZZN
	08411-10	00136	• FILTER, XTAL, bandpass 0.4 kHz (QCU) Filter No. 6..................	1		PAOZZN
	08412	00136	• FILTER, XTAL, bandpass 1.2 kHz (QCU) Filter No. 7..................	1		PAOZZN
	08412-10	00136	• FILTER, XTAL, bandpass 1.2 kHz (QCU) Filter No. 7..................	1		PAOZZN
	08413	00136	• FILTER, XTAL, bandpass 3.2 kHz (QCU) Filter No. 8..................	1		PAOZZN
	08413-10	00136	• FILTER, XTAL, bandpass 3.2 kHz (QCU) Filter No. 8..................	1		PAOZZN
	08414	00136	• FILTER, XTAL, bandpass 6.8 kHz (QCU) Filter No. 9..................	1		PAOZZN
	08414-10	00136	• FILTER, XTAL, bandpass 6.8 kHz (QCU) Filter No. 9..................	1		PAOZZN

FIGURE 7-1. RECEIVER ASSEMBLY. RADIO R-2174(P)/URR (Cont)

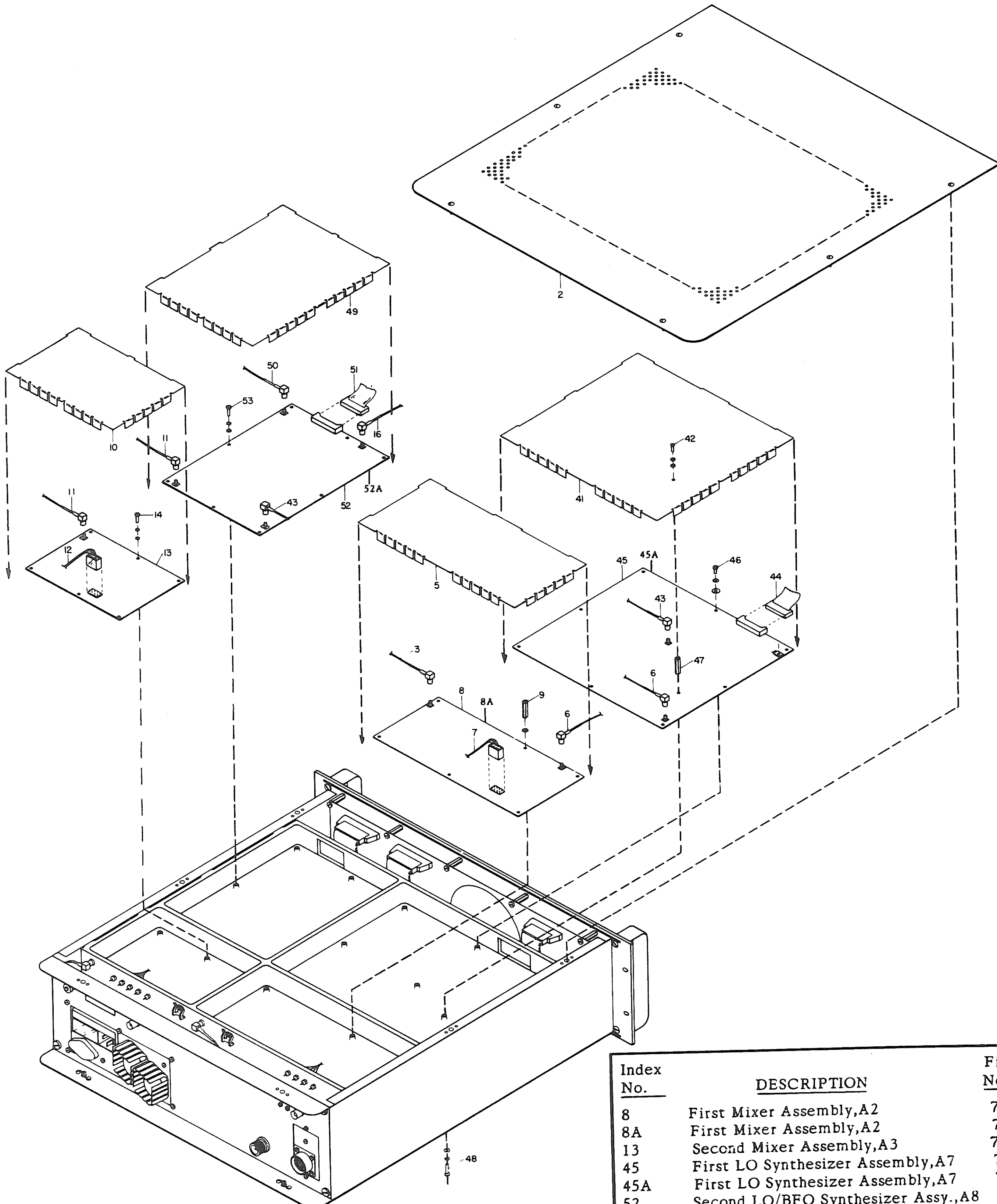
FIGURE & INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-1						
/1-26	08415	00136	. FILTER, XTAL, bandpass 16 kHz (QCU) .... Filter No. 10	1		PAOZZN
	08415-10	00136	. FILTER, XTAL, bandpass 16 kHz (QCU) .... Filter No. 10	1		PAOZZN
	08416	00136	. FILTER, XTAL, bandpass 0.5 kHz (QCU) .... Filter No. 11	1		PAOZZN
	08416-10	00136	. FILTER, XTAL, bandpass 0.5 kHz (QCU) .... Filter No. 11	1		PAOZZN
	08417	00136	. FILTER, XTAL, bandpass 1.0 kHz (QCU) .... Filter No. 12	1		PAOZZN
	08417-10	00136	. FILTER, XTAL, bandpass 1.0 kHz (QCU) .... Filter No. 12	1		PAOZZN
	08418	00136	. FILTER, XTAL, bandpass 2.0 kHz (QCU) .... Filter No. 13	1		PAOZZN
	08418-10	00136	. FILTER, XTAL, bandpass 2.0 kHz (QCU) .... Filter No. 13	1		PAOZZN
	08419	00136	. FILTER, XTAL, bandpass 3.0 kHz (QCU) .... Filter No. 14	1		PAOZZN
	08419-10	00136	. FILTER, XTAL, bandpass 3.0 kHz (QCU) .... Filter No. 14	1		PAOZZN
	08420	00136	. FILTER, XTAL, bandpass 6.0 kHz (QCU) .... Filter No. 15	1		PAOZZN
	08420-10	00136	. FILTER, XTAL, bandpass 6.0 kHz (QCU) .... Filter No. 15	1		PAOZZN
/1-27	08465	23386	. MAIN IF/AF ASSEMBLY Circuit Card. A4....... (Figure 7-5)	1		PAOLDT
/1-28	MS35233-14	96906	. SCREW, Machine, Pan Head, 4-40 x 5/16 ..... (AP)	12		PAOZZN
	MS35338-78	81349	. WASHER, Split Lock, No. 4 (AP)	12		PAOZZN
	MS15795-303	96906	. WASHER, Flat, No. 4 (AP)	12		XBOZZN
/1-29	08497	23386	. PLATE, Base, IF, A4	1		XBOZZN
/1-30	MS35249-35	96906	. SCREW, Machine, Flat Head 6-32 x 3/8 .... (AP)	1		PAOZZN

FIGURE 7-1. RECEIVER ASSEMBLY. RADIO R-2174(P)/USS

FIGURE & INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-1						
/1-31	MS35233-27	96906	. SCREW, Machine, Pan Head 6-32 x 5/16 (AP)	10		PAOZZN
	MS35338	81349	. WASHER, Split Lock, No. 6 (AP)	10		PAOZZN
/1-32	08390	23386	. ISB ASSEMBLY, Circuit Card A5 (Optional) (Figure 7-6)	1		PAOLDT
/1-32B	08390-2	23386	. ISB ASSEMBLY, Circuit Card A5 with Mounting Plate and Cable.	1		PAOLDT
/1-33	MS35233-14	96906	. SCREW, Machine, Pan Head, 4-40 x 5/16 (AP)	4		PAOZZN
	MS35338-78	81349	. WASHER, Split Lock, No. 4 (AP)	4		PAOZZN
	MS15795-303	96906	. WASHER, Flat, No. 4 (AP)	4		PAOZZN
/1-34	08564	23386	. BASE, Plate, ISB, A5, Mounting	1		XBFZZN
/1-35	MS35233-27	96906	. SCREW, Machine, Pan Head, 6-32 x 5/16 (AP)	4		PAOZZN
	MS35338-79	81349	. WASHER, Split Lock No. 6 (AP)	4		PAOZZN
/1-36	MS35233-14	96906	. SCREW, Machine, Pan Head, 4-40 x 5/16 (AP)	8		PAOZZN
	MS35338-78	81349	. WASHER, Split Lock, No. 4 (AP)	8		PAOZZN
	MS15795-303	96906	. WASHER, Flat No. 4 (AP)	8		PAOZZN
/1-37	08391	23386	. SERIAL ASYNCHRONOUS INTERFACE ASSEMBLY, Circuit Card, A6A1 (Optional) (Figure 7-7)	1		PAFLDT
/1-39	MS35233-14	96906	. SCREW, Machine, Pan Head, 4-40 x 5/16 (AP)	2		PAOZZN
	MS35338-78	81349	. WASHER, Split Lock, No. 4 (AP)	2		PAOZZN
	MS15795-303	96906	. WASHER, Flat No. 4 (AP)	1		PAOZZN
/1-40	08392	96906	. . MICROCOMPUTER ASSEMBLY, Circuit Card A6A2 (Figure 7-8)	1		PAOLDT

FIGURE 7-1. RECEIVER ASSEMBLY RADIO R-2174 (P)/URR (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-1						
/1-54	08569	23386	• CABLE ASSEMBLY, ... W19, DC Power	1		MOOZZN
/1-55	08454	23386	• PANEL, Front	1		XBOZZN
/1-64	08570	23386	• CABLE ASSEMBLY, W20, ... AC line switching	1		MOOZZN
/1-90	17250	16428	• CABLE ASSEMBLY, W18, ... AC line in	1		MOOZZN
/1-91	08389	23386	• POWER SUPPLY ASSEMBLY, ... Module, A10 (Figure 7-12)	1		PAOODT
/1-92	MS35233-28	96906	• SCREW, Machine, Pan Head, ... 6-23 x 3/8 (AP)	5		PAOZZN
	MS35338-79	81349	• WASHER, Split Lock, No. 6 (AP). . . .	5		PAOZZN
	MS15795-305	81349	• WASHER, Flat, No. 6 (AP)	5		PAOZZN
/1-93	08518	23386	• • COVER, Power Supply. . . . . (Reference Figure 7-12)	1		XB
/1-94	4459-M07-F09	04729	• • SCREW, Machine, Pan Head, ... 8-32 (Captive) (AP)	4		PAOZZN
	MS35338-80	81349	• • WASHER, Split Lock, No. 8 . . . . . (AP)	4		PAOZZN



Index No.	DESCRIPTION	Figure No.
8	First Mixer Assembly,A2	7-3
8A	First Mixer Assembly,A2	7-3
13	Second Mixer Assembly,A3	7-4
45	First LO Synthesizer Assembly,A7	7-9
45A	First LO Synthesizer Assembly,A7	7-9
52	Second LO/BFO Synthesizer Assy.,A8	7-10
52A	Second LO/BFO Synthesizer Assy.,A8	7-10

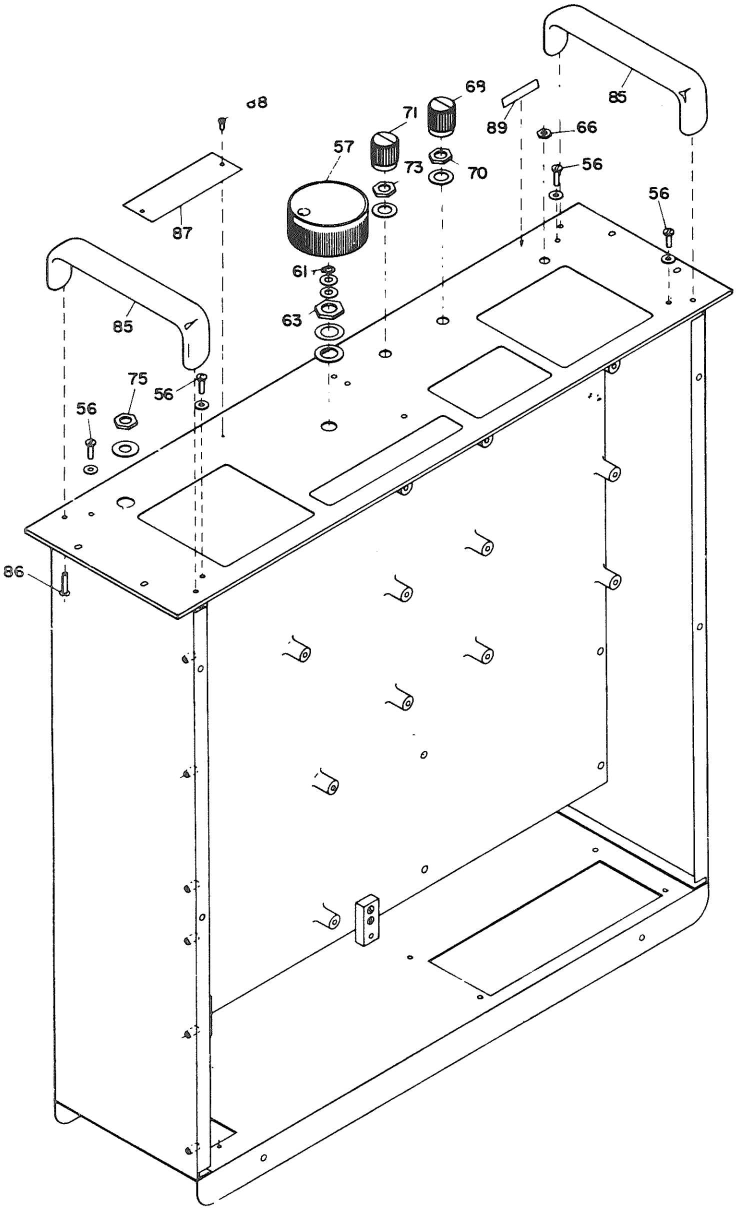
Figure 7-1. Receiver Assembly, Radio, R-2174(P)/URR (Sheet 2 of 5)

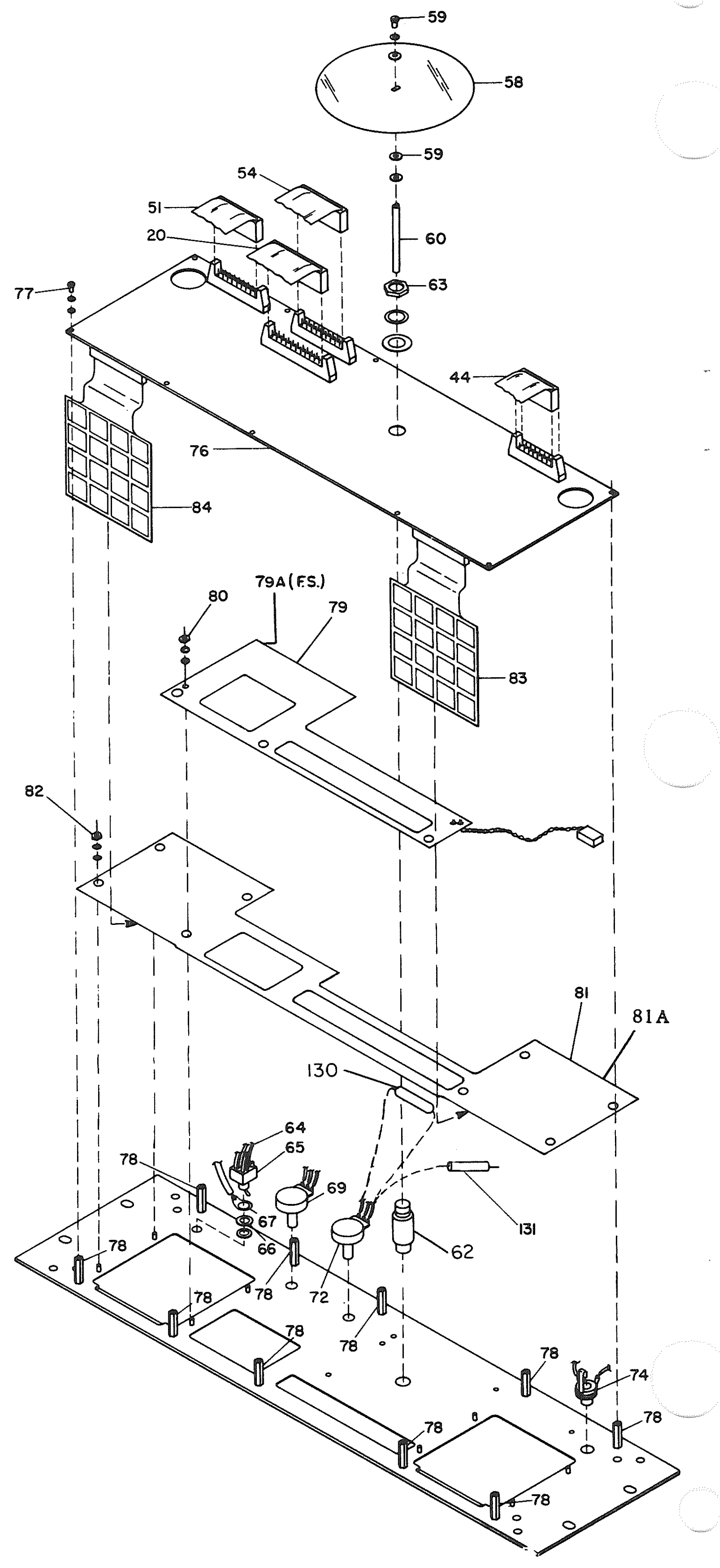
FIGURE 7-1. RECEIVER ASSEMBLY, RADIO R-2174(P)/URR(Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-1						
/2-2	08521	23386	• COVER, Bottom............	1		XBOZZN
/2-5	09108	23386	• COVER, Shield, A2........	1		XBOZZN
/2-6	08555-2	23386	• CABLE ASSEMBLY, W2, Coax.	1		MOOZZN
/2-7	08561	23386	• CABLE ASSEMBLY, W21,..... DC Supply, A2	1		MOOZZN
/2-8	08386	23386	• FIRST MIXER ASSEMBLY..... Circuit Card, A2, (Figure 7-3)	1		PAOLDT
/2-8A	09635	23386	• FIRST MIXER ASSEMBLY..... Circuit Card, A2, (Figure 7-3)	1	A	PAOLDT
/2-9	09097	23386	• STANDOFF, Spacer Retaining(AP)............	6		PAOZZN
	5804-17-1	86928	• WASHER, Spring, No.4(AP)	6		PAOZZN
/2-10	08666	23386	• COVER, Shield, A3........	1		XBOZZN
/2-11	08555-4	23386	• CABLE ASSEMBLY, W4, Coax	1		MOOZZN
/2-12	08560	23386	• CABLE ASSEMBLY, W22...... DC Supply, A3	1		MOOZZN
/2-13	08191	23386	• SECOND MIXER ASSEMBLY.... Circuit Card, A3, (Figure 7-4)	1		PAOLDT
/2-14	MS35233-14	96906	• SCREW,Machine,Pan Head,.. 4-40 x 5/16(AP)	6		PAOZZN
	MS35338-78	81349	• WASHER,Splt Lock,No.4(AP)	6		PAOZZN
	MS15795-303	96906	• WASHER, Flat, No.4(AP)...	6		PAOZZN
/2-41	08667	23386	• COVER, Shield, A7........	1		XBOZZN
/2-42	MS35233-3	96906	• SCREW, Machine, Pan Head, 2-56 x 1/4(AP)	1		PAOZZN
	MS35338-77	81349	• WASHER,Splt Lock,No.2(AP)	1		PAOZZN
	MS35233-22	96906	• WASHER, Flat, No.2(AP)...	1		PAOZZN
/2-43	08555-3	23386	• CABLE ASSEMBLY, W3, Coax.	1		MOOZZN
/2-44	08376	23386	• CABLE ASSEMBLY, W13...... Control	1		MOOZZN
/2-45	08361	23386	• FIRST LO SYNTHESIZER..... ASSEMBLY, Circuit Card A7 (Figure 7-9)	1		PAOLDT
/2-45a	09134	23386	• FIRST LO SYNTHESIZER..... ASSEMBLY, Circuit Card A7 (Figure 7-9)	1	A	PAOLDT
/2-46	MS35233-14	96909	• SCREW, Machine, Pan Head, 4-40 x 5/16(AP)	12		PAOZZN
	MS35338-78	81349	• WASHER,Splt Lock,No.4(AP)	12		PAOZZN
	MS15795-303	96906	• WASHER, Flat, No.4(AP)...	12		PAOZZN
/2-47	08648	23386	• STANDOFF, Insulated......	1		PAOZZN
/2-48	MS35233-8	96906	• SCREW, Machine, Pan Head, 4-40 x 11/16(AP)	1		PAOZZN
	MS35338-78	81349	• WASHER,Splt Lock,No.4(AP)	2		PAOZZN
	MS15795-303	96906	• WASHER, Flat, No.4(AP)...	2		PAOZZN
/2-49	08668	23386	• COVER, Shield, A8........	1		XBOZZN
/2-50	08556-1	23386	• CABLE ASSEMBLY, W7, Coax.	1		MOOZZN

FIGURE 7-1. RECEIVER ASSEMBLY, RADIO R-2174(P)/URR(Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-1						
/2-51	08558	23386	• CABLE ASSEMBLY,W14,Cntrol	1		MOOZZN
/2-52	08387	23386	• SECOND LO/BFO SYNTHESIZER ASSEMBLY, Circuit Card A8 (Figure 7-10)	1		PAOLDT
/2-52 A	09632	23386	• Second LO/BFO SYNTHESIZER ASSEMBLY, Circuit Card A8 (Figure 7-10)	1	A	PAOLDT
/2-53	MS35233-14	96906	• SCREW, Machine, Pan Head, 4-40 x 5/16(AP)	8		PAOZZN
	MS35338-78	81349	• WASHER,Splt Lock,No.4(AP)	8		PAOZZN
	MS15795-303	96906	• WASHER, Flat No. 4(AP)	8		PAOZZN





Index No.	DESCRIPTION	Figure No.
76	Front Panel Interface Assembly	7-11
79	Circuit Card Assembly, LCD Lamp Board	7-13
79A	Circuit Card Assembly, LCD-LED Board	7-13
81	Diffuser	7-1
81A	Diffuser	7-1

Figure 7-1. Receiver Assembly, Radio, R-2174(P)/URR (Sheet 3 of 5)

FIGURE 7-1. RECEIVER ASSEMBLY RADIO R-2174(P)/URR (Cont)

FIGURE & INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-1						
/3-20	08563	23386	. CABLE ASSEMBLY, W15, Control	1		MOOZZN
/3-44	08376	23386	. CABLE ASSEMBLY, W13, Control	1		MOOZZN
/3-51	08558	23386	. CABLE ASSEMBLY, W14, Control	1		MOOZZN
/3-54	08569	23386	. CABLE ASSEMBLY, W19, DC Power	1		MOOZZN
/3-56	MS35234-63	96906	. SCREW, Machine, Pan Head, 10-32 x 1/2 (AP)	4		PAOZZN
	5610-280-031	86928	. WASHER, Nylon 0.200 inches I.D.(AP)	4		PAOZZN
/3-57	08557	23386	. KNOB, Encoder, Modified	1		PAOZZN
/3-58	08538	23386	. DISK, Encoder	1		PAFZZN
/3-59	MS35233-27	96906	. SCREW, Machine, Pan Head, 6-32 x 5/16 (AP)	1		PAOZZN
	MS35338-79	81349	. WASHER, Split Lock, No. 6 (AP)	1		PAOZZN
	MS15795-305	81349	. WASHER, Split Lock, No. 6 (AP)	1		PAOZZN
	CYL-1400-250	08523	. WASHER, Spring (AP)	1		PAOZZN
	5710-54-25	86928	. WASHER, Flat (AP)	1		PAOZZN
/3-60	08553	23386	. SHAFT, Encoder	1		XBOZZN
/3-61	3100-25	27440	. RING, Retainer, Shaft, Encoder (AP)	1		PAOZZN
	5710-54-25	86928	. WASHER, Flat (AP)	1		PAOZZN
	5720-21	86928	. WASHER, Shim, 1/4 inch	AR		PAFZZN
/3-62	08554	23386	. BUSHING, Spacer, Encoder	1		XBOZZN
/3-63	76050-NP	73734	. NUT, HEX 1/2 X 20 X 1/8 inch thick (AP)	2		PAOZZN
	5806-28-1	86928	. WASHER, Spring (AP)	2		PAOZZN
	5710-94-015	86928	. WASHER, Flat (AP)	2		PAOZZN
	5610-84-032	86928	. WASHER, Nylon (AP)	1		PAOZZN
/3-64	08570	23386	. CABLE ASSEMBLY, W20, AC Line Switching	1		MOOZZN
/3-65	JMT-223G	55459	. . SWITCH, S1, Miniature DPDT	1		PAOZZN
/3-66			. . NUT, HEX, 1/4 X 24 (AP)	1		
/3-67			. . LUG, Solder, 1/4 inch I.D.	1		
/3-68	MS91528-1D2B	86797	. KNOB, Potentionmeter, R23	1		PAOZZN
/3-69	08552	23386	. . POTENTIONMETER, IF Gain R23, 50K ohms	1		PAFZZN
/3-70	9002-NP	73734	. NUT, 3/8 X 32 (AP)	1		PAOZZN
	30-350	73734	. WASHER, Internal Tooth, 3/8 (AP)	1		PAOZZN
/3-71	MS91528-1D2B	86797	. KNOB, Potentionmeter, R22	1		PAOZZN
/3-72	08551	23386	. POTENTIONMETER, AF Gain R22, 25K ohms	1		PAFZZN
/3-73	9002-NP	73734	. NUT, 3/8 X 32 (AP)	1		PAOZZN
	30-350	73734	. WASHER, Internal Tooth, 3/8 (AP)	1		PAOZZN

FIGURE 7-1. RECEIVER ASSEMBLY, RADIO R-2174(P)/URR(Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-1						
/3-74	JJ-034	81349	• CONNECTOR, Phone Jack, J4	1		PAFZZN
/3-75			• NUT, Hex, 3/8 x 32(AP)...	1		PAOZZN
			• WASHER, Internal Tooth,.. 3/8(AP)	1		PAOZZN
/3-76		23386	• FRONT PANEL INTERFACE.... ASSEMBLY, Circuit Card, A9 (Figure 7-11)	1		PAFLDT
/3-77	MS35233-14	96906	• SCREW, Machine, Pan Head, 4-40 x 5/16(AP)	10		PAOZZN
	MS35338-78	81349	• WASHER,Splt Lock,No.4(AP)	10		PAOZZN
	MS15795-303	96906	• WASHER, Flat, No.4(AP)...	10		PAOZZN
/3-78	8109-A-0440	96906	• STANDOFF, Amaton.........	10		PAOZZN
/3-79	08946	23386	• CIRCUIT CARD ASSEMBLY,... LCD Lamp Board (Fig. 7-13)	1		XBOZZN
/3-79A	09501	23386	• CIRCUIT CARD ASSEMBLY,... LCD-LED Board (Figure 7-13.1)	1	A	XBOZZN
/3-80	MS35649-44	81349	• NUT, Hex, 4-40(AP).......	3		PAOZZN
	MS35338-78	81349	• WASHER,Splt Lock,No.4(AP)	3		PAOZZN
	MS15795-303	96906	• WASHER, Flat, No.4(AP)...	3		PAOZZN
/3-81	08944	23386	• LIGHT DIFFUSER...........	1		XBOZZN
/3-81A	09500	23386	• LIGHT DIFFUSER...........	1	A	XBOZZN
/3-82	MS35649-44	81349	• NUT, Hex, 4-40(AP).......	5		PAOZZN
	MS35338-78	81349	• WASHER,Splt Lock,No.4(AP)	5		PAOZZN
	MS15795-303	96906	• WASHER, Flat, No.4(AP)...	5		PAOZZN
/3-83	09078	23386	• SWITCH, S3, Keyboard..... Frequency	1		PAFZZN
/3-84	08498-2	23386	• SWITCH, S4, Keyboard, Mode.....................	1		PAFZZN
/3-85	27VX-10-B07A -5B	28198	• HANDLE, Front Panel......	2		XBOZZN
/3-86	MS35250-72	96906	• SCREW,Machine,Flat Head.. 10-32(AP)	2		PAOZZN
/3-87	08675	23386	• PLATE, Identification....	1		XBOZZN
/3-88	MS24641-1	96906	• SCREW, Self tapping, No.2 x 1/8(AP)	2		PAOZZN
/3-89	05000-2*	23386	• LOGO, Decal, RACAL.......	1		XBOZZN
/3-130	812M112X7R0103M	23386	• CAPACITOR, C10, Ceramic.. 0.01 uf, 50WVDC, $\pm$20%	1		PADZZN
/3-131	MS90539-15	96906	• COIL, L1, 1000 uh........	1		PADZZN

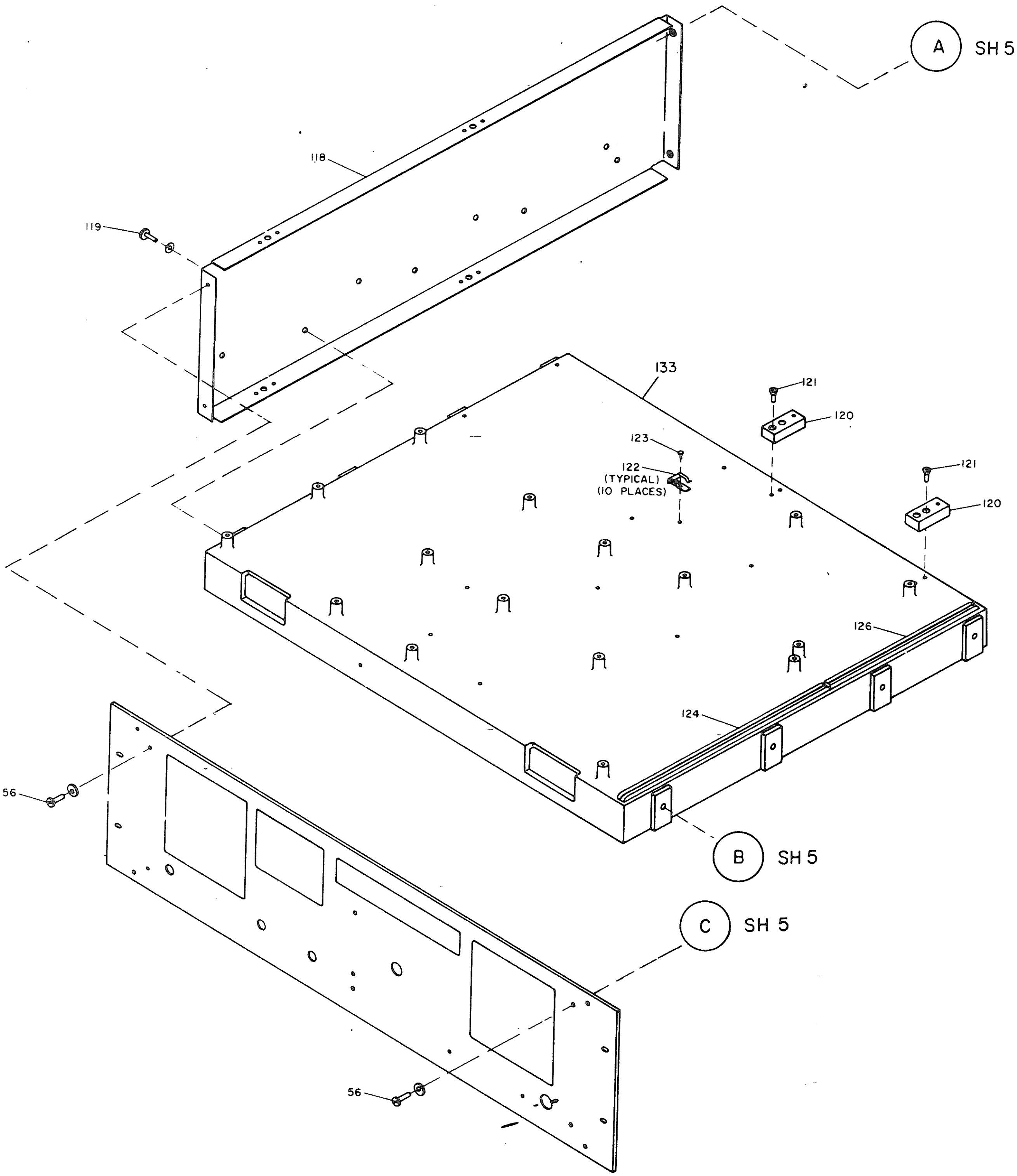


Figure 7-1. Receiver Assembly, Radio, R-2174(P)/URR (Sheet 4 of 5)

FIGURE 7-1. RECEIVER ASSEMBLY RADIO R-2174 (P)/URR (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-1						
/4-56	MS35234-63	96906	• SCREW, Machine, Pan Head, ... 10-32 x 1/2 (AP)	4		PAOZZN
	5610-280-031	86928	• WASHER, Nylon, ... 0.200 inches I.D. (AP)	4		PAOZZN
/4-118	08469	23386	• GUSSET, Left	1		XBOZZN
/4-119	MS35233-43	96906	• SCREW, Machine, Pan Head . . . . 8-32 x 3/8 (AP)	4		PAOZZN
	5806-10-1	86928	• WASHER, Spring, No. 8 (AP)	4		PAOZZN
/4-120	08656	23386	• BLOCK, Filter Al, Mounting	2		MFOZZN
/4-121	MS51958-14	96906	• SCREW, Machine, Flat Head,. . . . . . . 6-32 x 1/2 (AP)	2		PAOZZN
/4-122	FCS-10	95987	• CLAMP, Cable	10		PAOZZN
/4-123	MS35249-20	96906	• SCREW, Machine, Flat Head,. . . . . . . 4-40 x 1/4 (AP)	1		PAOZZN
/4-124	GV-7000	07556	• SLIDE, Circuit Card.	1		XBOZZN
/4-126	08562	23386	• SLIDE, Circuit Card, Modified.	1		MOOZZN
/4-133	08467	23386	• CHASSIS, Receiver	1		XA

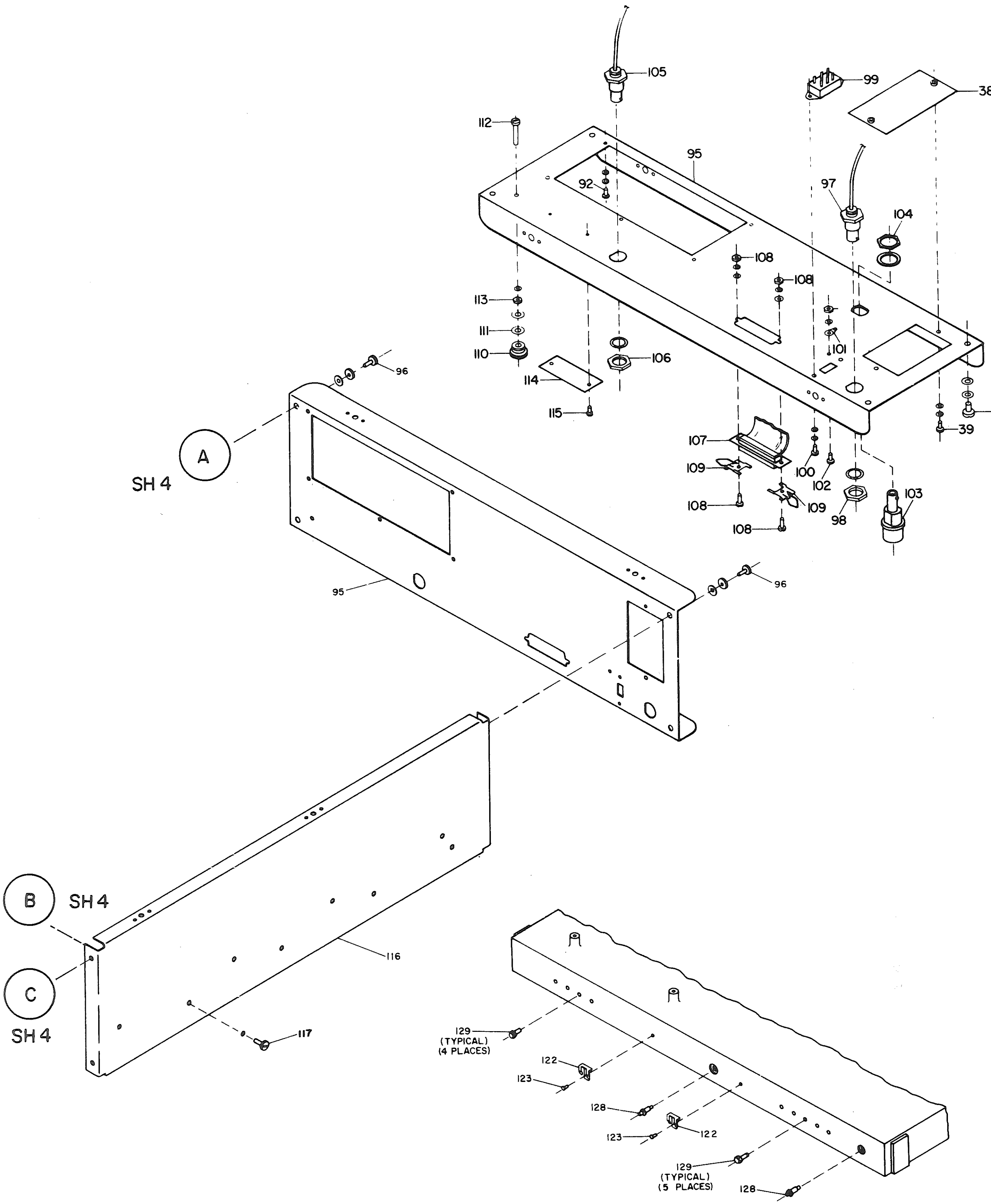


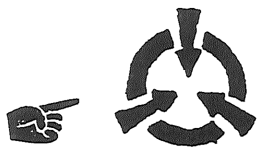
Figure 7-1. Receiver Assembly, Radio, R-2174(P)/URR (Sheet 5 of 5)

FIGURE 7-1. RECEIVER ASSEMBLY RADIO R-2174 (P)/URR (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-1						
/5-38	08492	23386	• PLATE, Blanking, for A6A1 .... Position	1		XBOZZN
/5-39	MS35233-14	96906	• SCREW, Machine, Pan Head,....... 4-40 x 5/16 (AP)	2		PAOZZN
/5-92	MS35233-28	96906	• SCREW, Machine, Pan Head,....... 6-32 x 3/8 (AP)	5		PAOZZN
	MS35338-79	81349	• WASHER, Split Lock, No. 6 (AP)....	5		PAOZZN
	MS 15795-305	81349	• WASHER, Flat, No. 6 (AP)........	5		PAOZZN
/5-95	08445	23386	• PANEL, Rear	1		XBOZZN
/5-96	MS35233-43	96906	• SCREW, Machine, Pan Head,....... 8-32 x 3/8 (AP)	4		PAOZZN
	MS35338-80	81349	• WASHER, Split Lock, No. 8 (AP)....	4		PAOZZN
	MS15795-307	81349	• WASHER, Flat, No. 8 (AP)........	4		PAOZZN
/5-97	KC19-110	91836	• CONNECTOR, J7, BNC	1		PAOZZN
/5-98			• • NUT, (AP)	1		
			• • WASHER, (AP)	1		
/5-99	GF326	27193	• SWITCH, Internal/External, ... S2, Slide, DPDT	1		PAFZZN
/5-100	MS35233-14	96906	• SCREW, Machine, Pan Head,....... 4-40 x 5/16 (AP)	2		PAOZZN
	MS 35338-78	81349	• WASHER, Split Lock, No. 4 (AP)....	2		PAOZZN
	MS15795-303	96906	• WASHER, Flat No. 4 (AP)	2		PAOZZN
/5-101	1488-4	83330	• LUG, Solder, No. 4	1		PAFZZN
/5-102	MS35233-14	96906	• SCREW, Machine, Pan Head .... 4-40 x 5/16 (AP)	1		PAOZZN
	MS35649-44	81349	• NUT, Hex, 4-40 (AP)...........	1		PAOZZN
	MS35338-78	81349	• WASHER, Split Lock, No. 4 (AP)....	1		PAOZZN
/5-103	UG-606/U	81349	• CONNECTOR, J1, N-BNC	1		PAOZZN
/5-104			• • NUT, (AP)	1		
			• • WASHER, (AP)	1		
/5-105	KC19-110	91836	• CONNECTOR, J2, BNC .... Bulkhead	1		PAOZZN
/5-106			• • NUT, (AP)	1		
			• • WASHER, (AP)	1		
/5-107	3483-1000	75037	• CONNECTOR, J3, D .... Subminiature, 25 Pin	1		XA
/5-108	MS35233-14	96906	• SCREW, Machine, Pan Head,....... 4-40 x 5/16 (AP)	2		PAOZZN
	MS35649-44	81349	• NUT, Hex, 4-40, (AP)	2		PAOZZN
	MS35338-78	81349	• WASHER, Split Lock, No. 4 (AP)....	2		PAOZZN
	MS 15795-303	96906	• WASHER, Flat, No. 4 (AP)........	2		PAOZZN
/5-109	D110277	71468	• LATCH, Connector, J3...........	2		PAOZZN
/5-110	8072-NP	73743	• NUT, Ground Lug, ... Knurled, 10-32	1		PAFZZN
/5-111	MS15795	81349	• WASHER, Flat, No. 10...........	2		PAOZZN
/5-112	MS35234-65	96906	• SCREW, Ground Lug, Machine ..... Pan Head, 10-32 x 3/4	1		PAOZZN
/5-113	MS35650-104	81349	• NUT, Hex, 10-32 (AP)...........	1		PAOZZN
	MS35338-81	81349	• WASHER, Split Lock, No. 10 (AP)...	1		PAOZZN

FIGURE 7-1. RECEIVER ASSEMBLY RADIO R-2174 (P)/URR (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-1–						
/5-114	08676	23386	• PLATE, Serial Number.	1		XBOZZN
/5-115	MS24641-1	96906	• SCREW, Self tapping, No. 2 (AP)	2		PAOZZN
/5-116	08468	23386	• GUSSET, Right.	1		XBOZZN
/5-117	MS35233-43	96906	• SCREW, Machine, Pan Head, ... 8-32 x 3/8 (AP)	4		PAOZZN
	5806-10-1	86928	• WASHER, Spring, No. 8 (AP)	4		PAOZZN
/5-122	FCS-10	95987	• CLAMP, Cable	10		PAOZZN
/5-123	MS35249-20	96906	• SCREW, Machine, Flat Head,. . . . . . . 4-40 x 1/4 (AP)	1		PAOZZN
/5-128	051-075-0000	98291	• CONNECTOR, J5 and J6,. . . . . SMB-SMB	2		PAFZZN
/5-129	BSF-1BBGP102M	04222	• CAPACITOR, Feed thru, ... C1 thru C9, .001 uf ±20%	9		PADZZN



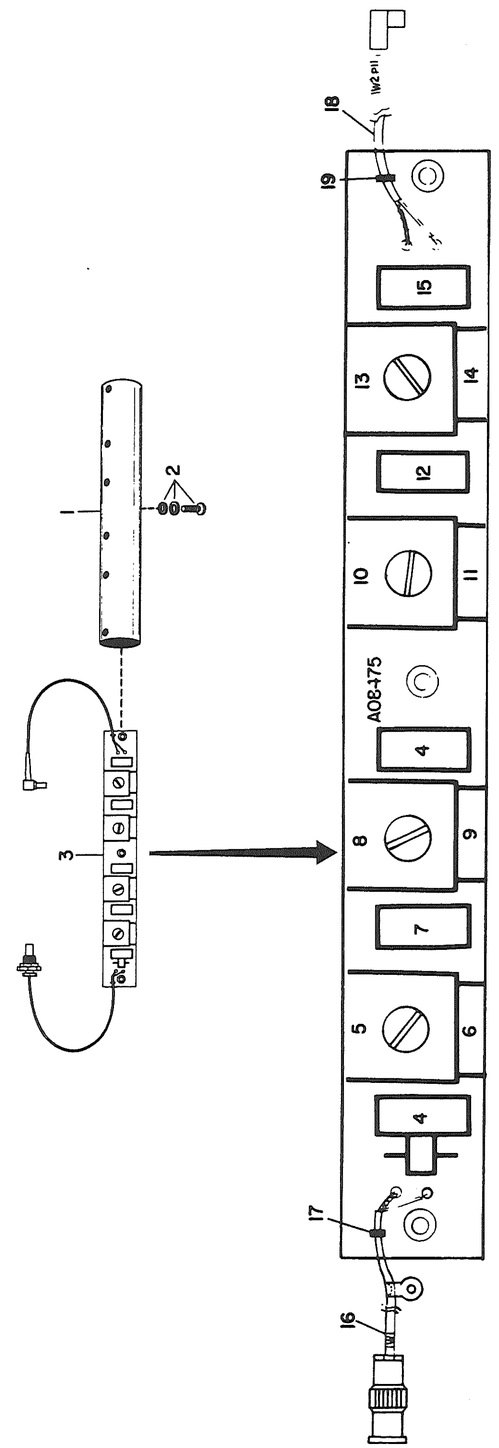
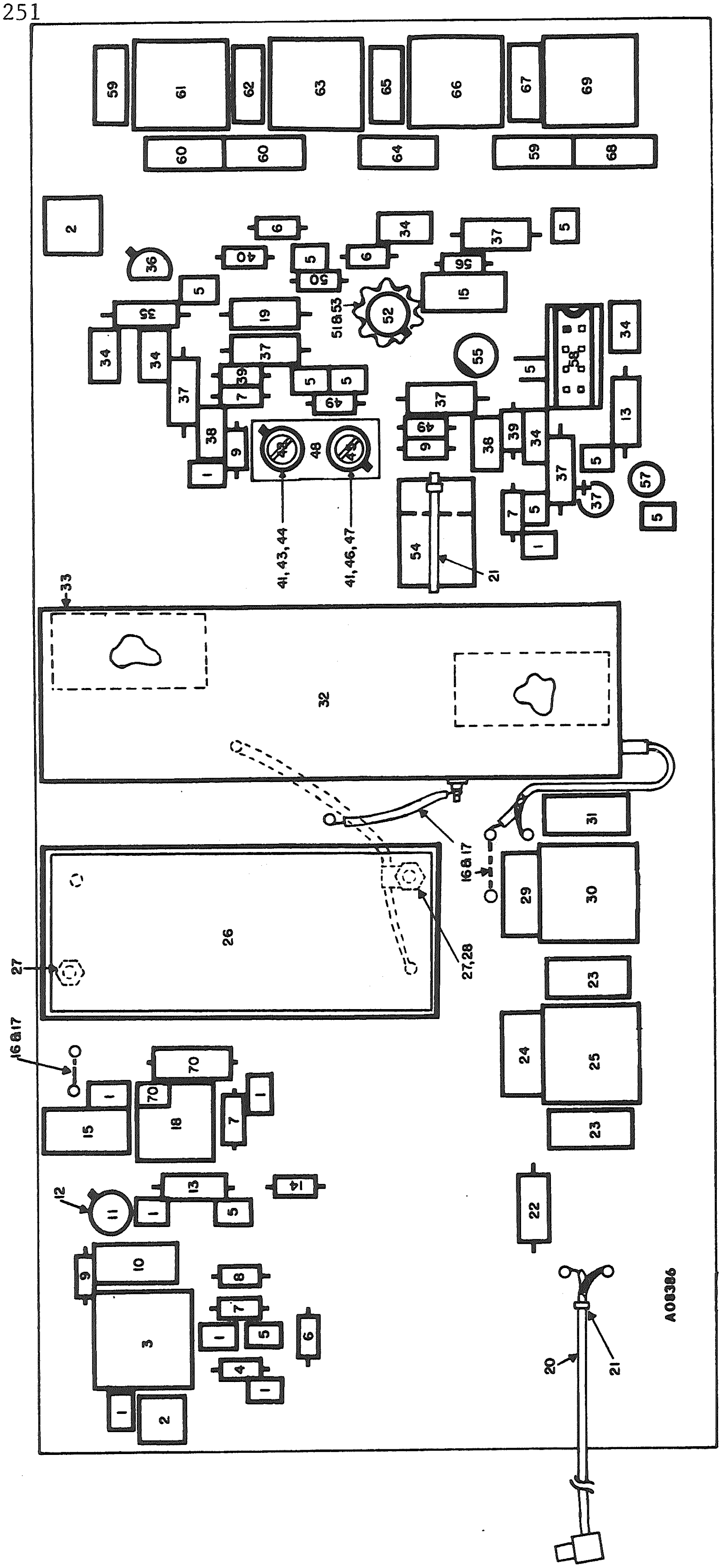


Figure 7-2. Low Pass Filter Assembly, Module, A1

FIGURE 7-2. LOW PASS FILTER ASSEMBLY, A1

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-2-	08385	23386	• LOW PASS FILTER . . . . ASSEMBLY, A1	1		PAFLDT
-1	08470	23386	• • CASE, Low Pass Filter Module . . .	1		XBOZZN
-2	MS35233-13	96906	• • SCREW, Machine, Pan Head, ... 4 - 40 x ¼ (AP)	1		PAOZZN
	MS35338-78	81349	• • WASHER, Split Lock,. . . . . No. 4 (AP)	1		PAOZZN
	MS35233-23	96906	• • WASHER, Flat, No. 4 (AP)	1		PAOZZN
-3	08475	23386	• • LOW PASS FILTER. . . . . ASSEMBLY, A1A1, Circuit Card	1		PADZZN
-4	CMR05F111G0DR	81349	• • • CAPACITOR, C1 and C5, ... Mica, 110 pf, 500 WVDC, ±2%	2		PADZZN
-5	08477-1	23386	• • • COIL, L1, RF Variable	1		PADZZN
-6	CMR05C100GODR	81349	• • • CAPACITOR, C2, Mica, ... 10 pf, 500 WVDC, ±5%	1		PADZZN
-7	CMR05F151GODR	81349	• • • CAPACITOR, C3, Mica, ... 150 pf, 500 WVDC, ±2%	1		PADZZN
-8	08477-2	23386	• • • COIL, L2, RF Variable	1		PADZZN
-9	CMR05E750G0DR	81349	• • • CAPACITOR, C4, Mica, ... 75 pf, 500 WVDC, ±5%	1		PADZZN
-10	08477-3	23386	• • • COIL, L3, RF Variable	1		PADZZN
-11	CMR05F910G0DR	81349	• • • CAPACITOR, C6, Mica, ... 91 pf, 500 WVDC, ±2%	1		PADZZN
-12	CMR05F121G0DR	81349	• • • CAPACITOR, C7, Mica, ... 120 pf, 500 WVDC, ±2%	1		PADZZN
-13	08477-4	23386	• • • COIL, L4, RF Variable	1		PADZZN
-14	CMR05E430G0DR	81349	• • • CAPACITOR, C8, Mica, ... 43 pf, 500 WVDC, ±2%	1		PADZZN
-15	CMR05E820G0DR	81349	• • • CAPACITOR, C9, Mica, ... 82 pf, 500 WVDC, ±2%	1		PADZZN
-16	08480	23386	• • • CABLE ASSEMBLY, W1.	1		MOOZZN
-17	MS18034-4	96906	• • • TYRAP, Cable.	1		PAOZZN
-18	08479-4	23386	• • • CABLE ASSEMBLY, W2.	1		MOOZZN
-19	MS18034-4	96906	• • • TYRAP, Cable.	1		PAOZZN



NOTE: Refer to Parts List for differences in the R-2174A Receiver.

Figure 7-3. First Mixer Assembly, Circuit Card, A2

FIGURE 7-3. FIRST MIXER ASSEMBLY, CIRCUIT CARD, A2

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-3	08386	23386	• FIRST MIXER ASSEMBLY,... Circuit Card, A2	1		PAOLDT
7-3	09635	23386	• FIRST MIXER ASSEMBLY,... Circuit Card, A2	1	A	PAOLDT
-1	CY15C102M	71590	• • CAPACITORS, C16,C19,.. C30,C32,C33,C35,C40, Ceramic, 0.001 uf, 18 WVDC, + 20%	7		PADZZN
-2	051-351-0000-220	98291	• • CONNECTOR, J1,J3,SMB..	2		PAOZZN
-3	08503	23386	• • TRANSFORMER, T3,...... RF Variable	1		PADZZN
-4	KS8379	04713	• • DIODE, CR3, Pin.......	1		PADZZN
-5	C320C103M1U1C1	31433	• • CAPACITOR,C10,C13,C14, C21,C22,C29,C34,C36,C37, C39,and C42,Ceramic,0.01 uf, 50 WVDC, + 20%	11		PADZZN
-6	RL07S102G	81349	• • RESISTOR,R1,R5,andR17, Fixed Film, 1K ohms, + 2%, 1/4 Watt	3		PADZZN
-7	RL07S221G	81349	• • RESISTOR,R7,R11,R14,.. and R15, Fixed Film,220 ohms, + 2%, 1/4 Watt	4		PADZZN
-8	RL07S103G	81349	• • RESISTOR, R19, Fixed.. film, 10K ohms, + 2%, 1/4 Watt	1		PADZZN
-9	RLR07C100GR	81349	• • RESISTOR, R12, R13 and R16, Fixed Film,10 ohms, + 2%, 1/4 Watt	3		PADZZN
-10	CMR05E330GODR	81349	• • CAPACITOR,C31,Mica,33. pf, 500 WVDC, + 2%	1		PADZZN
-11	U310	17896	• • TRANSISTOR, Q5, Field. Effect	1		PADZZN
-12	7717-HWHT	13103	• • PAD, Transistor, Q5...	1		PADZZN
-13	LT10K133	81349	• • CHOKE,L13 and L14, RF, 15 uH, + 10%	2		PADZZN
-14	RL07S101G	81349	• • RESISTOR, R18, Fixed.. Film, 100 ohm, + 2% 1/4 Watt	1		PADZZN
-15	CMR05E270GODR	81349	• • CAPACITOR,C44,Mica.... 27 pf, + 2%	1		PADZZN
-16	MIL-W-3861/S-24	81349	• • WIRE, Link 1 and Link. 2, Buss No. 24	AR		PAOZZN
-17	MIL-I-22129C-24	81349	• • SLEEVING, PTFE Tubing. No. 24	AR		PAOZZN
-18			• • Not Used..............			PADZZN
-19	LT4K085	81349	• • CHOKE, L6, RF, 2.2 uH. + 10%	1		PADZZN
-20	08479-1	23386	• • CABLE ASSEMBLY, W1,Coax	1		MOOZZN
-21	MS3367-4-0	96906	• • TYRAP, Cable, W1......	1		PADZZN
-22	LT10K196	81349	• • CHOKE, L15, RF,0.27 uH	1		PADZZN
-23	CMR05F101GODR	81349	• • CAPACITOR, C23 and C25 Mica, 100 pf, 500 WVDC, + 2%	2		PADZZN

FIGURE 7-3. FIRST MIXER ASSEMBLY, CIRCUIT CARD, A2(Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-3						
-24	CMR05F910GODR	81349	• • CAPACITOR, C24, Mica,.. 91 pf, 500 WVDC, ± 2%	1		PADZZN
-25	08477-2	23386	• • COIL ASSEMBLY,L11,RF,.. Variable	1		PADZZN
-25a	08477-6	23386	• • COIL ASSEMBLY,L11,RF,.. Variable	1	A	PADZZN
-26	08404	23386	• • FILTER, FL1, 40.455.MHz	1		PADZZN
-27	MS35649-44	81349	• • NUT, Hex, 4-40(AP).....	2		PAOZZN
	MS35338-78	81349	• • WASHER,Splt Lock,No.4.. (AP)	2		PAOZZN
	MS15795-303	96906	• • WASHER, Flat, No.4(AP).	1		PAOZZN
-28	1488-4	83330	• • LUG, cable, No. 4......	1		PAOZZN
-29	CMR05E430GODR	81349	• • CAPACITOR,C26,Mica,43.. pf 500 WVDC, ± 2%	1		PADZZN
-30	08477-5	23386	• • COIL ASSEMBLY, L12, RF. Variable	1		PADZZN
-30a	08477-7	23386	• • COIL ASSEMBLY, L12, RF. Variable	1	A	PADZZN
-31	CMR05E680GODR	81349	• • CAPACITOR,C27,Mica,68.. pf 500 WVDC, ± 2%	1		PADZZN
-32	08504	23386	• • MIXER BOX ASSEMBLY,.... U1, First Mixer	1		PADZZN
-33	MS35649-44	81349	• • NUT, Hex, 4-40(AP).....	4		PAOZZN
	MS35388-78	81349	• • WASHER,Splt Lock,No.4.. (AP)	4		PAOZZN
	MS15795-303	96906	• • WASHER, Flat, No.4(AP).	4		PAOZZN
-34	MS39014101-1593	81349	• • CAPACITOR,C11,C15,C18.. C28,C43,Ceramic,0.1 uf, 50 WVDC, ± 20%	5		PADZZN
-35	RCR20G150JS	81349	• • RESISTOR,R6,Composition 15 ohms, ± 5%, 1/2 Watt	1		PADZZN
-36	2N4126	04713	• • TRANSISTOR,Q1,Silicon,. PNP	1		PADZZN
-37	LT10K131	81349	• • CHOKE,L5,L7,L8,L9,L10,. RF, 10 uH, ± 10%	5		PADZZN
-38	MS39014102-1419	81349	• • CAPACITOR,C17,C20,Cer,. 1 uf, 500 WVDC, ± 20%	2		PADZZN
-39	IN916B	07623	• • DIODE, CR1 and CR2.....	2		PADZZN
-40	RL07S562G	81349	• • RESISTOR,R2,Fixed Film. 5.6K, ± 2%, 1/4 Watt	1		PADZZN
-41	K1935	13103	• • HEAT SINK, Transistor,. Q3 and Q4	2		PAOZZN
-42	2N5160	04713	• • TRANSISTOR,Q3,Silicon.. High Power, PNP	1		PADZZN
-43	MS35233-12	96906	• • SCREW,Machine,Pan Head. 4-40 x 3/16(AP)	1		PAOZZN
	MS35338-78	81349	• • WASHER,Splt Lock,No.4.. (AP)	1		PAOZZN
	MS15795-303	96906	• • WASHER, Flat, No.4(AP).	1		PAOZZN
-44	69011-1058	78912	• • PAD, Transistor, Q3....	1		PAOZZN
-45	JANTX2N3866	81349	• • TRANSISTOR,Q4, Silicon, High Power, PNP	1		PAOZZN

FIGURE 7-3. FIRST MIXER ASSEMBLY, CIRCUIT CARD, A2(Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-3						
-46	MS35233-12	96906	• • SCREW,Machine,Pan Head 4-40 x 3/16(AP)	1		PAOZZN
	MS35338-78	81349	• • WASHER,Splt Lock,No.4. (AP)	1		PAOZZN
	MS15795-303	96906	• • WASHER,Flat,No.4(AP)..	1		PAOZZN
-47	69011-1058	78912	• • PAD, Transistor, Q4...	1		PAOZZN
-48	08495	23386	• • PLATE, Heat Sink...... Transistors Q3 and Q4	1		PAOZZN
-48a	09226	23386	• • PLATE, Heat Sink...... Transistors Q3 and Q4	1	A	PADZZN
-49	RL07S122G	81349	• • RESISTOR,R8,R10,Fixed. Film,1.2K ohm,± 2%, 1/4 Watt	2		PADZZN
-50	RL07S222G	81349	• • RESISTOR,R4,Fixed Film 2.2K ohm,± 2%, 1/4 Watt	1		PADZZN
-51	2257R	13103	• • HEAT SINK, Trans. Q2,.	1		PADZZN
-52	JANTX2N3866	81349	• • TRANSISTOR,Q2,Silicon, High Power, NPN	1		PADZZN
-53	69011-1058	78912	• • PAD, Transistor, Q2...	1		PADZZN
-54	08501	23386	• • TRANS. T1,RF, Wideband	1		PADZZN
-55	RJ50FW502	81349	• • RESISTOR, Variable, R9 5K ohms, ± 10%	1		PADZZN
-56	RL07S470G	81349	• • RESISTOR,R3,Fixed Film 47 ohms, ± 2%, 1/4 Watt	1		PADZZN
-57	T362B156K020AS	31433	• • CAPACITOR, C38, C41,.. Tantalum,15 uf,20 WVDC, ± 20%	2		PADZZN
-58	08499-4	23386	• • CONNECTOR,J2,Control..	1		PAOZZN
-59	CMR05F151GODR	81349	• • CAPACITOR,C2,C7,Mica,. 150 pf, 500 WVDC, ± 2%	2		PADZZN
-60	CMR05E820GODR	81349	• • CAPACITOR,C1,C3,Mica,. 82 pf, 500 WVDC, ± 2%	2		PADZZN
-61	08500-1	23386	• • COIL ASSEMBLY, L1, RF. Variable	1		PADZZN
-62	CM05CD180G03	81349	• • CAPACITOR, C4, Mica,.. 18 pf, 500 WVDC, ± 2%	1		PADZZN
-63	08500-2	23386	• • COIL ASSEMBLY, L2, RF. Variable	1		PADZZN
-64	CMR05F271GODR	81349	• • CAPACITOR, C5, Mica,.. 270 pf, 500 WVDC, ± 2%	1		PADZZN
-65	CMR05C100GODR	81349	• • CAPACITOR, C6, Mica,.. 10 pf, 500 WVDC, ± 5%	1		PADZZN
-66	08500-3	23386	• • COIL ASSEMBLY, L3, RF. Variable	1		PADZZN
-67	CMR05E300GODR	81349	• • CAPACITOR, C8, Mica,.. 30 pf, 500 WVDC, ± 2%	1		PADZZN
-68	CMR05F241GODR	81349	• • CAPACITOR, C9, Mica,.. 240 pf, 500 WVDC, ± 2%	1		PADZZN
-69	08500-4	23386	• • COIL ASSEMBLY, L4 RF.. Variable	1		PADZZN
-70	MS18130-5	96906	• • COIL ASSEMBLY, L16,L17 0.56 uH	2		PADZZN

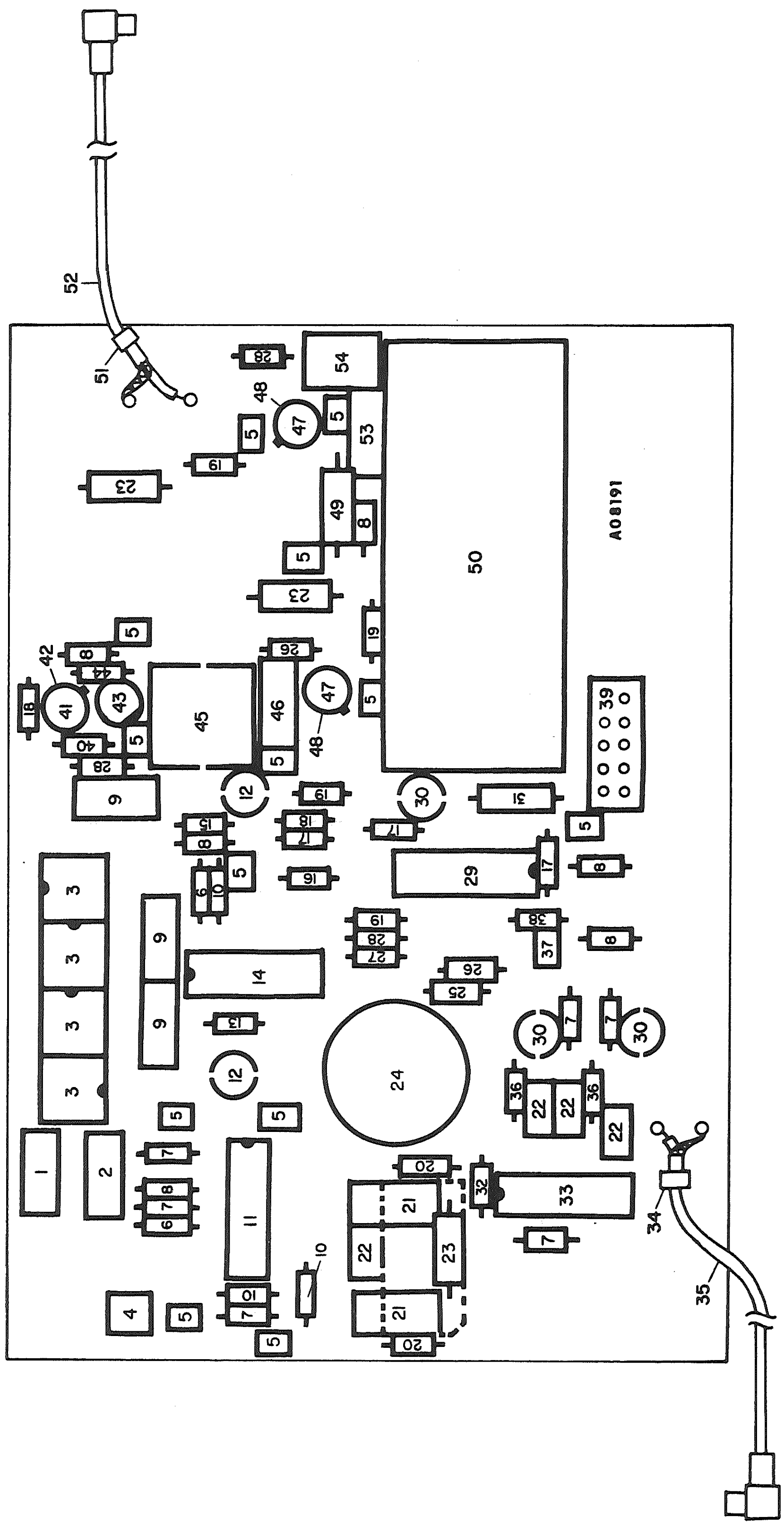


Figure 7-4. Second Mixer Assembly, Circuit Card, A3

FIGURE 7-4. SECOND MIXER ASSEMBLY, CIRCUIT CARD, A3

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-4-	08191	23386	• SECOND MIXER ASSEMBLY, ... Circuit Card, A3	1		PAOLDT
-1	CMR05E820G0DR	81349	• • CAPACITOR, C18, Mica, ... 82 pf, 500 WVDC, ±2%	1		PADZZN
-2	CMR05F331G0DR	81349	• • CAPACITOR, C19, Mica, 330 pf, . 500 WVDC, ±2%	1		PADZZN
-3	08522	23386	• • COIL, L5, L6, L7, L8, RF . . . . . . Variable	4		PADZZN
-4	051-351-000-220	98291	• • CONNECTOR, J2, RF, SMB	1		PAOZZN
-5	CY15C102M	71590	• • CAPACITOR, C1, C2, C5, C6, . . . C8, C10, C11, C12, C14, C20, C21, C22, C23, Mica, 1000 pf, 50 WVDC, ±20%	13		PADZZN
-6	RL07S103G	81349	• • RESISTOR, R17, R36, Fixed. . . . Film, 10K ohms, ±2%, ¼ watt	2		PADZZN
-7	RL07S470G	81349	• • RESISTOR, R30, R31, R32, ... R40, R44, R45, Fixed Film, 47 ohms, ±2%, ¼ watt	6		PADZZN
-8	RL07S101G	81349	• • RESISTOR, R2, R3, R20, R21, . . R27, R35, Fixed Film, 100 ohms, ±2%, ¼ watt	6		PADZZN
-9	CMR05E680G0DR	81349	• • CAPACITOR, C15, C16, C17, . . . Mica, 68 pf, 500 WVDC, ±2%	3		PADZZN
-10	RL07S102G	81349	• • RESISTOR, R19, R29, R33, ... Fixed Film, 1K ohms, ±2%, ¼ watt	3		PADZZN
-11	MC1496L	04713	• • INTEGRATED CIRCUIT, U3, . . . Second Mixer	1		PADZZN
-12	T362A105M035AS	31433	• • CAPACITOR, C7, C30, ... Tantalum, 1 uf, 35 WVDC, ±20%	2		PADZZN
-13	RL07S561G	81349	• • RESISTOR, R15, Fixed Film, . . . 560 ohms, ±2%, ¼ watt	1		PADZZN
-14	CA3046E	02735	• • INTEGRATED CIRCUIT, U1, . . . Transistor Array	1		PADZZN
-15	KS8379	04713	• • DIODE, CR1, Pin.	1		PADZZN
-16	RL07S104G	81349	• • RESISTOR, R9, Fixed Film. . . . . 100K ohms, ±2%, ¼ watt	1		PADZZN
-17	RL07S223G	81349	• • RESISTOR, R5, R6, R11, ... Fixed Film, 22K ohms, ±2%, ¼ watt	3		PADZZN
-18	RL07S472G	81349	• • RESISTOR, R7, R23, Fixed . . . . Film, 4.7K ohms, ±2%, ¼ watt	2		PADZZN
-19	RL07S221G	81349	• • RESISTOR, R1, R10, R13, ... R18, Fixed Film, 220 ohms, ±2%, ¼ watt	4		PADZZN
-20	RL07S122G	81349	• • RESISTOR, R38, R39, Fixed. . . . Film, 1.2K ohms, ±2%, ¼ watt	2		PADZZN

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-4-						
-21	D155E220D0	81349	• • CAPACITOR, C31, C32, Mica, . . . 22 pf, 500 WVDC, ±2%	2		PADZZN
-22	MS39014101-1593	81349	• • CAPACITOR, C24, thru C27,. . . . Ceramic, 0.1 uf, 50 WVDC, ±20%	4		PADZZN
-23	LT10K133	81349	• • CHOKE, L1, L3, L9, RF, ... 15 uH, ±10%	3		PADZZN
-24	08530	23386	• • TRANSFORMER ASSEMBLY, . . T2	1		PADZZN
-25	RLR07C390GR	81349	• • RESISTOR, R34, Fixed Film, . . . 39 ohms, ±2%, ¼ watt	1		PADZZN
-26	RLR07C100GR	81349	• • RESISTOR, R16, R37, Fixed. . . . Film, 10 ohms, ±2%, ¼ watt	2		PADZZN
-27	RL07S270G	81349	• • RESISTOR, R14, Fixed Film, . . . 27 ohms, ±2%, ¼ watt	1		PADZZN
-28	RL07S222G	81349	• • RESISTOR, R8, R12, R28, ... Fixed Film, 2.2K ohms, ±2%, ¼ watt	3		PADZZN
-29	CA324E	02735	• • INTEGRATED CIRCUIT, ... U2, 324 Quad Operational Amplifier	1		PADZZN
-30	T362B156M020AS	31433	• • CAPACITOR, C13, C28, C29, . . . Tantalum, 15 uf, 20 WVDC, 20%	3		PADZZN
-31	LT10K012	81349	• • CHOKE, L4, RF, 100 uH, ±5%. . .	1		PADZZN
-32	RL07S152G	81349	• • RESISTOR, R43, Fixed Film, . . . 1.5K ohms, ±2%, ¼ watt	1		PADZZN
-33	MC1733CP	04713	• • INTEGRATED CIRCUIT, ... U4, Operational Amplifier	1		PADZZN
-34	MS18034-4	96906	• • TIE WRAP CABLE, W2	1		PAOZZN
-35	08479-3	23386	• • CABLE, W2, 455 kHz Output . . .	1		MOOZZN
-36	RL07S331G	81349	• • RESISTOR, R41, R42, Fixed. . . . Film, 330 ohms, ±2%, ¼ watt	2		PADZZN
-37	C320C103M1U1C1	31433	• • CAPACITOR, C4, Ceramic, ... 0.01 uf, 50 WVDC, ±20%	1		PADZZN
-38	RLR07C224GR	81349	• • RESISTOR, R4, Fixed Film, ... 220K ohms, ±2%, ¼ watt	1		PADZZN
-39	08499-5	23386	• • CONNECTOR, J1	1		PAOZZN
-40	RL07S393G	81349	• • RESISTOR, R22, Fixed Film, . . . 39K ohms, ±2%, ¼ watt	1		PADZZN
-41	JAN2N918	81349	• • TRANSISTOR, Q3, NPN.	1		PADZZN
-42	7717-HWHT	13103	• • PAD, Transistor, Q3	1		PADZZN
-43	RJ50FW501	81349	• • RESISTOR, R26, Variable, ... 500 ohms, ±20%	1		PADZZN
-44	RL07S560G	81349	• • RESISTOR, R25, Fixed Film, . . . 56 ohms, ±2%, ¼ watt	1		PADZZN
-45	08503	23386	• • TRANSFORMER, T1, RF . . . . . . Variable	1		PADZZN
-46	CMR05E330G0DR	81349	• • CAPACITOR, C9, Mica, 33 pf, . . . 550 WVDC, ±2%	1		PADZZN
-47	U310	17896	• • TRANSISTOR, Q1, Q2, Field . . . Effect	2		PADZZN

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-4-						
-48	7717-HWHT	13103	• • PAD, Transistor, Q1 and Q2.	2		PADZZN
-49	LT4K078	81349	• • CHOKE, L2, RF, 0.56 uH	1		PADZZN
-50	08576	23386	• • FILTER, FL1, 40.455 MHz	1		PADZZN
-51	MS18034-4	96906	• • TIE WRAP, Cable W1	1		PAOZZN
-52	08479-2	23386	• • CABLE, W1, 40.455 MHz Input . .	1		MOOZZN
-53	CM05CD150G03	81349	• • CAPACITOR, C33, Mica, ... 15 pf, 500 WVDC, ±1 pf	1		PADZZN
-54	9311	91293	• • CAPACITOR, C3, Variable, ... Ceramic, 5-50 pf	1		PADZZN

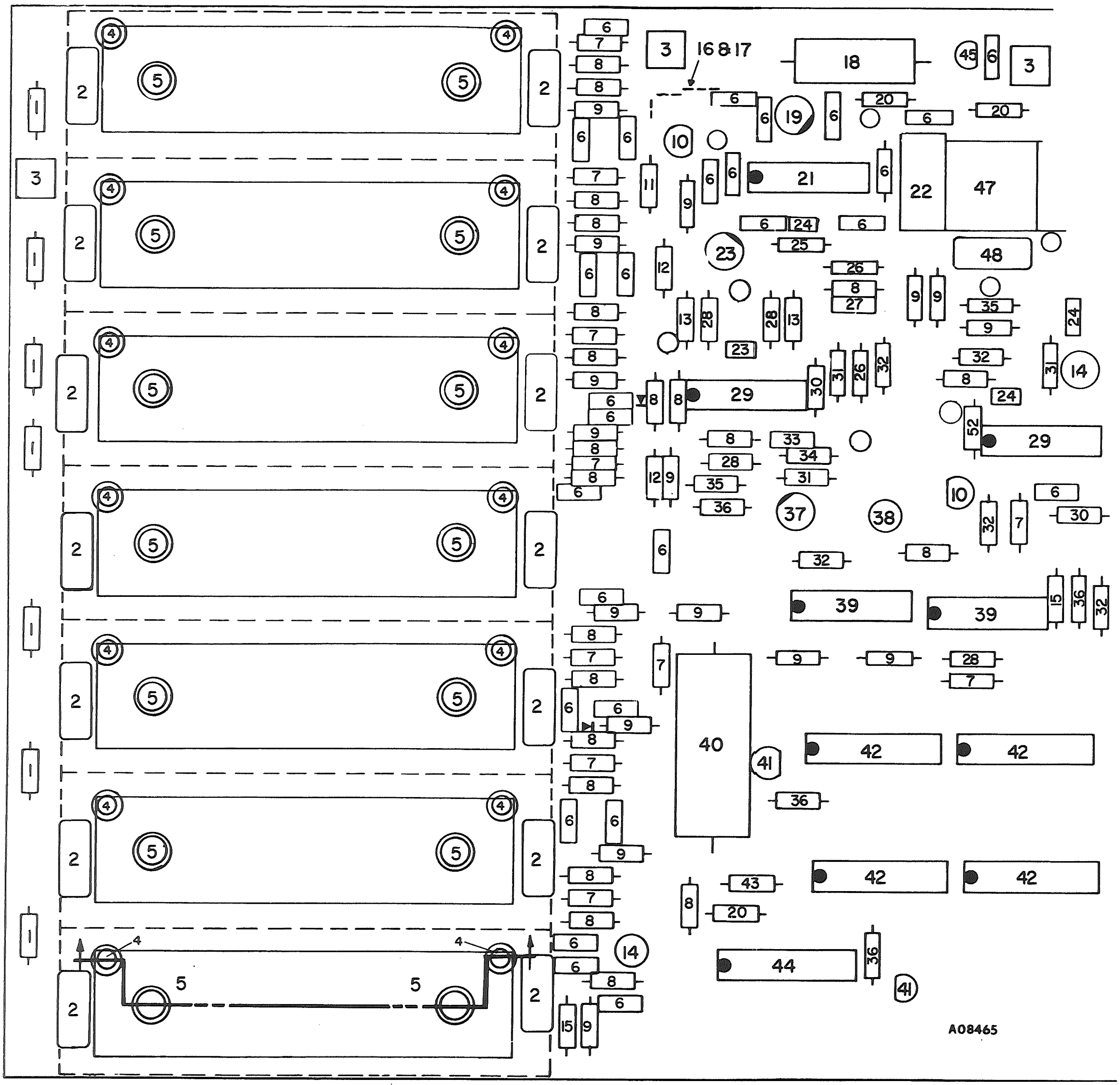


Figure 7-5. Main IF/AF Assembly, Circuit Card, A4 (Sheet 1 of 2)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-5-/	08465	23386	• MAIN IF/AF ASSEMBLY, ... Circuit Card, A4	1		PAODDT
/1, 2-1	RL07S472G	81349	• • RESISTOR, R1 thru R7, ... R50, R92, R126, R136, R137, Fixed Film, 4.7K ohms, ±2%, ¼ watt	12		PADZZN
/1, 2-2	Not Used		• • CAPACITOR, C1 thru C12, ... C48, C55, C90, C109, C110	17		PADZZN
/1, 2-3	051-351-0000-220	98291	• • CONNECTOR, J1, J3 thru J6, ... RF, 700209	5		PAOZZN
/1-4	NS-441-B1	06776	• • SOCKET, Filter Pin, 0.040 ..... diameter	14		XA
/1-5	NS-432-100	06776	• • SOCKET, Filter Pin, 0.100 ..... diameter	14		XA
/1, 2-6	MS39014101-1593	81349	• • CAPACITOR, C13 through C19,.. C21 thru C31, C33, C34, C36, C38 thru C40, C45, C49, C50, C54, C56, C57, C60 thru C67, C72, C75 thru C79, C81, C82, C94, C100, C101, C103, C104, C111, C112, C120, C121, ceramic, 0.1 uf, 50 WVDC, ±20%	55		PADZZN
/1, 2-7	RL07S103G	81349	• • RESISTOR, R16 thru R22, ... R24, R33, R36, R40, R53, R57, R58, R71, R86, R88, R89, R130, R132, R135, Fixed Film, 10K ohms, ±2%, ¼ watt	21		PADZZN
/1, 2-8	IN916B	07623	• • DIODE, CR1 thru CR16, CR18 .. thru CR31	30		PADZZN
/1, 2-9	RL07S102G	81349	• • RESISTOR, R9 thru R15, R23... R28, R55, R62, R66, R68, R70, R72, R77 thru R79, R85, R87, R102, R144, R145, Fixed Film, 1K ohms, ±2%, ¼ watt	23		PADZZN
/1, 2-10	2N5089	04713	• • TRANSISTOR, Q1, Q2, Q6 ..... thru Q10, NPN, High Power	7		PADZZN
/1, 2-11	RL07S101G	81349	• • RESISTOR, R25, R60, ... R141, Fixed Film,100 ohms, ±2%, ¼ watt	3		PADZZN
/1, 2-12	RL07S222G	81349	• • RESISTOR, R34, R51, R101, ... R128, Fixed Film, 2.2K ohms, ±2%, ¼ watt	4		PADZZN
/1, 2-13	RL07S104G	81349	• • RESISTOR, R37, R95, ... R96, R117, R122, R123, R125, R129, R140, R150, R151, Fixed Film, 100K ohms, ±2%, ¼ watt.	11		PADZZN

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-5- /1, 2-14	T362B156M020AS	31433	• • CAPACITOR, C20, C32, C52, . . . C58, C80, C93, C102, C113, Tantalum, 15 uf, 20 WVDC, ±20%	8		PADZZN
/1, 2-15	RL07S152G	81349	• • RESISTOR, R27, R44, R64, ... R94, R113, R143, Fixed Film, 1.5K ohms, ±2%, ¼ watt	6		PADZZN
/1-16	MIL-W-3861/S-24	81349	• • WIRE, Link 1, Buss No. 24	AR		PAOZZN
/1-17	MIL-I-221296-24	81349	• • SLEEVING, Link 1, PTFE. . . . . . tubing, No. 24	AR		PAOZZN
/1, 2-18	ET101X025A5	30983	• • CAPACITOR, C35, C73, ... Electrolytic, 100 uf, 25 WVDC, –10 +50%	2		PADZZN
/1-19	RJ50FW202	81349	• • RESISTOR, R39, Variable, ... 2K ohms	1		PADZZN
/1, 2-20	RL07S470G	81349	• • RESISTOR, R8, R29, R46, ... R80, R82, R115, Fixed Film, 47 ohms, ±2%, ¼ watt	6		PADZZN
/1-21	UA757MQB	34148	• • INTEGRATED CIRCUIT, U8, . . . IF Amplifier	1		PADZZN
/1, 2-22	CMR06F152G0DR	81349	• • CAPACITOR, C44, C47, Mica, . . . 1500 pf, 500 WVDC, ±2%	2		PADZZN
/1-23	RL07S503G	81349	• • RESISTOR, R47, Variable, ... 50K ohms	1		PADZZN
/1, 2-24	C320C103M1U1C1	31433	• • CAPACITOR, C43, C51, C53, . . . C69, C70, ceramic, 0.01 uf, 50 WVDC, ±20%	5		PADZZN
/1, 2-25	RL07S681G	81349	• • RESISTOR, R43, R48, Fixed. . . . Film, 680 ohms, ±2%, ¼ watt	2		PADZZN
/1-26	RL07S123G	81349	• • RESISTOR, R76, R98, Fixed. . . . Film, 12K ohms, ±2%, ¼ watt	2		PADZZN
/1, 2-27	RL07S682G	81349	• • RESISTOR, R74, R81, R108, . . . Fixed Film, 6.8K ohms, ±2%, ¼ watt	3		PADZZN
/1, 2-28	RL07S473G	81349	• • RESISTOR, R32, R38, R41, ... R52, R90, R93, R103, Fixed Film, 47K ohms, ±2%, ¼ watt	7		PADZZN
/1, 2-29	CA324E	02735	• • INTEGRATED CIRCUIT, U7, . . . U14, U17, operational amplifier	3		PADZZN
/1-30	RL07S273G	81349	• • RESISTOR, R99, R146, ... Fixed Film, 27K ohms, ±2%, ¼ watt	2		PADZZN
/1, 2-31	RL07S153G	81349	• • RESISTOR, R65, R69, R97, ... R107, R129, R131, R134, Fixed Film, 15K ohms, ±2%, ¼ watt	7		PADZZN
/1, 2-32	RL07S223G	81349	• • RESISTOR, R26, R30, R49, ... R61, R73, R83, R91, R124, R147, Fixed Film, 22K ohms, ±2%, ¼ watt	9		PADZZN

FIGURE 7-5. MAIN IF/AF ASSEMBLY, CIRCUIT CARD, A4 (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-5-						
/1-33	MS39014102-1419	81349	• • CAPACITOR, C74, Ceramic, ... 1 uf, 50 WVDC, ±20%	1		PADZZN
/1-34	RLR07C184GR	81349	• • RESISTOR, R106, Fixed Film, . . 180K ohms, ±2%, ¼ watt	1		PADZZN
/1-35	RL07S183G	81349	• • RESISTOR, R67, R104, Fixed . . . Film, 18K ohms, ±2%, ¼ watt	2		PADZZN
/1, 2-36	Not Used		• • RESISTOR, R42, R54, R56, ... R59, R63, R138, R148, R149, Not Used	8		PADZZN
/1-37	RJ50FW685	81349	• • RESISTOR, R105, Variable . . . . . 10K ohms	1		PADZZN
/1, 2-38	T362A685M035AS	31433	• • CAPACITOR, C42, C59, C83, . . . C85, C91, C95, C96, C97, C98, C106, Tantalum, 6.8 uf, 35 WVDC, ±20%	10		PADZZN
/1-39	CD4066BFX	02735	• • INTEGRATED CIRCUIT, U11, . . U12, Quad, Bilateral Switch	2		PADZZN
/1-40	ET471X025A01	30983	• • CAPACITOR, C92, Electro- . . . . . lytic, 470 uf, 25 WVDC, -10 +100%	1		PADZZN
/1, 2-41	Not Used		• • TRANSISTOR, Q3, Q4, Q5, ... Q11, Not Used	4		PADZZN
/1, 2-42	**CD4042BE**	02735	• • INTEGRATED CIRCUIT, U2 . . . U4, U13, U15, U23, Quad Latch	5		PADZZN
/1, 2-43	RLR07C100GR	81349	• • RESISTOR, R100, R133, Fixed . . Film, 10 ohms, ±2%, ¼ watt	2		PADZZN
/1-44	CD40N28BCN	27014	• • INTEGRATED CIRCUIT, U1, . . . BCD Decoder	1		PADZZN
/1-45	LM78L1ZAWC	27014	• • INTEGRATED CIRCUIT, U6, . . . 12V Regulator	1		PADZZN
/2-46	RL07S471G	81349	• • RESISTOR, R35, R75, R110, . . . Fixed Film, 470 ohms, ±2%, ¼ watt	3		PADZZN
/1, 2-47	08485	23386	• • COIL ASSEMBLY, L1, L2, RF . . .	2		PADZZN
/1-48	CMR05E820G0DR	81349	• • CAPACITOR, C46, Mica, ... 82 pf, 500 WVDC, ±2%	1		PADZZN
/1, 2-49	RL07S332G	81349	• • RESISTOR, R31, R84, R109, . . . R111, R112, R114, R116, R121, Fixed Film, 3.3K ohms, ±2%, ¼ watt	8		PADZZN
/2-50	CY15C102M	71590	• • CAPACITOR, C37, ceramic, ... 100 pf, 50 WVDC, ±20%	1		PADZZN
/2-51	CA3046E	02735	• • INTEGRATED CIRCUIT, U10, . . Transistor Array	1		PADZZN
/1-52	RLR07C105GR	81349	• • RESISTOR, R152, Fixed Film, . . 1 meg ohms, ±2%, ¼ watt	1		PADZZN
/2-53	C320C223M1U1CA	31433	• • CAPACITOR, C41, Ceramic, ... 0.022 uf, 50 WVDC, ±20%	1		PADZZN
/2-54	RLR07C334GR	81349	• • RESISTOR, R45, Fixed Film, . . . 330K ohms, ±2%, ¼ watt	1		PADZZN

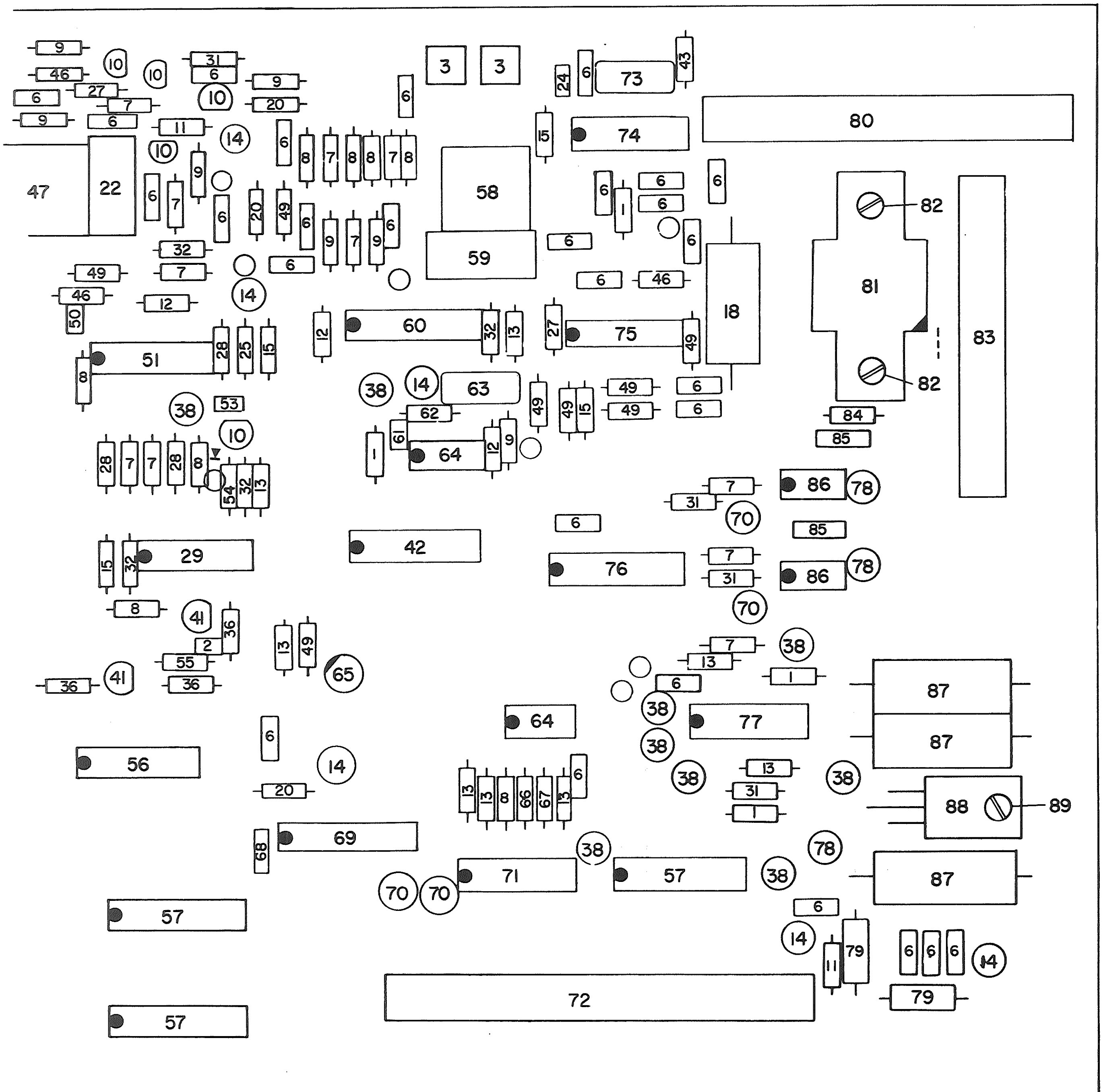


Figure 7-5. Main IF/AF Assembly, Circuit Card, A4 (Sheet 2 of 2)

FIGURE 7-5. MAIN IF/AF ASSEMBLY CIRCUIT CARD, A4 (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-5-						
/2-55	Not Used		• • DIODE, CR17, Not Used	1		PADZZN
/2-56	M38510/05101BCA	81349	• • INTEGRATED CIRCUIT, ... U9, Flip Flop	1		PADZZN
/2-57	CD40109BF3	54590	• • INTEGRATED CIRCUIT, ... U3, U5, U16, Level Translator	3		PADZZN
/2-58	08531	23386	• • COIL ASSEMBLY, L3, RF	1		PADZZN
/2-59	CMR06F332G0DR	81349	• • CAPACITOR, C68, Mica, ... 3300 pf, 500 WVDC, ±2%	1		PADZZN
/2-60	CD4053BD/3	02735	• • INTEGRATED CIRCUIT, ... U19, Multiplexer/Demultiplexer	1		PADZZN
/2-61	C320C152K2R5C1	31433	• • CAPACITOR, C88, Ceramic, ... 1500 pf, 100 WVDC, ±10%	1		PADZZN
/2-62	RL07S822G	81349	• • RESISTOR, R127, ... Fixed Film, 8.2K ohms, ±2%, ¼ watt	1		PADZZN
/2-63	DM15F821F0300-WV4CR	72136	• • CAPACITOR, C89, Mica, ... 820 pf, 300 WVDC, ±2%	1		PADZZN
/2-64	CA1458E	02735	• • INTEGRATED CIRCUIT, ... U22, U28, Dual Operational Amplifier	2		PADZZN
/2-65	RJ50FW502	81349	• • RESISTOR, R119, Variable, ... 5K ohms	1		PADZZN
/2-66	RL07S683G	81349	• • RESISTOR, R120, Fixed . . . . . . Film, 68K ohms, ±2%, ¼ watt	1		PADZZN
/2-67	RL07S393G	81349	• • RESISTOR, R118, Fixed . . . . . . Film, 39K ohms, ±2%, ¼ watt	1		PADZZN
/2-68	DTZ-10	71590	• • CAPACITOR, C84, Ceramic, ... 10 pf, ±5%	1		PADZZN
/2-69	SN7524N	01295	• • INTEGRATED CIRCUIT, ... U21, 8 Bit Buffer Multiplying	1		PADZZN
/2-70	T362A105M035AS	31433	• • CAPACITOR, C86, C87, ... C114, C116, Tantalum, 1.0 uf, 35 WVDC, ±20%	4		PADZZN
/2-71	M38510/11201BCB	02735	• • INTEGRATED CIRCUIT, ... U24, Quad Voltage Comparator	1		PADZZN
/2-72	3432-2003	75037	• • CONNECTOR, J2, ... Ribbon, 40 way	1		PADZZN
/2-73	CMR05F101G0DR	81349	• • CAPACITOR, C71, Mica, ... 100 pf, 500 WVDC, ±2%	1		PADZZN

FIGURE 7-5. MAIN IF/AF ASSEMBLY CIRCUIT CARD, A4 (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-5- /2-74	MC1357P	04713	• • INTEGRATED CIRCUIT, ... U18, FM Detector	1		PADZZN
/2-75	MC1496L	04713	• • INTEGRATED CIRCUIT, ... U20, Product Detector	1		PADZZN
/2-76	CD22100F	02735	• • INTEGRATED CIRCUIT, ... U25, 4 x 4 Crosspoint Switch	1		PADZZN
/2-77	ULN2278B	56289	• • INTEGRATED CIRCUIT, ... U26, Audio Amplifier, 2 watt	1		PADZZN
/2-78	T362C686M015AS	31433	• • CAPACITOR, C107, C118, ... C119, Tantalum, 68 uf, 15 WVDC, ±20%	3		PADZZN
/2-79	LT10K012	81349	• • CHOKE, L4, L5, 100 uH . . . . ±5%	2		PADZZN
/2-80	3431-2003	75037	• • CONNECTOR, J8, ... Ribbon, 34 way	1		PADZZN
/2-81	08535	23386	• • TRANSFORMER ASSEMBLY, . . T1	1		PADZZN
/2-82	MS35649-44	81349	• • NUT, Hex, No. 4 (AP)	2		PAOZZN
	MS35338-78	81349	• • WASHER, Split Lock, ... No. 4 (AP)	2		PAOZZN
	MS15795-303	96906	• • WASHER, Flat, No. 4, (AP)	2		PAOZZN
	MS35233-14	96906	• • SCREW, Machine, Pan Head, ... 4-40 x 5/16 (AP)	2		PAOZZN
/2-83	3429-2003	75037	• • CONNECTOR, J7, ... Ribbon, 26 way	1		PADZZN
/2-84	RN55D1400F	81349	• • RESISTOR, R142, Fixed . . . . . . Film, 140 ohms, ±2%, ¼ watt	1		PADZZN
/2-85	DD-391	71590	• • CAPACITOR, C115, C117, ... Ceramic, 390 pf, 500 WVDC, ±10%	2		PADZZN
/2-86	MC3340L	04713	• • INTEGRATED CIRCUIT, ... U30, U31, Electronic Attenuator	2		PADZZN
/2-87	3071FE221T016SF	30983	• • CAPACITOR, C99, C105, ... C108, Electrolytic, 220 uf, 16 WVDC, −10 +50%.	3		PADZZN
/2-88	M38510/10708BEA	81349	• • INTEGRATED CIRCUIT, ... U27, Voltage Regulator, +15 volts, 7812			PADZZN
/2-89	MS35649-44	81349	• • NUT, Hex, No. 4 (AP)	1		PAOZZN
	MS35338-78	81349	• • WASHER, Split Lock, ... No. 4 (AP)	1		PAOZZN
	MS15795-303	96906	• • WASHER, Flat, No. 4 (AP)	1		PAOZZN
	MS35233-14	96906	• • SCREW, Machine, Pan Head, ... 4-40 x 5/16 (AP)	1		PAOZZN

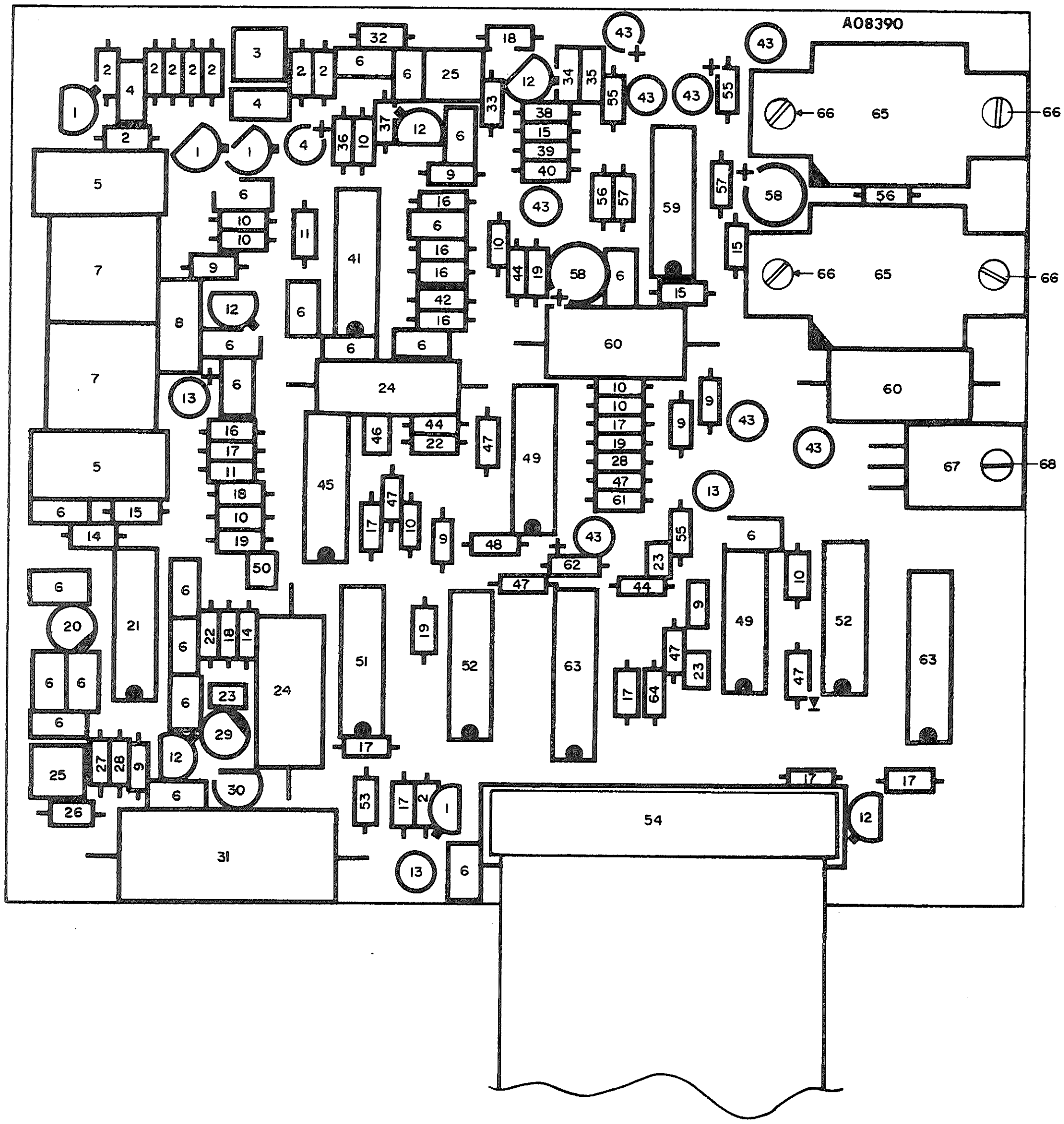


Figure 7-6. ISB Assembly, Circuit Card, A5

FIGURE 7-6. ISB ASSEMBLY, CIRCUIT CARD, A5

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-6	08390	23386	• ISB ASSEMBLY, Circuit Card, A5. . .	1		PAOLDT
-1	Not Used		• • TRANSISTOR, Q2, Q4, ... Q5, Q9, Not Used	4		
-2	Not Used		• • RESISTOR, R31, R33, R36, ... R40, R42, R44, R46, R47, R50, R62, R80, Not Used	11		
-3	Not Used		• • CONNECTOR, J2, Not Used	1		
-4	Not Used		• • CAPACITOR, C20, C22, ... C27, C29, Not Used	4		
-5	CMR06F152G0DR	81349	• • CAPACITOR, C16, C19, ... Mica, 1500 pf, 500 WVDC, ±2%	2		PADZZN
-6	M39014101-1593	81349	• • CAPACITOR, C1, C3, C5, ... C7, C8, C10, C12 thru C15, C21, C23, C28, C30, C31, C33 thru C37, C45, C54, Ceramic,0.1 uf, 50 WVDC, ±20%	22		PADZZN
-7	08485	23386	• • COIL, L1, L2, RF Variable	2		PADZZN
-8	CMR05E820G0DR	81349	• • CAPACITOR, C18, Mica, ... 82 pf, 500 WVDC, ±2%	1		PADZZN
-9	RL07S102G	81349	• • RESISTOR, R12, R30, R39, ... R48, R51, R53, R59, Fixed Film, 1K ohms, ±2%, ¼ watt	7		PADZZN
-10	RL07S103G	81349	• • RESISTOR, R10, R11, ... R14, R29, R34, R35, R43, R56, R63, Fixed Film, 10K ohms, ±2%, ¼ watt	9		PADZZN
-11	RL07S471G	81349	• • RESISTOR, R8, R64, Fixed . . . . Film, 470 ohms, ±2%, ¼ watt	2		PADZZN
-12	2N5089	04713	• • TRANSISTOR, Q1, Q3, ... Q6 thru Q8, NPN, High Power	5		PADZZN
-13	T362B156K020AS	31433	• • CAPACITOR, C9, C26, ... C53, Tantalum, 15 uf, 20 WVDC, ±20%	3		PADZZN
-14	RL07S470G	81349	• • RESISTOR, R16, R22, ... Fixed Film, 47 ohms, ±2%, ¼ watt	2		PADZZN
-15	RL07S472G	81349	• • RESISTOR, R27, R72, R73,. . . . . R78, Fixed Film, 4.7K ohms, ±2%, ¼ watt	4		PADZZN
-16	RL07S332G	81349	• • RESISTOR, R6, R65. . . . . thru R67, R69, Fixed Film, 3.3K ohms, ±2%, ¼ watt	5		PADZZN

FIGURE 7-6. ISB ASSEMBLY, CIRCUIT CARD, A5 (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-6-						
-17	RL07S223G	81349	• • RESISTOR, R1, R5, R26, ... R32, R37, R41, R54, R58, Fixed Film, 22K ohms, ±2%, ¼ watt	8		PADZZN
-18	RL07S222G	81349	• • RESISTOR, R7, R25, R81, ... Fixed Film, 2.2K ohms, ±2%, ¼ watt	3		PADZZN
-19	RL07S473G	81349	• • RESISTOR, R9, R13, R15, ... R28, Fixed Film, 47K ohms, ±2%, ¼ watt	4		PADZZN
-20	RJ50FW202	81349	• • RESISTOR, R19, ... Variable, 2K ohms	1		PADZZN
-21	UA757DC	07263	• • INTEGRATED CIRCUIT, ... U6, Operational Amplifier	1		PADZZN
-22	RL07S681G	81349	• • RESISTOR, R17, R24, ... Fixed Film, 680 ohms, ±2%, ¼ watt	2		PADZZN
-23	C320C103M1U1C1	31433	• • CAPACITOR, C17, C24, C25, . . . Ceramic, 0.01 uf, 50 WVDC, ±20%	3		PADZZN
-24	ET101X025A5	30983	• • CAPACITOR, C4, C50, ... Electrolytic, 100 uf, 25 WVDC, –10 +50%	2		PADZZN
-25	051-351-0000-220	98291	• • CONNECTOR, J1, J3, RF	2		PADZZN
-26	RL07S101G	81349	• • RESISTOR, R21, Fixed . . . . Film, 100 ohms, ±2%, ¼ watt	1		PADZZN
-27	RL07S563G	81349	• • RESISTOR, R3, Fixed. . . . . Film, 56K ohms, ±2%, ¼ watt	1		PADZZN
-28	RL07S123G	81349	• • RESISTOR, R4, R52, Fixed. . . . . Film, 12K ohms, ±2%, ¼ watt	2		PADZZN
-29	RJ50FW503	81349	• • RESISTOR, R23, Variable, ... 50K ohms	1		PADZZN
-30	LM78L1ZAWC	27014	• • INTEGRATED CIRCUIT, ... U1, +12 volt regulator	1		PADZZN
-31	ET471X025A01	30983	• • CAPACITOR, C52, ... Electrolytic, 470 uf, 25 WVDC, –10 +100%	1		PADZZN
-32	RL07S391G	81349	• • RESISTOR, R61, Fixed . . . . Film, 390 ohms, ±2%, ¼ watt	1		PADZZN
-33	RL07S220G	81349	• • RESISTOR, R83, Fixed . . . . Film, 22 ohms, ±2%, ¼ watt	1		PADZZN

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-6-						
-34	CCR06CQ222GR	81349	• • CAPACITOR, C46, Ceramic, 2200 pf, 50 WVDC, ±5%	1		PADZZN
-35	CCR06CG472GR	81349	• • CAPACITOR, C44, Ceramic, 4700 pf, 50 WVDC, ±5%	1		PADZZN
-36	RL07S333G	81349	• • RESISTOR, R55, Fixed Film, 33K ohms, ±2%, ¼ watt	1		PADZZN
-37	RLR07C330GR	81349	• • RESISTOR, R60, Fixed Film, 33 ohms, ±2%, ¼ watt	1		PADZZN
-38	RL07S822G	81349	• • RESISTOR, R79, Fixed Film, 8.2K ohms, ±2%, ¼ watt	1		PADZZN
-39	RL07S393G	81349	• • RESISTOR, R74, Fixed Film, 39K ohms, ±2%, ¼ watt	1		PADZZN
-40	RL07S683G	81349	• • RESISTOR, R75, Fixed Film, 68K ohms, ±2%, ¼ watt	1		PADZZN
-41	MC1496L	04713	• • INTEGRATED CIRCUIT, U11, Product Detector	1		PADZZN
-42	RL07S122G	81349	• • RESISTOR, R68, Fixed Film, 1.2K ohms, ±2%, ¼ watt	1		PADZZN
-43	T362A685M035AS	31433	• • CAPACITOR, C11, C32, C38, C39, C41, C42, C43, C51, Tantalum, 6.8 uf, 35 WVDC, ±20%	8		PADZZN
-44	RL07S152G	81349	• • RESISTOR, R2, R18, R38, Fixed Film, 1.5K ohms, ±2%, ¼ watt	3		PADZZN
-45	CA3046E	02735	• • INTEGRATED CIRCUIT, U2, Transistor Array	1		PADZZN
-46	C320C223M1U1CA	31433	• • CAPACITOR, C6, Ceramic, 0.022 uf, 50 WVDC, ±20%	1		PADZZN
-47	1N916B	07623	• • DIODE, CR1 thru CR6	6		PADZZN
-48	RLR07C334GR	81349	• • RESISTOR, R20, Fixed Film, 330K ohms, ±2%, ¼ watt	1		PADZZN
-49	CA324E	02735	• • INTEGRATED CIRCUIT, U3, U10, Quad Operational Amplifier	2		PADZZN
-50	CY15C102M	71590	• • CAPACITOR, C2, Ceramic, 1000 pf, 18 WVDC, ±20%	1		PADZZN

FIGURE 7-6. ISB ASSEMBLY, CIRCUIT CARD, A5 (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-6-						
-51	M38510/05101BEA	81349	• • INTEGRATED CIRCUIT, ... U4, +12 volt regulator	1		PADZZN
-52	CD4066BEX	02735	• • INTEGRATED CIRCUIT, ... U5, U9, Quad Bilateral Switch	2		PADZZN
-53	RLR07C100GR	81349	• • RESISTOR, R85, Fixed. . . . . Film, 10 ohms, ±2%, ¼ watt	1		PADZZN
-54	08486	23386	• • CABLE, W1, Ribbon.	1		XA
-55	RL07S153G	81349	• • RESISTOR, R45, R70, ... R71, Fixed Film, 15K ohms, ±2%, ¼ watt	3		PADZZN
-56	RN55D1400F	81349	• • RESISTOR, R82, R84, ... Fixed Film, 140 ohms, ±2%, ¼ watt	2		PADZZN
-57	RL07S104G	81349	• • RESISTOR, R76, R77, ... Fixed Film, 100K ohms, ±2%, ¼ watt	2		PADZZN
-58	T362C686M015AS	31433	• • CAPACITOR, C48, C49, ... Tantalum, 68 uf, 15 WVDC, ±20%	2		PADZZN
-59	LM1877N-9	27014	• • INTEGRATED CIRCUIT, ... U12, Audio Amplifier, 2 watt, dual	1		PADZZN
-60	3071FE221T0168F	30983	• • CAPACITOR, C40, C47, ... Electrolytic, 220 uf, 16 WVDC, −10 +50%	2		PADZZN
-61R	RL07S682G	81349	• • RESISTOR, R57, Fixed . . . . Film, 6.8K ohms, ±2%, ¼ watt	1		PADZZN
-62	RLR07C105GR	81349	• • RESISTOR, R86, Fixed . . . . Film, 1 meg ohms, ±2%, ¼ watt			PADZZN
-63	8101901EB	14933	• • INTEGRATED CIRCUIT, ... U7, U8, Quad Latch	2		PADZZN
-64	RL07S183G	81349	• • RESISTOR, R49, Fixed . . . . Film, 18K ohms, ±2%, ¼ watt	1		PADZZN
-65	08535	23386	• • TRANSFORMER ASSEMBLY, . . T1, T2, Audio	2		PADZZN
-66	MS35649-44	81349	• • NUT, Hex, 4-40 (AP).	2		PAOZZN
	MS35338-78	81349	• • WASHER, Split Lock, ... No. 4 (AP)	2		PAOZZN
	MS15795-303	96906	• • WASHER, Flat, No. 4 (AP)	2		PAOZZN
	MS35233-14	96906	• • SCREW, Machine, Pan Head, ... 4-40 x 5/16 (AP)	2		PAOZZN
-67	M38510/10708BEA	81349	• • INTEGRATED CIRCUIT, ... U13, +15 volt regulator	1		PADZZN

FIGURE 7-6. ISB ASSEMBLY, CIRCUIT CARD, A5 (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-6-						
-68	MS35649-44	81349	• • NUT, Hex, 4-40 (AP)	1		PAOZZN
	MS35338-78	81349	• • WASHER, Split Lock,. . . . . No. 4 (AP)	1		PAOZZN
	MS15795-303	96906	• • WASHER, Flat, No. 4 (AP)	1		PAOZZN
	MS35233-14	96906	• • SCREW, Machine, Pan Head, ... 4-40 x 5/16 (AP)	1		PAOZZN

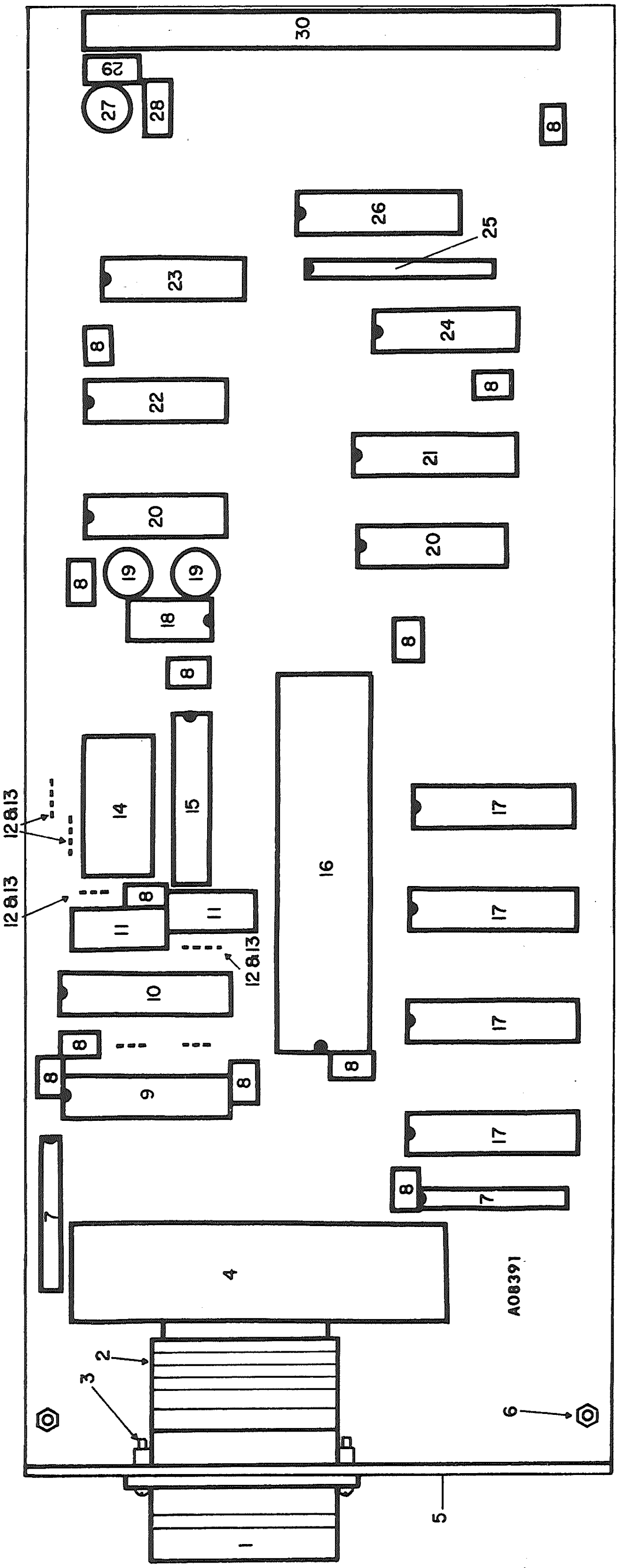


Figure 7-7. Serial Asynchronous Interface Assembly, Circuit Card, A6A1

FIGURE 7-7. SERIAL ASYNCHRONOUS INTERFACE ASSEMBLY,CIRCUIT CARD, A6A1

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-7-	08391	23386	● ● ASYNCHRONOUS . . . . INTERFACE ASSEMBLY, Circuit Card, A6A1	1		PAFLDT
-1	MS90376-16Y	96906	● ● ● COVER, Dust,. . . . . Connector W1J1	1		PAOZZN
-2	M83723-02R-1626N	81349	● ● ● CONNECTOR, W1J1,. . . . . . . 26 Pin	1		PAFZZN
-3	MS35649-44	81349	● ● ● NUT, Hex, 4-40 (AP)	5		PAOZZN
	MS35338-78	81349	● ● ● WASHER, Split Lock, ... No. 4 (AP)	5		PAOZZN
	MS15795-303	96906	● ● ● WASHER, Flat, ... No. 4 (AP)	5		PAOZZN
	MS35233-14	96906	● ● ● SCREW, Machine, ... Pan Head, 4-40 x 5/16 (AP)	5		PAOZZN
-4	08493	23386	● ● ● CABLE ASSEMBLY, ... W1	1		XA
-5	08471	23386	● ● ● PLATE, Connector. . . . . mounting, J1	1		XA
-6	22M-40	13257	● ● ● NUT, Hex, Elastic Stop, ... 4-40 (AP)	2		PAOZZN
	MS35233-15	96906	● ● ● SCREW, Machine, ... Pan Head, 4-40 x 3/8 (AP)	2		PAOZZN
-7	SIP-8-223	91637	● ● ● INTEGRATED CIRCUIT, ... U1, U10, Resistor Network, 22K, 8 pin	2		PADZZN
-8	C320C103M1U1C1	31433	● ● ● CAPACITOR, C4, ... C7, C8, C9, C11 thru C18, Ceramic, 0.01 uf, 50 WVDC, ±20%	12		PADZZN
-9	AM26LS32CN	01295	● ● ● INTEGRATED CIRCUIT, ... U2, Quad differential line receiver	1		PADZZN
-10	AM26LS30PC	34335	● ● ● INTEGRATED CIRCUIT, ... U3, Quad line driver	1		PADZZN
-11	CMR05F301G0DR	81349	● ● ● CAPACITOR, C10, C19, ... Mica, 300 pf, 500 WVDC, ±5%	2		PADZZN
-12	MIL-W-3861/5-22	81349	● ● ● WIRE, Links, LK1,. . . . . LK3, LK4, LK5, Buss No. 22	AR		PAOZZN
-13	MIL-I- 22129C-22	81349	● ● ● SLEEVING, Links, LK1, ... LK3, LK4, LK5, PTFE tubing No. 22	AR		PAOZZN
-14	08490	23386	● ● ● CRYSTAL, Y1, ... 4.9152 MHz	1		PAOZZN
-15	AH5016C-5	27014	● ● ● INTEGRATED CIRCUIT, ... U4, Baud Rate Generator	1		PADZZN

FIGURE 7-7. SERIAL ASYNCHRONOUS INTERFACE ASSEMBLY,CIRCUIT CARD, A6A1 (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-7-						
-16	COM6402P	53848	• • • INTEGRATED CIRCUIT, ... U9, UART	1		PADZZN
-17	CD4503BCN	27014	• • • INTEGRATED CIRCUIT, ... U11 thru U14, Hex three state buffer	4		PADZZN
-18	LM7905CN	27014	• • • INTEGRATED CIRCUIT, ... U5, –5 volts regulator	1		PADZZN
-19	T362A685M035AS	31433	• • • CAPACITOR, C5, C6, ... Tantalum, 6.8 uf, 35 WVDC, ±20%	2		PADZZN
-20	M38510/05001BCB	81349	• • • INTEGRATED CIRCUIT, ... U6, U15, Quad 2 input NAND	2		PADZZN
-21	M38510/30107BEB	81349	• • • INTEGRATED CIRCUIT, ... U16, Quad D Flip Flop	1		PADZZN
-22	M38510/3003BCB	81349	• • • INTEGRATED CIRCUIT, ... U7, Hex inverter	1		PADZZN
-23	CD4085BF	02735	• • • INTEGRATED CIRCUIT, ... U8, Dual AND/OR inverter gate	1		PADZZN
-24	M38510/06203BEA	81349	• • • INTEGRATED CIRCUIT, ... U17, Dual 4 input NOR gate	1		PADZZN
-25	4310R-101-223	32997	• • • INTEGRATED CIRCUIT, ... U18, Resistor network, 22K, 10 pin	1		PADZZN
-26	CD4529BCN	27014	• • • INTEGRATED CIRCUIT, ... U19, Dual 4 channel data select	1		PADZZN
-27	T362B226K015AS	31433	• • • CAPACITOR, C3, ... Tantalum, 22 uf, 15 WVDC, ±20%	1		PADZZN
-28	MS39014101-1593	81349	• • • CAPACITOR, C1, ... Ceramic, 0.1 uf, 50 WVDC, ±20%	1		PADZZN
-29	MS39014/2-1356	81349	• • • CAPACITOR, C2, ... Ceramic, 0.22 uf, 50 WVDC, ±20%	1		PADZZN
-30	08491	23386	• • • CONNECTOR, P1, ... 50 pin, 2 section	1		PADZZN

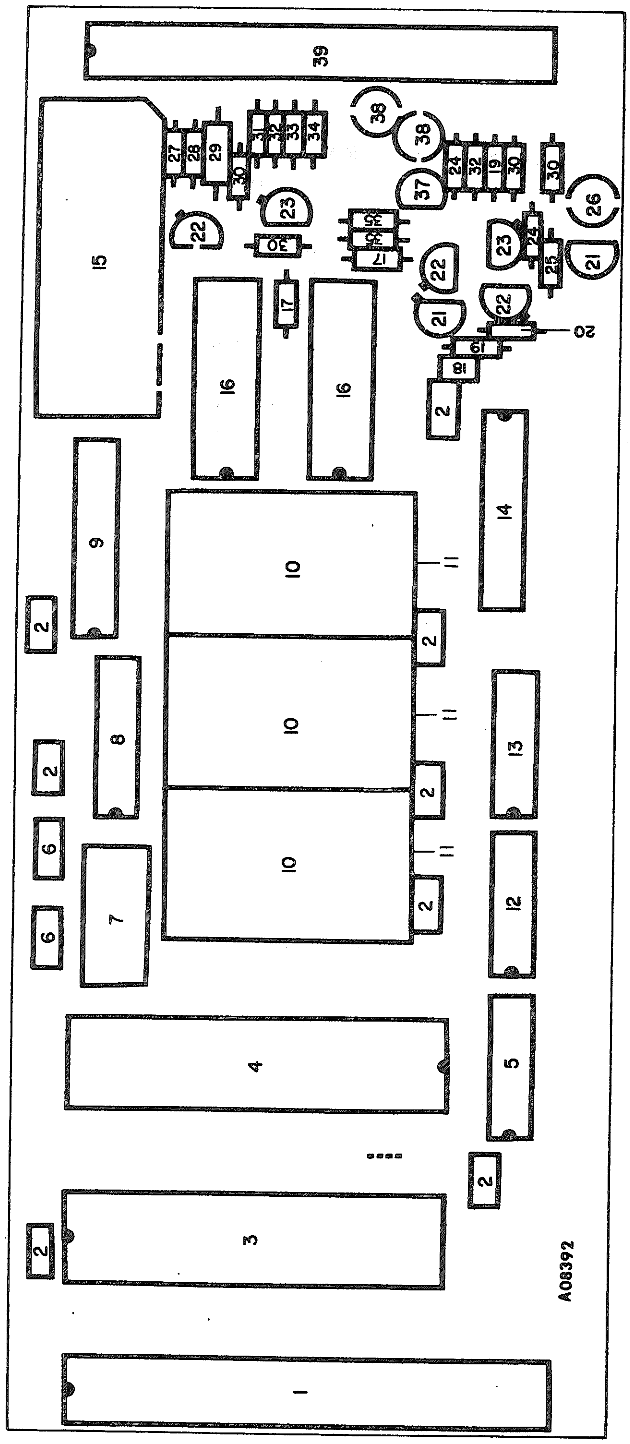


Figure 7-8. Microcomputer Assembly, Circuit Card, A6A2

FIGURE 7-8. MICROCOMPUTER ASSEMBLY, CIRCUIT CARD, A6A2

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-8-	08392	23386	• • MICROCOMPUTER .... ASSEMBLY, Circuit Card, A6A2 (with EPROM ROM set)	1		PAODDT
7-1/1-40	08392-3	23386	• • MICROCOMPUTER ASSEMBLY, Circuit Card A6A2 (without EPROM, ROM set)	1		
-1	65000-036	22526	• • • CONNECTOR, J2, ... 34 pin	1		PADZZN
-2	MS39014101-1593	81349	• • • CAPACITOR, C3 thru ...... C10, C18, Ceramic, 0.1 uf, 50 WVDC, ±20%	9		PADZZN
-3	MK3850	50088	• • • INTEGRATED CIRCUIT, ... U1, Central Processor Unit	1		PADZZN
-4	MK3853	50088	• • • INTEGRATED CIRCUIT, ... U2, System Memory Interface	1		PADZZN
-5	M38510/30005BCB	81349	• • • INTEGRATED CIRCUIT, ... U10, Triple 3 input NAND	1		PADZZN
-6	DTZ-15	71590	• • • CAPACITOR, C1, C2, ... Ceramic, 15 pf, Non Polarized, ±5%	2		PADZZN
-7	08487	23386	• • • CRYSTAL, Y1, ... 2 MHz	1		PADZZN
-8	M38510/30702BEB	49956	• • • INTEGRATED CIRCUIT, ... U3, Decoder, Demultiplexer	1		PADZZN
-9	M38510/31004BEA	81349	• • • INTEGRATED CIRCUIT, ... U4, octal, 3 state transceiver	1		PADZZN
-10	08449	23386	• • • INTEGRATED CIRCUIT, ... U5, U6, U14, Firmware, EPROM, ROM, 1 set of 3	1		PAOZZN
-11	A23-2023Z	K1935	• • • SOCKET, XU5, XU6, ... XU14, integrated circuit	3		PADZZN
-12	M38510/30301BCB	81349	• • • INTEGRATED CIRCUIT, ... U11, Quad 2 input NOR	1		PADZZN
-13	M38510/3003BCB	81349	• • • INTEGRATED CIRCUIT, ... U12, Hex inverter	1		PADZZN
-14	SN74S374N	01295	• • • INTEGRATED CIRCUIT, ... U13, octal tri state D flip flop	1		PADZZN
-15	DS2SD	24446	• • • BATTERY, BT1, Nickel ..... Cadmium, 2.4 VDC	1		PAFZZN
-16	PS101L	34649	• • • INTEGRATED CIRCUIT, ... U7, U8, Random access memory	2		PADZZN
-17	RL07S103G	81349	• • • RESISTOR, R3, R8, ... Fixed Film, 10K ohms, ±2%, ¼ watt	2		PADZZN

FIGURE 7-8. MICROCOMPUTER ASSEMBLY, CIRCUIT CARD, A6A2 (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-8-						
-18	CY15C102M	71590	• • • CAPACITOR, C15, ... Ceramic, 0.001 uf, 50 WVDC, ±20%	1		PADZZN
-19	RL07S333G	81349	• • • RESISTOR, R10, R15, ... Fixed Film, 33K ohms, ±2%, ¼ watt	2		PADZZN
-20	RL07S104G	81349	• • • RESISTOR, R14,.......... Fixed Film, 100K ohms, ±2%, ¼ watt	1		PADZZN
-21	TIS74	01295	• • • TRANSISTOR, Q6, ... Q7, Field effect	2		PADZZN
-22	2N3904	04713	• • • TRANSISTOR, Q2, Q3, ... Q5, Low Power, NPN	3		PADZZN
-23	2N3906	04713	• • • TRANSISTOR, Q1, Q4, ... Low Power, PNP	2		PADZZN
-24	RL07S473G	81349	• • • RESISTOR, R4, R12,....... Fixed Film, 47K ohms, ±2%, ¼ watt	2		PADZZN
-25	RLR07C100GR	81349	• • • RESISTOR, R13,.......... Fixed Film, 10 ohms, ±2%, ¼ watt	1		PADZZN
-26	T362A685M035AS	31433	• • • CAPACITOR, C17, ... Tantalum, 15 uf, 20 WVDC, ±20%	1		PADZZN
-27	RL07S271G	81349	• • • RESISTOR, R9, Fixed ...... Film, 270 ohms, ±2%, ¼ watt	1		PADZZN
-28	JAN1N270	81349	• • • DIODE, CR3, ... Germanium	1		PADZZN
-29	T210A475M010MS	31433	• • • CAPACITOR, C16, ... Tantalum, 4.7 uf, 10 WVDC, ±20%	1		PADZZN
-30	1N916B	07623	• • • DIODE, CR2, CR4, ... CR5, CR6	4		PADZZN
-31	JAN1N752A	81349	• • • DIODE, CR1,. .... Zener, 5.6 volts	1		PADZZN
-32	RL07S102G	81349	• • • RESISTOR, R1, R7,........ Fixed Film, 1K ohms, ±2%, ¼ watt	2		PADZZN
-33	RL07S470G	81349	• • • RESISTOR, R11,.......... Fixed Film, 47 ohms, ±2%, ¼ watt	1		PADZZN
-34	RL07S393G	81349	• • • RESISTOR, R2, ... Fixed Film, 39K ohms, ±2%, ¼ watt	1		PADZZN
-35	RL07S124G	81349	• • • RESISTOR, R5, ... Fixed Film, 120K ohms, ±2%, ¼ watt	1		PADZZN

FIGURE 7-8. MICROCOMPUTER ASSEMBLY, CIRCUIT CARD, A6A2 (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-8-						
-36	RL07S823G	81349	• • • RESISTOR, R6, ... Fixed Film, 82K ohms, ±2%, ¼ watt	1		PADZZN
-37	LM78L1ZAWC	27014	• • • INTEGRATED CIRCUIT, ... U9, +12 volt regulator	1		PADZZN
-38	T362A685M035AS	31433	• • • CAPACITOR, C13, C14, ... Tantalum, 6.8 uf, 35 WVDC, ±20%	2		PADZZN
-39	3431-2002	75037	• • • CONNECTOR, J1, ... 34 pin	1		PADZZN

NOTE: Refer to Parts List for differences in the R-2174A Receiver.

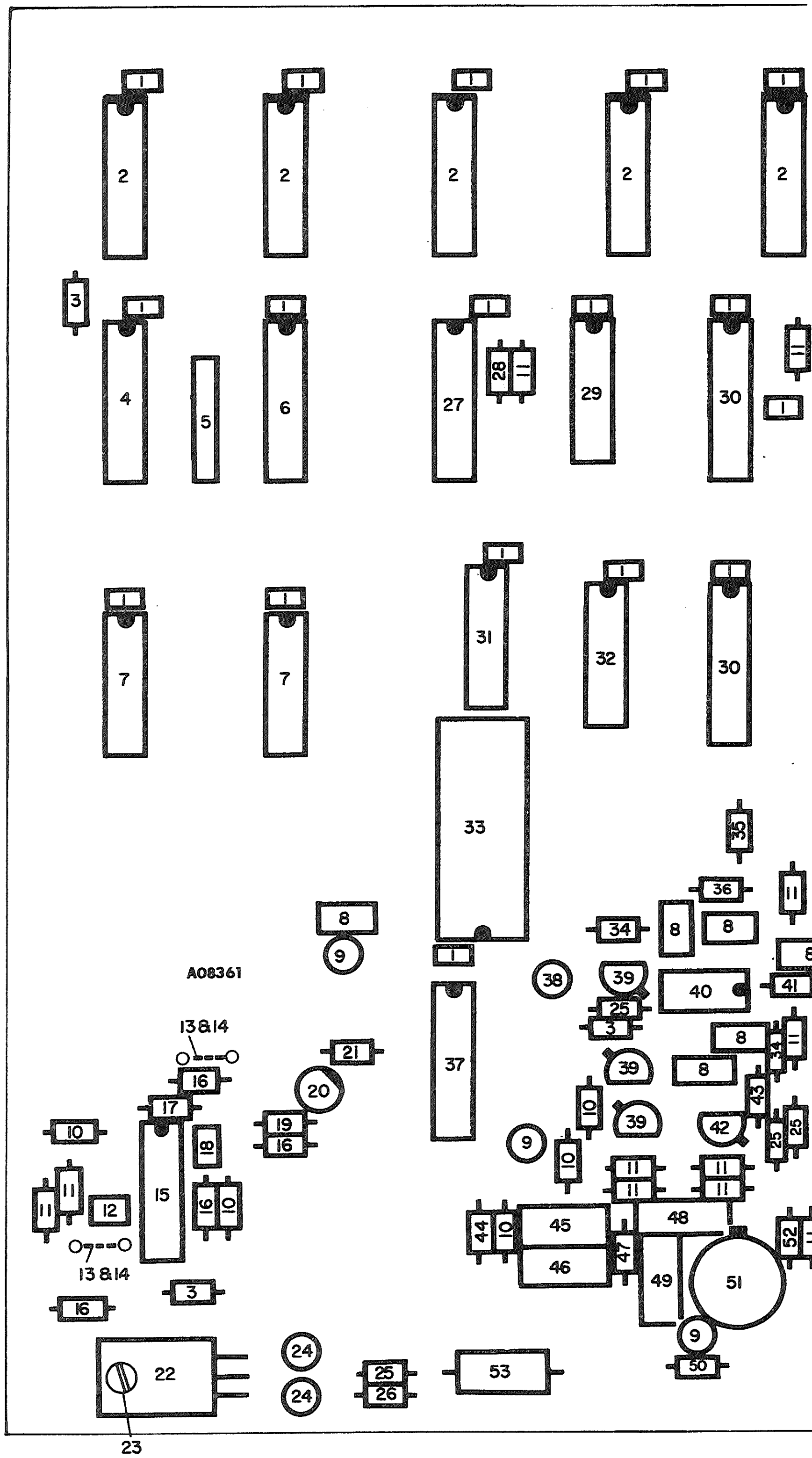


Figure 7-9. First L.O. Synthesizer Assembly, Circuit Card, A7 (Sheet 1 of 2)

FIGURE 7-9. FIRST L.O. SYNTHESIZER ASSEMBLY, CIRCUIT CARD, A7

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-9	08361	23386	• FIRST LOCAL OSCILLATOR... SYNTHESIZER ASSEMBLY, Circuit Card, A7	1		PAOLDT
7-9	09134	23386	• FIRST LOCAL OSCILLATOR... SYNTHESIZER ASSEMBLY, Circuit Card, A7	1	A	PAOLDT
/1,2-1	C320C103M1U1C1	31433	• • CAPACITOR, C5, C7, C9, C11, C13 thru C34, C39, C44, C47, C48, C55, C85, Ceramic, 0.01 uf, 100 WVDC, ± 20%	32		PADZZN
/1,2-2	CD4094BEX	02735	• • INTEGRATED CIRCUIT,..... U8 thru U14, 8 bit register,shift and store	7		PADZZN
/1,2-3	RL07S103G	81349	• • RESISTOR, R3, R50, R62, R73, R81, R82, R83,Fixed Film, 10K ohm, ± 2%, 1/4 Watt	7		PADZZN
/1-4	CD40174BCN	27014	• • INTEGRATED CIRCUIT,U18,. Hex D flip flop	1		PADZZN
/1-5	750-61-10K	32997	• • INTEGRATED CIRCUIT,U16, Transistor Array,10K ohm 6 pin	1		PADZZN
/1-6	N82S83N	18324	• • INTEGRATED CIRCUIT,U15,. 4 bit BCD adder	1		PADZZN
/1-7	M38510/05701BCB	81349	• • INTEGRATED CIRCUIT,U20,. U21, 18 bit static shift register	2		PADZZN
/1,2-8	MS39014101-1593	81349	• • CAPACITOR, C35, C37,.... C42, C51, C59, C62 thru C77, C93, C96, Ceramic, 0.1 uf, 100 WVDC, ± 20%	23		PADZZN
/1,2-9	T362A685M035AS	31433	• • CAPACITOR, C1 thru C4,.. C6, C8, C12, C36, C38, C45, C46, C49, C50, C57, C60, C61, C79, C83, C84, C94, Tantalum, 6.8 uf, 35 WVDC, ± 20%	20		PADZZN
/1,2-10	RL07S332G	81349	• • RESISTOR, R53, R54, R59. R69, R84, Fixed Film,3.3 K ohms, ± 2%, 1/4 Watt	5		PADZZN
/1,2-11	1N916B	07623	• • DIODE, CR1, CR2, CR5.... thru CR16, CR19, CR20,.. Silicon	16		PADZZN
/1-12	C312C222M1U1CA	31433	• • CAPACITOR, C90, Ceramic. 2200 pf, 100 WVDC, ± 20%	1		PADZZN
/1-13	MIL-W-3861/S-24	81349	• • WIRE, Buss No. 24.......	AR		PAOZZN
/1-14	MIL-I-22129C-24	81349	• • TUBING, PTFE No. 24.....	AR		PAOZZN
/1-15	CA339E	02735	• • INTEGRATED CIRCUIT, U34 Quad Voltage Comparator	1		PADZZN

FIGURE 7-9. FIRST L.O. SYNTHESIZER ASSEMBLY, CIRCUIT CARD, A7 (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-9- /1, 2-16	RL07S102G	81349	• • RESISTOR, R25, R61, ... R63, R68, R70, R90, R95, R97, Fixed Film, 1K ohms, ±2%, ¼ watt	8		PADZZN
/1-17	RL07S154G	81349	• • RESISTOR, R80, Fixed . . . . Film, 150K ohms, ±2%, ¼ watt	1		PADZZN
/1-18	C320C473M5U1CA	31433	• • CAPACITOR, C89, Ceramic, ... 0.047 uf, 100 WVDC, ±20%	1		PADZZN
/1-19	RL07S104G	81349	• • RESISTOR, R77, ... Fixed Film, 100K ohms, ±2%, ¼ watt	1		PADZZN
/1-20	RJR50FP201	81349	• • RESISTOR, R5, Variable, ... 200 ohms	1		PADZZN
/1, 2-21	RL07S151G	81349	• • RESISTOR, R4, R91, ... Fixed Film, 150 ohms, ±2%, ¼ watt	2		PADZZN
/1-22	MC7812CT	04713	• • INTEGRATED CIRCUIT, ... U39, +12 volt regulator	1		PADZZN
/1-23	MS35649-44	81349	• • NUT, Hex, 4-40 (AP)	1		PAOZZN
	MS35338-78	81349	• • WASHER, Split Lock, ... No. 4 (AP)	1		PAOZZN
	MS15795-303	96906	• • WASHER, Flat, No. 4 (AP)	1		PAOZZN
	MS35233-14	96906	• • SCREW, Machine, ... Pan Head, 4-40 x 5/16 (AP)	1		PAOZZN
/1-24	T362A105M035AS	31433	• • CAPACITOR, C86, C87, ... Tantalum, 1 uf, 35 WVDC, ±10%	2		PADZZN
/1, 2-25	RL07S471G	81349	• • RESISTOR, R24, R34, ... R35, R38, R40 thru R44, R46, R48, R49, R55, R58, R86, Fixed Film, 470 ohms, ±2%, ¼ watt	15		PADZZN
/1-26	JAN1N757A	81349	• • DIODE, CR18, ... Zener, 9.1 volts	1		PADZZN
/1-27	CD4503BD/883	27014	• • INTEGRATED CIRCUIT, ... U2, Hex 3 state buffer	1		PADZZN
/1, 2-28	RL07S473G	81349	• • RESISTOR, R1, R87, R89, ... Fixed Film, 47K ohms, ±2%, ¼ watt	3		PADZZN
/1-29	CD4070BCN	27014	• • INTEGRATED CIRCUIT, ... U7, Quad exclusive OR gate	1		PADZZN
/1, 2-30	M38510/30106BEB	81349	• • INTEGRATED CIRCUIT, ... U3, U5, U6, 6 bit D flip flop	3		PADZZN
/1-31	M38510/30102BCB	81349	• • INTEGRATED CIRCUIT, ... U19, Dual D flip flop	1		PADZZN

FIGURE 7-9. FIRST L.O. SYNTHESIZER ASSEMBLY, CIRCUIT CARD, A7 (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-9-						
/1-32	M38510/30301BCB	81349	• • INTEGRATED CIRCUIT, ... U4, Quad 2 input NOR gate	1		PADZZN
/1-33	CD40108BEX	02735	• • INTEGRATED CIRCUIT, ... U22, 4 x 4 multiport register	1		PADZZN
/1, 2-34	RL07S222G	81349	• • RESISTOR, R17, R52, ... R56, Fixed Film, 2.2K ohms, ±2%, ¼ watt	3		PADZZN
/1, 2-35	RL07S821G	81349	• • RESISTOR, R15, R30, ... R33, R37, R47, Fixed Film, 820 ohms, ±2%, ¼ watt	5		PADZZN
/1-36	RL07S472G	81349	• • RESISTOR, R51, ... Fixed Film, 4.7K ohms, ±2%, ¼ watt	1		PADZZN
/1-37	DAC20CQ	31148	• • INTEGRATED CIRCUIT, ... U23, Digital to analog converter	1		PADZZN
/1, 2-38	T362C336M025AS	31433	• • CAPACITOR, C41, C56, ... Tantalum, 33 uf, 25 WVDC, ±10%	2		PADZZN
/1, 2-39	MIL-S-19500/291B	81349	• • TRANSISTOR, Q6, Q7, ... Q8, Q11, Silicon, PNP, ZN4126	4		PADZZN
/1-40	LM145BN	27014	• • INTEGRATED CIRCUIT, ... U33, Dual operational amplifier	1		PADZZN
/1-41	RL07S563G	81349	• • RESISTOR, R45, ... Fixed Film, 56K ohms, ±2%, ¼ watt	1		PADZZN
/1, 2-42	JANTX2N2222A	81349	• • TRANSISTOR, Q9, Q10, ... Low power, NPN, 2N4124	2		PADZZN
/1-43	RL07S392G	81349	• • RESISTOR, R57, Fixed . . . . Film, 3.9K ohms, ±2%, ¼ watt	1		PADZZN
/1, 2-44	RL07S123G	81349	• • RESISTOR, R67, R79, ... Fixed Film, 12K ohms, ±2%, ¼ watt	2		PADZZN
/1-45	CMR05E270G0DR	81349	• • CAPACITOR, C80, ... Mica, 27 pf, 100 WVDC, ±5%	1		PADZZN
/1-46	CMR05F101G0DR	81349	• • CAPACITOR, C78, ... Mica, 100 pf, 100 WVDC, ±5%	1		PADZZN
/1, 2-47	RL07S220G	81349	• • RESISTOR, R9, R22, ... R60, Fixed Film, 22 ohms, ±2%, ¼ watt	3		PADZZN

NOTE: Refer to Parts List for differences in the R-2174A Receiver.

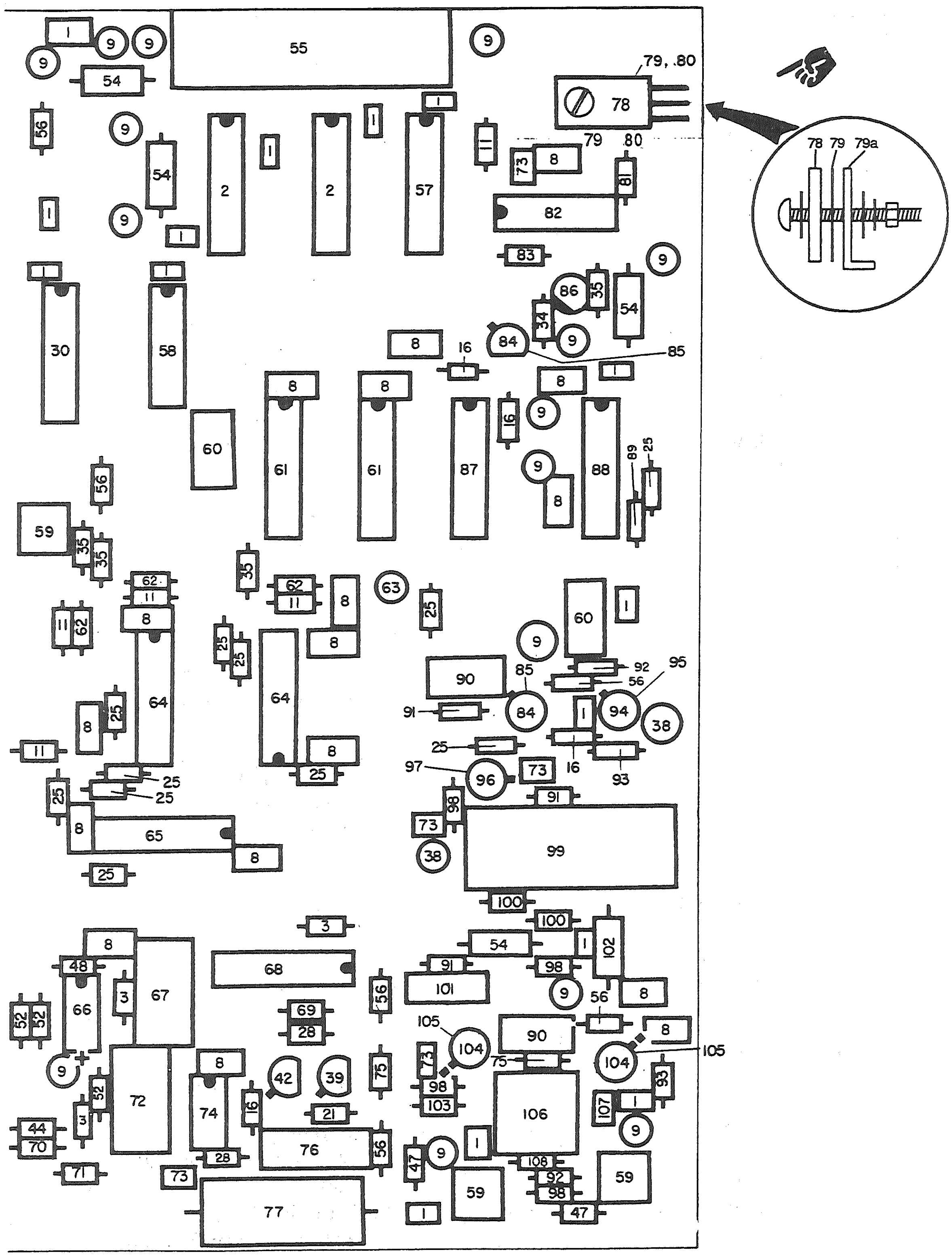


Figure 7-9. First L.O. Synthesizer Assembly, Circuit Card, A7 (Sheet 2 of 2)

FIGURE 7-9. FIRST L.O. SYNTHESIZER ASSEMBLY, CIRCUIT CARD, A7 (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-9-						
/1-48	652A1E102J	14752	• • CAPACITOR, C81, ... Polyester, 0.001 uf, 400 WVDC, ±10%	1		PADZZN
/1-49	C280MCH/A47K	30983	• • CAPACITOR, C82, ... Polycarbonate, 0.047 uf, 100 WVDC, ±10%	1		PADZZN
/1-50	RL07S393G	81349	• • RESISTOR, R64,........... Fixed Film, 39K ohms, ±2%, ¼ watt	1		PADZZN
/1-51	AD518JH883B	24355	• • INTEGRATED CIRCUIT,...... U35, Operational amplifier analog devices	1		PADZZN
/1, 2-52	RL07S153G	81349	• • RESISTOR, R65, R74 .... thru R76, Fixed Film, 15K ohms, ±2%, ¼ watt	4		PADZZN
/1-53	CS13BE156M	81349	• • CAPACITOR, C88, ... Tantalum, 15 uf, 20 WVDC, ±20%	1		PADZZN
/2-54	LT10K129	81349	• • CHOKE, L1 thru L4, ... Fixed RF, 6.8 uH, ±10%	4		PADZZN
/2-55	3492-1002	75037	• • CONNECTOR, J1, PCB, ... Right angle, 20 way	1		PADZZN
/2-56	RLR07C100GR	81349	• • RESISTOR, R2, R12, ... R28, R72, R92, R94, Fixed Film, 10 ohms, ±2%, ¼ watt	6		PADZZN
/2-57	M38510/054-01BEA	81349	• • INTEGRATED CIRCUIT,...... U17, 4 bit full adder	1		PADZZN
/2-58	M38510/05202BCB	81349	• • INTEGRATED CIRCUIT,...... U1, Quad 2 input NOR gate	1		PADZZN
/2-59	051-351-0000-220	98291	• • CONNECTOR, J2, J3, ... J7, PCB, Coax, SMB, male	3		PADZZN
/2-60	CMR05E470G0DR	81349	• • CAPACITOR, C103,.......... C104, Mica, 47 pf, 500 WVDC, ±5%	2		PADZZN
/2-61	M38510/31505BEA	81349	• • INTEGRATED CIRCUIT,...... U30, U31, Decode up-down counter	2		PADZZN
/2-62	RL07S221G	81349	• • RESISTOR, R31, R32,........ R36, Fixed Film, 220 ohms, ±2%, ¼ watt	3		PADZZN
/2-63	T362C157K006AS	31433	• • CAPACITOR, C53, ... Tantalum, 150 uf, 6 WVDC, ±20%	1		PADZZN
/2-64	F10231PC	07263	• • INTEGRATED CIRCUIT,...... U26, U28, Dual D flip flop	2		PADZZN

FIGURE 7-9. FIRST L.O. SYNTHESIZER ASSEMBLY, CIRCUIT CARD, A7 (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-9-						
/2-65	F10211PC	07263	• • INTEGRATED CIRCUIT, ... U32, Dual NOR gate	1		PADZZN
/2-66	LM1458N	27014	• • INTEGRATED CIRCUIT, ... U37, Dual operational amplifier	1		PADZZN
/2-67	CM06FD472JN3	81349	• • CAPACITOR, C91, Mica, ... 4700 pf, 100 WVDC, ±5%	1		PADZZN
/2-68	AD201A	24355	• • INTEGRATED CIRCUIT, ... U36, Analog switch	1		PADZZN
/2-69	RL07S124G	81349	• • RESISTOR, R88, ... Fixed Film, 120K ohms, ±2%, ¼ watt	1		PADZZN
/2-70	RL07S822G	81349	• • RESISTOR, R66, Fixed . . . . Film, 8.2K ohms, ±2%, ¼ watt	1		PADZZN
/2-71	RL07S272G	81349	• • RESISTOR, R78, Fixed . . . . Film, 2.7K ohms, ±2%, ¼ watt	1		PADZZN
/2-72	CMR05F222G0DR	81349	• • CAPACITOR, C92, ... Mica, 2200 pf, 100 WVDC, ±5%	1		PADZZN
/2-73	CY15C102M	71590	• • CAPACITOR, C40, C43, ... C52, C54, C95, Ceramic, 0.001 uf, 100 WVDC, ±20%	5		PADZZN
/2-74	CA3140BT/3	32293	• • INTEGRATED CIRCUIT, ... U40, Operational amplifier	1		PADZZN
/2-75	RL07S681G	81349	• • RESISTOR, R11, R93, ... Fixed Film, 680 ohms, ±2%, ¼ watt	2		PADZZN
/2-76	C280MCH/A1M	30983	• • CAPACITOR, C97, ... Polycarbonate, 1.0 uf, 100 WVDC, ±10%	1		PADZZN
/2-77	MKC-1860-533/06	52763	• • CAPACITOR, C98, ... Polycarbonate, 3.3 uf, 63 WVDC, ±10%	1		PADZZN
/2-78	2N4921	04713	• • TRANSISTOR, Q4, ... High Power, NPN, 2N4921	1		PADZZN
/2-79	08670	23386	• • WASHER, Q4,. . . . . Insulator,modified	1		MOOZZN
/2-79a	08707	23386	• • MOUNTING BRACKET, ...	1		PADZZN
/2-80	120-5	05820	• • COMPOUND, Thermal, ... Wakefield No. 128	AR		PAOZZN
/2-81	RL07S470G	81349	• • RESISTOR, R18,. . . . . Fixed Film, 47 ohms, ±2%, ¼ watt			PADZZN

FIGURE 7-9. FIRST L.O. SYNTHESIZER ASSEMBLY, CIRCUIT CARD A7(Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-9						
/2-82	M38510/10201BEA	81349	• • INTEGRATED CIRCUIT,.... U24, Voltage regulator	1		PADZZN
/2-83	SK2-1/4-1ROJ	52783	• • RESISTOR, R19,......... Composition, 1 ohm, 5%, 1/4 Watt	1		PADZZN
/2-84	JAN2N2369A	81349	• • TRANSISTOR, Q5, Q13, Silicon, NPN, 2N2369	2		PADZZN
/2-85	69011-1058	78912	• • PAD,Transistor,Q5,Q13,.	2		PADZZN
/2-86	RLO7S501G	81349	• • RESISTOR,R16,Variable, 500 ohms	1		PADZZN
/2-87	M38510/31506BEA	81349	• • INTEGRATED CIRCUIT,.... U29, Binary up-down counter	1		PADZZN
/2-88	11C90DCQR	07263	• • INTEGRATED CIRCUIT,.... U27, Divider	1		PADZZN
/2-89	RLO7S820G	81349	• • RESISTOR, R71, Fixed... Film, 82 ohm, ± 2%, 1/4 Watt	1		PADZZN
/2-90	CMR05D100G0DR	81349	• • CAPACITOR, C58, C101,.. Mica, 10 pf., 500 WVDC, ± 1/2 pf	2		PADZZN
/2-90a	CMR05E820G0DR	81349	• • CAPACITOR, C101, Mica,. 82 pf, ± 2%, 500 WVDC	1	A	PADZZN
/2-91	RLO7S101G	81349	• • RESISTOR, R6, R29, R85, Fixed Film, 100 ohms, ± 2%, 1/4 Watt	3		PADZZN
/2-92	RLO7S331G	81349	• • RESISTOR, R21, R27,.... Fixed Film, 330 ohms, ± 2%, 1/4 Watt	2		PADZZN
/2-93	RLO7S152G	81349	• • RESISTOR, R10, R26,.... Fixed Film, 1.5K ohms,± 2%, 1/4 Watt	2		PADZZN
/2-94	JAN2N918	81349	• • TRANSISTOR,Q12,Silicon, Low Power, NPN	1		PADZZN
/2-95	69011-1058	78912	• • PAD, Transistor, Q12,..	1		PADZZN
/2-96	MIL-S-19500/428	81349	• • TRANSISTOR, Q1, Field.. effect	1		PADZZN
/2-97	69011-1058	78912	• • PAD, Transistor, Q1....	1		PADZZN
/2-98	RLO7S680G	81349	• • RESISTOR, R7, R8, R14,. R23, Fixed Film, 68 ohms, ± 2%, 1/4 Watt	4		PADZZN
/2-99	08304	23386	• • COIL ASSEMBLY, L5,Local oscillator, air wound	1		PADZZN
/2-99a	09255	23386	• • COIL ASSEMBLY, L5,Local oscillator, air wound	1	A	PADZZN
/2-100	DKV6522B	52673	• • DIODE, CR3, CR4,....... Varactor	2		PADZZN

FIGURE 7-9 FIRST L.O. SYNTHESIZER ASSEMBLY, CIRCUIT CARD, A7 (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-9						
/2-101	C280MCH/A68K	30983	• • CAPACITOR, C99,....... Polycarbonate, 0.068 uf, 100 WVDC, ± 10%	1		PADZZN
/2-102	LT10K133	81349	• • CHOKE, L6, Fixed RF,.. 15 uH, ± 10%	1		PADZZN
/2-103	RL07S391G	81349	• • RESISTOR, R13, Fixed.. Film, 390 ohms, ± 2%, 1/4 Watt	1		PADZZN
/2-104	MRF 517	81349	• • TRANSISTOR, Q2, Q3,... High Power, NPN	2		PADZZN
/2-105	N88026	17069	• • PAD, Transistor, Q2,.. Q3	2		PADZZN
/2-106	08502-1	23386	• • TRANSFORMER, T1,...... Wideband	1		PADZZN
/2-107	C312C479K2G5CA	31433	• • CAPACITOR, C100,...... Ceramic, 4.7 pf	1		PADZZN
/2-108	RLR07C390GR	81349	• • RESISTOR, R20, Fixed.. Film, 39 ohms, ± 2%, 1/4 Watt	1		PADZZN

NOTE: Refer to Parts List for differences in the R-2174A Receiver.

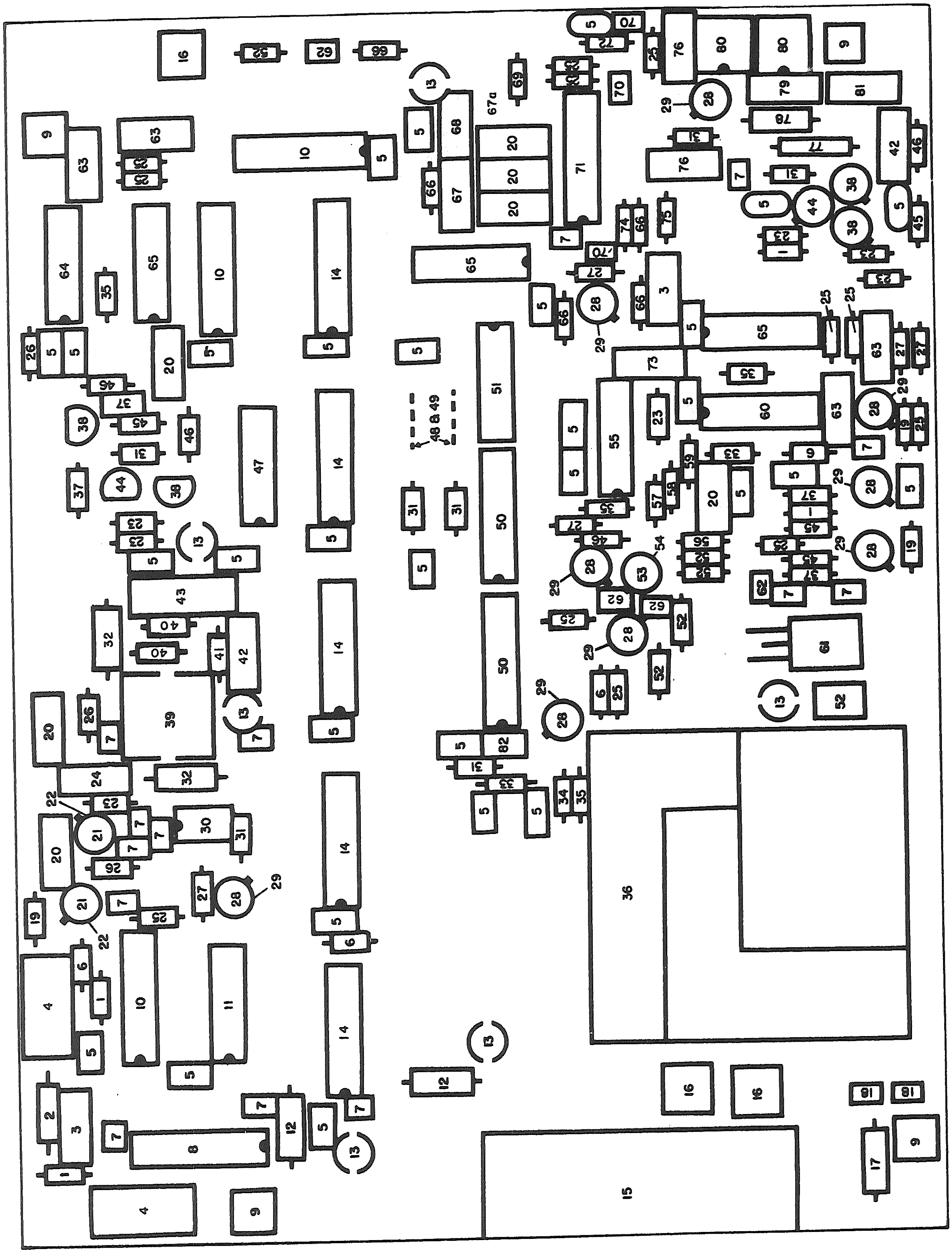


Figure 7-10. Second L.O./BFO Synthesizer Assembly, Circuit Card, A8

FIGURE 7-10. SECOND LOCAL OSCILLATOR SYNTHESIZER ASSEMBLY, CIRCUIT CARD, A8

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-10	08387	23386	• SECOND LOCAL OSCILLATOR... SYNTHESIZER ASSEMBLY, Circuit Card, A8	1		PAOLDT
7-10	09632	23386	• SECOND LOCAL OSCILLATOR... SYNTHESIZER ASSEMBLY, Circuit Card, A8	1	A	PAOLDT
-1	RL07S821G	81349	• • RESISTOR, R22, R35,..... R76, R77, Fixed Film, 820 ohms, + 2%, 1/4 Watt	4		PADZZN
-2	LT10K020	81349	• • INDUCTOR, L6, RF, 220... uH, + 10%	1		PADZZN
-3	CMR05F151GODR	81349	• • CAPACITOR, C28, C64,.... Mica, 150 pf, 500 WVDC,. + 2%	2		PADZZN
-4	CM06FD821JN3	81349	• • CAPACITOR, C63, C65,.... Mica, 820 pf, 500 WVDC,. + 5%	2		PADZZN
-5	MS39014101-1593	81349	• • CAPACITOR, C3, C4, C9,.. C11, C12, C13, C15 thru C19, C21, C22, C24, C27, C30, C39, C43, C44, C45, C47, C48, C62, C66 thru C71, C73, C74, C75, Ceramic, 0.1 uf, 50 WVDC + 20%	32		PADZZN
-6	RL07S331G	81349	• • RESISTOR, R11, R27, R69 R70, Fixed Film,330 ohm + 2%, 1/4 Watt	4		PADZZN
-6a	Not Used		• • R70	1	A	
-7	C320C103M1U1C1	31433	• • CAPACITOR, C5, C8, C14, C32, C42, C52, C53, C58 thru C61, C72, C78, C80, Cer., 0.01 uf, 50 WVDC + 20%	14		PADZZN
-8	11C90DCQR	07263	• • INTEGRATED CIRCUIT, U19. Divide by 10/11, Prescaler	1		PADZZN
-9	051-351-0000-220	98291	• • CONNECTOR, J1 thru J4,.. SMB, Push on	4		PADZZN
-10	M38510/3031BCB	81349	• • INTEGRATED CIRCUIT, U8,. U9, U20, Dual decade counter	3		PAOODT
-11	M38510/30301BCB	81349	• • INTEGRATED CIRCUIT,..... U12, Quad 2 NOR gate	1		PADZZN
-12	LT10K128	81349	• • INDUCTOR, L7, L8, RF,... 5.6 uH, + 10%	2		PADZZN
-13	T362A685M035AS	31433	• • CAPACITOR, C1, C23, C49. C54, C79, C81, Tantalum, 6.8 uf, 35 WVDC, + 20%	6		PADZZN
-14	M38510/31503BEA	81349	• • INTEGRATED CIRCUIT, U14. thru U18,Synchronous 4 bit counter	5		PADZZN

FIGURE 7-10. SECOND LOCAL OSCILLATOR SYNTHESIZER ASSEMBLY, CIRCUIT CARD, A8(Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-10						
-15	3429-1002	75037	• • CONNECTOR, J5, Control/ Power,right angle,26 pin	1		PADZZN
-16	Not Used		• • CONNECTOR, J6, J7, J8,.. Not Used	3		
-16a	051-351-0000-220	98291	• • CONNECTOR, J8, SMB,..... Push on	1	A	PADZZN
-17	LT10K012	81349	• • INDUCTOR, L1, RF, 100... uH, ± 10%	1		PADZZN
-18	C320C473M5U1CA	31433	• • CAPACITOR, C6, C7,...... Ceramic, 0.047 uf, 50 WVDC, ± 20%	2		PADZZN
-19	RL07S182G	81349	• • RESISTOR, R19, R21,..... R75, Fixed Film, 1.8K ohms, ± 2%, 1/4 Watt	3		PADZZN
-20	CMR05F101GODR	81349	• • CAPACITOR, C2, C34,..... C35, C37, C46, C56, C57, Mica, 100 pf, 500 WVDC, ± 5%	7		PADZZN
-21	MIL-S-19500/428	81349	• • TRANSISTOR, Q18, Q19,... Field effect	2		PADZZN
-22	7717-HWHT	13103	• • PAD, Transistor, Q18,... Q19	2		PADZZN
-23	RL07S681G	81349	• • RESISTOR, R6, R33, R34.. R38, R59, R63, R67,Fixed Film, 68 ohms, ± 2%, 1/4 Watt	7		PADZZN
-24	CMR05E560GODR	81349	• • CAPACITOR, C55, Mica,... 56 pf, 500 WVDC, ± 5%	1		PADZZN
-25	RL07S102G	81349	• • RESISTOR, R10, R13, R23 R41, R43, R44, R45, R48, R49, R54, R57, R58, R74, R84, Fixed Film, 1K ohm, ± 2%, 1/4 Watt	14		PADZZN
-26	RLR07C564GR	81349	• • RESISTOR, R66, R68,..... Fixed Film, 560K ohms, ± 2%, 1/4 Watt	2		PADZZN
-27	RL07S472G	81349	• • RESISTOR, R7, R24, R25, R72, Fixed Film, 4.7K ohms, ± 2%, 1/4 Watt	4		PADZZN
-28	JAN2N2369A	81349	• • TRANSISTOR, Q1 thru Q6, Q10, Q11, Q20, Switching NPN	9		PADZZN
-29	7717-HWHT	13103	• • PAD, Transistor, Q1..... thru Q6, Q10, Q11, Q20	9		PADZZN
-30	4N28	07263	• • INTEGRATED CIRCUIT,..... U21, opto isolator	1		PADZZN
-30a	Not Used		• • INTEGRATED CIRCUIT,..... U21, opto isolator	1	A	PADZZN

FIGURE 7-10. SECOND LOCAL OSCILLATOR SYNTHESIZER ASSEMBLY, CIRCUIT CARD, A8 (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-10-						
-31	RL07S103G	81349	• • RESISTOR, R28, R29, ... R36, R47, R61, R73, R78, Fixed Film, 10K ohms, ±2%, ¼ watt	7		PADZZN
-32	LT10K138	81349	• • INDUCTOR, L3, L5, ... RF, 33 uH, ±5%	2		PADZZN
-33	RLR07C100GR	81349	• • RESISTOR, R12, R26, ... Fixed Film, 10 ohms, ±2%, ¼ watt	2		PADZZN
-34	RLR07C330GR	81349	• • RESISTOR, R9, Fixed. . . . . Film, 33 ohms, ±2%, ¼ watt	1		PADZZN
-35	RL07S470G	81349	• • RESISTOR, R8, R14, ... R32, R83, Fixed Film, 47 ohms, ±2%, ¼ watt	4		PADZZN
-36	08289	23386	• • OSCILLATOR, Y1, ... Oven controlled crystal	1		PADZZN
-37	1N916B	07623	• • DIODE, CR2, CR3, ... CR5, Silicon	3		PADZZN
-38	2N3904	04713	• • TRANSISTOR, Q7, Q9, ... Q15, Q17, Low power, NPN	4		PADZZN
-39	08525	23386	• • INDUCTOR, L4, ... RF, Variable	1		PADZZN
-40	MV 1650	81349	• • DIODE, CR6, CR7, ... Varicap	2		PADZZN
-41	RL07S183G	81349	• • RESISTOR, R65, ... Fixed Film, 18K ohms, ±2%, ¼ watt	1		PADZZN
-42	C280MCH/A100K	30983	• • CAPACITOR, C26, C51, ... Polycarbonate, 0.1 uf, 100 WVDC, ±20%	2		PADZZN
-43	C280MCH/A470K	30983	• • CAPACITOR, C50, ... Polycarbonate, 0.47 uf, 100 WVDC, ±20%	1		PADZZN
-44	2N4126	04713	• • TRANSISTOR, Q8, Q16, ... Low power, PNP	2		PADZZN
-45	RL07S332G	81349	• • RESISTOR, R18, R20, ... R37, R62, Fixed Film, 3.3K ohms, ±2%, ¼ watt	4		PADZZN
-46	RL07S222G	81349	• • RESISTOR, R5, R39, ... R60, R64, Fixed Film, 2.2K ohms, ±2%, ¼ watt	4		PADZZN
-47	M38510/31004BCB	27014	• • INTEGRATED CIRCUIT, ... U13, Quad 2 input AND	1		PADZZN
-48	MIL-W-3861/S-24	81349	• • WIRE, LK1, LK2, ... Links, Buss No. 24	AR		PAOZZN
-49	MIL-I-22129C-24	81349	• • TUBING, LK1, LK2, ... PTFE, No. 24	AR		PAOZZN

FIGURE 7-10. SECOND LOCAL OSCILLATOR SYNTHESIZER ASSEMBLY, CIRCUIT CARD, A8(Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-10						
-50	M38510/30901BEA	81349	• • INTEGRATED CIRCUIT,.... U4, U5, Data Selector	2		PADZZN
-51	M38510/31501BCB	81349	• • INTEGRATED CIRCUIT,.... U6, Decade Counter	1		PADZZN
-52	Not Used		• • RESISTOR, R1, R15, R16. R17, R30, R31, R56, R71 R79 thru R82, Not Used	12		-
-52a	RL07S470G	81349	• • RESISTOR, R56, Fixed... Film	1	A	PADZZN
-53	Not Used		• • TRANSISTOR, Q12, Q13,.. Q14, Q21, Not Used	4		-
-54	Not Used		• • PAD, Q12, Q13, Q14, Q21 Not Used	4		-
-55	M38510/10201BEA	81349	• • INTEGRATED CIRCUIT,.... U1, Voltage regulator	1		PADZZN
-56	IN4001	07623	• • DIODE, CR1.............	1		PADZZN
-57	SK2-1/4-1R0J	52783	• • RESISTOR, R2, Fixed.... Film, 1 ohm, ± 2%, 1/4 Watt	1		PADZZN
-58	RL07S392G	81349	• • RESISTOR, R3, Fixed.... Film, 3.9K ohms, ± 2%, 1/4 Watt	1		PADZZN
-59	RL07S682G	81349	• • RESISTOR, R4, Fixed.... Film, 6.8K ohms, ± 2%, 1/4 Watt	1		PADZZN
-60	M38510/30001BCB	81349	• • INTEGRATED CIRCUIT,.... U2, Quad 2 input NAND	1		PADZZN
-61	2N4921	04713	• • TRANSISTOR, Q22, High.. power, NPN	1		PADZZN
	B52600F003	04713	• • INSULATOR, Transistor,. Q22	1		PADZZN
-62	Not Used		• • CAPACITOR, C10, C82,... C84, C85, Not Used	4		PADZZN
-62a	CY15C102M	71590	• • CAPACITOR, C10, Ceramic 0.001 uf, 50 WVDC,± 20%	1	A	PADZZN
-63	CMR05F301G0DR	81349	• • CAPACITOR, C29, C31,... C83, C86, Mica, 39 pf, 500 WVDC, ± 2%	4		PADZZN
-64	DM74LS00NAT	27014	• • INTEGRATED CIRCUIT,.... U11, Quad input NAND	1		PADZZN
-65	M38510/30102BCA	81349	• • INTEGRATED CIRCUIT,.... U3, U7, U10, Dual D flip flop	3		PADZZN
-66	RL07S471G	81349	• • RESISTOR, R40, R42, R50 R51, R55, Fixed Film, 470 ohm, ± 2%, 1/4 Watt	5		PADZZN
-67	CMR05C5R0G0DR	81349	• • CAPACITOR, C38, Mica, 5 pf, 500 WVDC, ± 1/2 pf	1		PADZZN
-67a	CMR05C5R0G0DR	81349	• • CAPACITOR, C88, Mica, 5 pf, 500 WVDC, ± 1/2 pf	1	A	PADZZN
-68	37039	23386	• • CRYSTAL, Y2, 20 MHz....	1		PADZZN

FIGURE 7-10. SECOND LOCAL OSCILLATOR SYNTHESIZER ASSEMBLY, CIRCUIT CARD,A8 (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-10-						
-69	MIL-S-19500/383	81349	• • DIODE, CR4, ... Varicap, 22 pf	1		PADZZN
-70	CY15C102M	71590	• • CAPACITOR, C36, ... C40, C87, Ceramic, 0.001 uf, 50 WVDC, ±20%	3		PADZZN
-71	DM10115N	27014	• • INTEGRATED CIRCUIT, ... U22, Line Receiver	1		PADZZN
-72	RL07S101G	81349	• • RESISTOR, R53,. . . . . Fixed Film, 100 ohms, ±2%, ¼ watt	1		PADZZN
-73	CMR05C120G0DR	81349	• • CAPACITOR, C20, ... Mica, 12 pf, 500 WVDC, ±5%	1		PADZZN
-74	RL07S560G	81349	• • RESISTOR, R46, ... Fixed Film, 56 ohms, ±2%, ¼ watt	1		PADZZN
-75	RL07S221G	81349	• • RESISTOR, R52, Fixed . . . . Film, 220 ohms, ±2%, ¼ watt	1		PADZZN
-76	CMR05E680G0DR	81349	• • CAPACITOR, C33, C41, ... Mica, 68 pf, 500 WVDC, ±2%	2		PADZZN
-77	CS13BE335M	81349	• • CAPACITOR, C25, ... Tantalum, 3.3 uf, 15 WVDC, ±10%	1		PADZZN
-78	LT4K081	81349	• • INDUCTOR, L2, ... RF, 1 uH, ±10%	1		PADZZN
-79	CMR05E820G0DR	81349	• • CAPACITOR, C76, ... Mica, 82 pf, 500 WVDC, ±2%	1		PADZZN
-80	08522	23386	• • INDUCTOR, L9, L10, ... Variable	2		PADZZN
-81	CMR05F331G0DR	81349	• • CAPACITOR, C77, ... Mica, 330 pf, 500 WVDC, ±2%	1		PADZZN
-82	MS39014102-1419	81349	• • CAPACITOR, C75, Ceramic, ... 1 uf, 50WVDC, ±20%	1		PADZZN

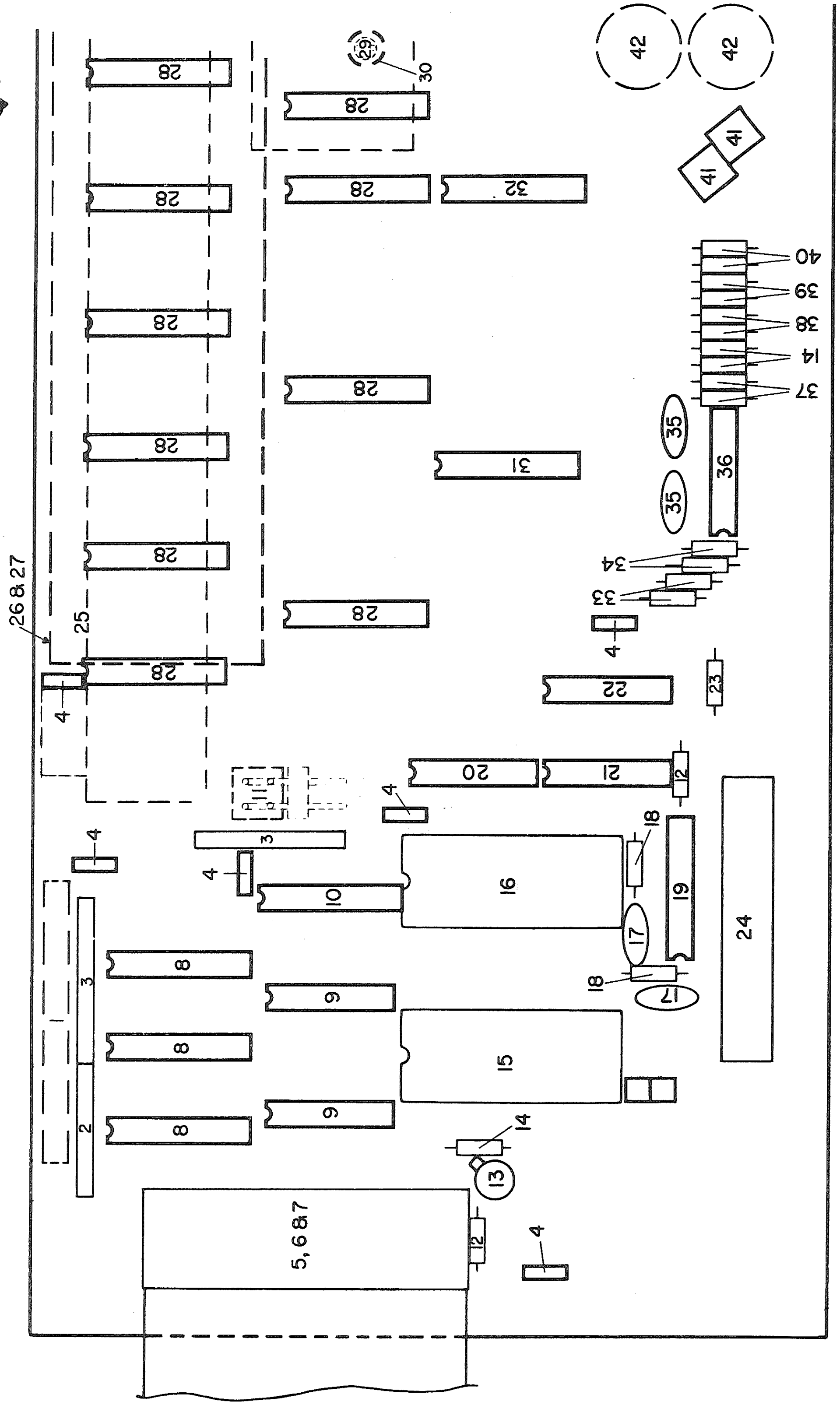


Figure 7-11. Receiver Control Assembly, Circuit Card, A9 (Sheet 1 of 2)

FIGURE 7-11. RECEIVER CONTROL ASSEMBLY, CIRCUIT CARD, A9

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-11-	08388	23386	• RECEIVER CONTROL. . . . . ASSEMBLY, Circuit Card, A9	1		PAFLDT
/1, 2-1	HBLB17S-5	09922	• • CONNECTOR, J2, J3, ... Switch Panel, 17 contact	2		PADZZN
/1, 2-2	SIP-8-103	91637	• • INTEGRATED CIRCUIT, ... U1, U5, Resistor array, 10K ohms, 7 resistors	2		PADZZN
/1, 2-3	4310R-101-103	32997	• • INTEGRATED CIRCUIT, ... U2, U6, U30, Resistor array, 10K ohms, 9 resistors	3		PADZZN
/1, 2-4	C320C103M1U1C1	31433	• • CAPACITOR, C1 thru . . . . C7, C9 thru C13, C16, C19 thru C24, Ceramic, 0.01 uf, 50 WVDC, ±20%	19		PADZZN
/1-5	08536	23386	• • CABLE ASSEMBLY, W1	1		XA
/1-6	3402-0000T	75037	• • • CONNECTOR, P1, ... 34 contact	1		XA
/1-7	3414-6034	75037	• • • CONNECTOR, ... 35 contact	1		XA
/1, 2-8	CD4503BCN	27014	• • INTEGRATED CIRCUIT, ... U7, U8, U9, U23, U24, U25, U42, U43, Hex 3 state buffer	8		PADZZN
/1-9	CD4066BEX	02735	• • INTEGRATED CIRCUIT, ... U27, U28, Quad bilateral switch	2		PADZZN
/1-10	CD4051BEMJ/883B	02735	• • INTEGRATED CIRCUIT, ... U29, 8 channel analog multiplexer	1		PADZZN
/1-11	08573	23386	• • CONNECTOR, J8, ... 4 contact	1		PADZZN
/1, 2-12	RL07S103G	81349	• • RESISTOR, R2, R6, ... R27, R28, Fixed Film, 10K ohms, ±2%, ¼ watt	4		PADZZN
/1-13	JAN2N2369A	81349	• • TRANSISTOR, Q1, ... Switching, NPN	1		PADZZN
/1-14	RL07S102G	81349	• • RESISTOR, R3, R14, R15, ... Fixed Film, 1K ohms, ±2%, ¼ watt	3		PADZZN
/1-15	MC14508BBJBS	04713	• • INTEGRATED CIRCUIT, ... U46, Dual 4 bit latch	1		PADZZN
/1, 2-16	CD4514BF/3	02735	• • INTEGRATED CIRCUIT, ... U35, U47, address decoder	2		PADZZN
/1-17	DTZ-20	71590	• • CAPACITOR, C14, C15, ... Ceramic, 20 pf, non polarized, ±5%	2		PADZZN
/1-18	RL07S333G	81349	• • RESISTOR, R4, R5,. . . . . Fixed Film 33K ohms, ±2%, ¼ watt	2		PADZZN

FIGURE 7-11. RECEIVER CONTROL ASSEMBLY, CIRCUIT CARD, A9 (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-11-						
/1-19	CD4528BF	27014	• • INTEGRATED CIRCUIT, ... U55, one shot multi-vibrator	1		PADZZN
/1-20	M38510/05204BCD	81349	• • INTEGRATED CIRCUIT, ... U48, Triple 3 input NOR gate	1		PADZZN
/1-21	CD4069UBE	02735	• • INTEGRATED CIRCUIT, ... U56, Hex inverter	1		PADZZN
/1-22	M38510/17001BCD	27014	• • INTEGRATED CIRCUIT, ... U57, Quad 2 input AND	1		PADZZN
/1-23	RL07S101G	81349	• • RESISTOR, R7, Fixed Film, ... 100 ohms, ±2%, ¼ watt	1		PADZZN
/1-24	3428-2002	70537	• • CONNECTOR, J6, ... 20 contact	1		PADZZN
/1-25	08270	23386	• • INTEGRATED CIRCUIT, ... U3, Liquid crystal display, Frequency	1		PBOZZN
/1-26	WB-11-55-G	06776	• • SOCKET, XU3A, ... 11 contact	4		XA
/1-27	WB-20-55-G	06776	• • SOCKET, XU3B, ... 20 contact	2		XA
/1, 2-28	CD4056BD	02735	• • INTEGRATED CIRCUIT, ... U10 thru U18, U31 thru U34, Display drivers, 7 segment	13		PADZZN
/1-29	HP5082-4468	28480	• • DISPLAY, DS5, ... Light emitting diode/ resistor assembly	1		PADZZN
/1-30	MIL-I-22129C-20	81349	• • SLEEVING, DS5, ...	AR		PAOZZN
/1, 2-31	CD4054BD	02735	• • INTEGRATED CIRCUIT, ... U19 thru U22, U36 thru U40, U49, Display drivers, 7 segment	10		PADZZN
/1-32	CD40N28BCN	27014	• • INTEGRATED CIRCUIT, ... U50, Decimal decoder	1		PADZZN
/1, 2-33	RL07S392G	81349	• • RESISTOR, R8, R9, ... R24, R25, Fixed Film, 3.9K ohms, ±2%, ¼ watt	4		PADZZN
/1-34	RL07S113G	81349	• • RESISTOR, R10, R11, ... Fixed Film, 11K ohms, ±2%, ¼ watt	2		PADZZN
/1-35	CK60BX101K	81349	• • CAPACITOR, C17, C18, ... Ceramic, 100 pf, non polarized, ±10%	2		PADZZN
/1-36	CA339E	02735	• • INTEGRATED CIRCUIT, ... U58, Quad voltage comparator	1		PADZZN

FIGURE 7-11. RECEIVER CONTROL ASSEMBLY, CIRCUIT CARD, A9 (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-11- /1-37	RLR07C105GR	81349	• • RESISTOR, R12, R13, ... Fixed Film, 1 meg ohms, ±2%, ¼ watt	2		PADZZN
/1-38	RL07S104G	81349	• • RESISTOR, R16, R17, ... Fixed Film, 100K ohms, ±2%, ¼ watt	2		PADZZN
/1-39	RL07S223G	81349	• • RESISTOR, R18, R19, ... R29 thru R32, Fixed Film, 22K ohms, ±2%, ¼ watt	6		PADZZN
/1-40	RL07S181G	81349	• • RESISTOR, R20, R21, ... Fixed Film, 180 ohms, ±2%, ¼ watt	2		PADZZN
/1-41	0PB706A	07374	• • INTEGRATED CIRCUIT, ... U59, U60, Optical transducer	2		PADZZN
/1-42	08473	12697	• • RESISTOR, R22, R23, ... Potentiometer, audio line, 25K ohms	2		PADZZN
/2-43	08526	23386	• • INTEGRATED CIRCUIT, ... U4, Liquid crystal display mode	1		PBOZZN
/2-44	WB-12-55-G	06776	• • SOCKET, XU4A, ... 12 contact	2		XA
/2-45	WB-14-55-G	06776	• • SOCKET, XU4B, ... 14 contact	2		XA
/2-46	3432-2002	75037	• • CONNECTOR, J5, ... IF, 40 contact	1		PADZZN
/2-47	3429-2002	75037	• • CONNECTOR, J4, J7, ... BF0, Power, 26 contact	2		PADZZN
/2-48	RL07S153G	81349	• • RESISTOR, R26, ... Fixed Film, 15K ohms, ±2%, ¼ watt	1		PADZZN
/2-49	CD4099	27014	• • INTEGRATED CIRCUIT, ... U61 thru U64, 8 bit addressable latch (Alternate: PN 1820-1665, FSCM 28480	4		PADZZN
/2-50	2N3906	04713	• • TRANSISTOR, Q2, ... Low power, PNP, 2N3906	1		PADZZN
/2-51	MS39014101-1593	81349	• • CAPACITOR, C8, ... Ceramic, 0.1 uf, 50 WVDC, ±20%	1		PADZZN
/2-52	RL07S203G	81349	• • RESISTOR, R1, ... Fixed Film, 20K ohms, ±2%, ¼ watt	1		PADZZN
/2-53	CD4047BEMJ/883B	02735	• • INTEGRATED CIRCUIT, ... U26, Monostable, Astable multivibrator	1		PADZZN

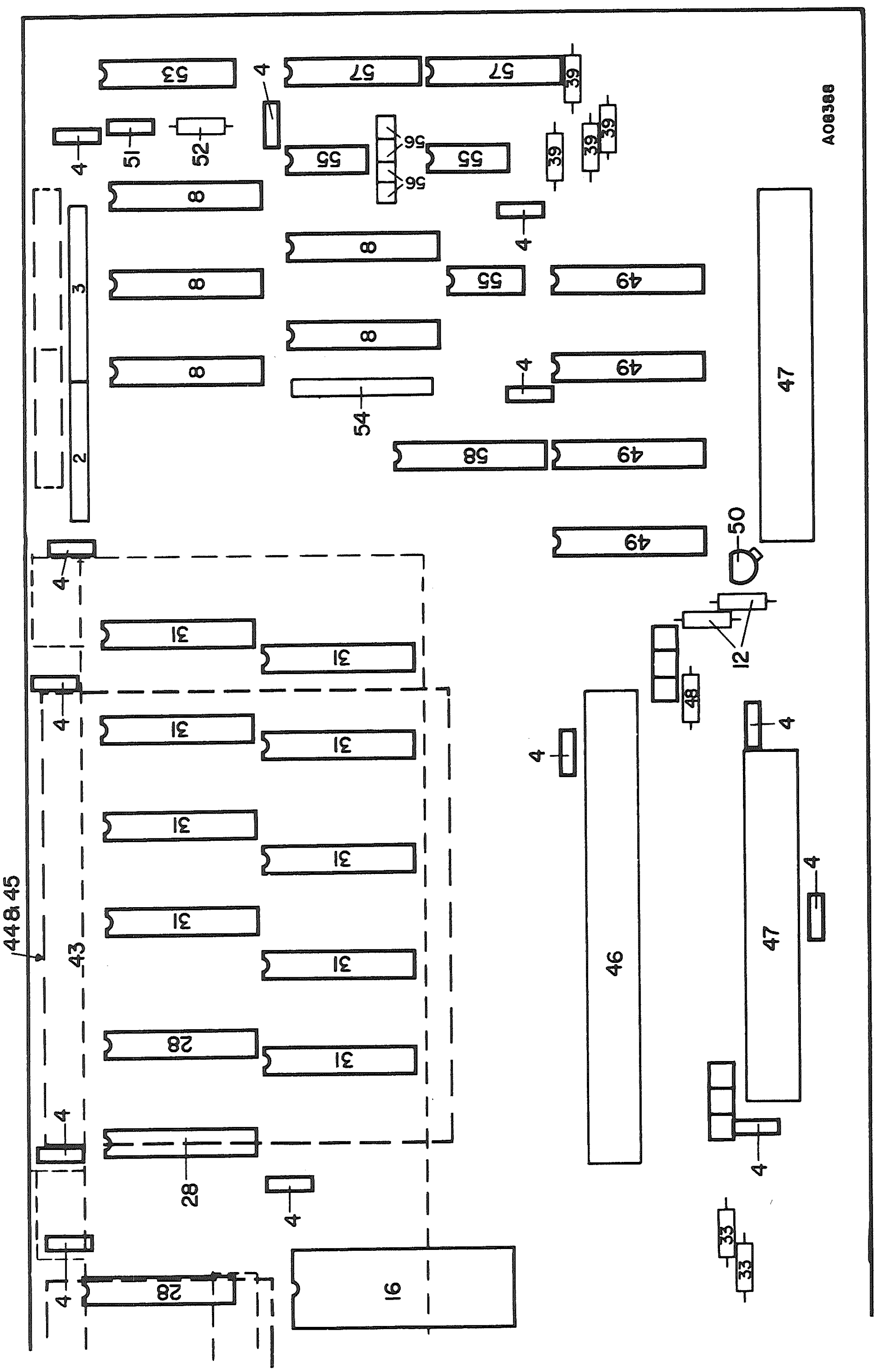


Figure 7-11. Receiver Control Assembly, Circuit Card, A9 (Sheet 2 of 2)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-11- /2-54	SIP-B-223	91637	• • INTEGRATED CIRCUIT, ... U41, Resistor array, 22K ohms, 7 resistors	1		PADZZN
/2-55	CD40107BEX	02735	• • INTEGRATED CIRCUIT, ... U44, U52, U53, Dual 2 input NAND, Buffer/ Driver	3		PADZZN
/2-56	HLMP6620	28480	• • DISPLAY, DS1 thru DS4, ... Light emitting diode/ resistor assembly	4		PADZZN
/2-57	M38510/05101BEA	81349	• • INTEGRATED CIRCUIT, ... U45, U54, flip flop	2		PADZZN
/2-58	CD4516BCN	27014	• • INTEGRATED CIRCUIT, ... U51, Divider	1		PADZZN

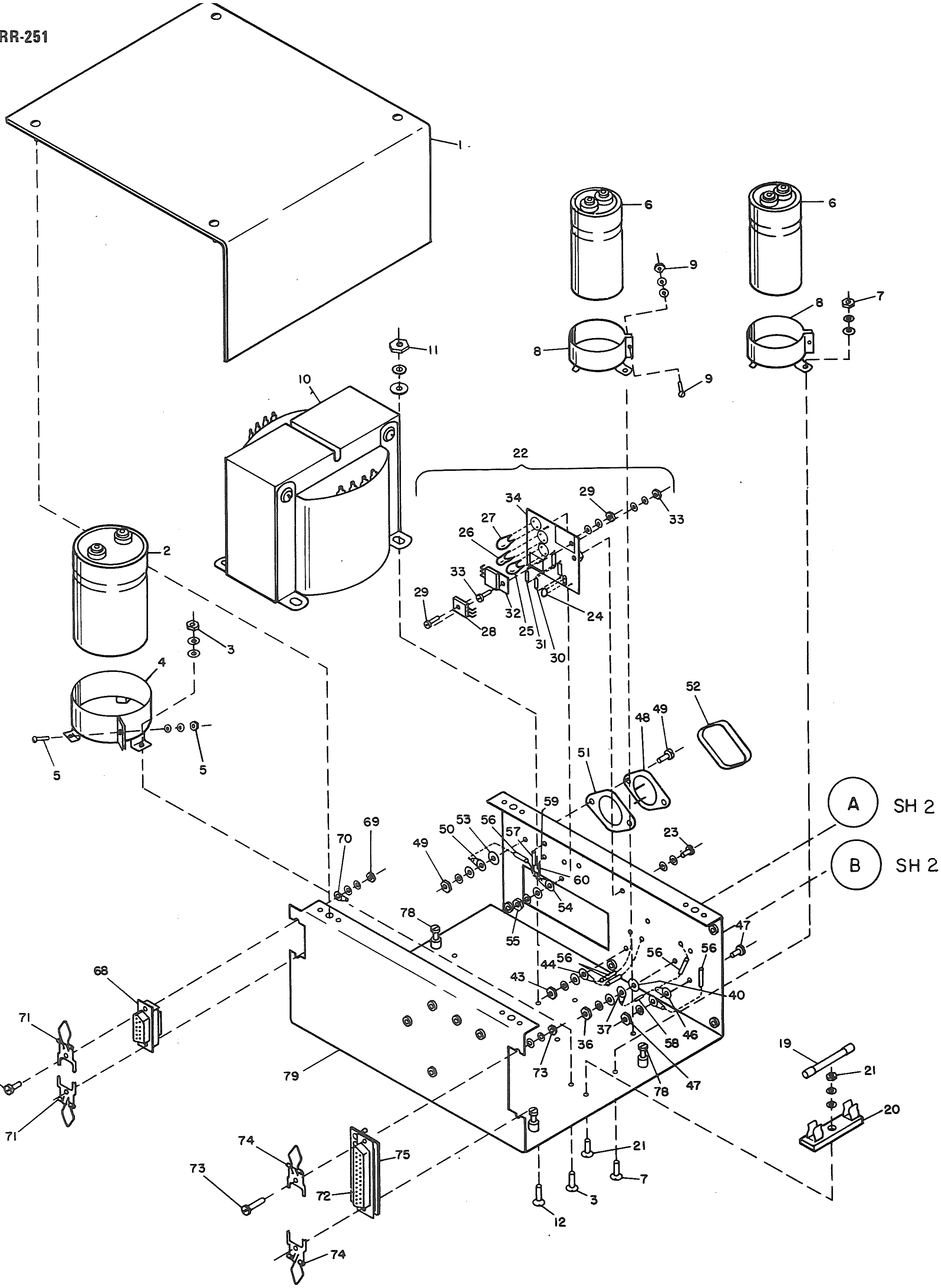


Figure 7-12. Power Supply Assembly, Module, A10 (Sheet 1 of 2)

FIGURE 7-12. POWER SUPPLY ASSEMBLY, MODULE, A10

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-12	08389	23386	• POWER SUPPLY ASSEMBLY, ... Module, A10	1		PAOODT
/1-1	08518	23386	• • COVER, Power Supply.	1		XB
/1-2	3186EA12340 25AMA2	30983	• • CAPACITOR, C1, ... Electrolytic, 12,500 uf, 25 WVDC, –10 +75%	1		PAOZZN
/1-3	MS35649-48	81349	• • NUT, Hex, 6-32 (AP).	3		PAOZZN
	MS35338-79	81349	• • WASHER, Split Lock, ... No. 6 (AP)	3		PAOZZN
	MS15795-305	81349	• • WASHER‘, Flat, ... No. 6 (AP)	3		PAOZZN
	AN507C-632-6	81349	• • SCREW, Machine, Flat Head . . . . 6-32 x 3/8 (AP)	3		PAOZZN
/1-4	4586-48	56289	• • • CLAMP, Capacitor, C1	1		PAOZZN
/1-5	MS35649-48	81349	• • • WASHER, Split Lock, ...	1		PAOZZN
	MS35338-79	81349	• • • WASHER, Split Lock, ... No. 6 (AP)	1		PAOZZN
	MS15795-305	81349	• • • WASHER, Flat,. . . . . No. 6 (AP)	1		PAOZZN
	AN507C-632-6	81349	• • • SCREW, Machine, ... Pan Head, 6-32 x 3/8 (AP)	1		PAOZZN
/1-6	3186BA522UO 40AM	30983	• • CAPACITOR, C4, C7, ... Electrolytic, 5200 uf, 40 WVDC, –10 +75%	2		PAOZZN
/1-7	MS35649-48	81349	• • NUT, Hex, 6-32 (AP).	2		PAOZZN
	MS35338-79	81349	• • WASHER, Split Lock, ... No. 6 (AP)	2		PAOZZN
	MS15795-305	81349	• • WASHER, Flat, No. 6 (AP).	2		PAOZZN
	AN507C-632-6	81349	• • SCREW, Machine, ... Flat Head, 6-32 x 3/8 (AP)	2		PAOZZN
/1-8	VR3	97244	• • • CLAMP, Capacitor, ... C4, C7	2		PAOZZN
/1-9	MS35649-48	81349	• • • NUT, Hex, 6-32 (AP).	1		PAOZZN
	MS35338-79	81349	• • • WASHER, Split Lock, ... No. 6 (AP)	1		PAOZZN
	MS15795-305	81349	• • • WASHER, Flat,. . . . . No. 6 (AP)	1		PAOZZN
	AN507C-632-6	81349	• • • SCREW, Machine, ... Pan Head, 6-32 x 3/8 (AP)	1		PAOZZN
/1-10	08517	23386	• • TRANSFORMER, T1, ... Power	1		PAOZZN
/1-11	MS35649-84	81349	• • NUT, Hex, 8-32 (AP).	4		PAOZZN
	MS35338-80	81349	• • WASHER, Split Lock, ... No. 8 (AP)	4		PAOZZN
	MS15795-307	81349	• • WASHER, Flat,. . . . . No. 8 (AP)	4		PAOZZN
/1-12	MS35234-10	96906	• • SCREW, Machine, Flat Head,. . . . 8-32 x 1/2 (AP)	4		PAOZZN

FIGURE 7-12. POWER SUPPLY ASSEMBLY, MODULE A10 (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-12–						
/1-19	F02B250V1-2A	81349	• • FUSE, F2, 1/2 amp,. . . . . Slow blow, 250V, 3AG	1		PAOZZN
/1-20	350244	79515	• • FUSE HOLDER, XF2, ... Clip type (for spare)	1		PAOZZN
/1-21	MS35649-44	81349	• • NUT, Hex, 4-40 (AP)	1		PAOZZN
	MS35338-78	81349	• • WASHER, Split Lock, ... No. 4 (AP)	1		PAOZZN
	MS15795-303	96906	• • WASHER, Flat,. . . . . No. 4 (AP)	1		PAOZZN
	MS35234-29	96906	• • SCREW, Machine, ... Flat Head, 4-40 x 3/8 (AP)	1		PAOZZN
/1-22	08593	23386	• • 20V REGULATOR . . . . ASSEMBLY, Circuit Card, A10A2	1		PADOFP
/1-23	MS35233-14	96906	• • SCREW, Machine, ... Pan Head, 4-40 x 5/16 (AP)	2		PAOZZN
	MS35338-78	81349	• • WASHER, Split Lock, ... No. 4 (AP)	2		PAOZZN
	MS15795-303	96906	• • WASHER, Flat, No. 4 (AP)	2		PAOZZN
/1-24	C320C103M1U1C1	31433	• • • CAPACITOR, A2C1, ... Ceramic, 0.01 uf, 50 WVDC, ±20%	1		PAFZZN
/1-25	T362A685M035AS	31433	• • • CAPACITOR, A2C2, ... Tantalum, 6.8 uf, 35 WVDC, ±20%	1		PAOZZN
/1-26	CX02N105M	81349	• • • CAPACITOR, A2C3, ... Tantalum, 1 uf, 35 WVDC, ±20%	1		PAOZZN
/1-27	T362A685M035AS	31433	• • • CAPACITOR, A2C4, ... Tantalum, 6.8 uf, 35 WVDC, ±20%	1		PAOZZN
/1-28	MJE800	04713	• • • TRANSISTOR, A2Q1, ... Voltage regulator	1		PAOZZN
/1-29	MS35649-44	81349	• • • NUT, Hex, 4-40 (AP)	1		PAOZZN
	MS35338-78	81349	• • • WASHER, Split Lock, ... No. 4 (AP)	1		PAOZZN
	MS15795-303	96906	• • • WASHER, Flat,. . . . . No. 4 (AP)	1		PAOZZN
	MS35233-14	96906	• • • SCREW, Machine, ... Pan Head, 4-40 x 5/16 (AP)	1		PAOZZN
/1-30	RL07S472G	81349	• • • RESISTOR, A2R1, ... Fixed Film, 4.7K ohms, ±2%, 1/4 watt	1		PAOZZN
/1-31	RL07S473G	81349	• • • RESISTOR, A2R2, ... Fixed Film, 47K ohms, ±2%, 1/4 watt	1		PAOZZN
/1-32	MC78M20CBD	04713	• • • INTEGRATED CIRCUIT,. . . . A2U1, 20 volt regulator	1		PAOZZN

FIGURE 7-12. POWER SUPPLY ASSEMBLY, MODULE A10 (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-12–						
/1-33	MS35649-44	81349	• • • NUT, Hex, 4-40 (AP)	1		PAOZZN
	MS35338-78	81349	• • • WASHER, Split Lock, ... No. 4 (AP)	1		PAOZZN
	MS15795-303	96906	• • • WASHER, Flat, No. 4 (AP)	1		PAOZZN
	MS35233-14	96906	• • • SCREW, Machine, ... Pan Head 4-40 x 5/16 (AP)	1		PAOZZN
/1-34	08592	23386	• • • PRINTED WIRING . . . . BOARD, A10A2	1		XA
/1-36	MS35649-48	81349	• • NUT, Hex, 6-32 (AP)	2		PAOZZN
	MS35338-79	81349	• • WASHER, Split Lock, ... No. 6 (AP)	2		PAOZZN
	MS15795-305	81349	• • WASHER, Flat, No. 6 (AP)	2		PAOZZN
/1-37	1488-6	83330	• • LUG, Solder, No. 6	1		PAOZZN
/1-40	5608-10	86928	• • WASHER, Shoulder insulating	2		PAFZZN
/1-43	MS35649-48	81349	• • NUT, Hex, 6-32 (AP)	2		PAOZZN
	MS35338-79	81349	• • WASHER, Split Lock, ... No. 6 (AP)	2		PAOZZN
	MS15795-305	81349	• • WASHER, Flat, No. 6 (AP)	2		PAOZZN
/1-44	1488-6	83330	• • LUG, Solder, No. 6 (AP)	1		PAOZZN
	MS35233-30	96906	• • SCREW, Machine, ... Pan Head, 6-32 x 1/2 (AP)	2		PAOZZN
/1-45	6015B	13103	• • HEAT, Sink, ... Regulator	1		PAOZZN
/1-46	1488-4	83330	• • LUG, Solder, No. 4	2		PAOZZN
/1-47	MS35649-44	81349	• • NUT, Hex, 4-40 (AP)	1		PAOZZN
	MS35338-78	81349	• • WASHER, Split Lock, ... No. 4 (AP)	1		PAOZZN
	MS35233-14	96906	• • SCREW, Machine, Pan Head, ... 4-40 x 5/16 (AP)	1		PAOZZN
/1-48	LM7915C	27014	• • INTEGRATED CIRCUIT, ... U3, –15 volt regulator	1		PAOZZN
/1-49	MS35649-48	81349	• • NUT, Hex, 6-32 (AP)	2		PAOZZN
	MS35338-79	81349	• • WASHER, Split Lock, ... No. 6 (AP)	2		PAOZZN
	MS15795-305	81349	• • WASHER, Flat, No. 6 (AP)	2		PAOZZN
/1-50	1488-6	83330	• • LUG, Solder, No. 6	1		PAOZZN
/1-51	5210-2	86928	• • INSULATOR, Regulator	1		PAOZZN
	MS35233-30	96906	• • SCREW, Machine, Pan Head, ... 6-32 x 1/2 (AP)	2		PAOZZN
/1-52	A22-2003	K1935	• • • COVER, Regulator	1		PAOZZN
/1-53	5608-10	86928	• • WASHER, Shoulder insulating	2		PAOZZN
/1-54	1488-4	83330	• • LUG, Solder, No. 4	1		PAOZZN
/1-55	MS35649-44	81349	• • NUT, Hex, 4-40 (AP)	1		PAOZZN
	MS35338-78	81349	• • WASHER, Split Lock, ... No. 4 (AP)	1		PAOZZN
	MS35233-14	96906	• • SCREW, Machine, ... Pan Head, 4-40 x 5/16 (AP)	1		PAOZZN
/1-56	T310A105M035AS	31433	• • CAPACITOR, C2, C3, ... C5, C6, C8, Tantalum, 1 uf, 35 WVDC, ±20%	5		PAOZZN

FIGURE 7-12. POWER SUPPLY ASSEMBLY, MODULE, A10 (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-12–						
/1-57	T310B685M035AS	31433	• • CAPACITOR, C9, Tantalum, 6.8 uf, 35 WVDC, ±20%	1		PAOZZN
/1-58	RLR07C330GR	81349	• • RESISTOR, R1, Metal Film, 33 ohms, ±2%, 1/4 watt	1		PAOZZN
/1-59	MIL-W-3861 /S-24	81349	• • WIRE, No. 24 Buss	AR		PAOZZN
	MIL-I-22129C –24	81349	• • SLEEVING, PTFE. tubing, No. 24	AR		PAOZZN
/1-60	MS39014/2-1356	81349	• • CAPACITOR, C11, Ceramic 0.22 uf, 50 WVDC, ±20%	1		PAOZZN
/1-68	M24308/2-1	81349	• • CONNECTOR, J2, AC switched power	1		PAFZZN
/1-69	MS35649-44	81349	• • NUT, Hex, 4-40 (AP)	2		PAOZZN
	MS35338-78	81349	• • WASHER, Split Lock, No. 4 (AP)	2		PAOZZN
	MS15795-303	96906	• • WASHER, Flat, No. 4 (AP)	2		PAOZZN
/1-70	1488-4	83330	• • LUG, Solder, No. 4	1		PAOZZN
	MS35233-14	96906	• • SCREW, Machine, Pan Head, 4-40 x 5/16 (AP)	2		PAOZZN
/1-71	D110277	71468	• • LOCK, Retainer, J2	2		PAOZZN
/1-72	08516-1	23386	• • CONNECTOR ASSEMBLY, J3, Power Supply	1		PAFZZN
/1-73	MS35649-44	81349	• • NUT, Hex, 4-40 (AP)	2		PAOZZN
	MS35338-78	81349	• • WASHER, Split Lock, No. 4 (AP)	2		PAOZZN
	MS15795-303	96906	• • WASHER, Flat, No. 4 (AP)	2		PAOZZN
	MS35233-14	96906	• • SCREW, Machine, Pan Head, 4-40 x 5/16 (AP)	2		PAOZZN
/1-74	D110277	71468	• • LOCK, Retainer, J3	2		PAOZZN
/1-75	08520	23386	• • • PRINTED WIRING BOARD, A10A1	1		XA
/1-78	4459-M07-F09	04729	• • SCREW, Machine, Pan Head, Captive, 8-32	4		PAOZZN
/1-79	08514	23386	• • CHASSIS, Power Supply	1		XA

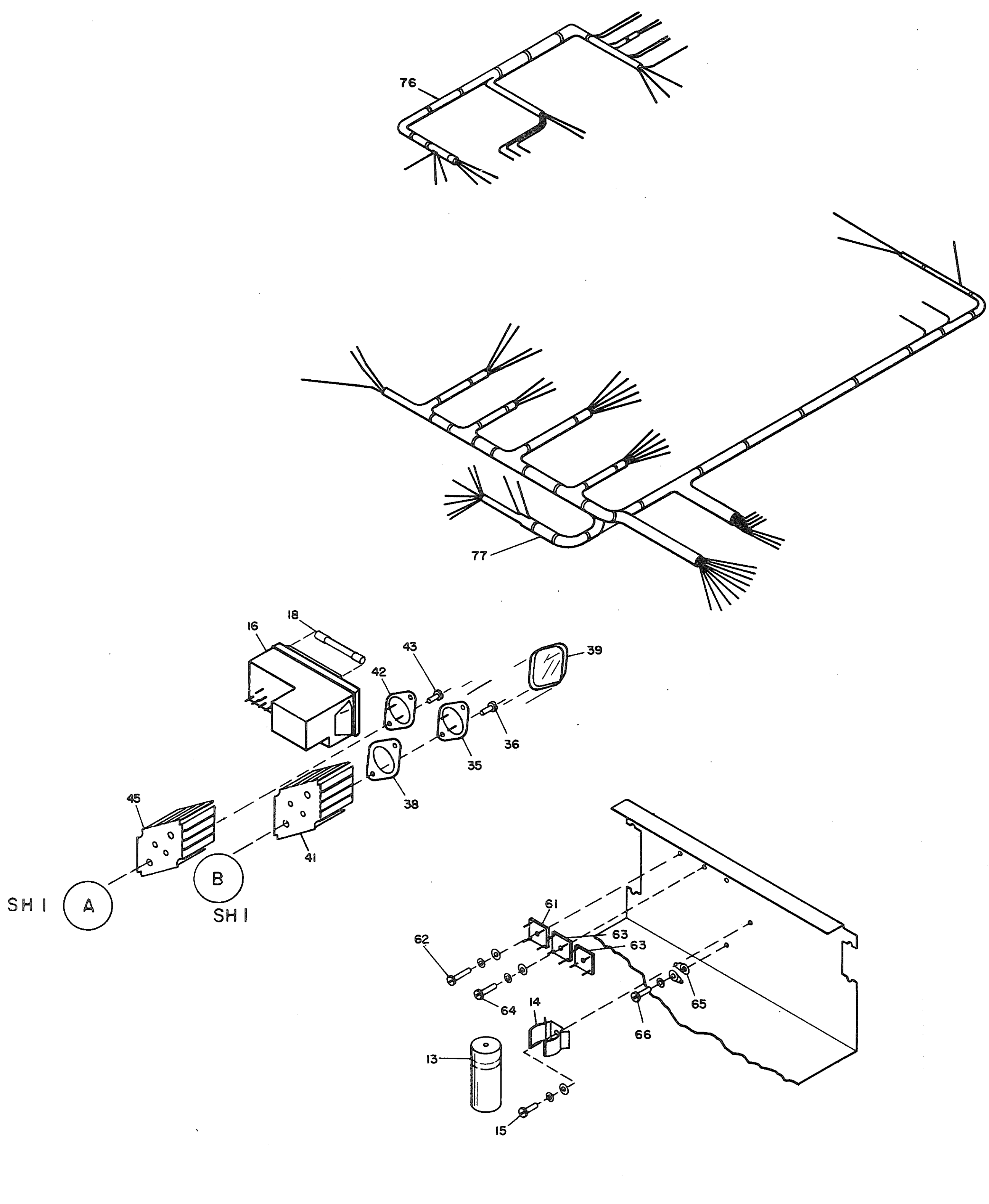


Figure 7-12. Power Supply Assembly, Module, A10 (Sheet 2 of 2)

FIGURE 7-12. POWER SUPPLY ASSEMBLY, MODULE A10 (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-12–						
/2-13	3050HJ122U 050JM	30983	• • CAPACITOR, C10, Electrolytic, 1200 uf, 50 WVDC, –10 +75%	1		PAOZZN
/2-14	SM-B603955	06915	• • CLIP, Component, C10, 7/8"	1		PAOZZN
/2-15	MS35233-27	96906	• • SCREW, Machine, Pan Head 6-32 x 5/16 (AP)	1		PAOZZN
	MS35338-79	81349	• • WASHER, Split Lock, No. 6 (AP)	1		PAOZZN
	MS15795-305	81349	• • WASHER, Flat, No. 6 (AP)	1		PAOZZN
/2-16	6J4	05245	• • CONNECTOR, J1, Power Input, Filter and Fuse	1		PAFZZN
/2-18	F02B250V1A	81349	• • FUSE, F1, 1 amp,	1		PAOZZN
/2-35	UA78H05KC	34148	• • INTEGRATED CIRCUIT, U1, +5 Volt Regulator	1		PAOZZN
/2-36	MS35649-48	81349	• • NUT, Hex, 6-32 (AP)	2		PAOZZN
	MS35338-79	81349	• • WASHER, Split Lock, No. 6 (AP)	2		PAOZZN
	MS15795-305	81349	• • WASHER, Flat, No. 6 (AP)	2		PAOZZN
/2-38	5210-2	86928	• • INSULATOR, Regulator.	1		PAOZZN
	MS35233-30	96906	• • SCREW, Machine, Pan Head, 6-32 x 1/2 (AP)	2		PAOZZN
/2-39	A22-2003	K1935	• • COVER, Regulator, U1	1		PAOZZN
/2-41	6015B	13103	• • HEAT SINK, Regulator, Thermology 6015B	1		PAOZZN
/2-42	M38510/10708 BYC	81349	• • INTEGRATED CIRCUIT, U2, +15 Volt Regulator	1		PAOZZN
/2-43	MS35649-48	81349	• • NUT, Hex, 6-32 (AP)	2		PAOZZN
	MS35338-79	81349	• • WASHER, Split Lock, No. 6 (AP)	2		PAOZZN
	MS15795-305	81349	• • WASHER, Flat, No. 6 (AP)	2		PAOZZN
/2-45	6015B	13103	• • HEAT SINK, Regulator, Thermology 6015B	1		PAOZZN
/2-61	VH148X	83003	• • DIODE, CR1, Rectifier.	1		PAOZZN
/2-62	MS35233-17	96906	• • SCREW, Machine, Pan Head, 4-40 x 1/2 (AP0	1		PAOZZN
	MS35338-78	81349	• • WASHER, Split Lock, No. 4 (AP)	1		PAOZZN
	MS15795-303	96906	• • WASHER, Flat, No. 4 (AP)	1		PAOZZN
/2-63	VS148X	83003	• • DIODE, CR2, CR3, Rectifier	2		PAOZZN
/2-64	MS35233-17	96906	• • SCREW, Machine Pan Head, 4-40 x 1/2 (AP)	1		PAOZZN
	MS35338-78	81349	• • WASHER, Split Lock, No. 4 (AP)	1		PAOZZN
	MS15795-303	96906	• • WASHER, Flat, No. 4 (AP)	1		PAOZZN
/2-65	1488-4	83330	• • LUG, Solder, No. 4	2		PAOZZN

FIGURE 7-12. POWER SUPPLY ASSEMBLY, MODULE, A10 (Cont.)

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-12— /2-66	MS35233-14	96906	• • SCREW, Machine, ... Pan Head, 4-40 x 5/16 (AP)	1		PAOZZN
	MS35338-78	81349	• • WASHER, Split Lock, ... No. 4 (AP)	1		PAOZZN
	MS15795-303	96906	• • WASHER, Flat, No. 4 (AP)	1		PAOZZN
/2-76	08513	23386	• • HARNESS, Wiring. . . . . Assembly, No. 1	1		MOOZZN
/2-77	08515	23386	• • HARNESS, Wiring. . . . . Assembly, No. 2	1		MOOZZN

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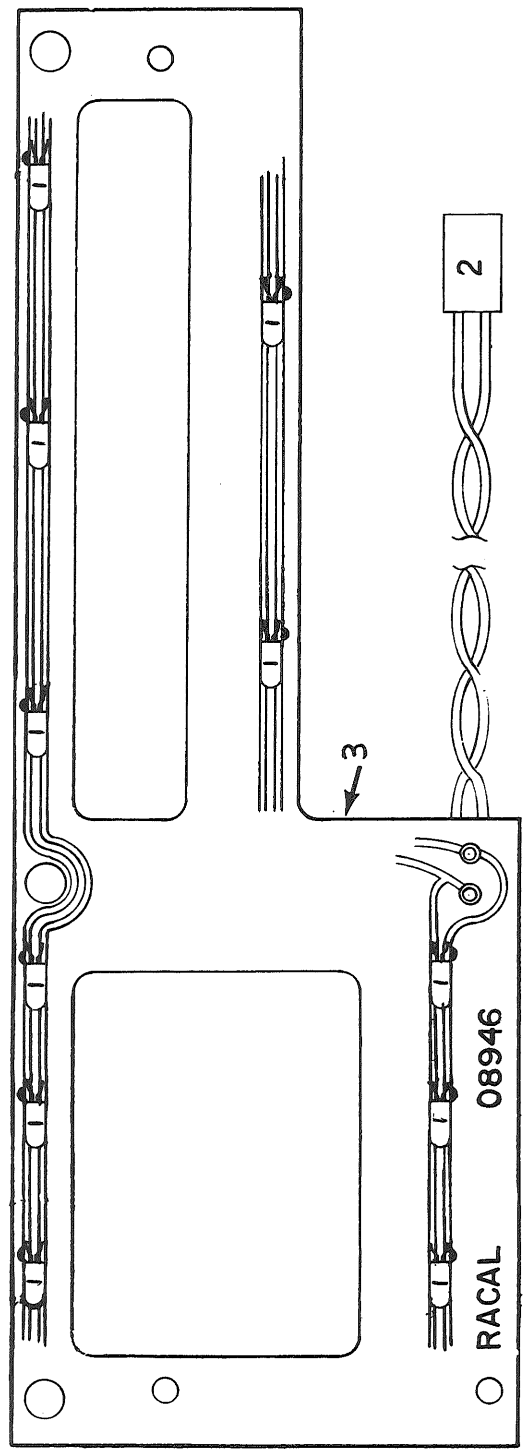

Figure 7-13. Circuit Card Assembly, LCD Lampboard

FIGURE 7-13. CIRCUIT CARD ASSEMBLY, LCD LAMP BOARD

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-13	08946	23386	• CIRCUIT CARD ASSEMBLY LCD LAMP BOARD	1		XBOZZN
/1-1	6838	05464	• • LAMP, DS1 thru DS11.... Incandescent, Type B25T, 28V at 0.24A	11		PAFZZN
/1-2	08948	23386	• • CABLE, W1..............	1		MOOZZN
/1-3	08945	23386	• • BOARD, Printed Wiring..	1		MOOZZN

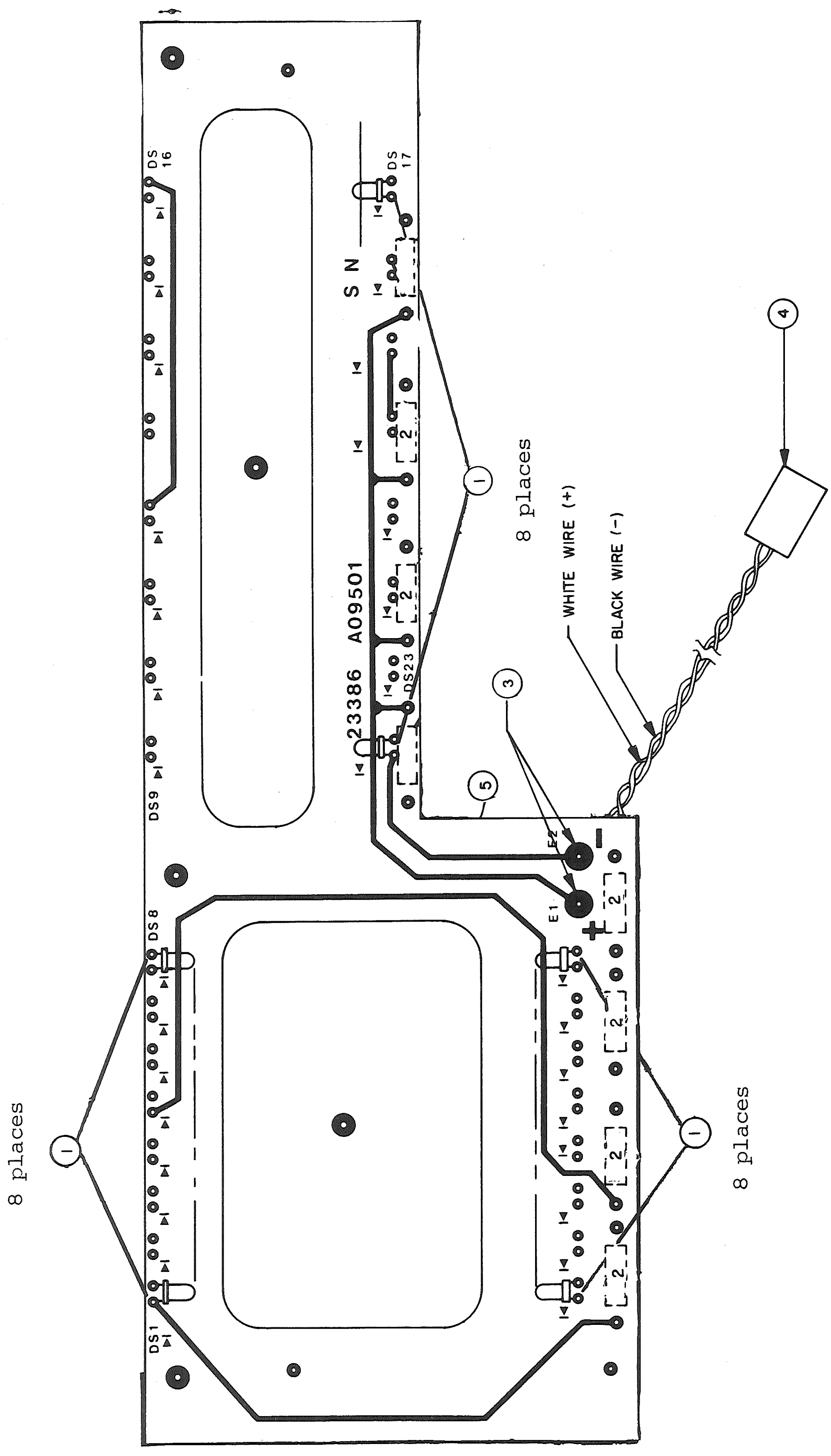

Figure 7-13.1 Circuit Card Assembly, LCD/LED Board

FIGURE 7-13.1. CIRCUIT CARD ASSEMBLY, LCD-LED BOARD

FIGURE & INDEX NO.	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY.	USABLE ON CODE	SMR CODE
7-13.1	09501	23386	• CIRCUIT CARD ASSEMBLY LCD-LED BOARD	1	A	XBOZZN
/1-1	09806	23386	• • LED-LCD DISPLAY........ DS1 thru DS8, DS17 thru DS32	24		PAFZZN
/1-2	RCR20G181JS	81349	• • RESISTOR, R1 thru...... R4, R6, R7, Fixed Composition, 180 ohms, ±5%, 1/2 W	6		PADZZN
/1-3	180-1461 02-05-00	71279	• • TERMINAL, E1, E2.......	2		PADZZN
/1-4	08320	23386	• • CABLE ASSEMBLY, W1.....	1		MOOZZN
/1-5	09502	23386	• • BOARD, Printed Wiring.. (without bulbs)	1		MOOZZN

SECTION III
NUMERICAL
INDEX

SECTION III. NUMERICAL INDEX

PART NUMBER	FIGURE & INDEX NO.	QTY. PER END ITEM
AD201A	7-9-68	1
AD518JH883B	7-9-51	1
AD7524JN	7-5-69	1
AH5016C-5	7-7-15	1
AM26LS30PC	7-7-10	1
AM26LS32CN	7-7-9	1
AN507C-632-6	7-12-3	7
A1004AL	7-3-41	2
A22-2003	7-12-39	2
A23-2023Z	7-8-11	3
BSF-1BBGP102M	7-1-129	9
B52600F003	7-10-61	1
CA-11-STL-T3WW	7-11-26	4
CA-12-STL-T3WW	7-11-44	2
CA-14-STL-T3WW	7-11-45	2
CA-20-STL-T3WW	7-11-27	2
CA1458E	7-5-64	2
CA3046E	7-4-14	3
CA3140BT/3	7-9-74	1
CA324E	7-5-29	6
CCR06CG222GR	7-6-34	1
CCR06CG472GR	7-6-35	1
CD22100F	7-5-76	1
CD40N28BCN	7-5-44	2
CD40107BEX	7-11-55	3
CD40108BEX	7-9-33	1
CD40109BEX	7-5-57	3
CD40174BMT	7-9-4	1
CD4042BE	7-5-42	7
CD4047BEMJ/883B	7-11-53	1
CD4051BEMJ/883B	7-11-10	1
CD4053BEX	7-5-60	1
CD4054BD	7-11-31	10
CD4056BD	7-11-28	13
CD4066BEX	7-5-39	6
CD4069UBE	7-11-21	1
CD4085BF	7-11-23	1
CD4094BEX	7-9-2	7
CD4099	7-11-49	4
CD4503BCN	7-7-17	13
CD4508BD/3	7-11-15	1
CD4514BD/3	7-11-16	2
CD4516BCN	7-11-58	1
CD4528BF	7-11-19	1
CD4529BCN	7-7-26	1
CK60BX101K	7-11-35	2
CMR05C5R0G0DR	7-10-67	1
CMR05C100G0DR	7-2-6	3
CMR05C120G0DR	7-10-73	1
CM05CD180G03	7-3-62	1

PART NUMBER	FIGURE & INDEX NO.	QTY PER END ITEM
CM05CD150G03	7-4-53	1
CMR05E270G0DR	7-9-45	1
CMR05E300G0DR	7-3-67	1
CMR05E330G0DR	7-3-10	2
CMR05E430G0DR	7-2-14	2
CMR05E470G0DR	7-9-60	2
CMR05E560G0DR	7-10-24	1
CMR05E680G0DR	7-3-31	6
CMR05E750G0DR	7-2-9	1
CMR05E820G0DR	7-2-15	7
CMR05F101G0DR	7-3-24	11
CMR05F111G0DR	7-2-4	2
CMR05F121G0DR	7-2-12	1
CMR05F151G0DR	7-2-7	5
CMR05F241G0DR	7-3-68	1
CMR05F271G0DR	7-3-64	1
CMR05F301G0DR	7-7-11	6
CMR05F331G0DR	7-4-2	2
CMR05F910G0DR	7-2-11	2
CMR06F152G0DR	7-5-22	4
CMR06F222G0DR	7-9-72	1
CMR06F332G0DR	7-5-59	1
CMR06F472G0DR	7-9-67	1
CM06FD821JN3	7-10-4	2
COM6402P	7-7-16	1
CS13BE156M	7-9-53	1
CS13BE335M	7-10-77	1
CYL-1400-250	7-1-59	1
CY15C102M	7-3-1	32
C280MCH/AIM	7-9-76	1
C280MCH/A100K	7-10-42	2
C280MCH/A47K	7-9-49	1
C280MCH/A470K	7-10-43	1
C312C222M1U1CA	7-9-12	1
C312C479K2G5CA	7-9-107	1
C320C103M1U1C1	7-3-5	98
C320C152K2R5C1	7-5-61	1
C320C223M1U1CA	7-5-53	2
C320C473M5U1CA	7-9-18	3
DAC-20CQ	7-9-37	1
DD-391	7-5-85	2
DKV6522B	7-9-100	2
DM10115N	7-10-71	1
DM74LS00NAT	7-10-64	1
DM74LS390N	7-10-10	3
DS3SD	7-8-15	1
DTZ-10	7-5-68	1
DTZ-15	7-8-6	2

SECTION III. NUMERICAL INDEX (Cont.)

PART NUMBER	FIGURE & INDEX NO.	QTY. PER END ITEM
DTZ-20	7-11-17	2
D110277	7-1-109	8
D155E220DO	7-4-21	2
ET101X025A5	7-5-18	4
ET471X025A01	7-5-40	2
FCS-10	7-1-122	10
F02B250V1A	7-12-19	1
F02B270V1-2A	7-12-18	1
F10211PC	7-9-65	1
F10231PC	7-9-64	2
GF326	7-1-99	1
GV-7000	7-1-124	1
HBLB17S-5	7-11-1	2
HLMP6620	7-11-56	4
HP5082-4468	7-11-29	1
JAN1N270	7-8-28	1
JAN1N752A	7-8-31	1
JAN1N757A	7-9-26	1
JAN2N2369A	7-9-84	12
JAN2N3823	7-9-96	2
JAN2N918	7-4-41	2
JANTX2N3866	7-3-45	2
JJ-034	7-1-74	1
JMT-223	7-1-65	1
KC19-110	7-1-97	2
KS8379	7-3-45	2
LM1458N	7-9-40	2
LM1877N-9	7-5-77	2
LM78L1ZAWC	7-5-45	3
LM7905CN	7-7-18	1
LM7915C	7-12-48	1
LT10K012	7-4-31	4
LT10K020	7-10-2	1
LT10K128	7-10-12	2
LT10K129	7-9-54	4
LT10K131	7-13-37	5
LT10K133	7-3-13	6
LT10K138	7-10-32	2
LT10K196	7-3-22	1
LT4K078	7-4-49	1
LT4K081	7-10-78	1
LR4K085	7-3-19	2
MC1357L	7-5-74	
MC1496L	7-4-11	3
MC1733CP	7-4-33	1
MC3340L	7-5-86	2
MC78M20CBD	7-12-32	1
MC7812CT	7-9-22	1
MIL-I-22129C-20	7-11-30	AR
MIL-I-22129C-24	7-3-17	AR

PART NUMBER	FIGURE & INDEX NO.	QTY PER END ITEM
MIL-S-19500/428	7-9-96	3
MIL-W-3861/S-22	7-7-12	AR
MIL-W-3861/S-24	7-3-16	AR
MJE800	7-12-28	1
MKC-1860-533/06	7-9-77	1
MK3850	7-8-3	1
MK3853	7-8-4	1
MRF517	7-9.1-104	2
MS15795-303	7-1-4	120
MS15795-305	7-1-24	28
MS15795-307	7-1-96	9
MS15795-308	7-1-111	2
MS18034-4	7-2-17	51
MS24641-1	7-1-88	4
MS3367-4	7-3-21	2
MS35233-3	7-1-42	1
MS35233-12	7-1-24	3
MS35233-13	7-2-2	1
MS35233-14	7-1-28	96
MS35233-15	7-7-6	2
MS35233-17	7-12-62	1
MS35233-18	7-1-4	2
MS35233-22	7-1-42	2
MS35233-27	7-1-25	14
MS35233-28	7-1-92	5
MS35233-30	7-12-38	6
MS35233-43	7-1-96	12
MS35234-10	7-12-12	4
MS35234-29	7-12-21	1
MS35234-63	7-1-56	4
MS35234-65	7-1-112	1
MS35249-20	7-1-123	10
MS35249-35	7-1-30	1
MS35250-72	7-1-86	4
MS35338-77	7-1-42	1
MS35338-78	7-1-4	125
MS35338-79	7-1-24	34
MS35338-80	7-1-94	12
MS35338-81	7-1-113	2
MS355233-8	7-1-48	1
MS35649-44	7-1-80	40
MS35649-48	7-12-3	17
MS35649-84	7-12-11	4
MS35650-104	7-1-113	1
MS3901401-1593	7-3-34	152
MS3901402-1419	7-3-38	3
MS3901412-1356	7-7-29	1
MS51958-14	7-1-121	4
MS90376-16Y	7-7-1	1
MS90539-15	7-1-131	1

SECTION III. NUMERICAL INDEX (Cont.)

PART NUMBER	FIGURE & INDEX NO.	QTY. PER END ITEM
MV1634	7-10-69	1
MV1650	7-10-40	2
M24308/2-1	7-12-68	1
M38510/05001BCB	7-7-20	2
M38510/05101BEA	7-5-56	4
M38510/05202BCB	7-9-58	1
M38510/05204BCB	7-11-20	1
M38510/054-01BEA	7-9-57	1
M38510/05701BCB	7-9-7	2
M38510/06203BEA	7-7-24	1
M38510/10201BEA	7-9-82	2
M38510/10708BEA	7-5-88	2
M38510/10708BYC	7-12-42	1
M38510/11201BCB	7-5-71	3
M38510/17001BCD	7-11-22	1
M38510/30001BCB	7-10-60	1
M38510/30005BCD	7-8-5	1
M38510/3003BCB	7-7-22	2
M38510/30102BCB	7-9-31	4
M38510/30106BEB	7-9-30	3
M38510/30107BEB	7-7-21	1
M38510/30301BCB	7-8-13	3
M38510/30702BEB	7-8-8	1
M38510/30901BEA	7-10-50	2
M38510/31004BCB	7-8-9	2
M38510/31501BCB	7-10-51	1
M38510/31503BEA	7-10-14	5
M38510/31505BEA	7-9-61	2
M38510/31506BEA	7-9-87	1
M83723-02R-1626N	7-7-2	1
NS-432-100	7-5-5	14
NS-441-B1	7-5-4	14
N82S83N	7-9-6	1
N88026	7-9-105	2
P5101L	7-8-16	3
R-2174(P)/URR	Reference	1
R-2174A(P)/URR	Reference	1
RB-67-1SK-7	7-1-68	2
RCR20G150JS	7-3-35	1
RCR20G181JS	7-13.1/1-2	6
RJR50FP201	7-9-20	1
RJ50FW103	7-5-37	1
RJ50FW202	7-5-19	2
RJ50FW501	7-4-43	2
RJ50FW502	7-3-55	2
RJ50FW503	7-5-23	2
RLR07C100GR	7-3-9	17
RLR07C105GR	7-5-52	4
RLR07C184GR	7-5-34	1
RLR07C224GR	7-4-38	1

PART NUMBER	FIGURE & INDEX NO.	QTY PER END ITEM
RLR07C330GR	7-6-37	3
RLR07C334GR	7-5-54	2
RLR07C390GR	7-4-25	2
RLR07C564GR	7-10-26	2
RL07S101G	7-3-14	16
RL07S102G	7-3-6	63
RL07S103G	7-3-8	53
RL07S104G	7-4-16	18
RL07S113G	7-11-34	2
RL07S122G	7-3-49	5
RL07S123G	7-5-26	6
RL07S124G	7-8-35	2
RL07S151G	7-9-21	2
RL07S152G	7-4-32	12
RL07S153G	7-5-31	15
RL07S154G	7-9-17	1
RL07S181G	7-11-40	2
RL07S182G	7-10-19	3
RL07S183G	7-5-35	5
RL07S203G	7-11-52	1
RL07S220G	7-6-33	4
RL07S221G	7-3-7	12
RL07S222G	7-3-50	18
RL07S223G	7-4-17	26
RL07S270G	7-4-27	1
RL07S271G	7-8-27	1
RL07S272G	7-9-71	1
RL07S273G	7-5-30	2
RL07S331G	7-4-36	8
RL07S332G	7-5-49	22
RL07S333G	7-6-36	5
RL07S391G	7-6-32	2
RL07S392G	7-9-43	6
RL07S393G	7-4-40	5
RL07S470G	7-3-56	21
RL07S471G	7-5-46	25
RL07S472G	7-4-18	24
RL07S473G	7-5-28	17
RL07S560G	7-4-44	2
RL07S561G	7-4-13	1
RL07S562G	7-3-40	1
RL07S563G	7-6-27	2
RL07S680G	7-9-98	4
RL07S681G	7-5-25	13
RL07S682G	7-5-27	5
RL07S683G	7-5-65	2
RL07S820G	7-9-89	1
RL07S822G	7-9-35	9
RL07S823G	7-8-36	1
RN55D1400F	7-5-84	3
SIP-8-103	7-11-2	2

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SIP-8-223	7-7-7	3
SK2-1/4-1R0J	7-9-83	2
SM-B603955	7-12-14	1
SN74S374N	7-8-14	1
T1S74	7-8-21	2
T210A475M010MS	7-8-29	1
T310A105M035AS	7-12-56	5
T310B685M035AS	7-12-57	1
T362A105M035AS	7-4-12	10
T352A685M035AS	7-5-38	50
T362B156K020AS	7-3-57	16
T362B226K015AS	7-7-27	1
T362C157K006AS	7-9-63	1
T362C336M025AS	7-9-38	2
T362C686M015AS	7-4-78	5
UA757DC	7-5-21	2
UA78H05KC	7-12-35	1
UG-606/U	7-1-103	1
U310	7-3-11	3
VH148X	7-12-61	1
VR3	7-12-8	2
VS148X	7-12-63	2
WB-11-55-G	A9-26	4
WB-12-55-G	A9-44	2
WB-14-55-G	A9-45	2
WB-20-55-G	A9-27	2
OPB706A	7-11-41	2
05000-2*	7-1-89	1
051-075-0000	7-1-128	2
051-351-0000-220	7-3-2	17
08191	7-1-13	1
08192	7-4-55	1
08270	7-11-25	1
08289	7-10-36	1
08304	7-9-99	1
08320	7-13.1/1-4	1
08360	7-9-109	1
08361	7-1-45	1
08376	7-1-44	1
08385	7-1-3	1
08386	7-1-8	1
08387	7-1-52	1
08388	7-1-76	1
08389	7-1-91	1
08390	7-1-32	1
08390-2	7-1-32B	1
08391	7-1-37	1
08392	7-8-	1
08392-3	7-1-40	1
08404	7-3-26	1

PART NUMBER	FIGURE & INDEX NO.	QTY PER END ITEM
08406	7-1-26	1
08407	7-1-26	1
08408	7-1-26	1
08409	7-1-26	1
08410	7-1-26	1
08411	7-1-26	1
08412	7-1-26	1
08413	7-1-26	1
08414	7-1-26	1
08415	7-1-26	1
08416	7-1-26	1
08417	7-1-26	1
08418	7-1-26	1
08419	7-1-26	1
08420	7-1-26	1
08441	7-11-59	1
08445	7-1-95	1
08449	7-8-10	3
08454	7-1-55	1
08465	7-1-27	1
08467	7-1-133	1
08468	7-1-116	1
08469	7-1-118	1
08470	7-2-1	1
08471	7-7-5	1
08473	7-11-42	2
08474	7-2-19	1
08475	7-2-3	1
08477-1	7-2-5	1
08477-2	7-2-8	2
08477-3	7-2-10	1
08477-4	7-2-13	1
08477-5	7-3-30	1
08477-6	7-3-25a	1
08477-7	7-3-30a	1
08479-1	7-3-20	1
08479-3	7-4-35	1
08479-4	7-2-18	1
08480	7-2-16	1
08482	7-8-40	1
		1
08484	7-6-69	1
08485	7-5-47	4
08486	7-6-54	1
08487	7-8-7	1
08489	7-7-31	1
08490	7-7-14	1
08491	7-7-30	1
08492	7-1-38	1
08493	7-7-4	1
08495	7-3-48	1

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PART NUMBER	FIGURE & INDEX NO.	QTY PER END ITEM
08496	7-1-22	1
08497	7-1-29	1
08498-2	7-1-84	1
08499-4	7-3-58	1
08499-5	7-4-39	1
08500-1	7-3-61	1
08500-2	7-3-63	1
08500-3	7-3-66	1
08500-4	7-3-69	1
08501	7-3-54	1
08502-1	7-9-106	1
08503	7-3-3	2
08504	7-3-32	1
08513	7-12-76	1
08514	7-12-79	1
08515	7-12-77	1
08516-1	7-12-72	1
08517	7-12-10	1
08518	7-1-93	1
08520	7-12-75	1
08521	7-1-1	2
08522	7-4-3	6
08524	7-10-83	1
08525	7-10-39	1
08526	7-11-43	1
08530	7-4-24	1
08531	7-5-58	1
08533	7-5-90	1
08535	7-5-81	3
08536	7-11-5	1
08538	7-1-58	1
08551	7-1-72	1
08552	7-1-69	1
08553	7-1-60	1
08554	7-1-62	1
08555-1	7-1-15	1
08555-2	7-1-6	1
08555-3	7-1-43	1
08555-4	7-1-11	1
08555-5	7-1-16	1
08555-6	7-1-17	1
08555-7	7-1-18	1
08556-1	7-1-50	1
08557	7-1-57	1
08558	7-1-51	1
08560	7-1-12	1
08561	7-1-7	1
08562	7-1-126	1
08563	7-1-20	1
08564	7-1-34	1

PART NUMBER	FIGURE & INDEX NO.	QTY PER END ITEM
08568	7-1-21	1
08569	7-1-54	1
08570	7-1-64	1
08573	7-11-11	1
08576	7-4-50	1
08578	7-3-70	1
08580	7-1-23	1
08592	7-12-34	1
08593	7-12-22	1
08648	7-1-47	1
08656	7-1-120	2
08666	7-1-10	1
08667	7-1-41	1
08668	7-1-49	1
08670	7-9-79	1
08675	7-1-87	1
08676	7-1-114	1
08707	7-9/1-23	1
08944	7-1-81	1
08945	7-13/1-3	1
08946	7-1-79	1
08948	7-13/1-2	1
09078	7-1-83	1
09097	7-1-9	6
09108	7-1-5	1
09134	7-1/2-45A	1
09226	7-3-48a	2
09255	7-9/2-99a	1
09500	7-1/3-81a	1
09501	7-1/3-79a	1
09502	7-13.1/1-1	1
09632	7-1-52a	1
09635	7-1-8A	1
09806	7-13.1/1-1	24
1N4001	7-10-56	1
1N916	7-3-39	62
11C90DCQR	7-9-88	2
120-5	7-9-80	AR
180-1461-02-05-00	7-13.1/1-3	2
1488-4	7-1-4	9
1488-6	7-12-37	3
17250	7-1-90	1
2N3904	7-8-22	7
2N3906	7-8-23	3
2N4124	7-9-42	2
2N4126	7-3-36	7
2N4921	7-9-78	2
2N5089	7-5-10	12
2N5160	7-3-42	1
22M-40	7-7-6	2
2257R	7-3-51	1

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30-350	7-1-70	2
3050HJ122-U050JM	7-12-13	1
3071FE22-1T016SF	7-5-87	5
3100-25	7-1-61	1
3186BA522-U040AM	7-12-6	2
3186EA123-4025AMA2	7-12-2	1
3402-0000T	7-11-6	1
3414-6034	7-11-7	1
3428-2002	7-11-24	1
3429-1002	7-10-15	1
3429-2002	7-11-47	2
3429-2003	7-5-83	1
3431-2002	7-8-39	1
3431-2003	7-5-80	1
3432-2002	7-11-46	1
3432-2003	7-5-72	1
3483-1000	7-1-107	1
3492-1002	7-9-55	1
350244	7-12-20	1
37039	7-10-68	1
4N28	7-10-30	1

PART NUMBER	FIGURE & INDEX NO.	QTY. PER END ITEM
4310R-101-103	7-11-3	3
4310R-101-223	7-7-25	1
4459-M07-F09	7-1-94	4
4586-48	7-12-4	1
5210-2	7-12-38	2
5608-10	7-12-40	4
5610-280-031	7-1-56	4
5610-84-032	7-1-63	
5710-54-25	7-1-59	2
5710-94-015	7-1-63	2
5720-21	7-1-61	AR
5804-17-1	7-1-9	6
5806-10-1	7-1-117	8
5806-28-1	7-1-63	2
6J4	7-12-16	1
6015B	7-12-41	2
65000-036	7-8-1	1
652A1E102J	7-9-48	2
69011-1058	7-3-44	7
6838	7-13/1-1	11
750-61-10K	7-9-5	1
76050-NP	7-1-63	2
7717-N-WHITE	7-3-12	15
8072-NP	7-1-110	1
81010901EB	7-6-63	2
8109-A-0440	7-1-78	10
9002-NP	7-1-70	2
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A1A1C9	7-2-15	A2J1	7-3-2	A3C14	7-4-5
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A1A1L3	7-2-10	A2L1	7-3-61	A3C19	7-4-2
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A2C6	7-3-65	A2L16	7-3-19	A3L1	7-4-23
A2C7	7-3-59	A2Q1	7-3-36	A3L2	7-4-49
A2C8	7-3-67	A2Q2	7-3-52	A3L3	7-4-23
A2C9	7-3-68	A2Q3	7-3-42	A3L4	7-4-31
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A4C21 thru C31	7-5-6	A4C108	7-5-87	A4R48	7-5-25
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A4C33 & C34	7-5-6	A4C113	7-5-14	A4R50	7-5-1
A4C35	7-5-18	A4C114	7-5-70	A4R51	7-5-12
A4C36	7-5-6	A4C115	7-5-85	A4R52	7-5-28
A4C37	7-5-50	A4C116	7-5-70	A4R53	7-5-7
A4C38 thru C40	7-5-6	A4C117	7-5-85	A4R55	7-5-9
A4C41	7-5-53	A4C118 & C119	7-5-78	A4R57 & R58	7-5-7
A4C42	7-5-38	A4C120 & C121	7-5-6	A4R60	7-5-11
A4C43	7-5-24	A4CR1 thru CR16	7-5-8	A4R61	7-5-32
A4C44	7-5-22	A4CR18 thru CR31	7-5-8	A4R62	7-5-9
A4C45	7-5-6	A4J1	7-5-3	A4R64	7-5-15
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A4C47	7-5-22	A4J3 thru J6	7-5-3	A4R66	7-5-9
A4C49 & C50	7-5-6	A4J7	7-5-83	A4R67	7-5-35
A4C51	7-5-24	A4J8	7-5-80	A4R68	7-5-9
A4C52	7-5-14	A4L1 & L2	7-5-47	A4R69	7-5-31
A4C53	7-5-24	A4L3	7-5-58	A4R70	7-5-9
A4C54	7-5-6	A4L4 & L5	7-5-79	A4R71	7-5-7
A4C56 & C57	7-5-6	A4Q1 & Q2	7-5-10		
A4C58	7-5-14	A4Q6 thru Q10	7-5-10		
A4C59	7-5-38				

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A4R74	7-5-27	A4R133	7-5-43	A5C7 & C8	7-6-6
A4R75	7-5-46	A4R134	7-5-31	A5C9	7-6-13
A4R76	7-5-26	A4R135	7-5-7	A5C10	7-6-6
A4R77 thru R79	7-5-9	A4R136 & R137	7-5-1	A5C11	7-6-43
A4R80	7-5-20	A4R139 & R140	7-5-13	A5C12 thru C15	7-6-6
A4R81	7-5-27	A4R141	7-5-11	A5C16	7-6-5
A4R82	7-5-20	A4R142	7-5-84	A5C17	7-6-23
A4R83	7-5-32	A4R143	7-5-15	A5C18	7-6-8
A4R84	7-5-49	A4R144 & R145	7-5-9	A5C19	7-6-5
A4R85	7-5-9	A4R146	7-5-30	A5C21	7-6-6
A4R86	7-5-7	A4R147	7-5-32	A5C23	7-6-6
A4R87	7-5-9	A4R150 & R151	7-5-13	A5C24 & C25	7-6-23
A4R88 & R89	7-5-7	A4R152	7-5-52	A5C26	7-6-13
A4R90	7-5-28	A4T1	7-5-81	A5C28	7-6-6
A4R91	7-5-32	A4U1	7-5-44	A5C30 & C31	7-6-6
A4R92	7-5-1	A4U2	7-5-42	A5C32	7-6-43
A4R93	7-5-28	A4U3	7-5-57	A5C33 thru C37	7-6-6
A4R94	7-5-15	A4U4	7-5-42	A5C38 & C39	7-6-43
A4R95 & R96	7-5-13	A4U5	7-5-57	A5C40	7-6-60
A4R97	7-5-31	A4U6	7-5-45	A5C41 thru C43	7-6-43
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A4R99	7-5-30	A4U8	7-5-21	A5C45	7-6-6
A4R100	7-5-43	A4U9	7-5-56	A5C46	7-6-34
A4R101	7-5-12	A4U10	7-5-51	A5C47	7-6-60
A4R102	7-5-9	A4U11 & U12	7-5-39	A5C48 & C49	7-6-58
A4R103	7-5-28	A4U13	7-5-42	A5C50	7-6-24
A4R104	7-5-35	A4U14	7-5-29	A5C51	7-6-43
A4R105	7-5-37	A4U15	7-5-42	A5C52	7-6-31
A4R106	7-5-34	A4U16	7-5-57	A5C53	7-6-13
A4R107	7-5-31	A4U17	7-5-29	A5C54	7-6-6
A4R108	7-5-27	A4U18	7-5-74	A5CR1thru CR6	7-6-47
A4R109	7-5-49	A4U19	7-5-60	A5J1	7-6-25
A4R110	7-5-46	A4U20	7-5-75	A5J3	7-6-25
A4R111 & R112	7-5-49	A4U21	7-5-69	A5L1 & L2	7-6-7
A4R113	7-5-15	A4U22	7-5-64	A5Q1	7-6-12
A4R114	7-5-49	A4U23	7-5-42	A5Q3	7-6-12
A4R115	7-5-20	A4U24	7-5-71	A5Q6 thru Q8	7-6-12
A4R116	7-5-49	A4U25	7-5-76	A5R1	7-6-17
A4R117	7-5-13	A4U26	7-5-77	A5R2	7-6-44
A4R118	7-5-67	A4U27	7-5-88	A5R3	7-6-27
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A4R121	7-5-49	A5	7-1-32	A5R6	7-6-16
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A4R124	7-5-32	A5C2	7-6-50		
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A4R126	7-5-1	A5C4	7-6-24		
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A5R14	7-6-10
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A5R75	7-6-40
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A5R78	7-6-15
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A5U2	7-6-45
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A5U12	7-6-59
A5U13	7-6-67
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A6A1	7-1-37
A6A1C1	7-7-28
A6A1C2	7-7-29
A6A1C3	7-7-27
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A6A1C7 thru C9	7-7-8
A6A1C10	7-7-11
A6A1C11 thru C18	7-7-8
A6A1C19	7-7-11
A6A1P1	7-7-30
A6A1U1	7-7-7
A6A1U2	7-7-9
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A6A1U5	7-7-18
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A6A1U16	7-7-21
A6A1U17	7-7-24
A6A1U18	7-7-25
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A6A2C1 & C2	7-8-6
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A6A2C17	7-8-26
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A6A2CR2	7-8-30
A6A2CR3	7-8-28
A6A2CR4 thru CR6	7-8-30
A6A2J1	7-8-39
A6A2J2	7-8-1
A6A2Q1	7-8-23
A6A2Q2 & Q3	7-8-22
A6A2Q4	7-8-23
A6A2Q5	7-8-22
A6A2Q6 & Q7	7-8-21
A6A2R1	7-8-32
A6A2R2	7-8-34
A6A2R3	7-8-17
A6A2R4	7-8-24
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A6A2R6	7-8-36
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A6A2R8	7-8-17
A6A2R9	7-8-27
A6A2R10	7-8-19
A6A2R11	7-8-33
A6A2R12	7-8-24
A6A2R13	7-8-25
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A6A2R15	7-8-19
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A6A2U12	7-8-13	A7C91	7-9-67	A7R22	7-9-47
A6A2U13	7-8-14	A7C92	7-9-72	A7R23	7-9-98
A6A2U14	7-8-10	A7C93	7-9-8	A7R24	7-9-25
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A6A2XU5 & XU6	7-8-11	A7C95	7-9-73	A7R26	7-9-93
A6A2XU14	7-8-11	A7C96	7-9-8	A7R27	7-9-92
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A7C6	7-9-9	A7C101	7-9-90	A7R33	7-9-35
A7C7	7-9-1	A7C103 & C104	7-9-60	A7R34 & R35	7-9-25
A7C8	7-9-9	A7CR1 & CR2	7-9-11	A7R36	7-9-62
A7C9	7-9-1	A7CR3 & CR4	7-9-100	A7R37	7-9-35
A7C11	7-9-1	A7CR5 thru CR16	7-9-11	A7R38	7-9-25
A7C12	7-9-9	A7CR18	7-9-26	A7R40 thru R44	7-9-25
A7C13 thru C34	7-9-1	A7CR19 & CR20	7-9-11	A7R45	7-9-41
A7C35	7-9-8	A7J1	7-9-55	A7R46	7-9-25
A7C36	7-9-9	A7J2 thru J4	7-9-59	A7R47	7-9-35
A7C37	7-9-8	A7L1 thru L4	7-9-54	A7R48 & R49	7-9-25
A7C38	7-9-9	A7L5	7-9-99	A7R50	7-9-3
A7C39	7-9-1	A7L6	7-9-102	A7R51	7-9-36
A7C40	7-9-73	A7Q1	7-9-96	A7R52	7-9-34
A7C41	7-9-38	A7Q2 & Q3	7-9-104	A7R53 & R54	7-9-10
A7C42	7-9-8	A7Q4	7-9-78	A7R55	7-9-25
A7C43	7-9-73	A7Q5	7-9-84	A7R56	7-9-34
A7C44	7-9-1	A7Q6 thru Q8	7-9-39	A7R57	7-9-43
A7C45 & C46	7-9-9	A7Q9 & Q10	7-9-42	A7R58	7-9-25
A7C47 & C48	7-9-1	A7Q11	7-9-39	A7R59	7-9-10
A7C49 & C50	7-9-9	A7Q12	7-9-94	A7R60	7-9-47
A7C51	7-9-8	A7Q13	7-9-84	A7R61	7-9-16
A7C52	7-9-73	A7R1	7-9-28	A7R62	7-9-3
A7C53	7-9-63	A7R2	7-9-56	A7R63	7-9-16
A7C54	7-9-73	A7R3	7-9-3	A7R64	7-9-50
A7C55	7-9-1	A7R4	7-9-21	A7R65	7-9-52
A7C56	7-9-38	A7R5	7-9-20	A7R66	7-9-70
A7C57	7-9-9	A7R6	7-9-91	A7R67	7-9-44
A7C58	7-9-90	A7R7 & R8	7-9-98	A7R68	7-9-16
A7C59	7-9-8	A7R9	7-9-47	A7R69	7-9-10
A7C60 & C61	7-9-9	A7R10	7-9-93	A7R70	7-9-16
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A7C78	7-9-46	A7R12	7-9-56	A7R72	7-9-56
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A7R85	7-9-91	A8C14	7-10-7	A8CR2 & CR3	7-10-37
A7R86	7-9-25	A8C15 thru C19	7-10-5	A8CR4	7-10-69
A7R87	7-9-28	A8C20	7-10-73	A8CR5	7-10-37
A7R88	7-9-69	A8C21 & C22	7-10-5	A8CR6 & CR7	7-10-40
A7R89	7-9-28	A8C23	7-10-13	A8J1 thru J4	7-10-9
A7R90	7-9-16	A8C24	7-10-5	A8J5	7-10-15
A7R91	7-9-21	A8C25	7-10-77	A8J8	7-10-16a
A7R92	7-9-56	A8C26	7-10-42	A8L1	7-10-17
A7R93	7-9-75	A8C27	7-10-5	A8L2	7-10-78
A7R94	7-9-56	A8C28	7-10-3	A8L3	7-10-32
A7R95	7-9-16	A8C29	7-10-63	A8L4	7-10-39
A7R97	7-9-16	A8C30	7-10-5	A8L5	7-10-32
A7T1	7-9-106	A8C31	7-10-63	A8L6	7-10-2
A7U1	7-9-58	A8C32	7-10-7	A8L7 & L8	7-10-12
A7U2	7-9-27	A8C33	7-10-76	A8L9 & L10	7-10-80
A7U3	7-9-30	A8C34 & C35	7-10-20	A8Q1 thru Q6	7-10-28
A7U4	7-9-32	A8C36	7-10-70	A8Q7	7-10-38
A7U5 & U6	7-9-30	A8C37	7-10-20	A8Q8	7-10-44
A7U7	7-9-29	A8C38	7-10-67	A8Q9	7-10-38
A7U8 thru U14	7-9-2	A8C39	7-10-5	A8Q10 & Q11	7-10-28
A7U15	7-9-6	A8C40	7-10-70	A815	7-10-38
A7U16	7-9-5	A8C41	7-10-76	A8Q16	7-10-44
A7U17	7-9-57	A8C42	7-10-7	A8Q17	7-10-38
A7U18	7-9-4	A8C43 thru C45	7-10-5	A8Q18 & Q19	7-10-21
A7U19	7-9-31	A8C46	7-10-20	A8Q20	7-10-28
A7U20 & U21	7-9-7	A8C47 & C48	7-10-5	A8Q22	7-10-61
A7U22	7-9-33	A8C49	7-10-13	A8R2	7-10-57
A7U23	7-9-37	A8C50	7-10-43	A8R3	7-10-58
A7U24	7-9-82	A8C51	7-10-42	A8R4	7-10-59
A7U26	7-9-64	A8C52 & C53	7-10-7	A8R5	7-10-46
A7U27	7-9-88	A8C54	7-10-13	A8R6	7-10-23
A7U28	7-9-64	A8C55	7-10-24	A8R7	7-10-27
A7U29	7-9-87	A8C56 & C57	7-10-20	A8R8	7-10-35
A7U30 & U31	7-9-61	A8C58 thru C61	7-10-7	A8R9	7-10-34
A7U32	7-9-65	A8C62	7-10-5	A8R10	7-10-27
A7U33	7-9-40	A8C63	7-10-4	A8R11	7-10-6
A7U34	7-9-15	A8C64	7-10-3	A8R12	7-10-33
A7U35	7-9-61	A8C65	7-10-4	A8R13	7-10-25
A7U36	7-9-68	A8C66 thru C71	7-10-5	A8R14	7-10-35
A7U37	7-9-66	A8C72	7-10-7	A8R18	7-10-45
A7U39	7-9-22	A8C73 thru C74	7-10-5	A8R19	7-10-19
A7U40	7-9-74	A8C75	7-10-82	A8R20	7-10-45
		A8C76	7-10-79	A8R21	7-10-19
A8	7-1-52	A8C77	7-10-81	A8R22	7-10-1
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A8C2	7-10-20	A8C79	7-10-13		
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A8R32	7-10-35	A8U13	7-10-47	A9U10 thru U18	7-11-28
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A8R42	7-10-66	A9	7-1-76	A9U36 thru U40	7-11-31
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A8R46	7-10-74	A9C8	7-11-51	A9U42 & U43	7-11-8
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A8R57 & R58	7-10-25	A9J4	7-11-47	A9U52 & U53	7-11-55
A8R59	7-10-23	A9J5	7-11-46	A9U54	7-11-57
A8R60	7-10-46	A9J6	7-11-24	A9U55	7-11-19
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A10C11	7-12-60				
A10CR1	7-12-61				
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R1	7-1-69				
R2	7-1-72				
S1	7-1-65				
S2	7-1-99				
S3	7-1-83				
S4	7-1-84				
W1	7-1-15				
W2	7-1-6				
W3	7-1-43				
W4	7-1-11				
W6	7-1-16				
W7	7-1-50				
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CHAPTER 8.
CIRCUIT DIAGRAMS

8-1 INTRODUCTION

This chapter contains circuit diagrams and Interconnection diagrams applicable to the R-2174(P)/URR Radio Receiver. A listing of all diagrams, showing Figure number and Page number for each, is shown for quick reference to any diagram.

UK and US Patents have been obtained covering the synthesizer circuits described on this page as follows: US Patent No. 4,204,174 Phase Locked Loop Variable Frequency Generator and US Patent No. 3,555,446 Frequency Synthesizer.

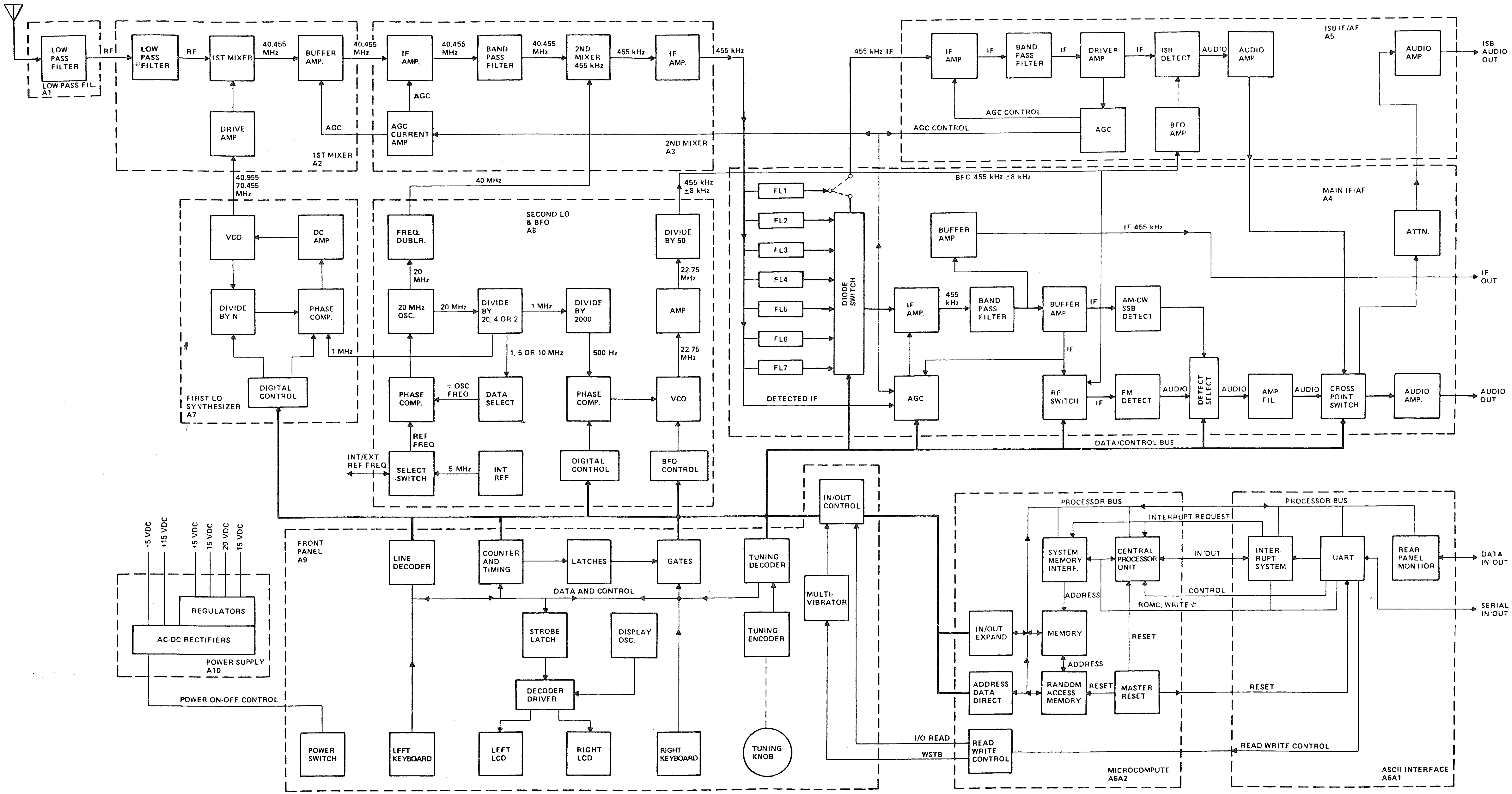


Figure 8-1 Overall, Simplified Functional, Block Diagram

NOTES:
(UNLESS OTHERWISE NOTED)
1. RESISTOR VALUES ARE IN OHMS 1/4 WATT K=1,000 M=1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS, LESS THAN ONE ARE IN MICROFARADS
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND OR ASSEMBLY DESIGN.

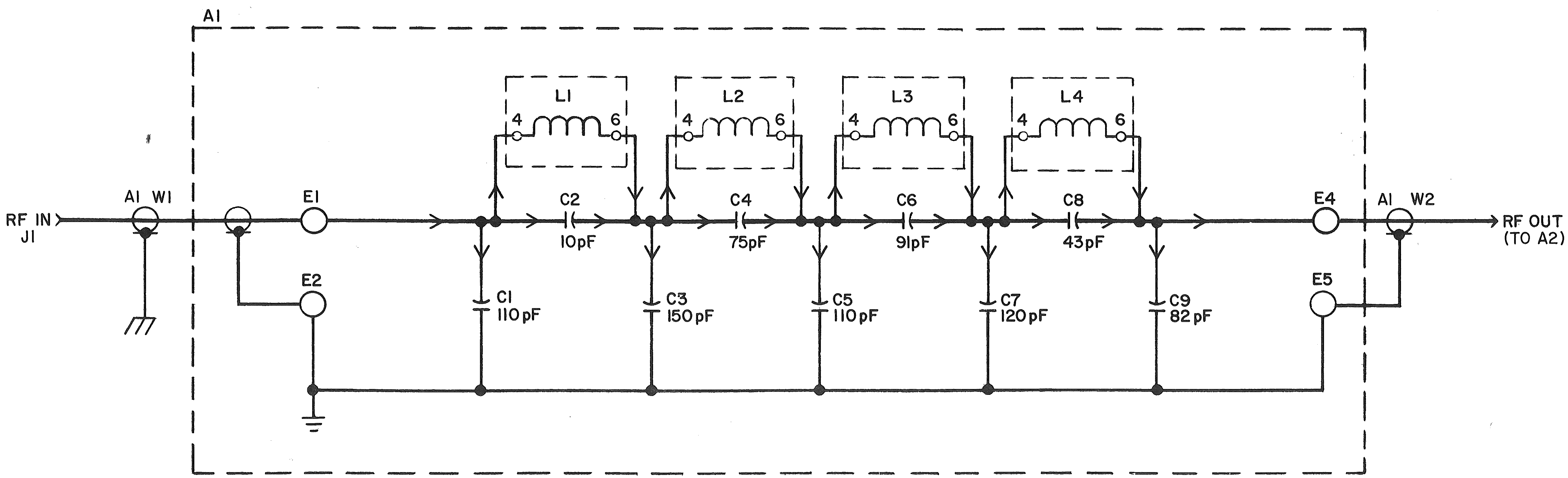


Figure 8-2 Schematic Diagram, RF Low Pass Filter, A1

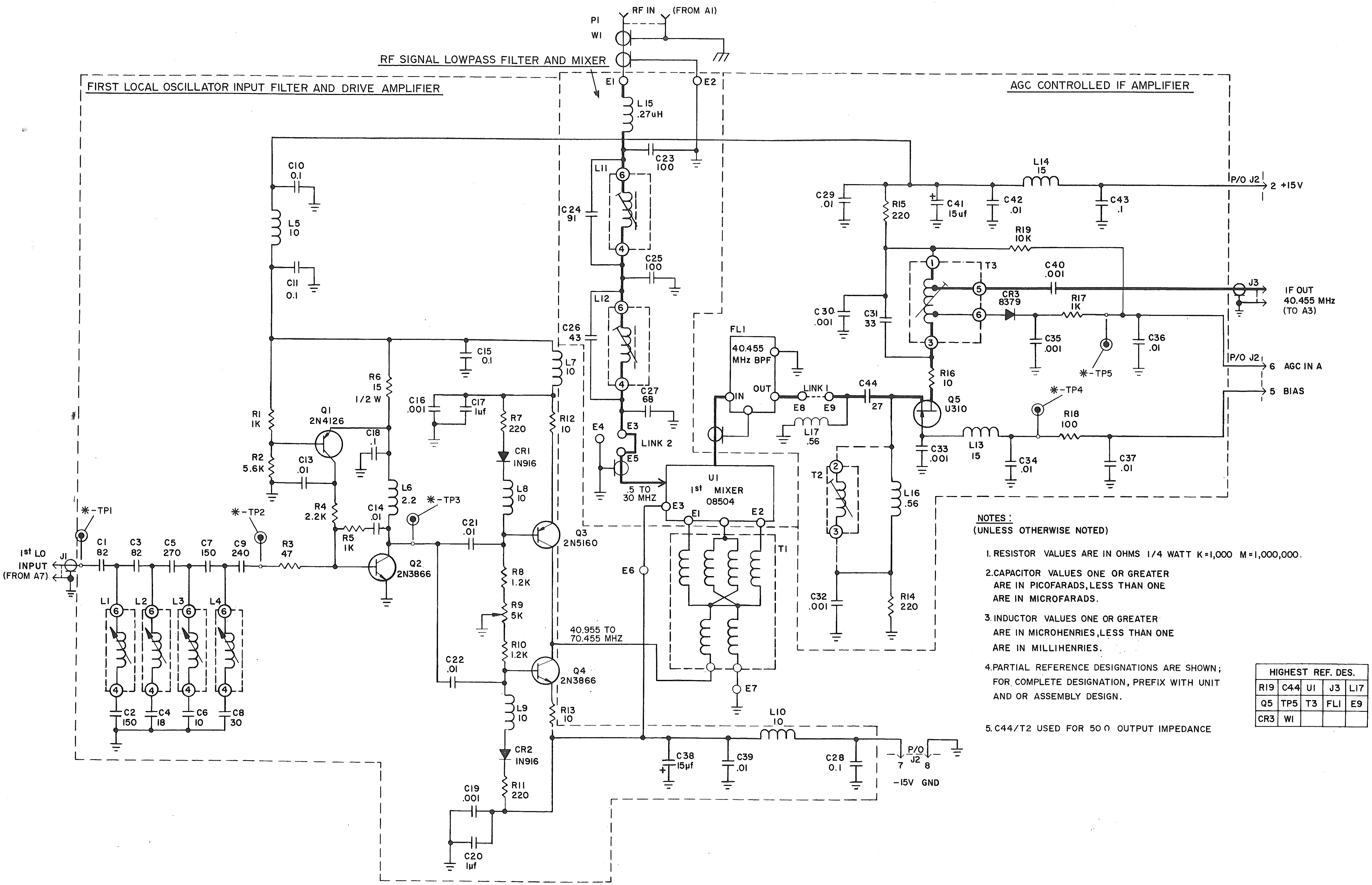
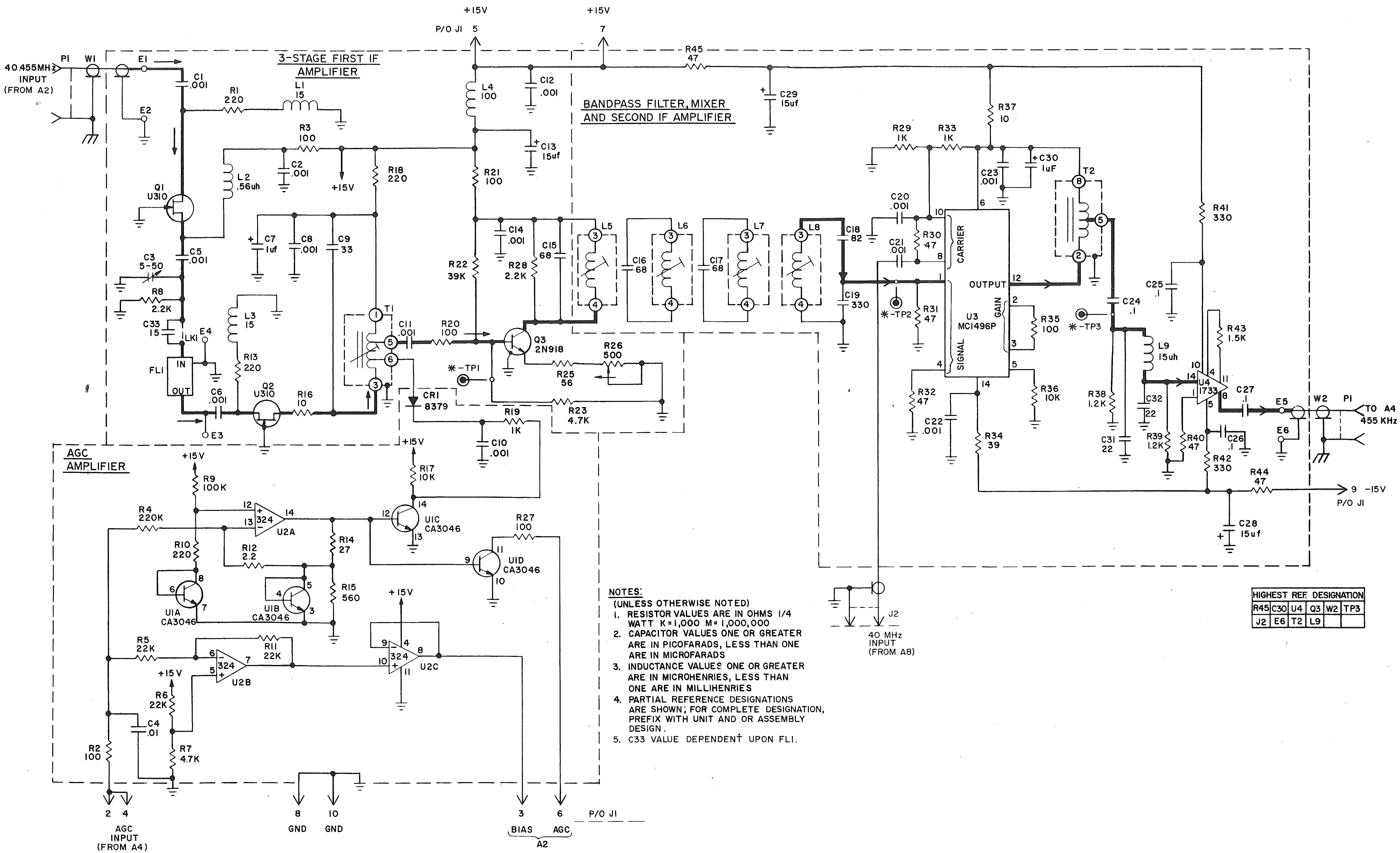


Figure 8-3 Schematic Diagram, 1st Mixer, A2



NOTES:
(UNLESS OTHERWISE NOTED)

1. RESISTOR VALUES ARE IN OHMS 1/4 WATT K=1,000 M=1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS, LESS THAN ONE ARE IN MICROFARADS
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND OR ASSEMBLY DESIGN.
5. C33 VALUE DEPENDENT UPON FL1.

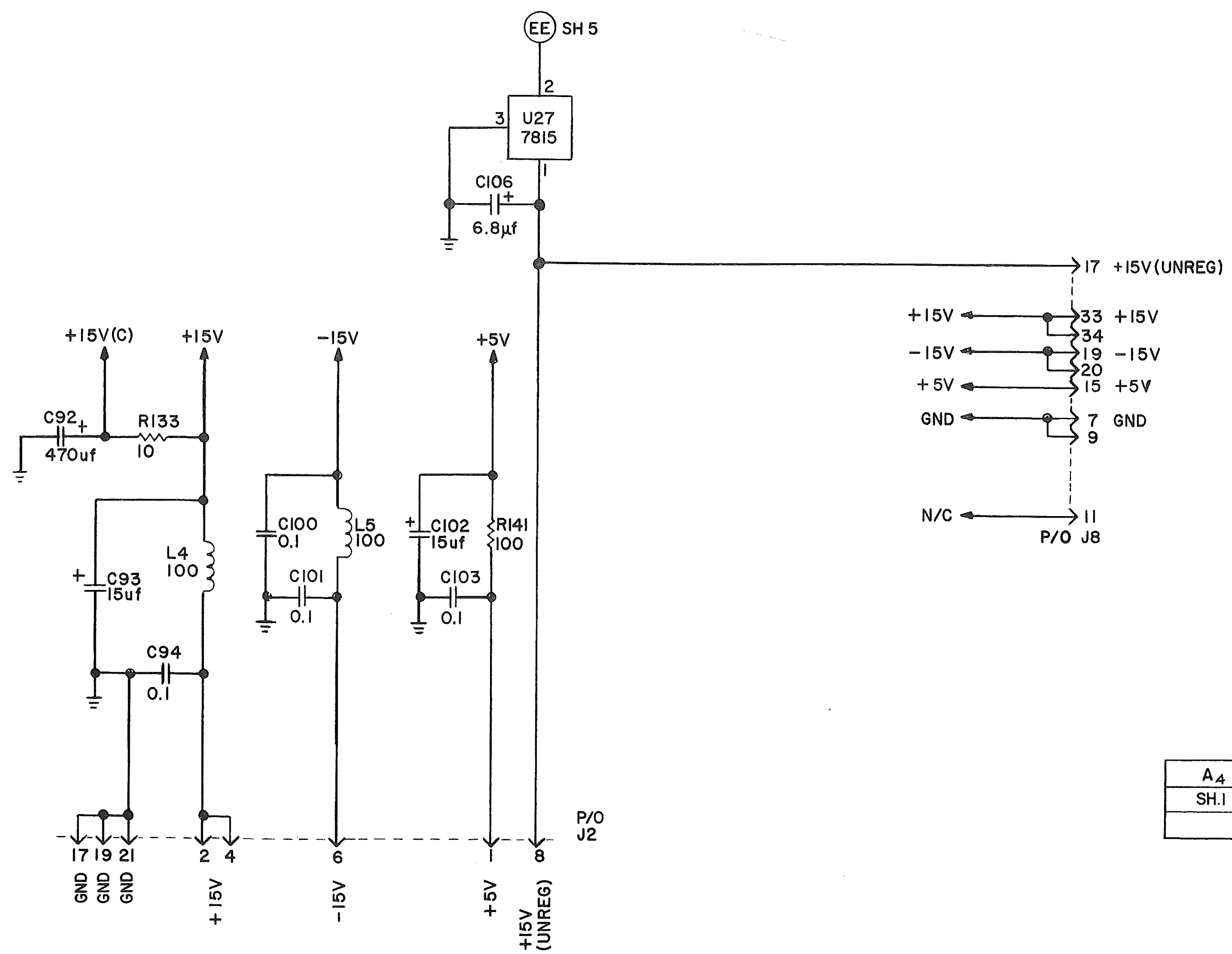
HIGHEST REF DESIGNATION					
R45	C30	U4	Q3	W2	TP3
J2	E6	T2	L9		

Figure 8-4 Schematic Diagram, 2nd Mixer, A3

NOTES: (UNLESS OTHERWISE NOTED)

1. RESISTOR VALUES ARE IN OHMS, K=1,000, M=1,000,000.
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICO FARADS, LESS THAN ONE ARE IN MICROFARADS.
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES LESS THAN ONE ARE IN MILLEHENRIES.
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND OR ASSEMBLY DESIGN.
5. + VALUE DEPENDENT ON FILTER COMPLEMENT.
6. FOR ISB OPERATION CONNECT LINK 1 TO ISB.
7. PROVIDE MUTE ONLY IF MUTE MODULE IS INSTALLED.

I.C. NO.	DEVICE	GND	+15V(B)	+15V(C)	-15V
U7	324	11		4	
U14	324	11		4	
U17	324	11		4	
U9	4013	7		14	
U11	4066	7		14	
U12	4066	7		14	
U19	4053	6, 7, 8		16	
U22	1458			8	4
U24	339	12		3	
U28	1458		8		4
U29	1458	4	8		



A4	A4	A4	A4	A4	A4
SH.1	SH.2	SH.3	SH.4	SH.5	SH.6
REVISION STATUS OF SHEETS					

Figure 8-5 Schematic Diagram, Main IF/AF, A4
(Sheet 1 of 6)

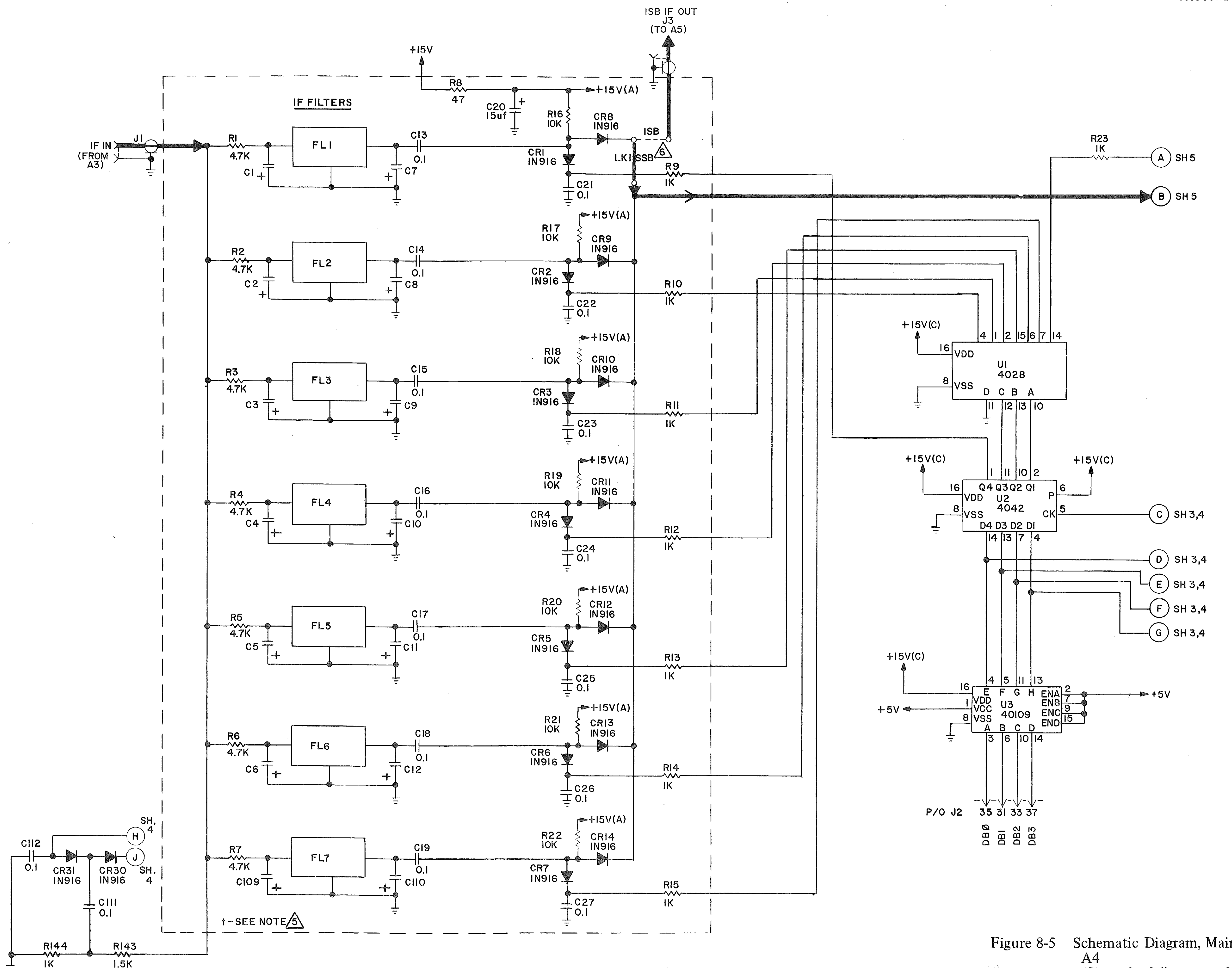


Figure 8-5 Schematic Diagram, Main IF/AF, A4
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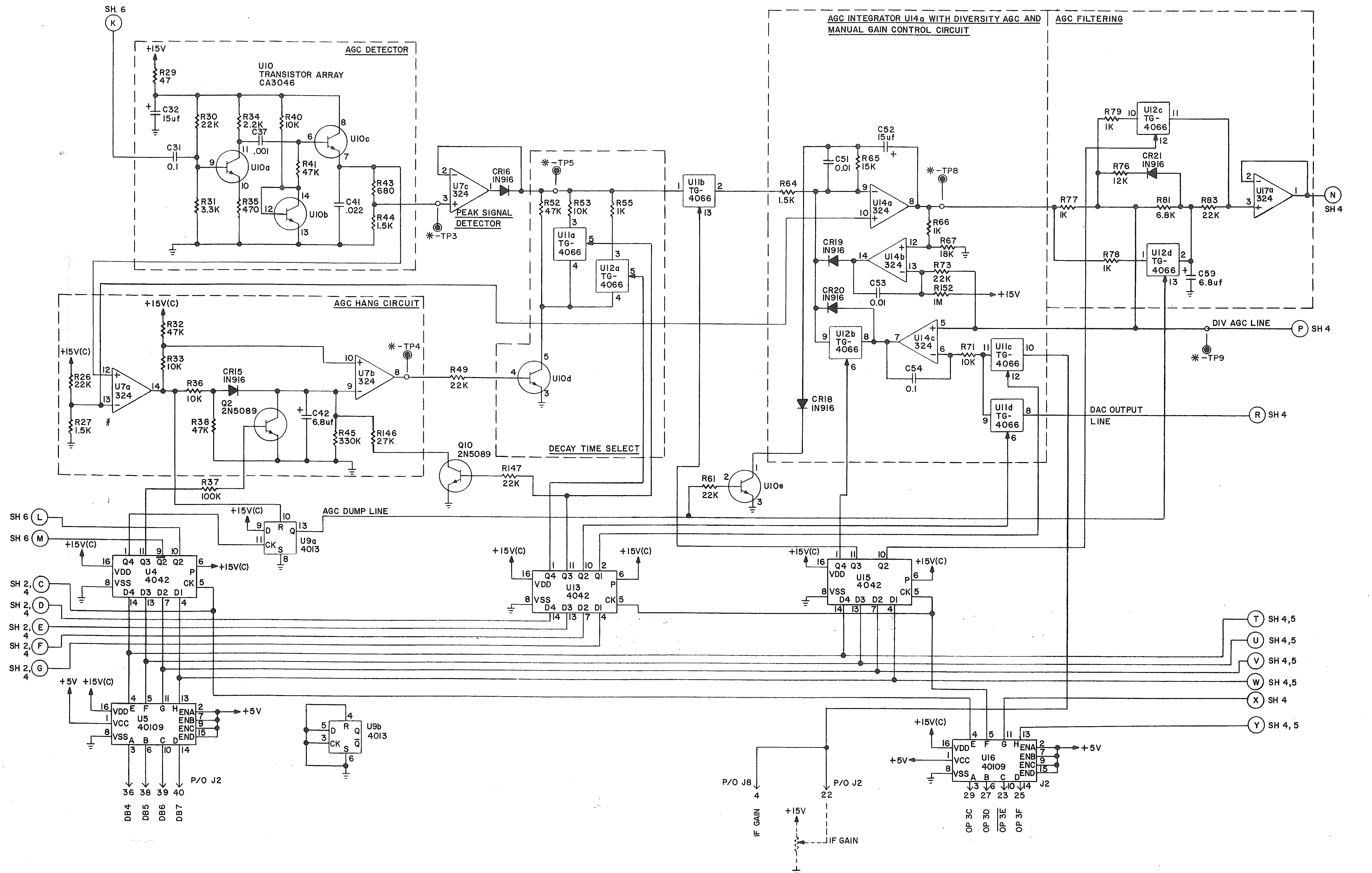


Figure 8-5 Schematic Diagram, Main IF/AF, A4
(Sheet 3 of 6)

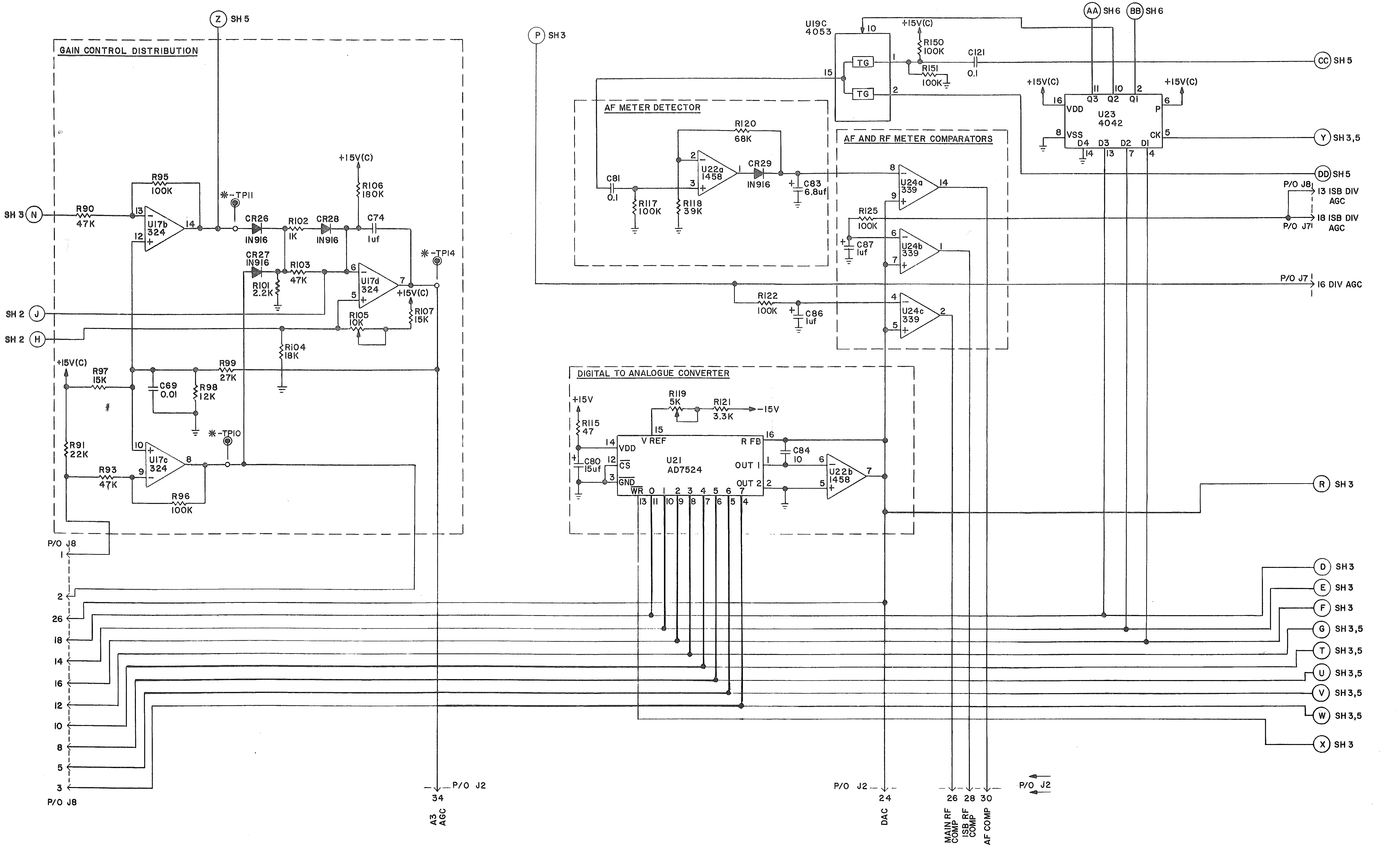


Figure 8-5 Schematic Diagram, Main IF/AF, A4 (Sheet 4 of 6)

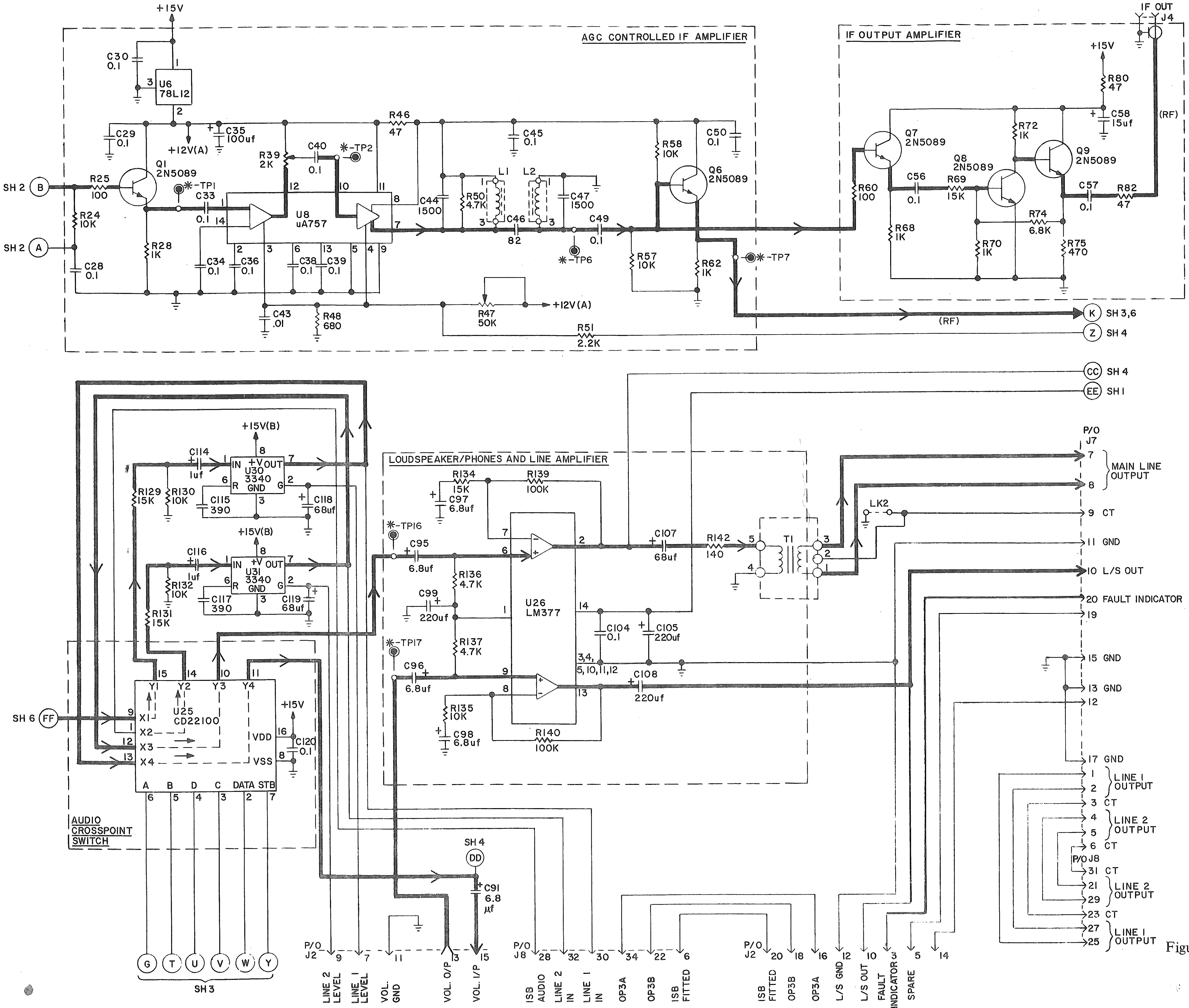


Figure 8-5 Schematic Diagram, Main IF/AF, A4 (Sheet 5 of 6)

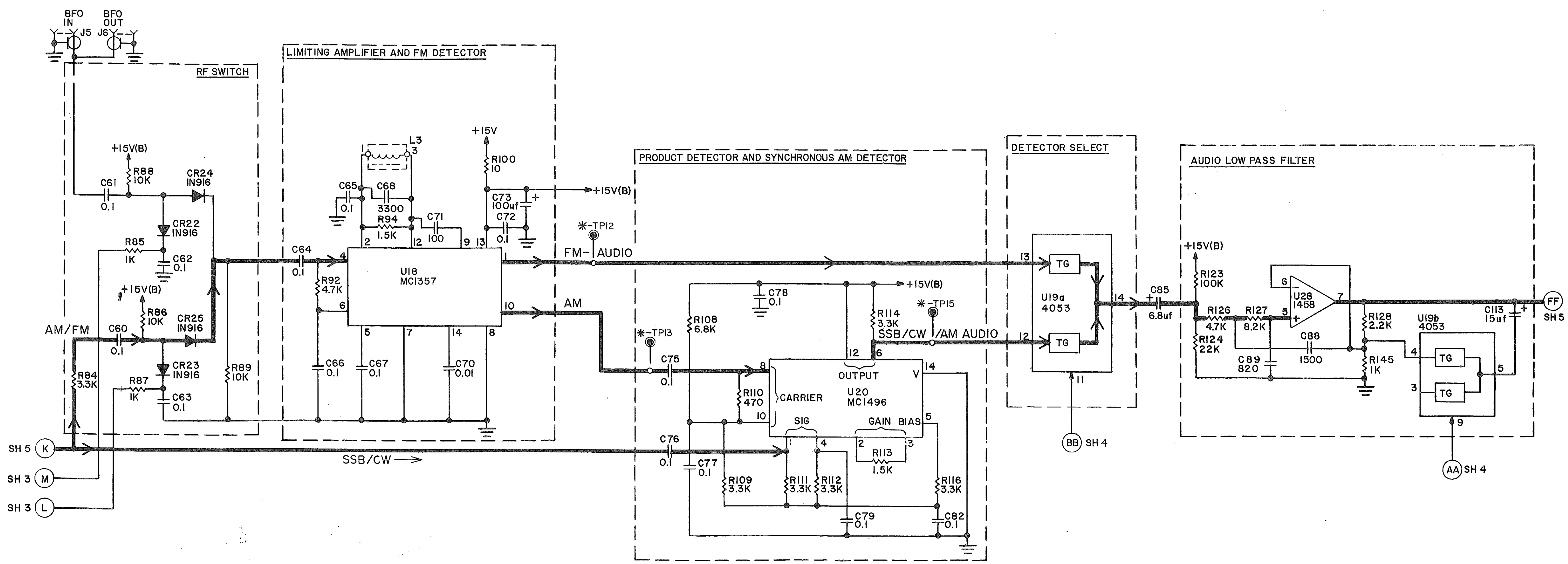
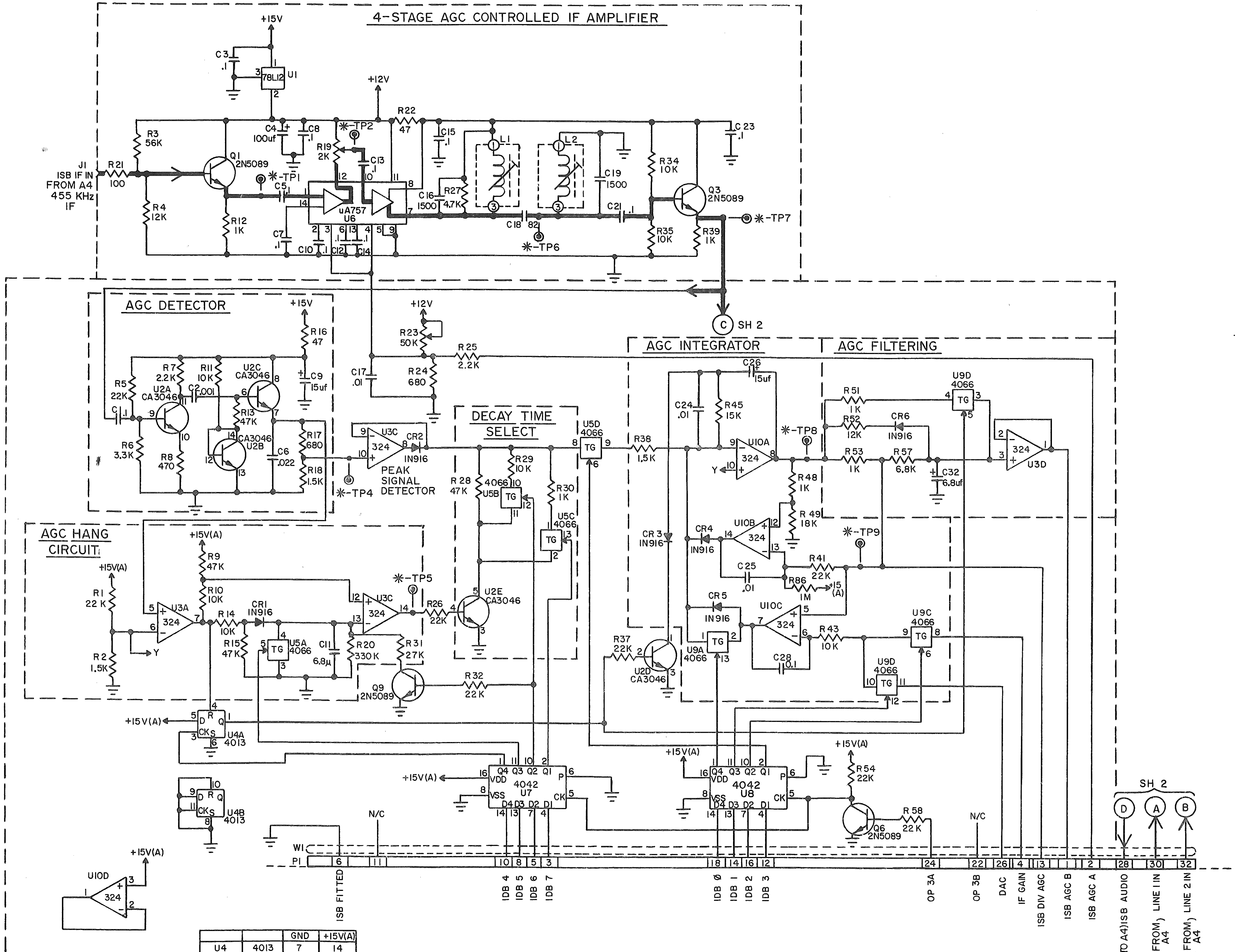


Figure 8-5 Schematic Diagram, Main IF/AF, A4 (Sheet 6 of 6)



		GND	+15V(A)
U4	4013	7	14
U7,U8	4042	8	16
U5,U9	4066	7	14
U3,U10	324	11	4

NOTES:
UNLESS OTHERWISE NOTED:
1. RESISTOR VALUES ARE IN OHMS 1/4 WATT K=1000 M=1,000,000.
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS, LESS THAN ONE ARE IN MICROFARADS.
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES.
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND OR ASSEMBLY DESIGN.

Figure 8-6 Schematic Diagram, ISB, A5 (Optional) (Sheet 1 of 2)

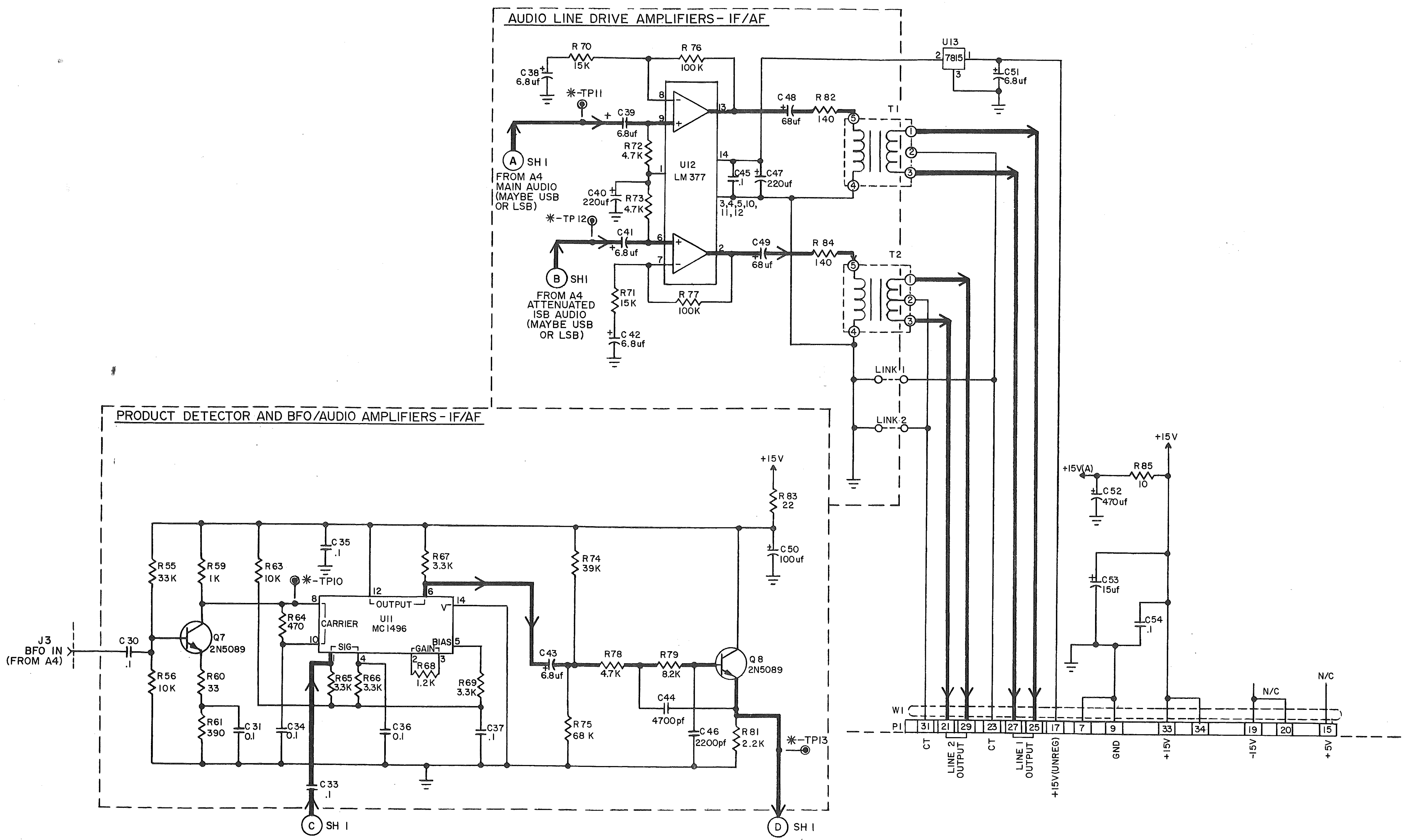


Figure 8-6 Schematic Diagram, ISB, A5 (Optional) (Sheet 2 of 2)

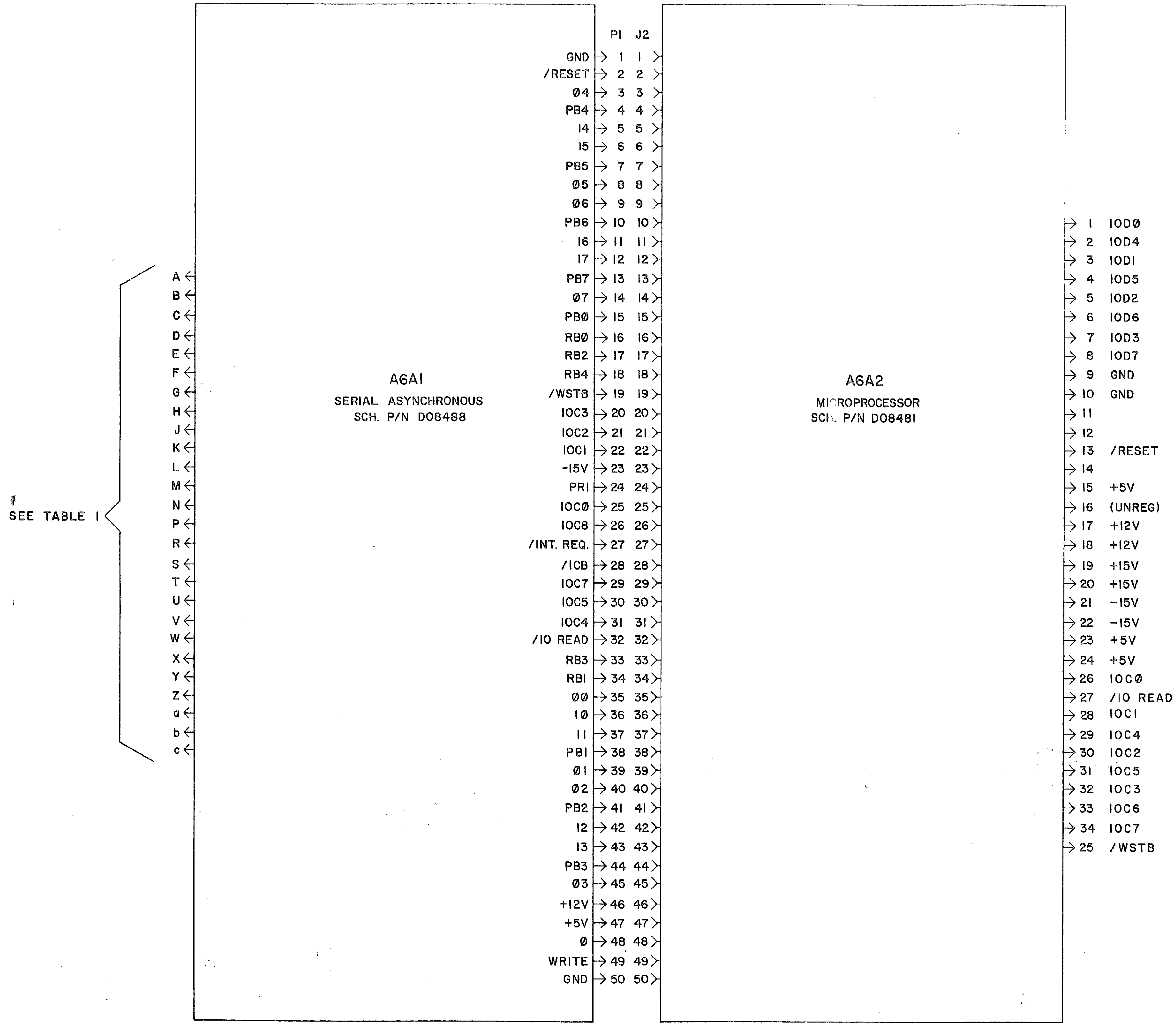
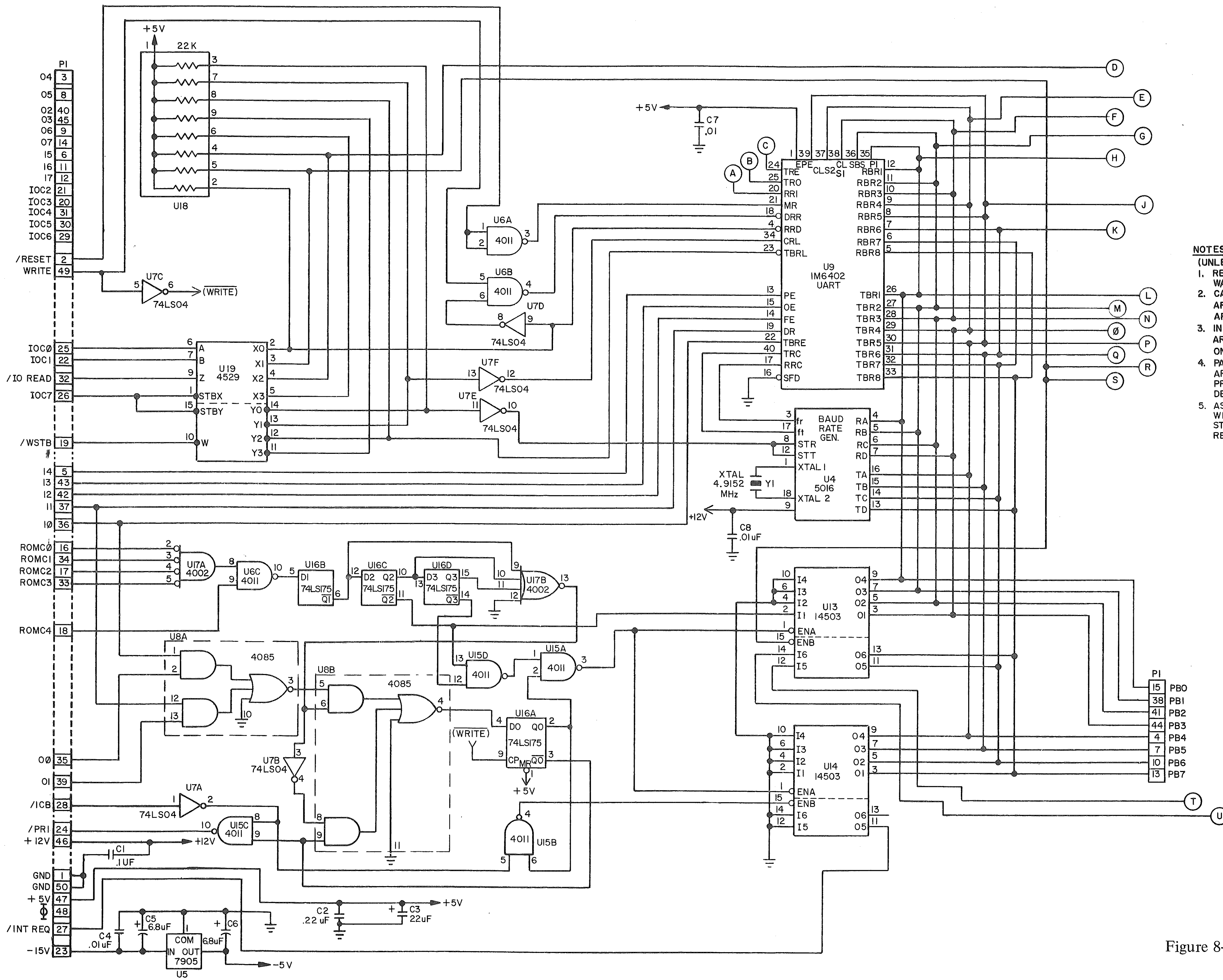


TABLE I

	FUNCTION
A	SYSTEM GND
B	DATA OUT A
C	DATA OUT GND
D	DATA OUT B
E	GND
F	DATA IN A'
G	DATA IN GND
H	DATA IN B'
J	GND
K	RECEIVER NUMBER D1-1
L	RECEIVER NUMBER D1-2
M	RECEIVER NUMBER D1-4
N	RECEIVER NUMBER D1-8
P	RECEIVER NUMBER D2-1
R	RECEIVER NUMBER D2-2
S	RECEIVER NUMBER D2-4
T	RECEIVER NUMBER D2-8
U	/ PARITY SELECT
V	EVEN/ODD PARITY
W	BAUD RATE B4
X	BAUD RATE B3
Y	BAUD RATE B2
Z	BAUD RATE B1
a	GND
b	GND
c	SYSTEM GND

Figure 8-7 Schematic Diagram, Microcomputer Assembly, A6

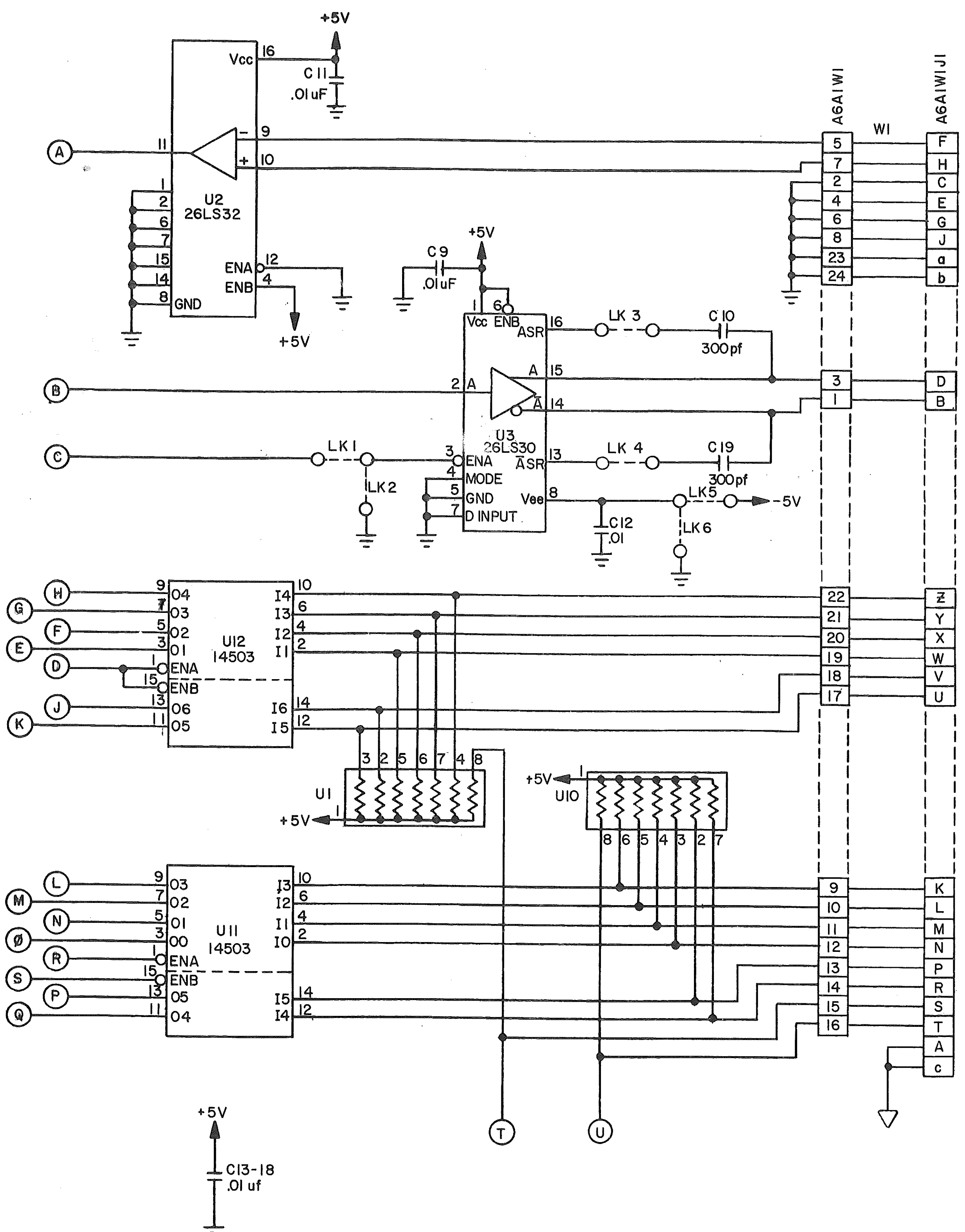


NOTES:
(UNLESS OTHERWISE NOTED)

1. RESISTOR VALUES ARE IN OHMS 1/4 WATT K=1,000 M=1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS, LESS THAN ONE ARE IN MICROFARADS
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND OR ASSEMBLY DESIGN.
5. AS SUPPLIED, THE DATA OUTPUT DRIVER IS WIRED FOR TRI-STATE OPERATION. THE TRI-STATE SYSTEM MAY BE DISABLED BY REMOVING LINK 1 AND INSTALLING LINK 2.

A2	A2
SH. 1	SH. 2
REVISION STATUS OF SHEETS	

Figure 8-8 Schematic Diagram, Serial Asynchronous Interface, A6A1 (Optional) (Sheet 1 of 2)



	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15	U16	U17	U18	U19
GND	–	8	5	11	1	7	7	7	3	–	8	8	8	8	7	8	7	–	8
+5V	1	16	1	2	–	14	14	14	1	1	16	16	16	16	14	16	14	1	16
+12V	–	–	–	9	–	–	–	–	–	–		–	–	–	–	–	–	–	–
-5V	–	–	8	–	2	–	–	–	–	–	–	–	–	–	–	–	–	–	–

TABLE I

J1 PINS	FUNCTION
A	SYSTEM GND
B	DATA OUT A
C	DATA OUT GND
D	DATA OUT B
E	GND
F	DATA IN A'
G	DATA IN GND
H	DATA IN B'
J	GND
K	RECEIVER NUMBER D1-1
L	RECEIVER NUMBER D1-2
M	RECEIVER NUMBER D1-4
N	RECEIVER NUMBER D1-8
P	RECEIVER NUMBER D2-1
R	RECEIVER NUMBER D2-2
S	RECEIVER NUMBER D2-4
T	RECEIVER NUMBER D2-8
U	/PARITY SELECT
V	EVEN/ODD PARITY
W	BAUD RATE B4
X	BAUD RATE B3
Y	BAUD RATE B2
Z	BAUD RATE B1
a	GND
b	GND
c	SYSTEM GND

TABLE II DATA CONNECTION

J1 PINS	MS188C	RS232C RS423	RS422
A	SYSTEM GND	SYSTEM GND	SYSTEM GND
B	N.U.	DATA OUT A	DATA OUT A
C	DATA OUT GND	DATA OUT GND	N.U.
D	DATA OUT	N.U.	DATA OUT B
E	JUMPER TO 'F'	N.U.	N.U.
F	JUMPER TO 'E'	DATA IN A'	DATA IN A'
G	DATA IN GND	DATA IN GND	N.U.
H	DATA IN	JUMPER TO 'J'	DATA IN B'
J	N.U.	JUMPER TO 'H'	N.U.

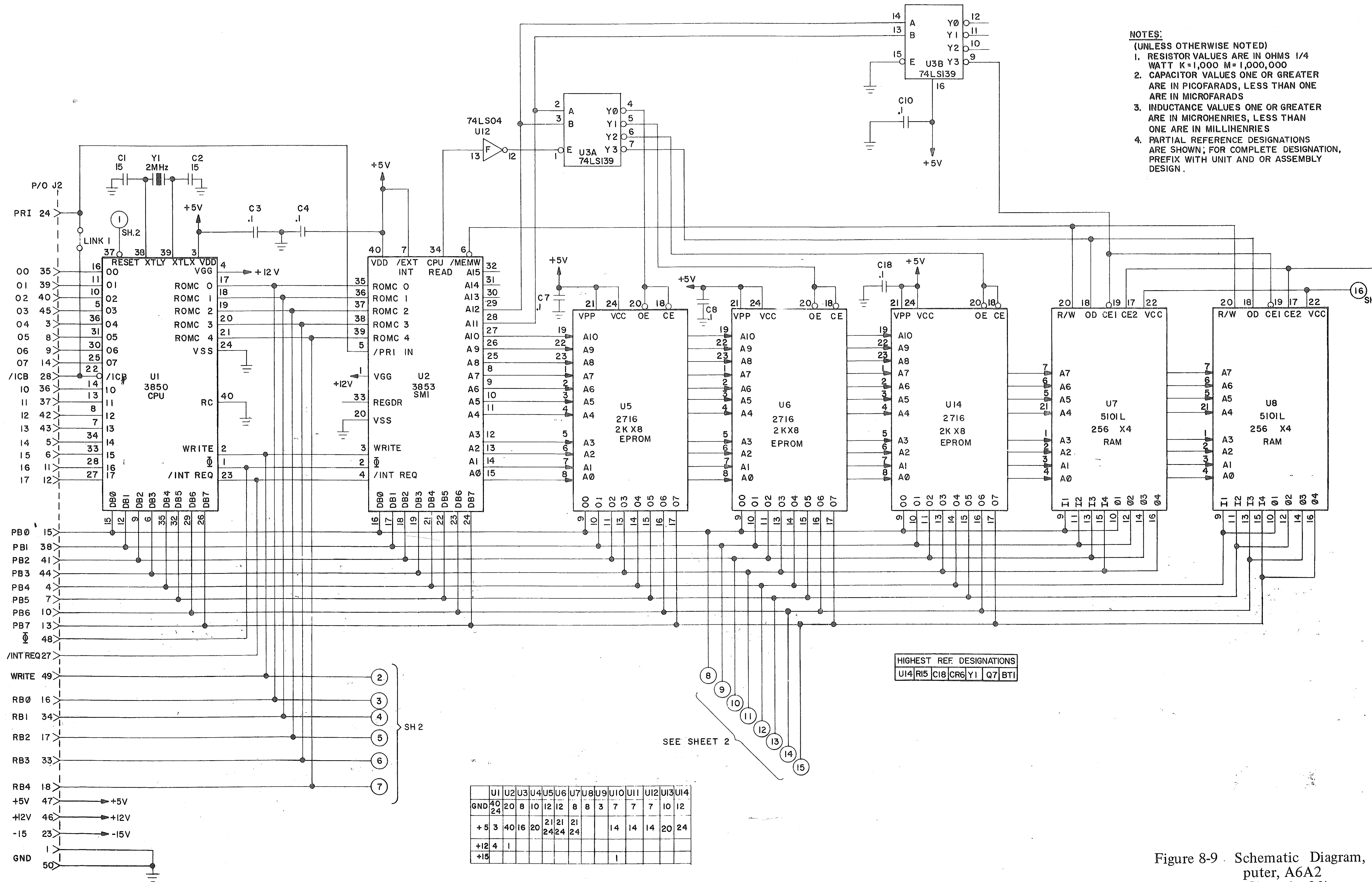
TABLE III
BAUD RATE SELECTION

DATA RATE SELECTION BIT W	X	Y	Z	DATA RATE (BAUD)
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

TABLE IV

LINK NO.	188C/232C/423	422
LK1	INSTALL	INSTALL
LK2	DELETE	DELETE
LK3	INSTALL	DELETE
LK4	INSTALL	DELETE
LK5	INSTALL	DELETE
LK6	DELETE	INSTALL

Figure 8-8 Schematic Diagram, Serial Asynchronous Interface, A6A1 (Optional) (Sheet 2 of 2)



NOTES:
(UNLESS OTHERWISE NOTED)
1. RESISTOR VALUES ARE IN OHMS 1/4 WATT K=1,000 M=1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS, LESS THAN ONE ARE IN MICROFARADS
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND OR ASSEMBLY DESIGN.

HIGHEST REF. DESIGNATIONS						
U14	R15	C18	CR6	Y1	Q7	BT1

	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14
GND	40 24	20	8	10	12	12	8	8	3	7	7	7	10	12
+5	3	40	16	20	21 24	21 24	21 24			14	14	14	20	24
+12	4	1												
+15										1				

Figure 8-9. Schematic Diagram, Microcomputer, A6A2 (Sheet 1 of 2)

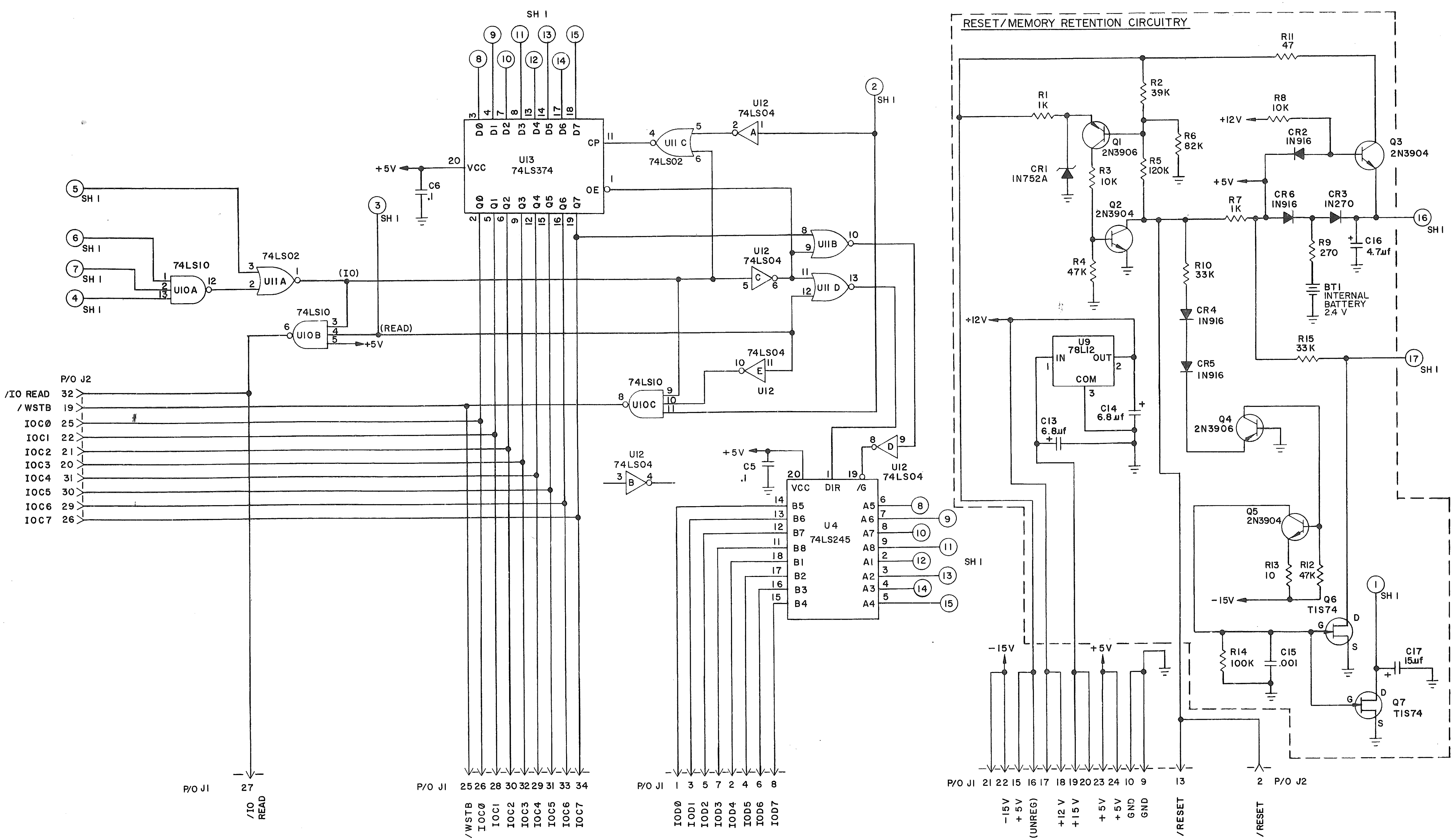
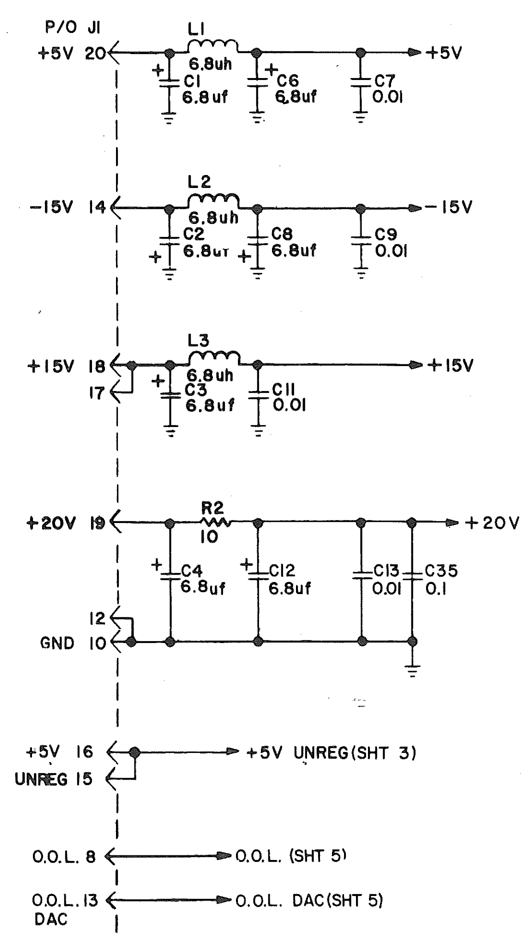


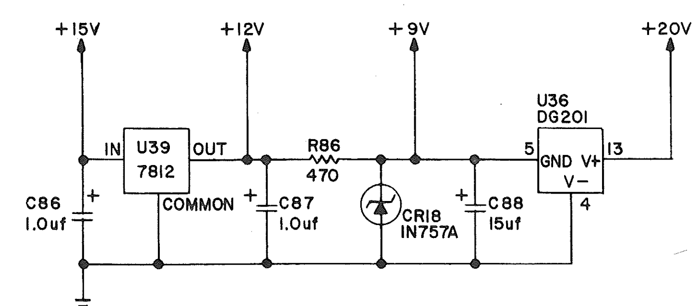
Figure 8-9 Schematic Diagram, Microcomputer, A6A2 (Sheet 2 of 2)

NOTES: (UNLESS OTHERWISE NOTED)

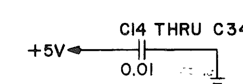
1. RESISTOR VALUES ARE IN OHMS; K=1,000; M=1,000,000.
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS. LESS THAN ONE ARE IN MICROFARADS.
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES.
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND OR ASSEMBLY DESIGN.

	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15	U16	U17	U18	U19	U20	U21	U22	U23
LOC	J16	*	*	*	G14	D14	*	H12	H12	G12	F12	E12	D12	C12	F9	E9	D9	F7	*	F6	E6	H4	H3
GND	7	8	8	7	8	8	7	8	8	8	8	8	8	8	8	–	8	8	7	7	7	12	—
+5V	14	16	16	14	16	16	14	16	16	16	16	16	16	16	16	1	16	16	14	14	14	24	—





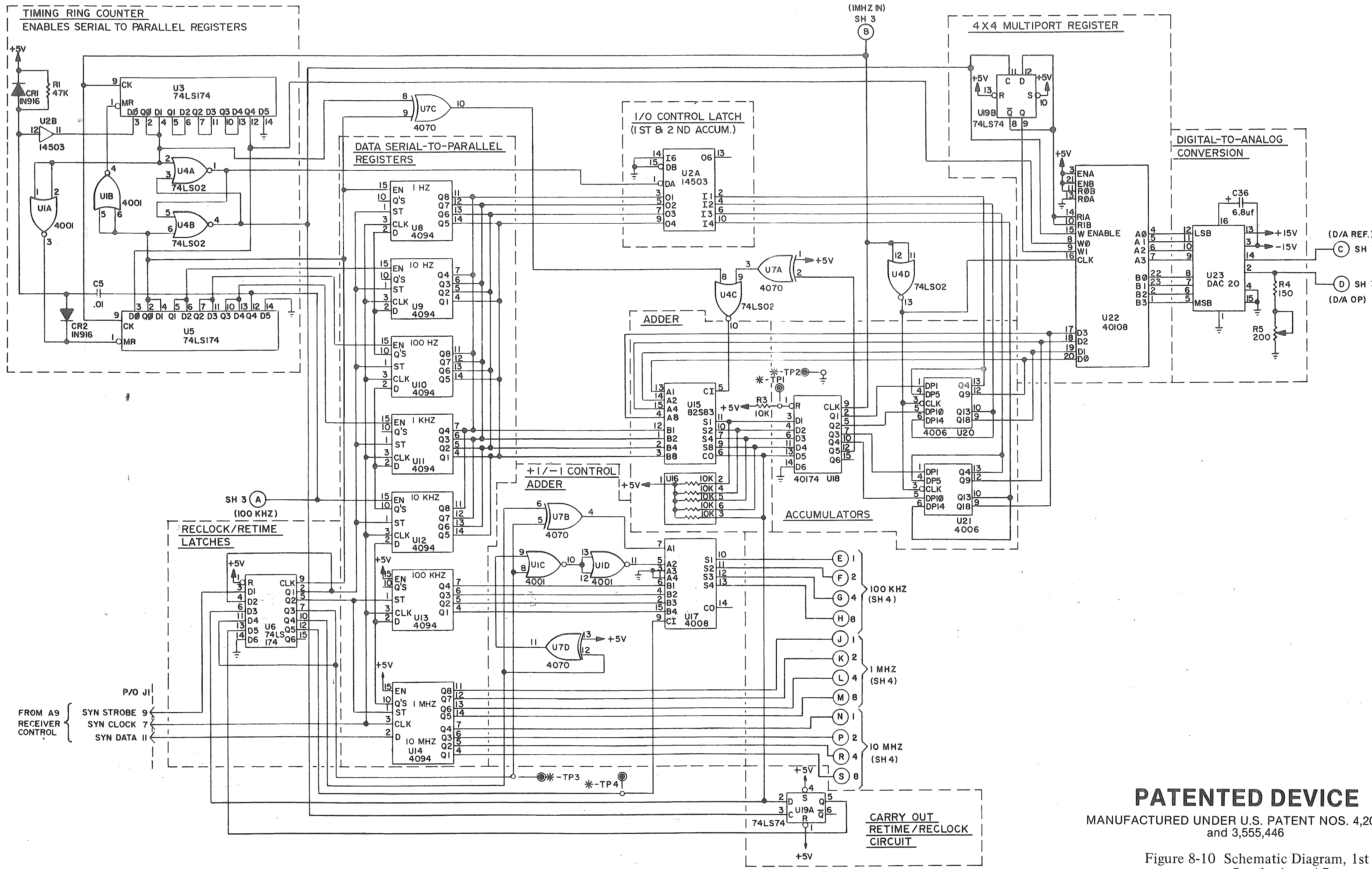
HIGHEST REF. DES.						
C104	R95	L6	U40	Q13	TP13	CR21
T1	J4					



PATENTED DEVICE

MANUFACTURED UNDER U.S. PATENT NOS. 4,204,174 and 3,555,446

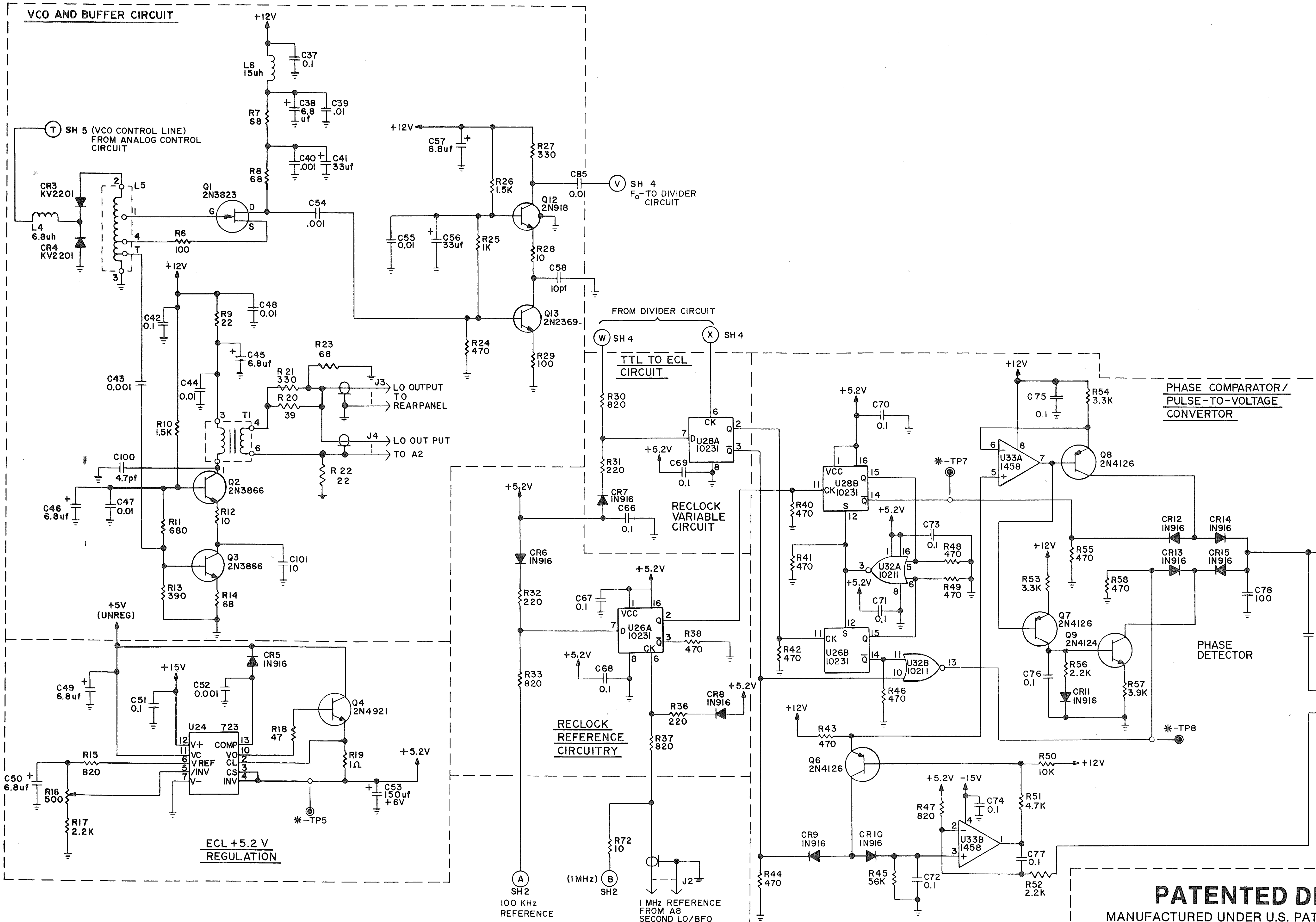
Figure 8-10 Schematic Diagram, 1st LO Synthesizer, A7 (Sheet 1 of 5)



PATENTED DEVICE

MANUFACTURED UNDER U.S. PATENT NOS. 4,204,174 and 3,555,446

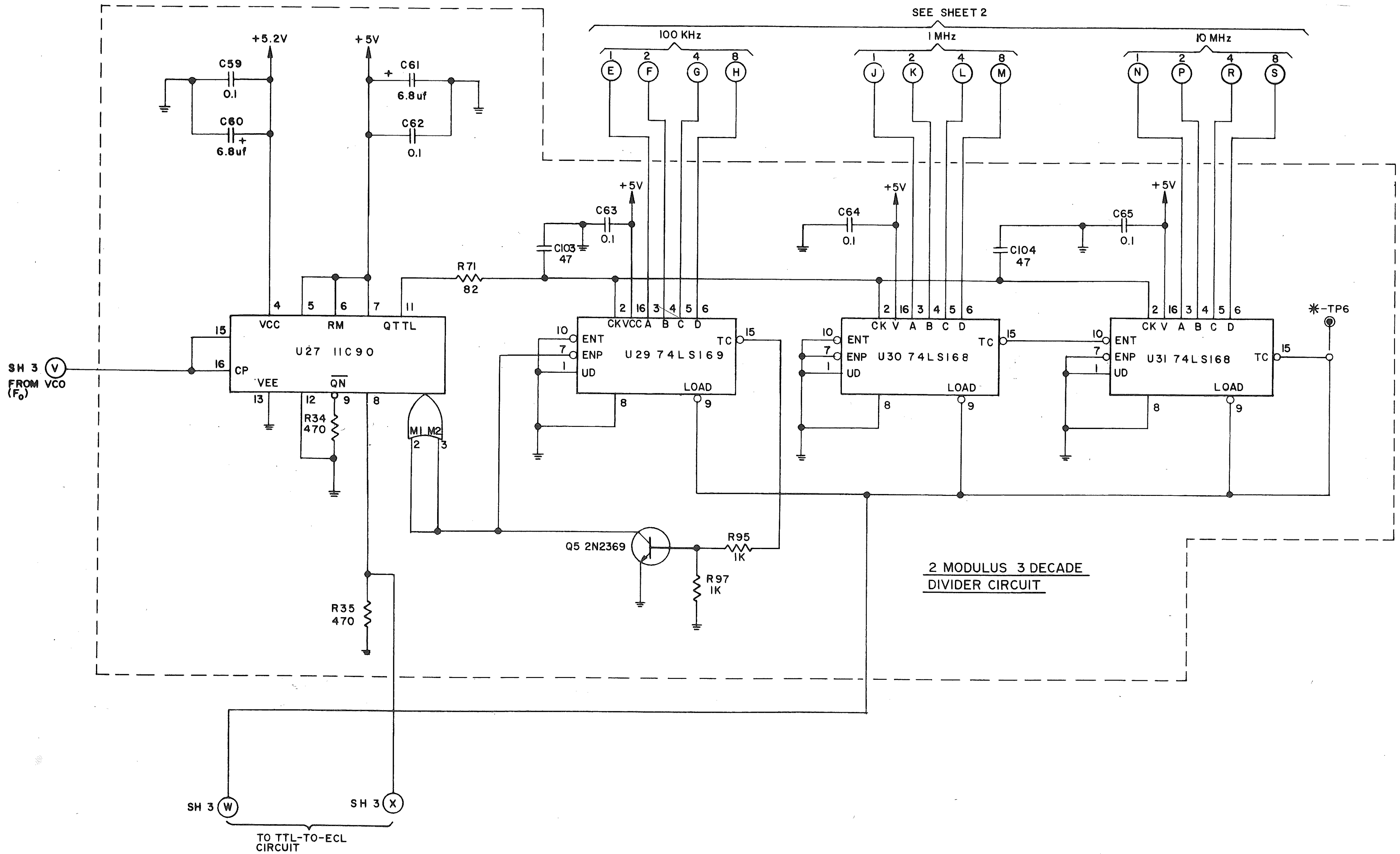
Figure 8-10 Schematic Diagram, 1st LO Synthesizer, A7 (Sheet 2 of 5)



PATENTED DEVICE

MANUFACTURED UNDER U.S. PATENT NOS. 4,204,174 and 3,555,446

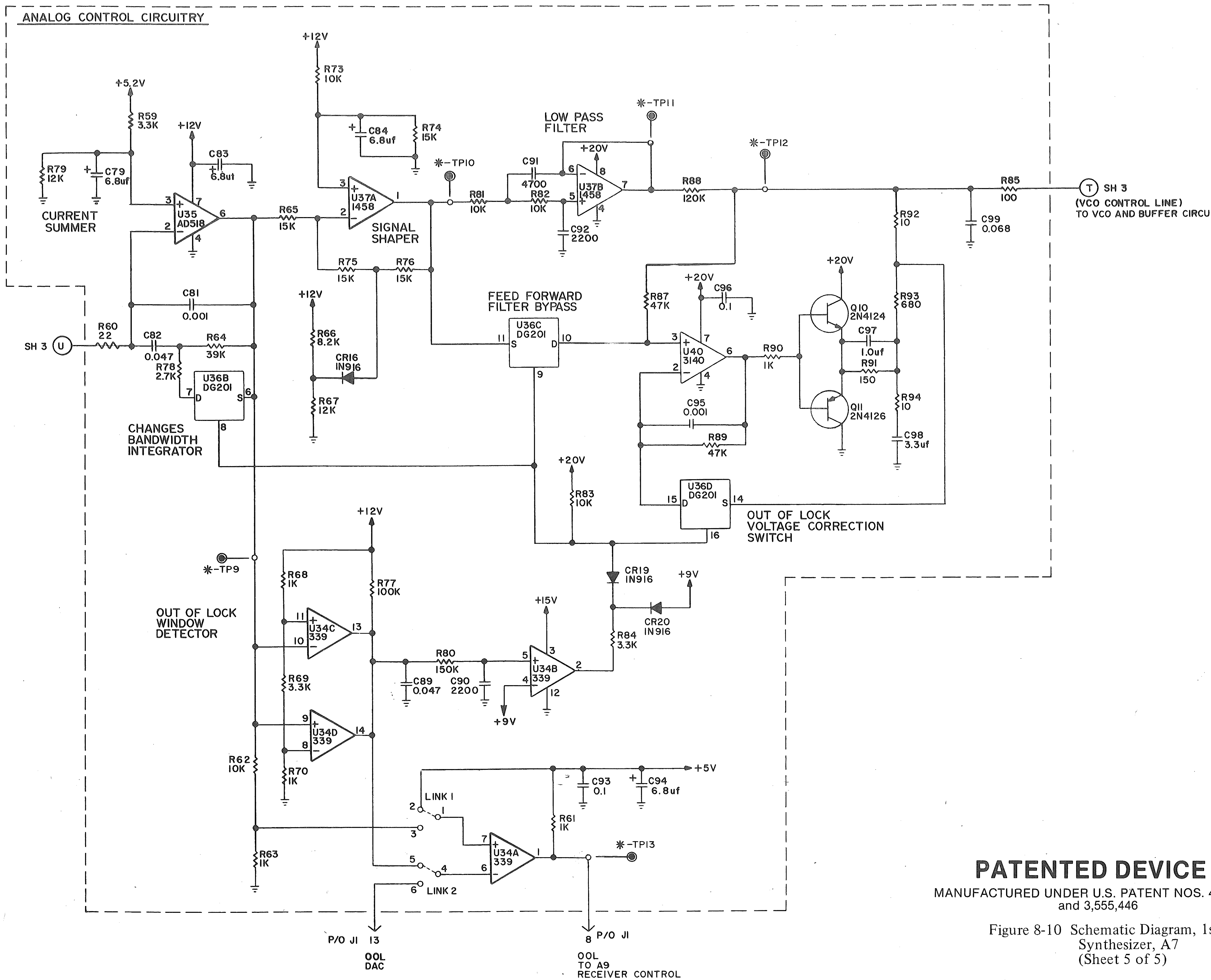
Figure 8-10 Schematic Diagram, 1st LO Synthesizer, A7 (Sheet 3 of 5)



PATENTED DEVICE

MANUFACTURED UNDER U.S. PATENT NOS. 4,204,174 and 3,555,446

Figure 8-10 Schematic Diagram, 1st LO Synthesizer, A7 (Sheet 4 of 5)



PATENTED DEVICE

MANUFACTURED UNDER U.S. PATENT NOS. 4,204,174 and 3,555,446

Figure 8-10 Schematic Diagram, 1st LO Synthesizer, A7 (Sheet 5 of 5)

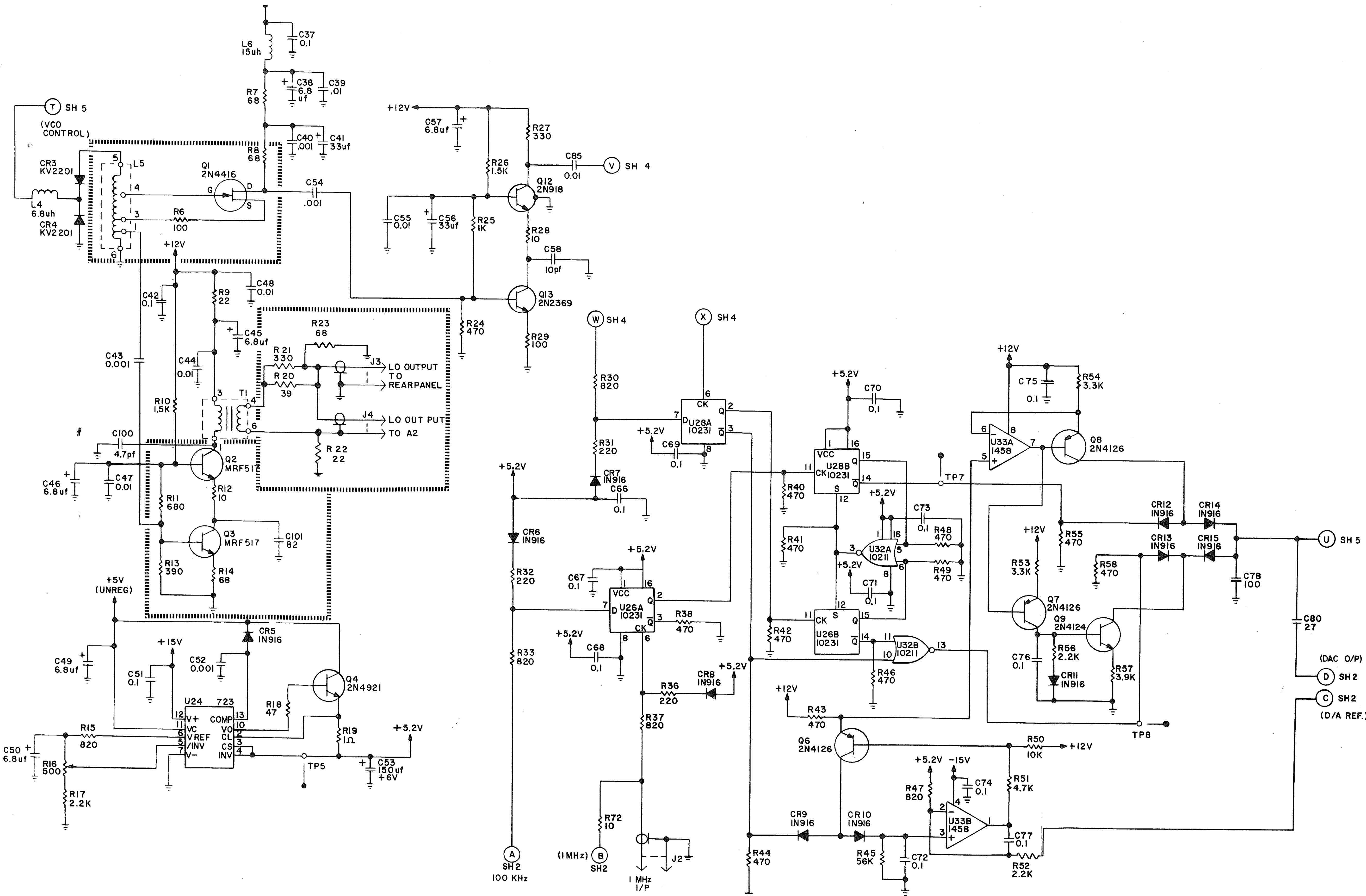


Figure 8-10.1 Schematic Diagram, 1st LO Synthesizer, A7 (Sheet 3 of 5)

NOTES:
(UNLESS OTHERWISE NOTED)
1. RESISTOR VALUES ARE IN OHMS 1/4 WATT K=1,000 M=1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS, LESS THAN ONE ARE IN MICROFARADS
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND OR ASSEMBLY DESIGN.

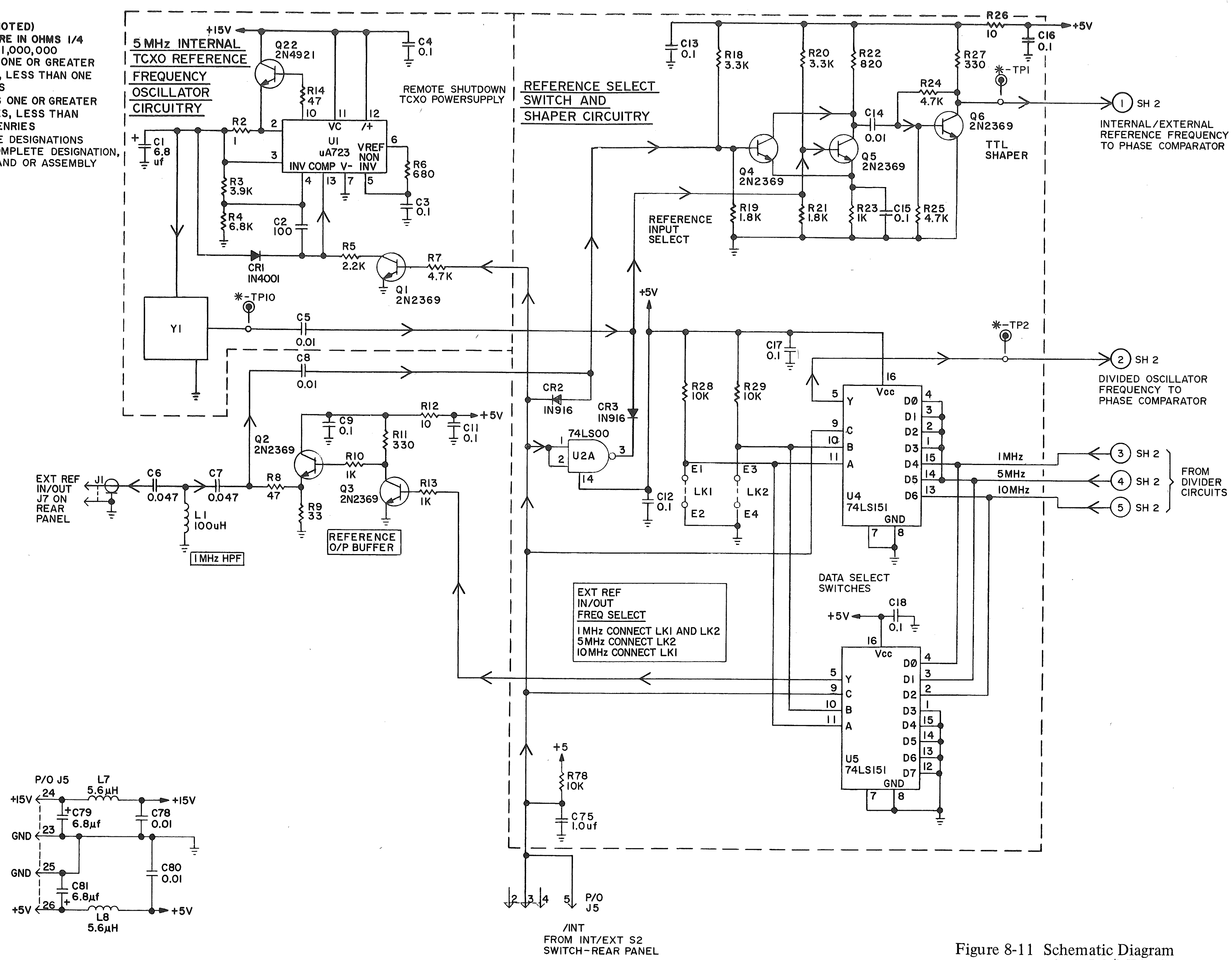


Figure 8-11 Schematic Diagram 2nd LO/BFO Synthesizer, A8 (Sheet 1 of 3)

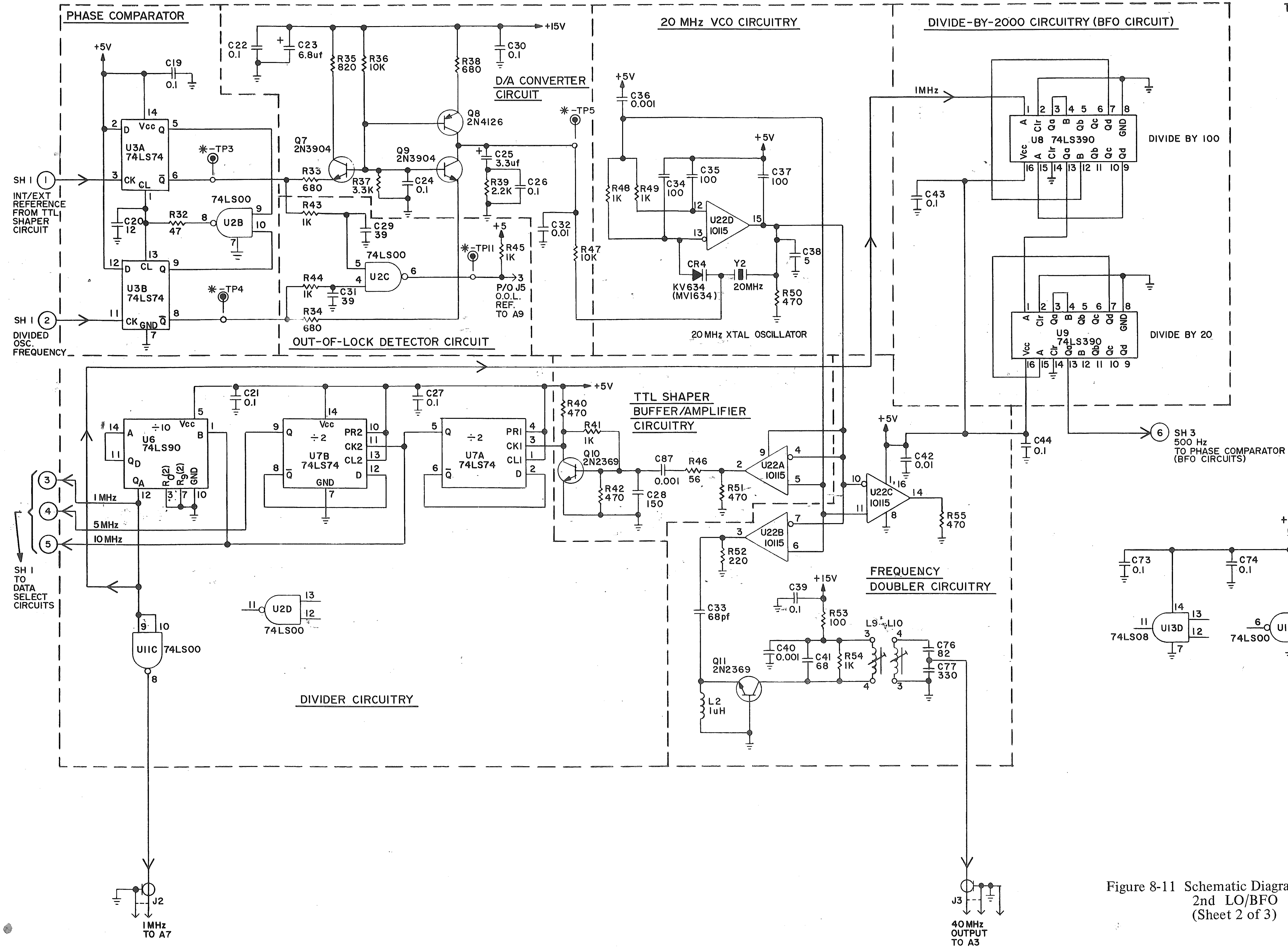


Figure 8-11 Schematic Diagram
2nd LO/BFO Synthesizer, A8
(Sheet 2 of 3)

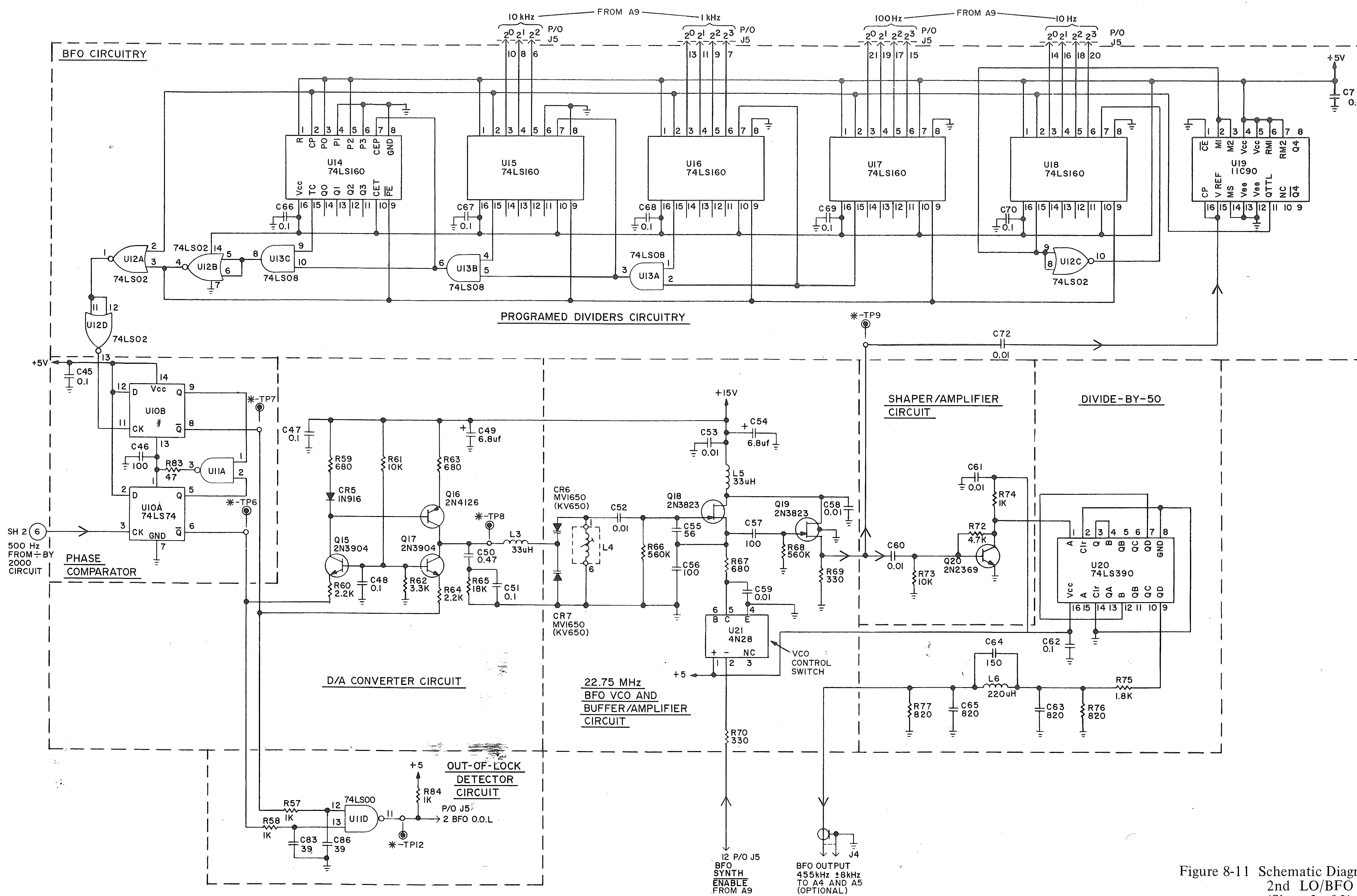


Figure 8-11 Schematic Diagram
2nd LO/BFO Synthesizer, A8
(Sheet 3 of 3)

NOTES:
(UNLESS OTHERWISE NOTED)
1. RESISTOR VALUES ARE IN OHMS 1/4 WATT K = 1,000 M = 1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS, LESS THAN ONE ARE IN MICROFARADS
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND OR ASSEMBLY DESIGN.
5. ASTERICKS INDICATE OPTIONAL PARTS.

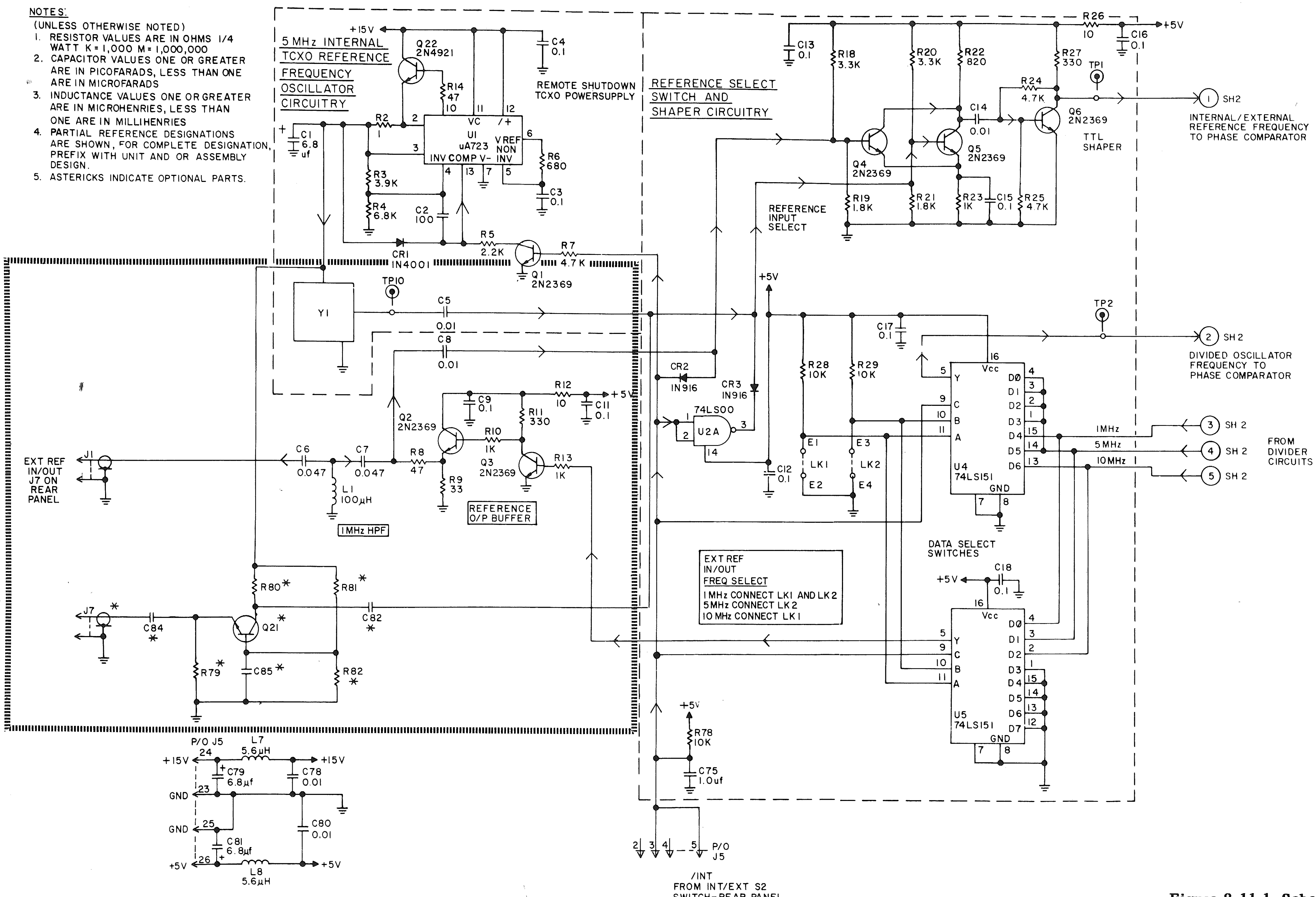


Figure 8-11.1 Schematic Diagram 2nd LO/BFO Synthesizer, A8 (Sheet 1 of 3)

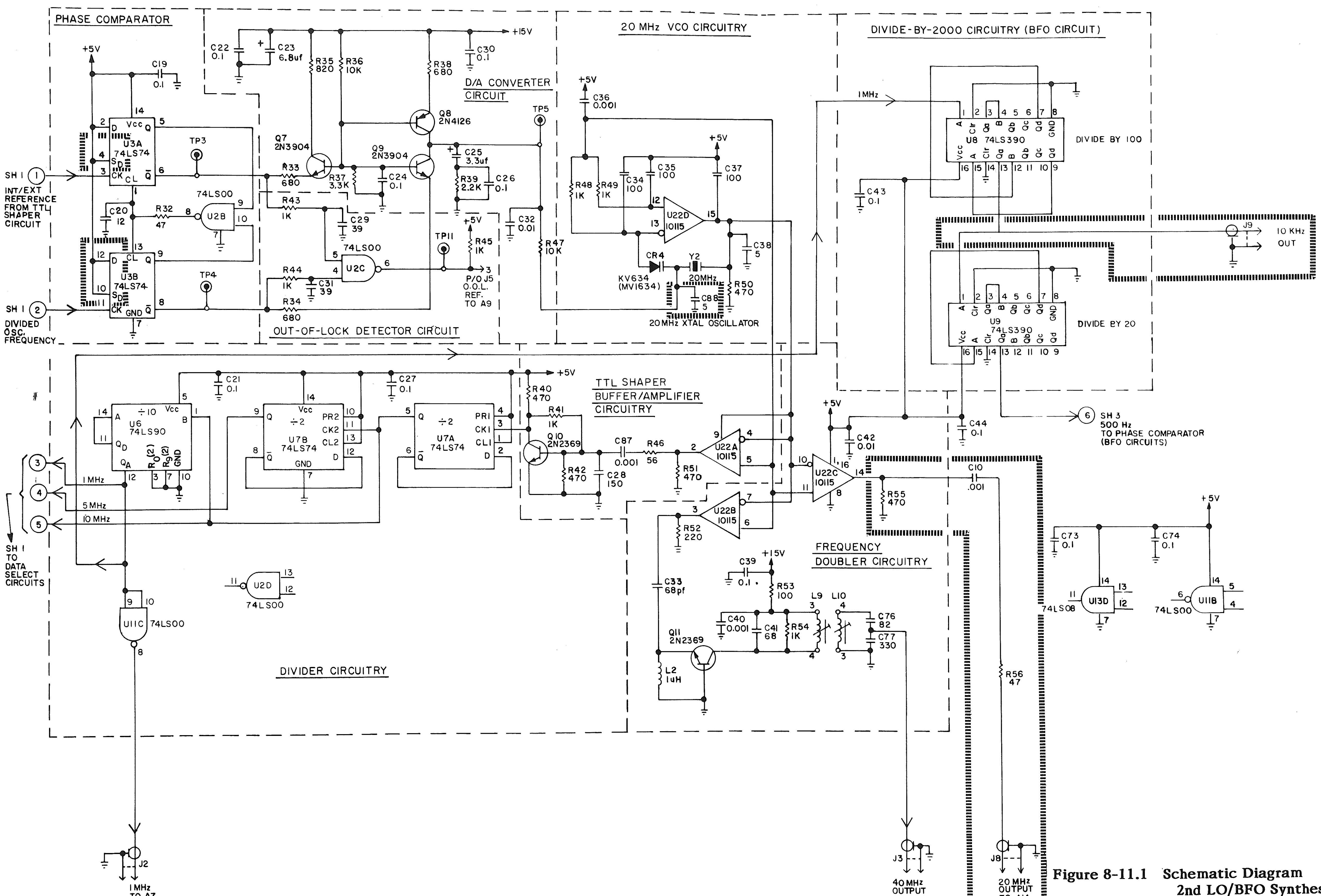


Figure 8-11.1 Schematic Diagram 2nd LO/BFO Synthesizer, A8 (Sheet 2 of 3)

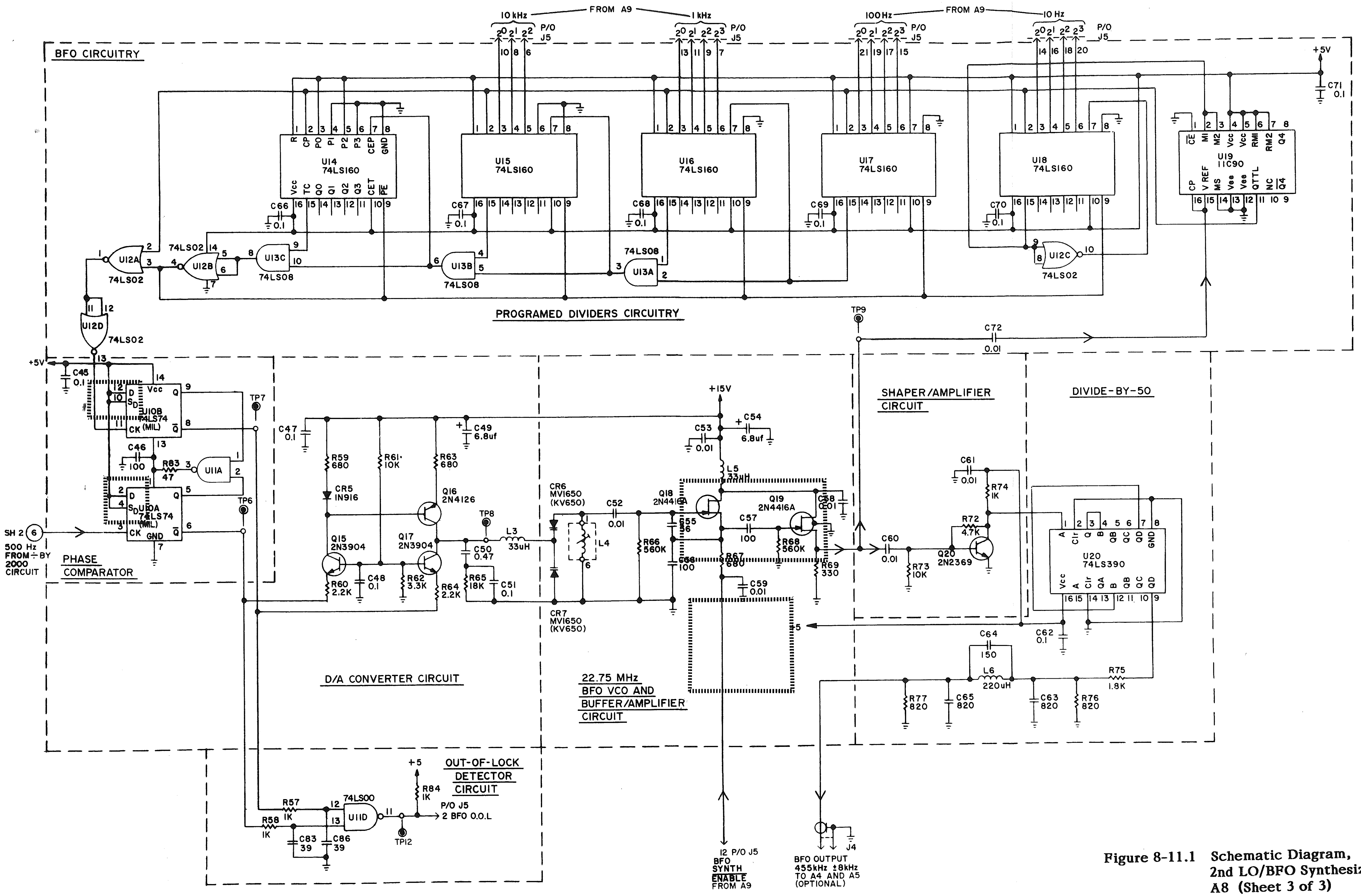
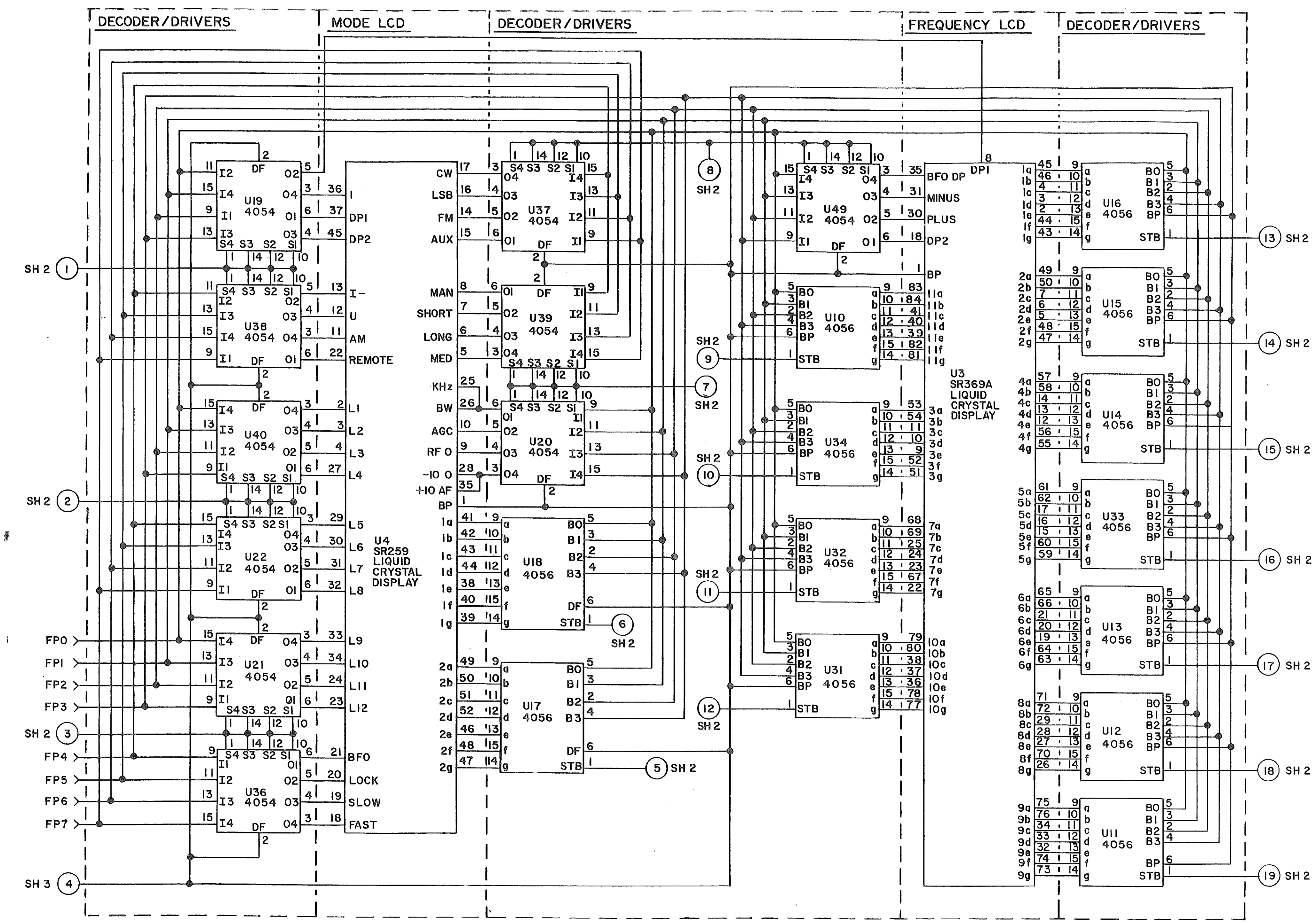


Figure 8-11.1 Schematic Diagram, 2nd LO/BFO Synthesizer, A8 (Sheet 3 of 3)



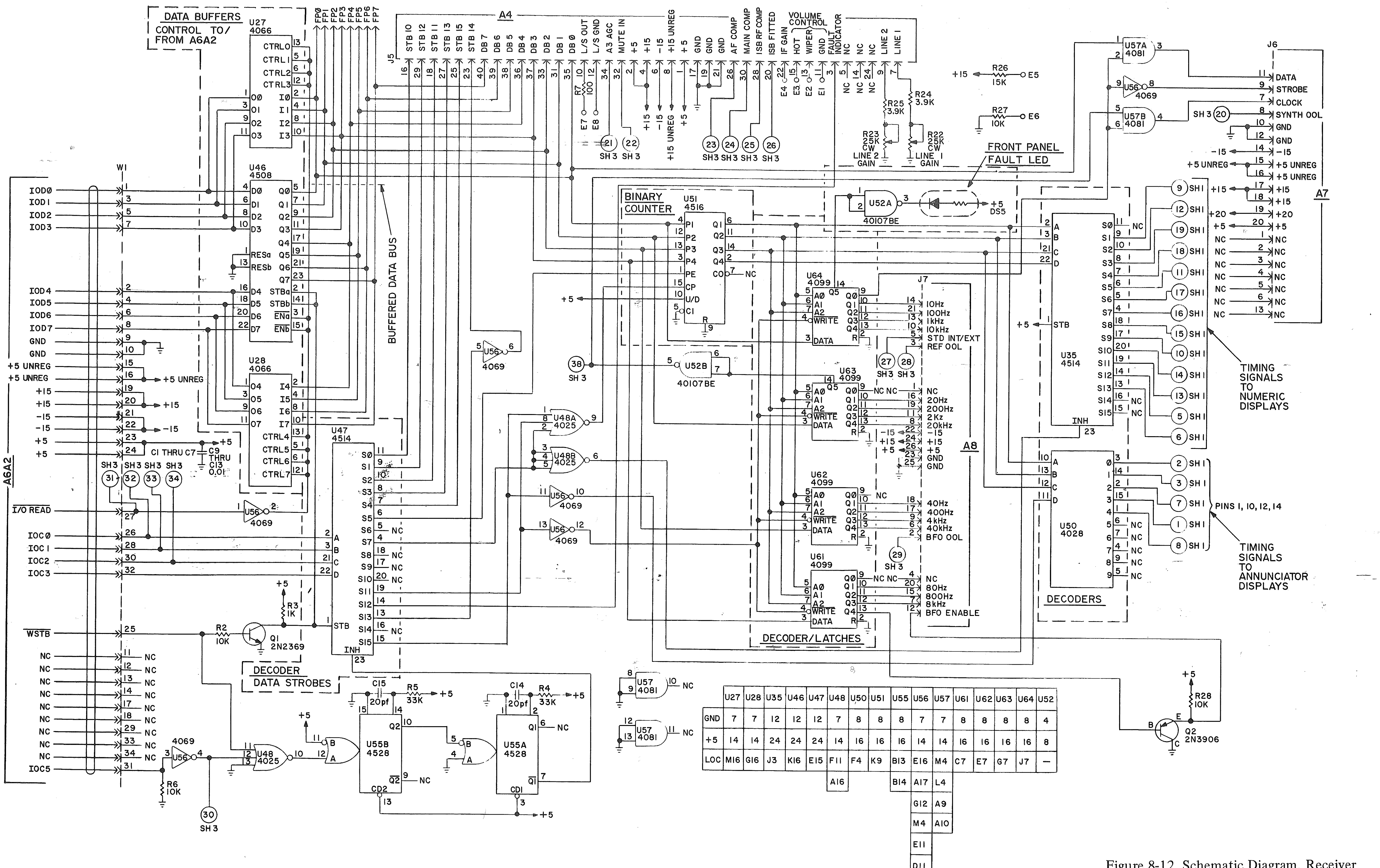
NOTES:
(UNLESS OTHERWISE NOTED)

1. RESISTOR VALUES ARE IN OHMS 1/4 WATT K=1,000 M=1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS, LESS THAN ONE ARE IN MICROFARADS
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND OR ASSEMBLY DESIGN.
5. LAST USED - U63, C24, R32, Q2, E8, J8, W1, DS4.

A	B	A 3
SH.1	SH.2	SH.3
REVISION STATUS OF SHEETS		

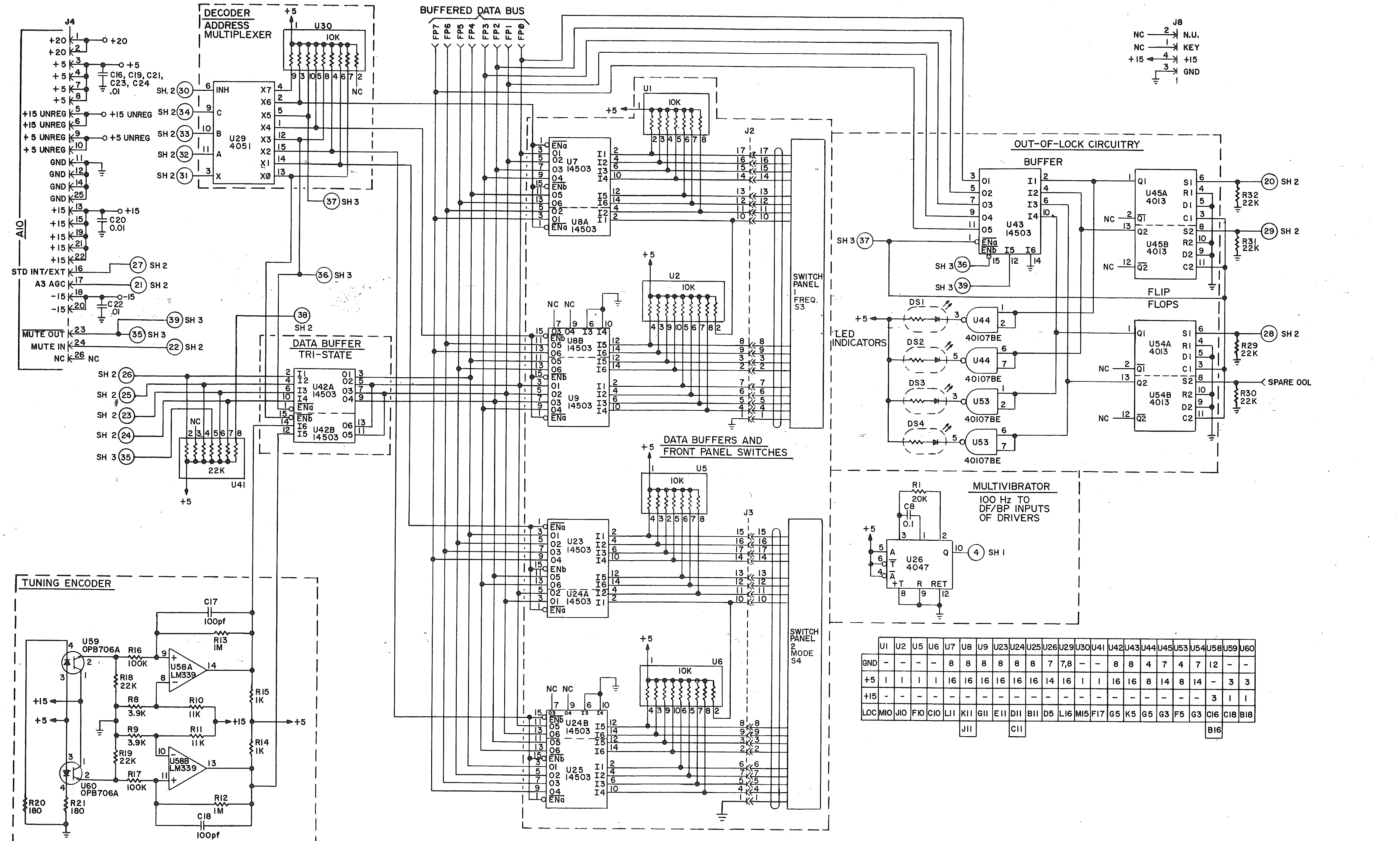
	U10	U11	U12	U13	U14	U15	U16	U17	U18	U19	U20	U21	U22	U31	U32	U33	U34	U36	U37	U38	U39	U40	U49
+5	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16
GND	7, 8	7, 8	7, 8	7, 8	7, 8	7, 8	7, 8	7, 8	7, 8	7, 8	7, 8	7, 8	7, 8	7, 8	7, 8	7, 8	7, 8	7, 8	7, 8	7, 8	7, 8	7, 8	7, 8
LOC	G10	A7	C7	D7	G7	J7	K7	D13	E13	K16	G13	F16	G16	C10	D10	F7	F10	E16	J13	J16	H13	H16	J10

Figure 8-12 Schematic Diagram, Receiver Control, A9 (Sheet 1 of 3)



	U27	U28	U35	U46	U47	U48	U50	U51	U55	U56	U57	U61	U62	U63	U64	U52
GND	7	7	12	12	12	7	8	8	8	7	7	8	8	8	8	4
+5	14	14	24	24	24	14	16	16	16	14	14	16	16	16	16	8
LOC	M16	G16	J3	K16	E15	F11	F4	K9	B13	E16	M4	C7	E7	G7	J7	—
						A16			B14	A17	L4					
										G12	A9					
										M4	A10					
										E11						
										D11						

Figure 8-12 Schematic Diagram, Receiver Control, A9 (Sheet 2 of 3)



	U1	U2	U5	U6	U7	U8	U9	U23	U24	U25	U26	U29	U30	U41	U42	U43	U44	U45	U53	U54	U58	U59	U60
GND	–	–	–	–	8	8	8	8	8	8	7	7,8	–	–	8	8	4	7	4	7	12	–	–
+5	1	1	1	1	16	16	16	16	16	16	14	16	1	1	16	16	8	14	8	14	–	3	3
+15	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	3	1	1
LOC	M10	J10	F10	C10	L11	K11	G11	E11	D11	B11	D5	L16	M15	F17	G5	K5	G5	G3	F5	G3	C16	C18	B18
						J11			C11												B16		

Figure 8-12 Schematic Diagram, Receiver Control, A9 (Sheet 3 of 3)

NOTES:
(UNLESS OTHERWISE NOTED)
1. RESISTOR VALUES ARE IN OHMS 1/4 WATT K=1,000 M=1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS, LESS THAN ONE ARE IN MICROFARADS
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND OR ASSEMBLY DESIGN.

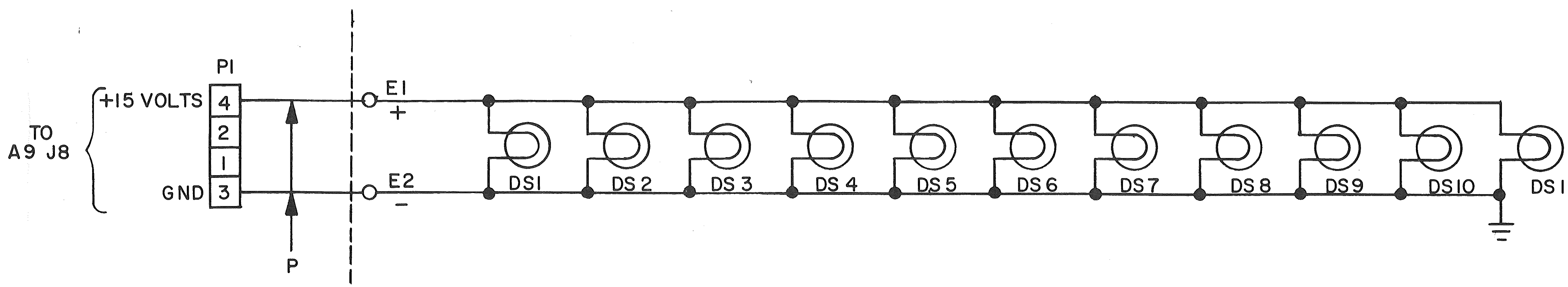
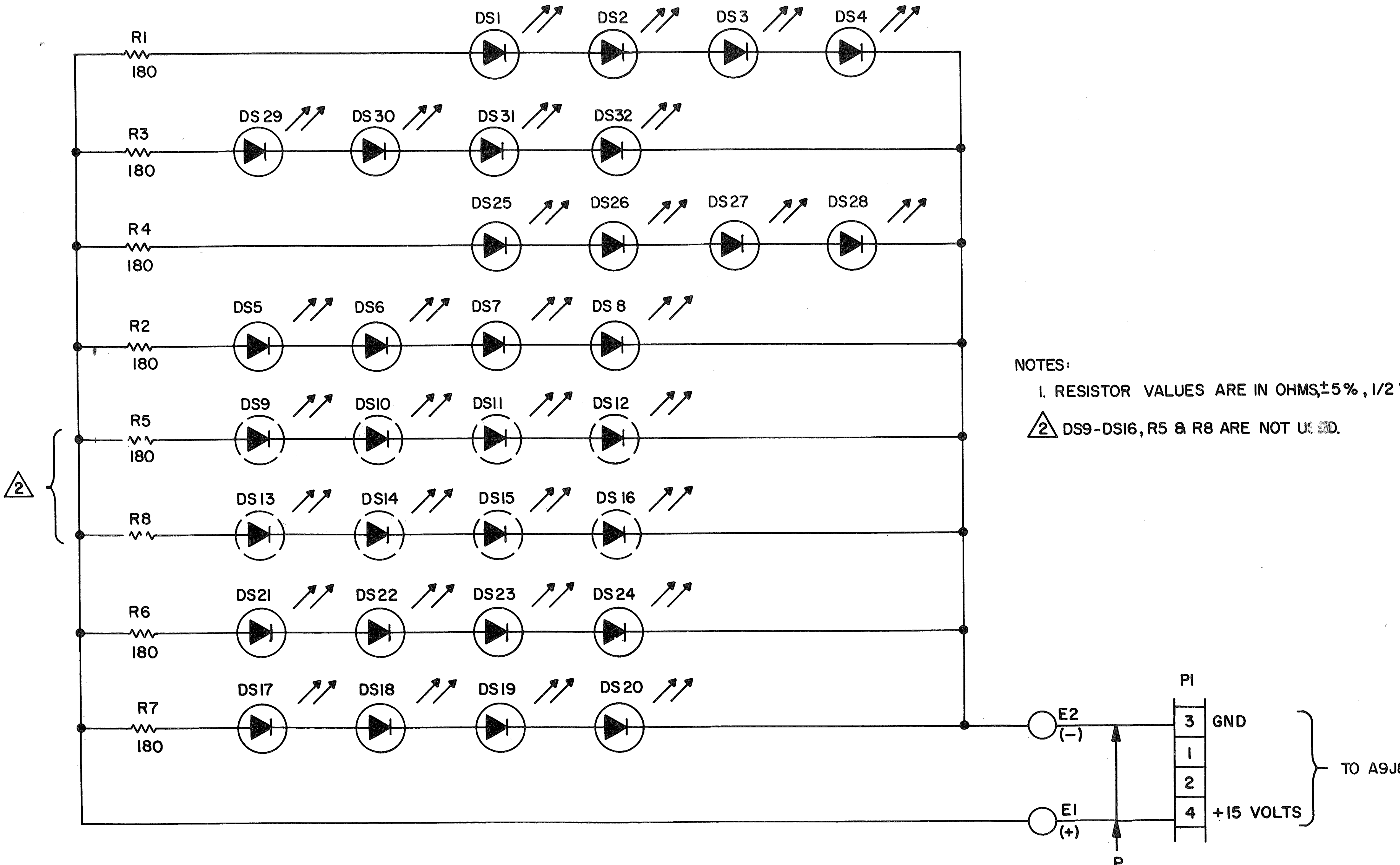


Figure 8-13 Schematic Diagram, Liquid Crystal Display Lamps

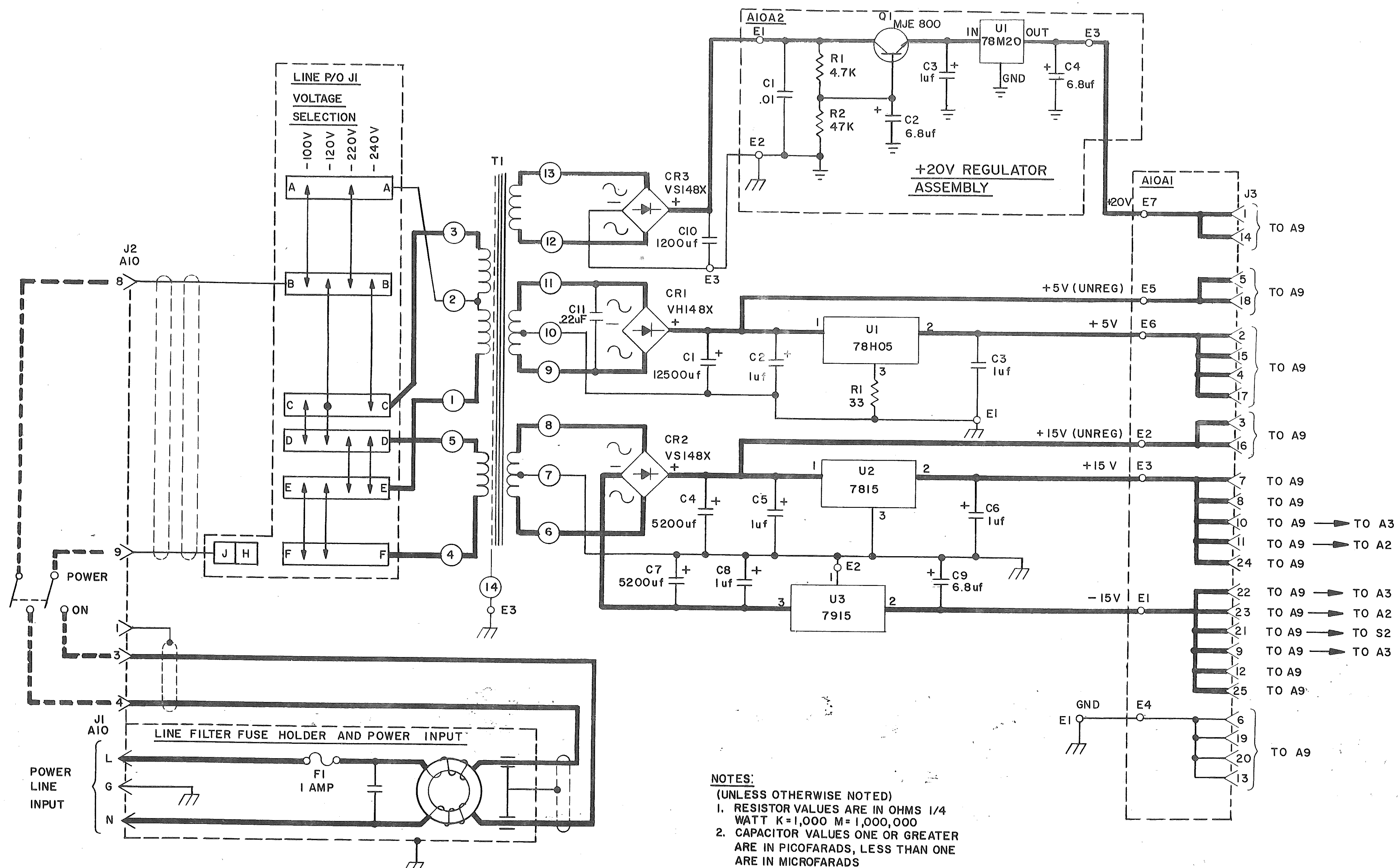


NOTES:

1. RESISTOR VALUES ARE IN OHMS,±5%, 1/2 WATT.

2 DS9-DS16, R5 & R8 ARE NOT USED.

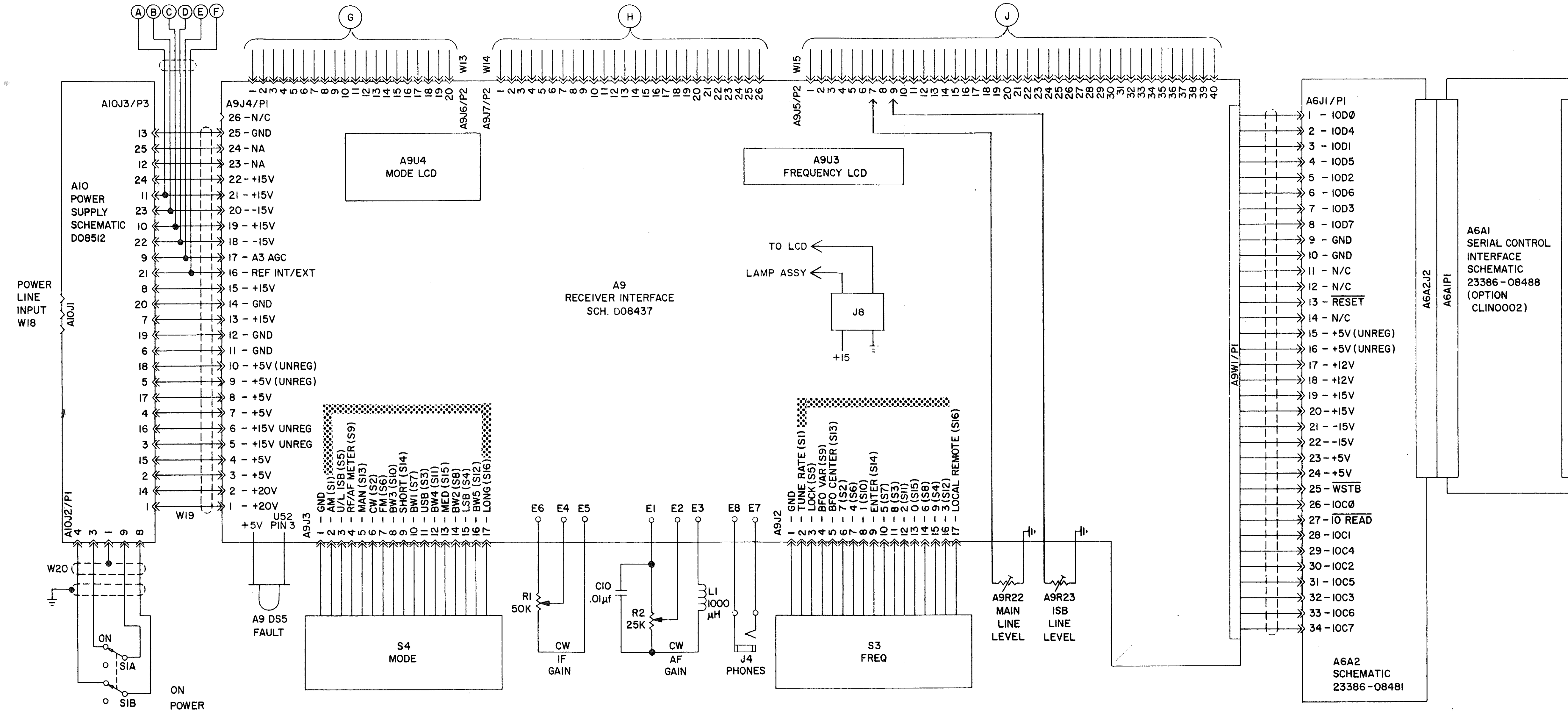
Figure 8-13.1 Schematic Diagram, Liquid Crystal Display LEDs



NOTES:
(UNLESS OTHERWISE NOTED)

1. RESISTOR VALUES ARE IN OHMS 1/4 WATT K=1,000 M=1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS, LESS THAN ONE ARE IN MICROFARADS
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND OR ASSEMBLY DESIGN.

Figure 8-14 Schematic Diagram, Power Supply, A10



NOTES:
(UNLESS OTHERWISE NOTED)

1. RESISTOR VALUES ARE IN OHMS 1/4 WATT K=1,000 M=1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS, LESS THAN ONE ARE IN MICROFARADS
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND OR ASSEMBLY DESIGN.
5. W10, W11 USED ONLY WITH A5 OPTION.

B4	B4
SH. 1	SH. 2
REVISION STATUS OF SHEETS	

Figure 8-15 Schematic Diagram, Interconnection Diagram, Radio Receiver, R-2174(P)/URR (Sheet 1 of 2)

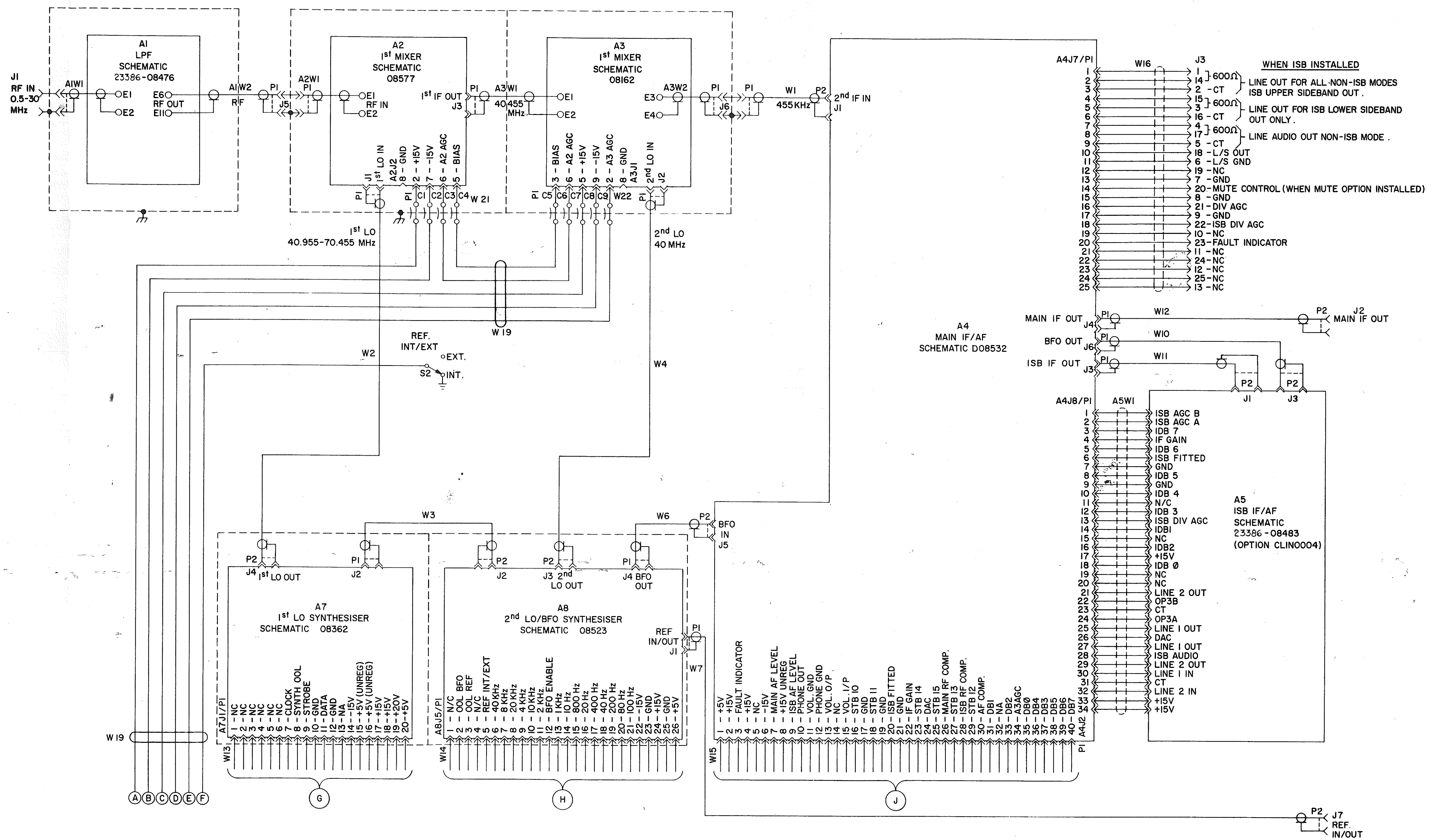


Figure 8-15 Schematic Diagram
Interconnection Diagram
Radio Receiver,
R-2174(P)/URR
(Sheet 2 of 2)