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MAINTENANCE MANUAL

HF-SSB RADIO SET PRC-174

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TABLE OF CONTENTS

TABLE OF CONTENTS (Cont'd.)

TABLE OF CONTENTS (Cont'd.)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (cont'd.)

LIST OF ILLUSTRATIONS (cont'd.)

LIST OF TABLES

LIST OF TABLES (cont'd.)

CHAPTER 1

INTRODUCTION

1-1. Scope

a. This manual contains instructions for maintenance of Radio Set PRC-174.

b. Detailed explanations of equipment functions are given in Chapter 2.

c. Troubleshooting procedures and acceptance testing, based upon automatic test set TS-1748 are given in Chapter 3.

d. Chapter 4 provides maintenance instructions.

e. Equipment maintenance procedures and forms conform to standard user practice.

f. Operating, installation, and field maintenance instructions for the equipment are given in publication OM-107-10 (OM 2124-09500-00).

CHAPTER 2

THEORY OF OPERATION

Section I. BLOCK DIAGRAM ANALYSIS

2-1. Functional Block Diagram (fig. 2-1)

a. Radio set PRC-174 is a high-frequency (HF), single sideband (SSB), and amplitude modulation (AM), portable radio receiving/transmitting set which operates over the frequency range of 2.0 to 29.9999 MHz. The PRC-174 is capable of receiving and transmitting two-way voice, digital data, and continuous-wave (CW) narrow- or wide-band telegraphy using upper sideband (USB) or lower sideband (LSB) modulation. It also provides voice communication using conventional amplitude modulation (AM). The high output power (20 watts) permits reliable communication over long distances, utilizing both ground-wave and sky-wave propagation. High selectivity and a wide dynamic range ensures clear, undisturbed communication and the ability to operate in a dense electromagnetic signal environment.
The radio set provides 280,000 RF channels with 100-Hz spacing. The operating frequency, which is generated by a highly stable and accurate frequency synthesizer, is easily selected, using front panel digital pushbuttons or a remote control unit. Once the frequency is selected, the antenna is automatically tuned upon initiation of the first transmission. Either whip and dipole antennas can be used.

b. The main components of Receiver/Transmitter RT-936/PRC-174 are:

(1) Panel assembly 1A1 - permits local operation of the radio set or connection to a remote control unit or to an automatic test set.

(2) Low-level AF, IF and RF signal processing section - consists of 5 modules carrying 1A2AX designations. All modules are active in both receive and transmit paths.

(3) RF power amplifier - carries 1A6 designation.

(4) Antenna matching circuits - carry 1A5AX designations.

(5) Synthesizer section - consists of 6 modules carrying 1A3AX designations.

(6) Control circuits - carry 1A7 designation.

(7) Power supply module - carries 1A4 designation.

2-2. Receive Mode Signal Path (fig. 2-2)

a. The incoming radio frequency (RF) signals, appearing at the whip or dipole antenna connector, pass through the matching network, module MN 1A5A1, to band-pass filters in module SNF 1A5A3. Before reaching the matching network, the signal arriving from the dipole connector passes through a 218-MHz low-pass filter, located on the motherboard. The filtered signals pass through a 109.35-MHz rejection filter (also located on the motherboard) and are then applied to the first mixer in module MIXER 1A2A1.

b. The received signals are up-converted to the 1-st IF frequency (109.35 MHz) by mixing them with the F1 (variable) synthesizer frequency

(111.35 to 139.3499 MHz).
After passing through a crystal filter, the 1-st IF signal is applied to the second mixer. The frequency of the F2 local oscillator signal supplied to this mixer depends on the operation mode: it is 114.6 MHz for the USB mode and 104.1 MHz for the LSB mode. This arrangement ensures that in SSB modes, an upper-sideband signal is obtained at the output of module MIXER 1A5A1. The frequency of the IF signal provided by the 2-nd mixer is 5.25 MHz. This signal is amplified by an IF amplifier with automatic gain control (AGC), then applied to the filters in module FILTER 1A2A5. Depending upon the operation mode, the signal passes through one of the following crystal filters:

(1) The 3-kHz bandwidth SSB filter - for voice, data and wideband CW (WCW) operation in LSB and USB modes.

(2) The 0.5-kHz bandwidth SSB filter - for narrowband CW (NCW) operation.

(3) The 6-kHz bandwidth filter - for amplitude modulation (AM) operation.

c. The filtered 5.25-MHz IF signal is again amplified by an AGC amplifier in module IF 1A2A2, and then demodulated as follows·

(1) For all SSB operation modes, demodulation is performed by a balanced demodulator, by mixing the IF signal with the 5.25-MHz signal generated by the module REF 1A3A6.

(2) For AM operation, the demodulation is performed by an envelope detector.

(3) A separate detector circuit provides an AGC voltage for module MIXER 1A2A1 and for the received signal level (S-METER) indication provided by module CONT 1A7.

d. The demodulated audio signal is amplified by module AUDIO 1A2A3 and applied to the front panel AUDIO connectors and to the FIX AUDIO line in the CONTR connector. A squelch circuit, operational only in the SAVE mode, disables the audio output when no useful signal is sensed.
The output level of the earphone audio output is controlled by a DC voltage, supplied by the VOLUME control or by a remote control unit.
Auditory indication signals, e.g, the "tuning-in-process", "tuning-failed", "low-battery" indications, generated by the module CONT 1A7, are added to the received signal within module AUDIO 1A2A3.

2-3. Transmit Mode Signal Path (fig. 2-1, 2-3)

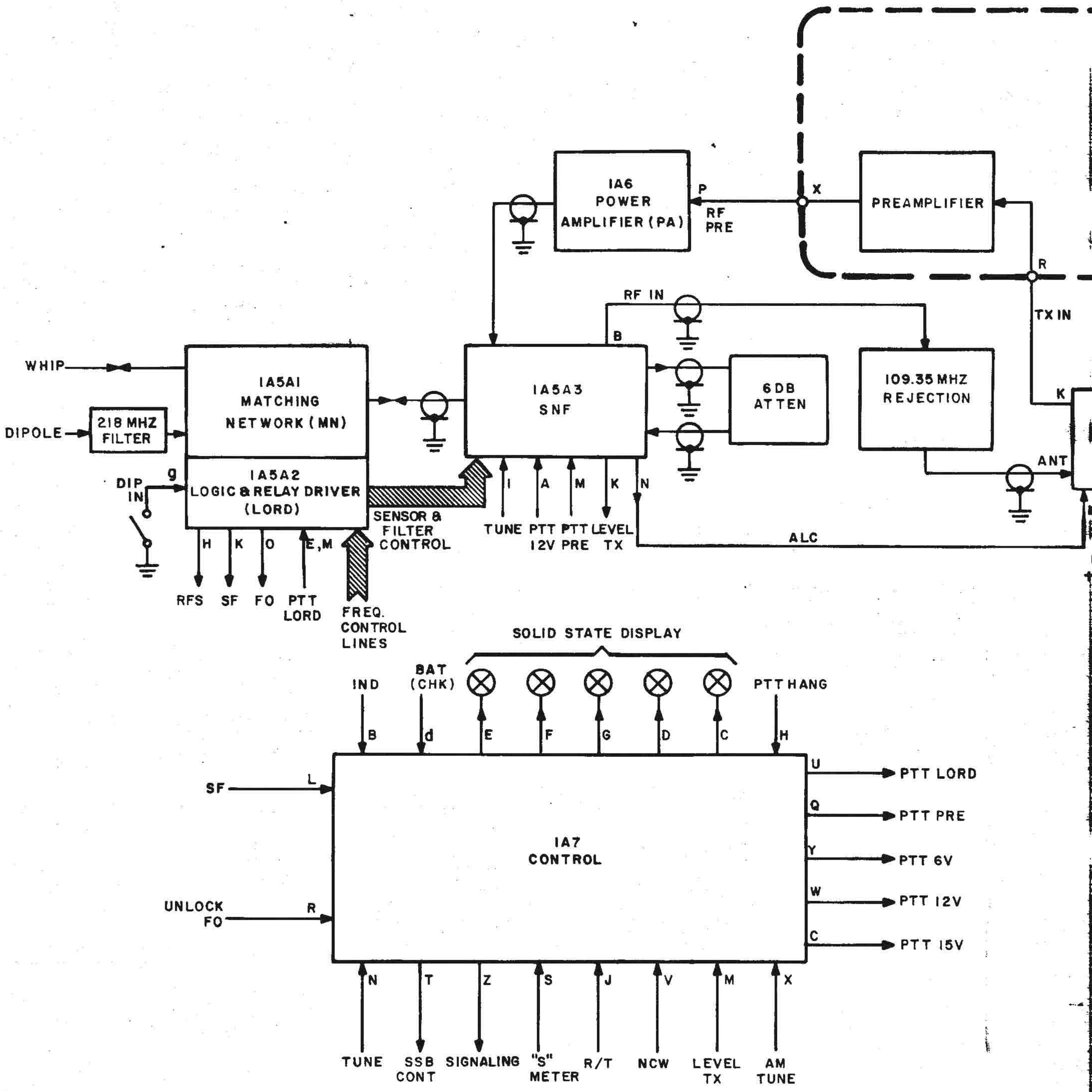
a. Module PRE 1A2A4 receives modulation signals from three sources and selects one of them for application to the balanced mixer in module IF 1A2A2 (see para. 2-6). These sources are:

(1) The microphone (pin F). This signal is amplified in a compressing amplifier which limits its maximum amplitude and reduces its peak-to-average-power ratio, to increase transmitted power.

(2) Data signal. This signal is also applied to the AUDIO connector (in place of the microphone signal). With the mode selector at DATA, the signal is connected directly to the modulator.

(3) 1-kHz CW audio tone. This signal is synthesized in module PRE 1A2A4 from a 10-kHz signal generated in module REF 1A3A6.

b. A sidetone is generated by applying the selected modulation signal to module AUDIO 1A2A3. The sidetone level is almost constant and is not influenced by the setting of the VOLUME control; it appears when the transmission power reaches proper levels.


IA6
POWER
AMPLIFIER (PA)
P
RF
PRE
X
PREAMPLIFIER
R
TX IN
RF IN
B
WHIP
DIPOLE
218 MHZ
FILTER
IA5A1
MATCHING
NETWORK (MN)
IA5A3
SNF
6DB
ATTEN
109.35 MHZ
REJECTION
K
ANT
DIP
IN
g
IA5A2
LOGIC & RELAY DRIVER
(LORD)
I
A
M
K
N
SENSOR &
FILTER
CONTROL
TUNE
PTT
12V PRE
PTT LEVEL
TX
ALC
H
K
O
E,M
RFS
SF
FO
PTT
LORD
FREQ.
CONTROL
LINES
SOLID STATE DISPLAY
IND
BAT
(CHK)
PTT HANG
B
d
E
F
G
D
C
H
SF
L
IA7
CONTROL
U
PTT LORD
Q
PTT PRE
Y
PTT 6V
W
PTT 12V
C
PTT 15V
UNLOCK
FO
R
N
T
Z
S
J
V
M
X
TUNE
SSB
CONT
SIGNALING
"S"
METER
R/T
NCW
LEVEL
TX
AM
TUNE

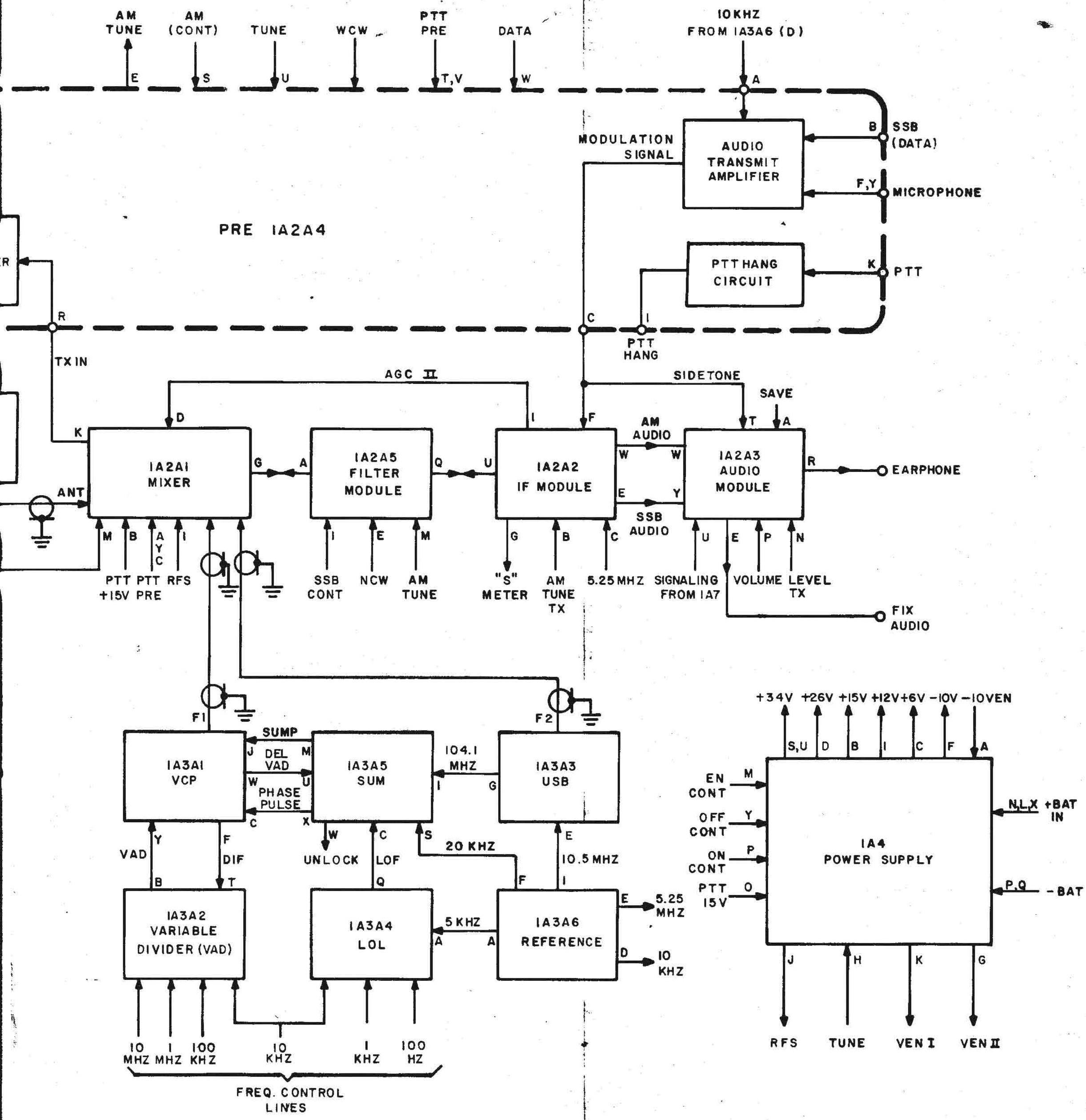
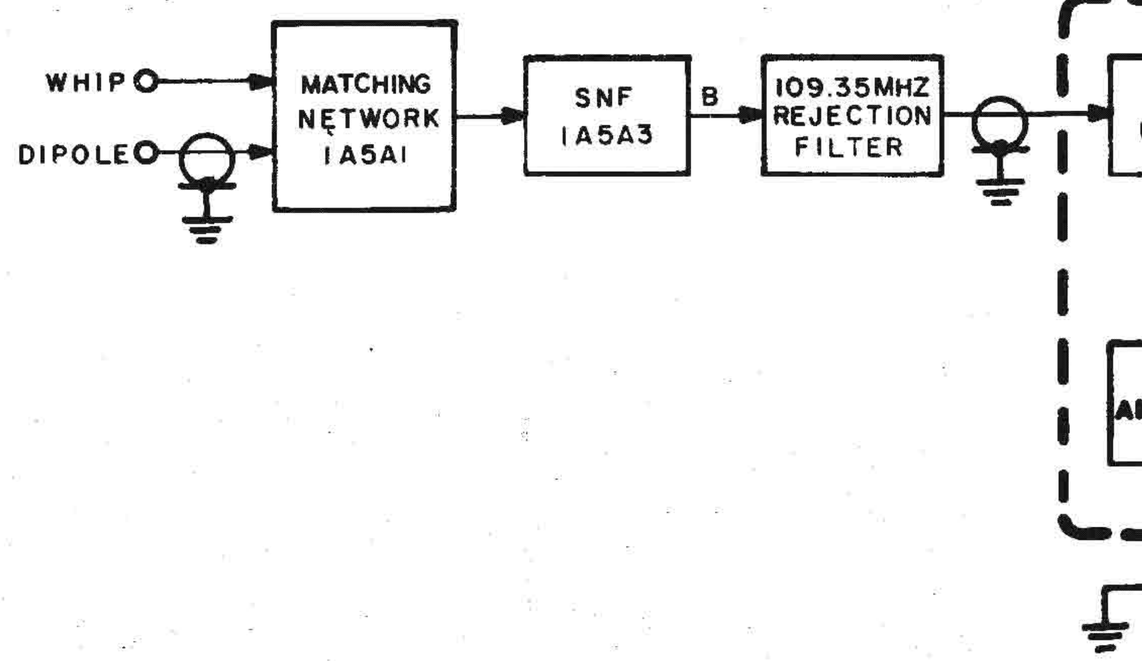


Fig. 2-1. RT-936/PRC-174, functional block diagram


WHIP
DIPOLE
MATCHING NETWORK 1A5A1
SNF 1A5A3
B
109.35MHZ REJECTION FILTER

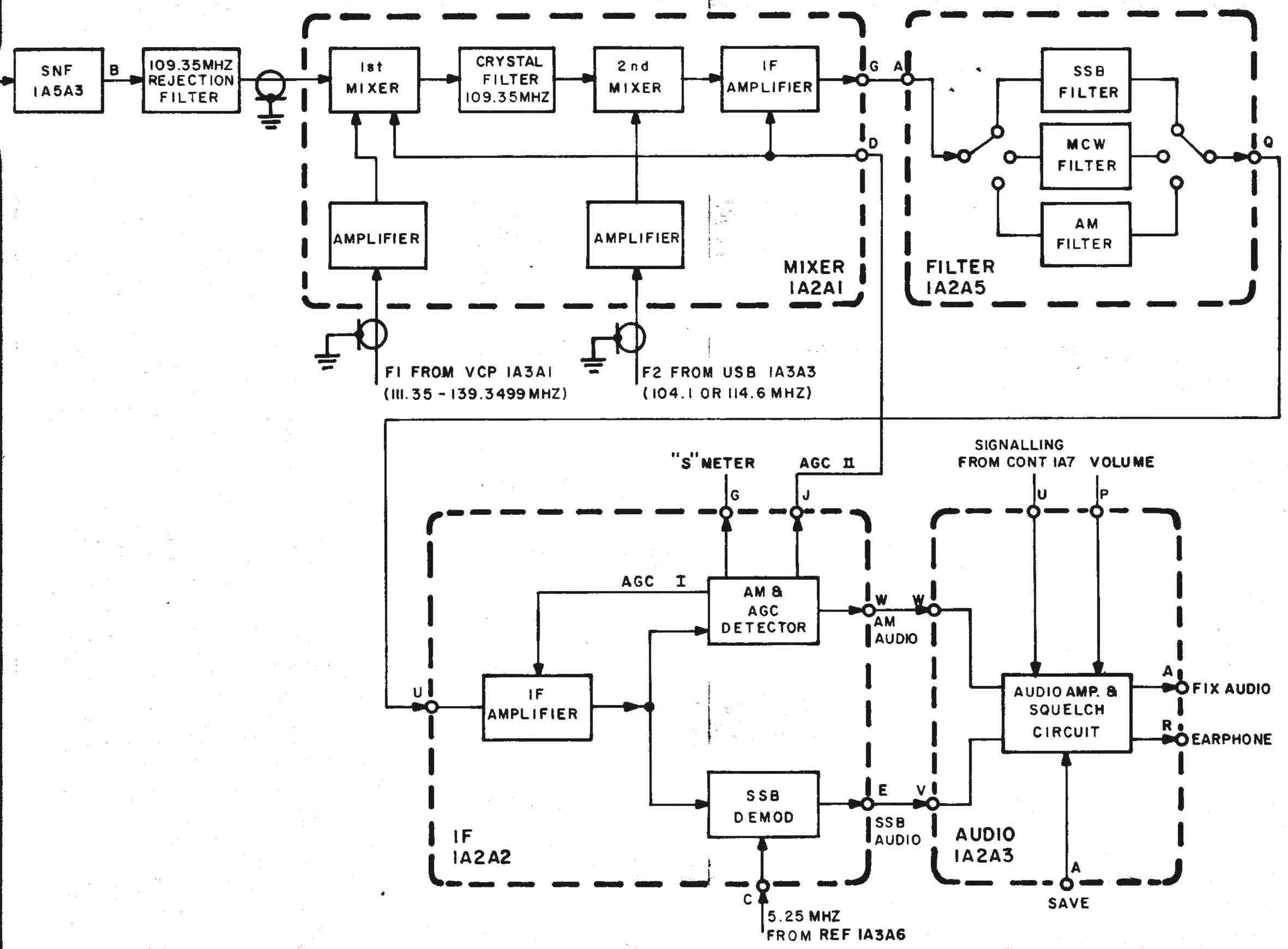


Fig. 2-2. Receiver block diagram

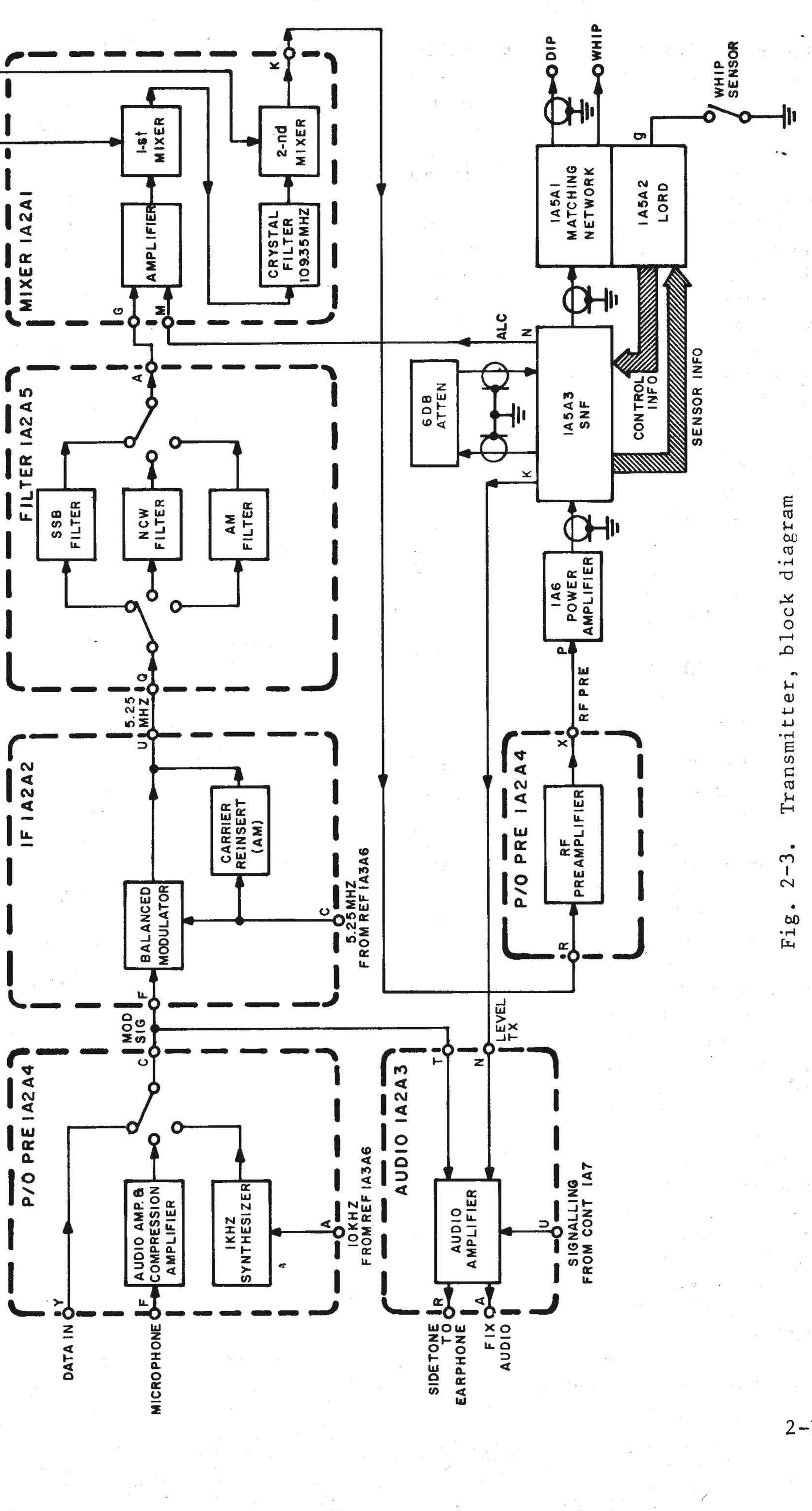


Fig. 2-3. Transmitter, block diagram

The signaling generated by module CONT 1A7 is added to the sidetone and the combined audio signal is supplied to the handset.

c. The modulation signal is converted, in module IF 1A2A2, to the 5.25-MHz intermediate frequency by mixing it with the 5.25-MHz carrier signal generated in module REF 1A3A6. The mixer is of the double-balanced type and therefore suppresses the carrier component. During tuning, and also when AM operation is selected, the carrier is reinjected after the mixer.

d. The 5.25-MHz IF signal is filtered by one of the three filters in module FILTER 1A2A5:

(1) The 3-kHz bandwidth SSB filter - for voice, data and WCW operation in LSB and USB modes.

(2) The 0.5-kHz bandwidth SSB filter - for NCW operation in LSB and USB modes.

(3) The 6-kHz bandwidth filter - for AM operation.

e. The filtered signal is applied to module MIXER 1A2A1. Its level is amplified and regulated in a gain-controlled amplifier, which is part of the automatic level control (ALC) loop of the transmit path. The signal is then up-converted to the 109.35-MHz frequency range by mixing with the F2 signal in the first mixer (104.1 MHz for LSB operation, or 114.6 MHz for USB operation).
The resulting signal is filtered and applied to the 2-nd mixer, where it is converted down to the transmitting frequency by mixing it with the F1 variable-frequency synthesizer signal. The F1 frequency can be varied in 100-Hz increments from 111.35 MHz (selected operating frequency 2.0000 MHz) to 139.3499 MHz (selected operating frequency 29.9999 MHz). The F1 frequency is always 109.35 MHz higher than the selected operating frequency.

f. The low-level RF signal generated by MIXER 1A2A1 is amplified by the RF preamplifier in module PRE 1A2A4 and then applied to the power amplifier in the module PA 1A6.

g. The 20-W output of the power amplifier is filtered by bandpass filters in module SNF 1A5A3 and passed to the matching network 1A5A1. An ALC voltage is developed by a forward-power detector in module SNF 1A5A3 and applied to the controlled amplifier in module MIXER 1A2A1.

h. During tuning, load impedance sensors, contained in module SNF 1A5A3, are inserted in the RF signal path. These sensors generate signals proportional to the magnitude of the resistive component and the phase of the load presented to the power amplifier via ther matching network. These signals pass to the logic and relay driver module LORD 1A5A2, which controls the operation of the matching network.

i. The matching circuit consists of a T-network, capable of matching both capacitive and inductive antennas. The network elements are digitally controlled by module LORD 1A5A2.

j. The matching cycle is automatically initiated each time the push-to-talk (PTT) line is grounded.

(1) Before the first transmission after frequency change or equipment turn-on, or when a gross antenna mismatch is sensed, a full matching cycle is performed.

(2) Matching is checked again each time the PTT is pressed. If the voltage standing wave ratio (VSWR) exceeds a certain value, antenna matching is carried out again. Module CONT 1A7 generates auditory and visual indications during matching.

k. The PTT signal from the handset or the telegraph key is applied to module PRE 1A2A4 (refer to fig. 2-1).

In the NCW and WCW modes, the internal PTT line (PTT HANG) remains active for approximately 1 second after the external PTT button is released, to permit CW transmission.

(1) The PTT HANG signal is applied to module CONT 1A7. In this module, several related control signals are generated (called PTT signals). The most important control functions provided by these signals are:

(2) Reversion of RF signal path through modules MIXER 1A2A1, FILTER 1A2A5 and IF 1A2A2, when going from transmission to reception or vice versa.

(3) Initiation of matching.

(4) Activation of the power amplifier in PA 1A6 and its +34 VDC power supply. The PTT lines are inhibited when receive-only operation is selected, or the synthesizer is unlocked, a frequency below 2.0000 MHz is selected and also while frequency is changed.

2-4. Synthesizer Block Diagram (fig. 2-1, 2-4)

a. The synthesizer modules provide the following output signals:

(1) F1 signal. The frequency of this signal may be varied in 100-Hz increments over the frequency range of 111.35 to 139.3499 MHz; its frequency is exactly 109.35 MHz above the operating frequency.

(2) F2 signal. Its frequency is 104.1 MHz for LSB operation and 114.6 MHz for USB.

(3) F3 5.25-MHz carrier. This frequency is used by module IF 1A2A2. In the transmit mode, this signal serves as the modulator carrier signal. In SSB receive modes, this signal serves the product detector. The generation of the 5.25-MHz signal is interrupted in the AM receive mode.

(4) F4 10-kHz signal. This signal is used by module PRE 1A2A4 to synthesize the 1-kHz CW tone.

b. Three more signals are generated and used internally:

(1) 10.5-MHz offsetting frequency. This signal is required for the operation of module USB 1A3A3.

(2) 20-kHz VCP reference. This is an internal reference signal required for the operation of the synthesizer phase-lock loop (PLL) circuits.

(3) 5-kHz reference. This is an internal signal, required for the operation of the LOL 1A3A4 PLL.

c. The synthesizer consists of 6 modules:

(1) Module VCP 1A3A1. This module is part of the PLL circuit which generates the F1 frequency. Its reference signals are the 20-kHz reference and the variable 104.13 to 104.1499 MHz signal generated by SUM 1A3A5.

(2) Module VAD 1A3A2. This module contains a variable (programmable) frequency divider. Its division ratio is set by the 10-MHz, 1-MHz, 100-kHz and 10-kHz digital frequency information. A 20-kHz frequency is obtained at its output, by division of the 7.22 to 35.20 MHz signal received from module VCP 1A3A1.

(3) Module USB 1A3A3. This module generates the F2 signal (104.1 MHz for LSB operation, 114.6 MHz for USB operation) under control of the USB/LSB control line. It also generates a 104.1-MHz signal for module SUM 1A3A5.

(4) Module LOL 1A3A4. This is a PLL circuit, providing output signals with frequencies in the range of 30.0 to 49.9 kHz, in 100-Hz increments. It uses the 5-kHz signal as its reference. The output frequency is controlled by the 10-kHz, 1-kHz and 100-Hz digital frequency information.

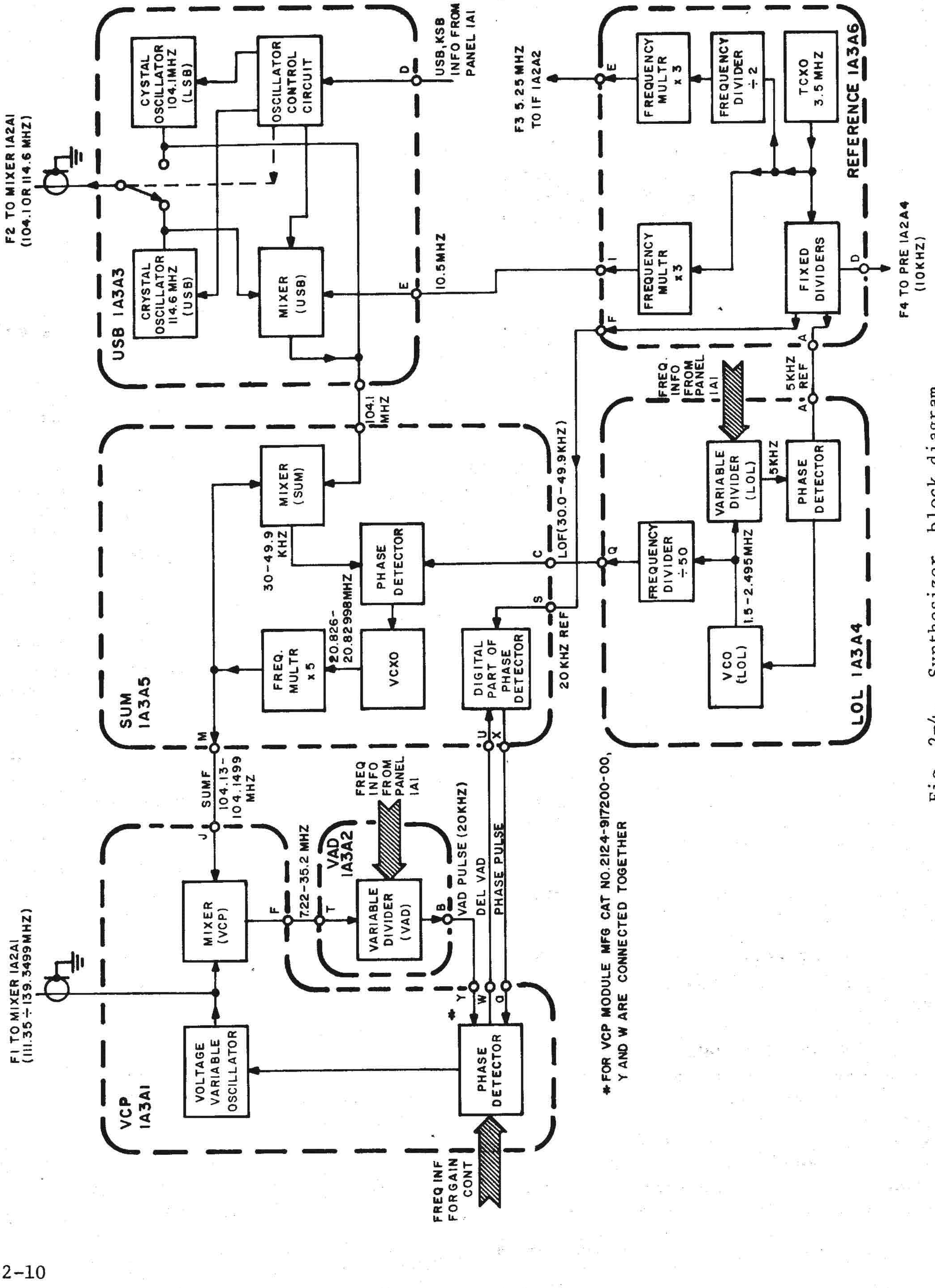


Fig. 2-4. Synthesizer, block diagram

*FOR VCP MODULE MFG CAT NO.2124-9172
Y AND W ARE CONNECTED TOGETHER

(5) Module SUM 1A3A5. This is a PLL circuit which effectively adds the frequencies of the LOL and USB modules output signals. It generates the SUMF signal, variable in 100-Hz increments over the frequency range of 104.13 to 104.1499 MHz. In addition, this module contains the digital part of the phase detector used with module VCP 1A3A1.

(6) Module REF 1A3A6. This module generates the reference signals for the synthesis of the transmit/receive frequency, the 5.25-MHz carrier, and the 10-kHz signal for module PRE 1A2A4.

d. Synthesizer Block Diagram Analysis.

(1) The synthesizer main reference is a frequency of 3.5 MHz, generated by a temperature compensated crystal oscillator (TCXO) contained in module REF 1A3A6.
The 20-kHz, 10-kHz and 5-kHz frequencies are derived from it by division, and the 10.5-MHz - by frequency multiplication.
The 5.25-MHz carrier is generated by halving the TCXO frequency and then tripling the resulting frequency.

(2) The LOL 1A3A4 output frequency is generated by a voltage controlled oscillator (VCO), whose output is divided by 50 before application to module SUM 1A3A5. Due to the PLL action, the VCO frequency is an exact multiple of the 5-kHz reference. The multiplication number is equal to the division ratio of the LOL variable divider (which is determined by the setting of the 10-kHz, 1-kHz and 100-Hz frequency controls). The output frequency of the divider, nominally 5 kHz, is phase-compared to the reference. The output of the phase detector is the control voltage for the VCO, and its magnitude is such as to keep the VCO frequency locked to the reference.

(3) Module USB 1A3A3 contains two crystal oscillators (104.1 MHz and 114.6 MHz). One of them is selected by the USB/LSB control line and its output is supplied to module MIXER 1A2A1, as the F2 frequency.
This module also generates a reference frequency - 104.1 MHz - for module SUM 1A3A5.

(a) When the 104.1-MHz oscillator operates, its output is directly connected to module SUM 1A3A5.

(b) When the 114.6-MHz oscillator operates, its output is converted down to 104.1 MHz by mixing it with the 10.5-MHz offsetting frequency supplied by REF 1A3A6 (in USB mode only).

(4) Module SUM 1A3A5 receives the 104.1-MHz signal from module USB 1A3A3 and the 30-to-49.9-kHz signal from module LOL 1A3A4, and produces a frequency equal to their sum. This sum frequency (SUMF) is applied to module VCP 1A3A1. The SUMF output frequency is generated by frequency multiplication of the volage-controlled crystal oscillator (VCXO) output, which covers the range of 20.826 to 20.82998 MHz. Its control voltage is produced by a phase detector, which compares the phase of LOL signal to that of the difference signal generated by mixing the SUMF frequency with the 104.1-MHz reference. The operation of the PLL circuit is such as to keep the SUMF frequency locked to the sum of the reference signal frequencies: (MHz) SUMF = LOF + 104.1, where LOF is the LOL output frequency.

(5) The SUMF signal is applied to the mixer in module VCP 1A3A1 and mixed with the VCO signal. The difference signal (7.22 to 35.20 MHz) is fed to the variable divider in module VAD 1A3A2.

(6) The division ratio of the variable divider is set by the 10-MHz, 1-MHz, 100-kHz and 10-kHz digital information, such that when the VCO operates at the correct frequency, the

divider output frequency is 20 kHz. The divider output is applied, together with the 20-kHz reference generated by module REF 1A3A6, to a phase detector. The digital part of this phase detector is located in module SUM 1A3A5 and the analog part - in module VCP 1A3A1. The output voltage of the phase detector is of such magnitude as to bring the VCO frequency, F1, to the value given by:

$$(MHz)\ F1 = 104.1 + LOF + 0.02\ N$$

where N is the division ratio of the variable divider.
As the required transmit/receive frequency is changed from 2 to 29.9999 MHz, N increases from 361 to 1760. The phase detector gain is also changed as a function of the required frequency, to keep the phase lock loop gain constant.

(7) The F1 frequency is 109.35 MHz higher than the transmit/receive frequency.

2-5. Power Supply Circuits (fig. 2-1)

a. The conversion of the battery voltage to the regulated supply voltages required by the radio set is performed by high-efficiency switching regulators contained in module PS 1A4. This module also contains the operation (on/off) relay, which can be controlled by the front-panel function selector or by a remote-control unit.

b. The power supply provides -10V, +6V, +12V and +15 VDC. In addition, a voltage of +34 VDC is generated during transmission (for the power amplifier circuits).

c. The battery voltage is filtered in the power supply module and applied to the power amplifier in module PA 1A6 and to module CONT 1A7.

Section II. CIRCUIT ANALYSIS

2-6. Module PRE 1A2A4 (fig. 2-5 through 2-10)

a. Functional Analysis (fig. 2-5). Module PRE 1A2A4 is used in the transmit path of the RT-936/PRC-174, to process the input audio signals in order to obtain the modulation signal, generate internal PTT and tuning control signals, and amplify the low level RF signal received from the MIXER 1A2A1 module to a level sufficient to drive the power amplifier in module PA 1A6. The most part of the module circuits are powered only in the tune and transmit mode (except for PTT signals generated by the control circuits).

(1) Audio signal processing. The module processes three types of signals: low-level microphone signal, data signal and 1-kHz CW modulation tone. A fourth input, designated SP, is available, however it is not used in the RT-936/PRC-174 and is therefore permanently connected to ground.
Each type of modulation signal follows a different path, up to the input of the modulation switch. The modulation switch allows to interrupt the modulation signal during tuning and also when the PTT line is not activated.

(a) Microphone (voice) signals are amplified and then pass through a compression amplifier, which ensures that the average level of the voice signal is held almost constant over a wide range of speech volumes. The compressed audio signal is further clipped, to increase its average-to-peak power ratio, and then passed to the modulation switch. The microphone path is enabled only in the AM and SSB

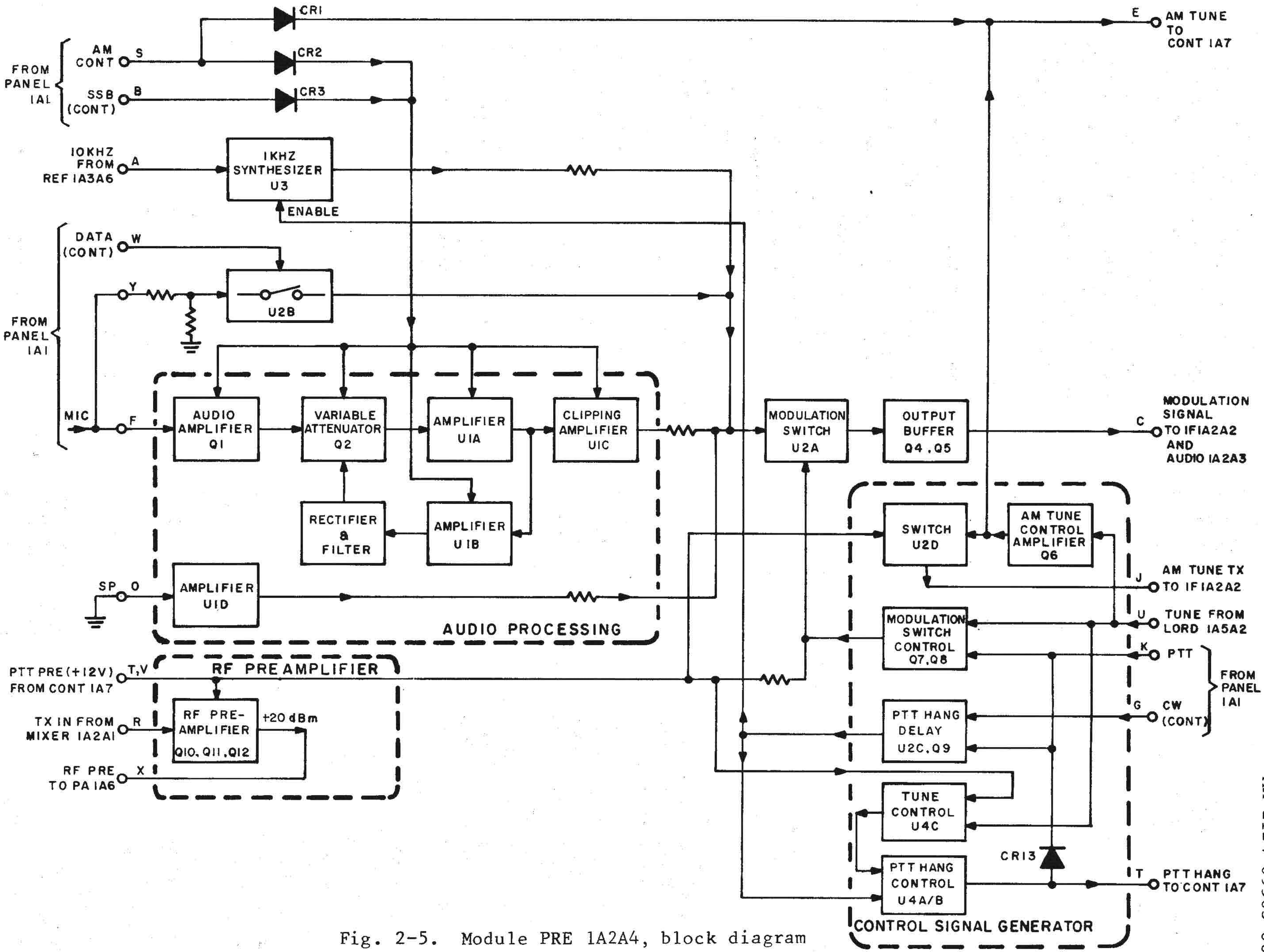


Fig. 2-5. Module PRE 1A2A4, block diagram

voice modes.

(b) Data signals arrive on the same line as the microphone signal, however in the DATA mode the input signal is directly connected to the modulation switch.

(c) 1-kHz CW modulation tone. This tone is synthesized from the 10-kHz signal received from the REF 1A3A6 module. The 1-kHz synthesizer circuit is enabled in the WCW and NCW modes, when the PTT line is activated. The audio signal passed by the modulation switch passes through a buffer to the IF 1A2A2 module, and also to the AUDIO 1A2A3 module, where it is used to generate a sidetone.

(2) Internal PTT and tuning control generation. The external PTT line is applied to a circuit which provides delay-upon-release (PTT HANG) when operating in the WCW and NCW modes. The same circuit also enables the 1-kHz synthesizer when the PTT line is activated during these modes. The internal PTT line, designated PTT HANG, is connected to module CONT 1A7. After tuning is started (under control of module LORD 1A5A2, following PTT line activation), a separate circuit keeps the PTT HANG line in the active state (irrespective of the state of the external PTT line) until tuning is completed. During tuning, the AM TUNE line (to module CONT 1A7 and FIL 1A2A5) and the AM TUNE TX line (to module IF 1A2A2) are pulled to a high level, thereby forcing the AM mode (which allows transmitting a continuous carrier signal) until tuning is completed. As explained in a. (1) above, the modulation signal is disconnected until tuning is completed.

(3) RF preamplifier. This circuit receives the modulated low-level RF signal from module MIXER 1A2A1 and amplifies it to the level required to drive the RF power amplifier in module PA 1A6.

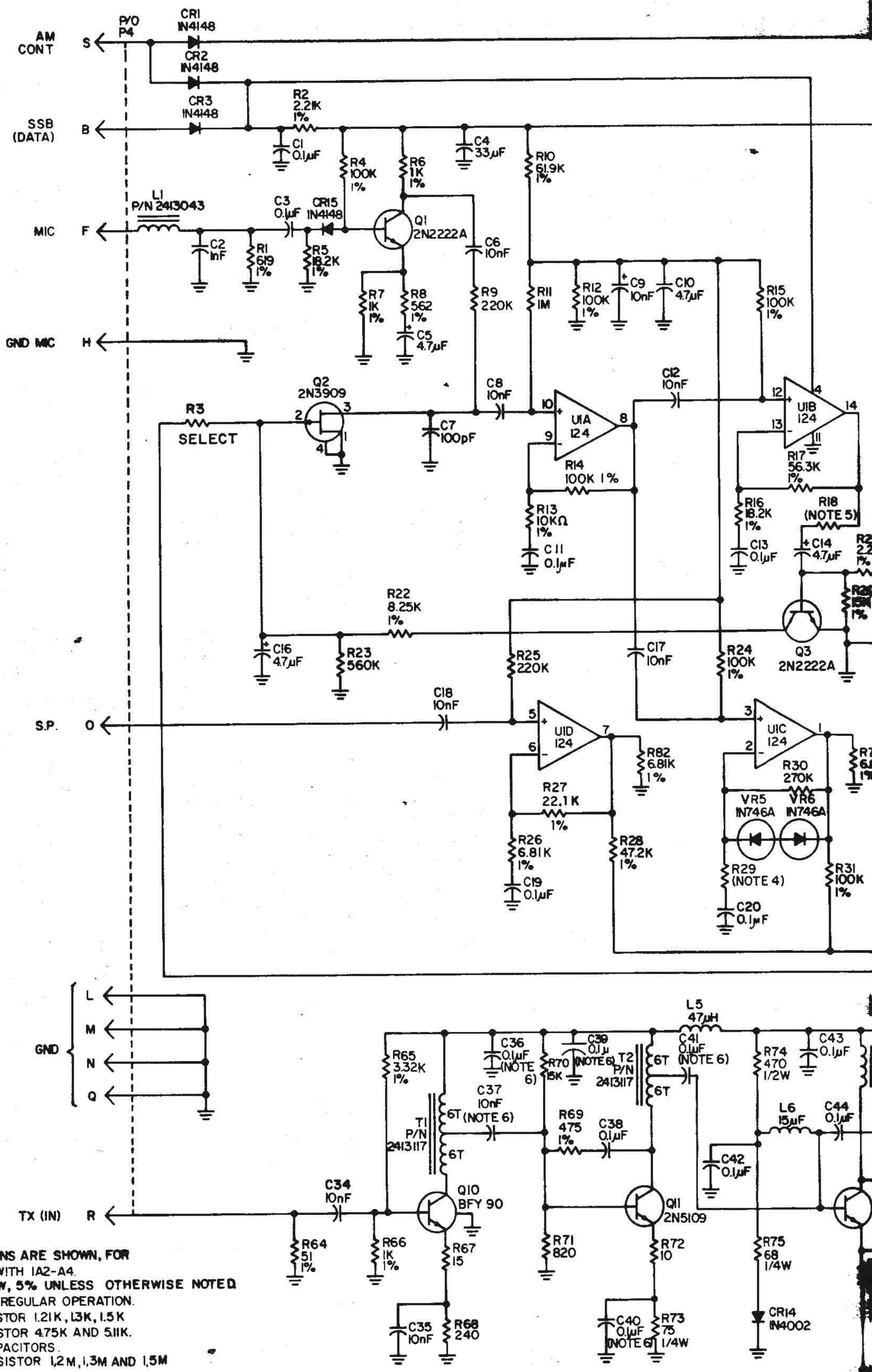
b. Circuit Analysis (fig. 2-6 through 2-10).

(1) Audio compression amplifier and clipper (AM/SSB speech processor) (fig. 2-6, 2-7). This circuit amplifies the microphone signal and performs compression and clipping to obtain a constant level audio modulation signal with a low peak-to-average power ratio. The complete circuit is powered only during AM or SSB operation, by the +12V voltage supplied via the AM CONT (pin S) or SSB (DATA) (pin B) line from the mode selector on the front panel assembly.

(a) The input signal appearing at pin F is filtered by L1 and C2, which serve to attenuate RF signals accompanying the audio. It is then applied to the input amplifier Q1, via coupling capacitor C3 and switch diode CR15. When the amplifier is powered, diode CR1 is forward-biased by the current flowing through R4 and R5 and passes the input signal with little attenuation. When the audio compression amplifier and clipper circuit is not powered, the diode and the base-emitter junction of Q1 do not receive bias and appear to the input signal as two unbiased back-to-back diodes in series, therefore presenting a high impedance to the audio signal.

(b) The output voltage of Q1 is coupled through C6 to the variable attenuator consisting of resistor R9 and the drain-source equivalent resistance of the field-effect transistor (FET) Q2.

(c) The attenuated signal is coupled, through C8, to the operational amplifier U1A, which operates as a non-inverting audio amplifier. Its gain is determined by the ratio of R14 to R13. Capacitor C11 reduces the DC gain to unity; its reactance, in the frequency range of interest, is small relative to the resistance of R13. The network comprised of R10, R12 and C9, C10 provides a filtered bias voltage for U1A and also for the other operational amplifiers used in the audio compression and clipper circuit[this bias voltage determines the



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH 1A2-A4.
2. ALL RESISTORS ARE IN OHMS, 1/8W, 5% UNLESS OTHERWISE NOTED.
3. THE JUMPER IS DISCONNECTED IN REGULAR OPERATION.
4. R29 IS FACTORY SELECTED RESISTOR 1.21K, 1.3K, 1.5K
5. R18 IS FACTORY SELECTED RESISTOR 4.75K AND 5.11K.
6. C36,37,39,40, 41, 50 ARE CHIP CAPACITORS.
7. R56 IS FACTORY SELECTED RESISTOR 1.2M, 1.3M AND 1.5M

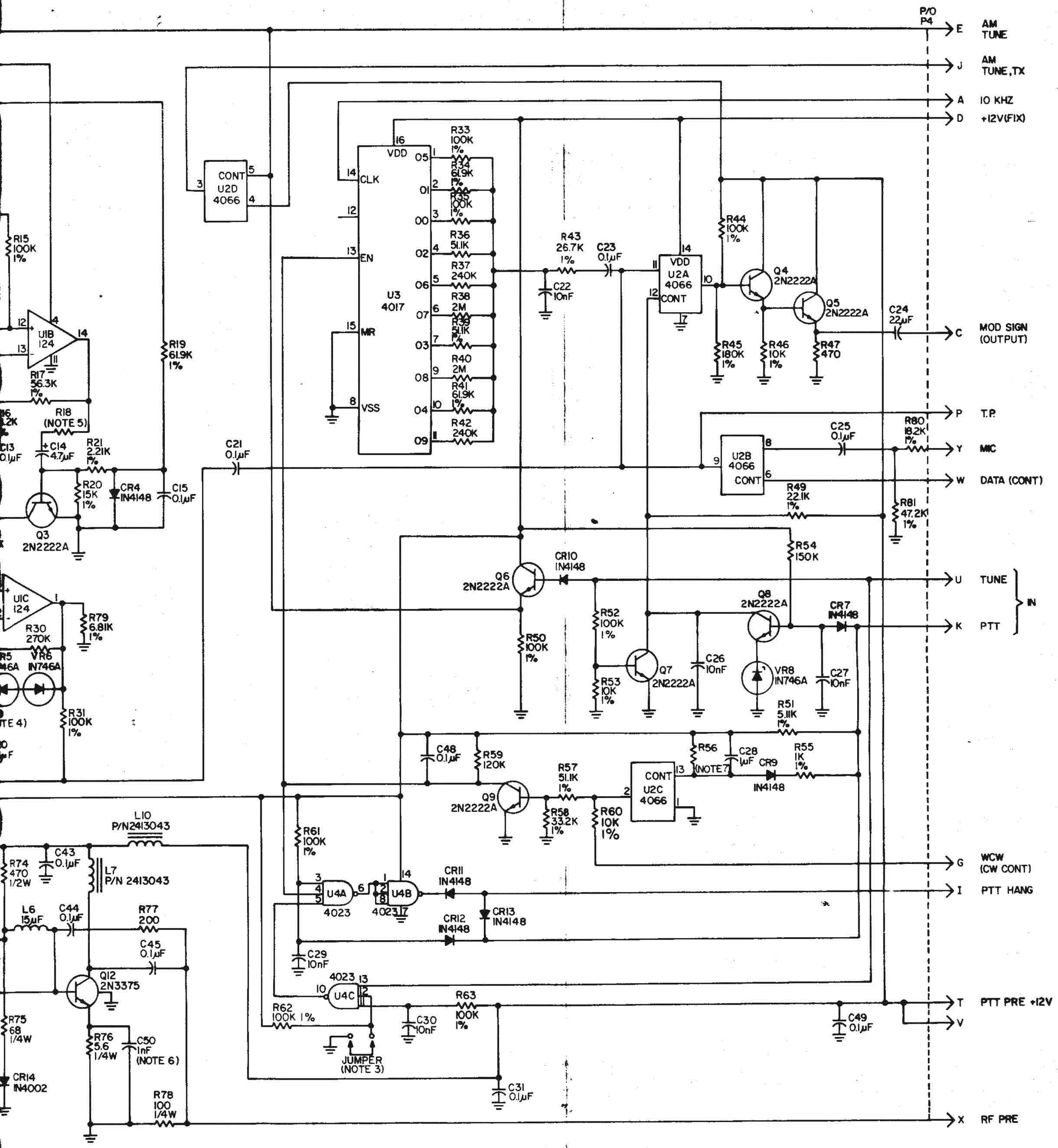


Fig. 2-6. Module PRE 1A2A4, schematic diagram

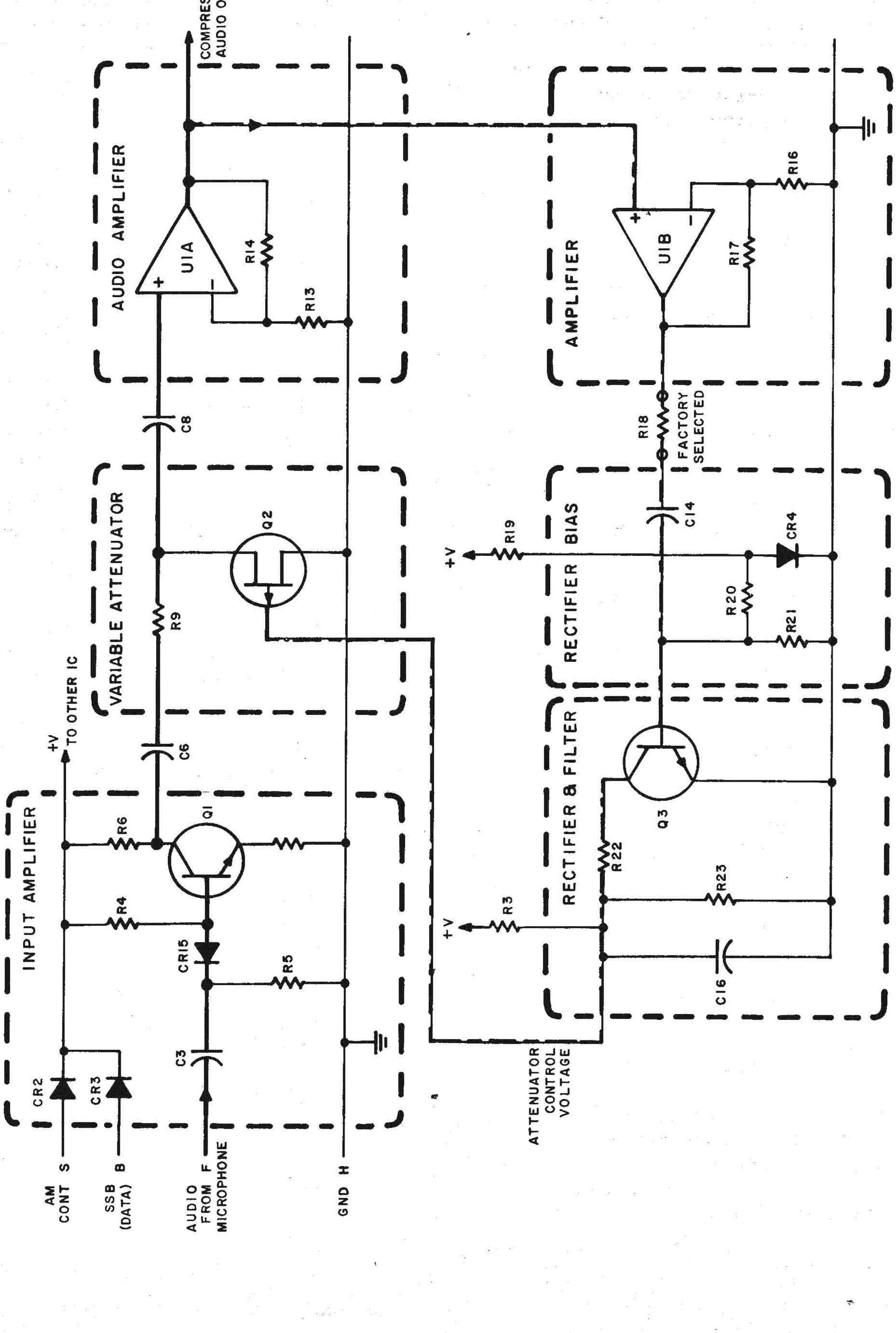


Fig. 2-7. Audio compression amplifier, simplified circuit diagram

quiescent output voltages.

(d) The signal appearing at the output of U1A is coupled through C17 to the clipper, U1C (see (e) below) and also to the circuit which develops the control voltage for the FET used in the variable attenuator.
The output signal of U1A is first amplified by a non-inverting amplifier, U1B, and then applied through factory-selected resistor R18 and capacitor C14 to the transistor rectifier Q3. This transistor is biased (by the voltage developing across CR4 and attenuated by R20 and R21) to the threshold of conduction and conducts only during the positive peaks of the speech signal. Resistor R18 is selected to adjust the onset of compression to the desired level. The collector of Q3 is connected through R3 and R22 to +12V. When no signal is detected, capacitor C16 charges to almost +8V. This causes the drain-to-source resistance of FET Q2 to be very high; thus, the attenuation introduced by the variable attenuator is negligible. When a sufficiently high-level signal appears, transistor Q3 starts to conduct. This causes C16 to discharge rapidly.
The decreased gate-source bias decreases the drain-source resistance of Q2, thereby increasing the attenuation of the speech signal, until the discharge of C16 through R22 and Q3 is balanced by the small charging current supplied through R3. The resulting output level of the compression amplifier is such that the speech peaks remain at a relatively constant level for a wide range of input signals.
When speech stops or its level decreases, the voltage on capacitor C16 starts increasing slowly, because of the very long charging time constant. This keeps the average level from changing during short interruptions (between words, etc); the circuit thus provides fast-attack, slow-release action.

(e) The compressed speech signal appearing at the output of U1A is coupled through capacitor C17 to the clipping amplifier U1C (fig. 2-6). The gain of this amplifier (normally determined by the ratio of R30 to R29) is relatively high. However, when its peak output voltage exceeds the Zener voltage of diode VR5 or VR6, these conduct and cause almost unity negative feedback. This reduces the instantaneous gain, thereby limiting the output voltage. The limiting action starts when the signal level is -10dB or higher (compared to the fixed compressed audio level). This causes clipping of the speech waveform, thereby improving the average speech power without affecting its intelligibility.
The clipping level is determined by the value selected for resistor R29.

(f) Speech signals may also be applied to pin 0. These are buffered by U1D and added to the main audio signal path through R28. However, this input is not used in the RT-936/-PRC-174, and is connected to ground on the motherboard PCB.

(2) 1-kHz synthesizer (fig. 2-6, 2-8). During CW operation, a 1-kHz signal is generated by U3. This integrated circuit is a decoded BCD counter. U3 receives a 10-kHz clock signal from module REF 1A3A6. The counter outputs are normally low, except for the one which corresponds to the internal state of the counter.
Resistors R33 to R42 convert each state to a current value, which is integrated by C22. The cyclic succession of the states causes the voltage across C22 to vary almost sinusoidally, thereby synthesizing the 1-kHz signal. The counter may change state only when the level applied to pin 13 (EN) is low. This condition occurs only when the PTT line is activated and the function selector is at WCW or NCW.

Fig. 2-8 shows typical waveforms.

(3) Modulation signal selector (fig. 2-6, 2-9). The simplified selector circuit is shown in fig. 2-9: its purpose is to select the desired signal and apply it to the input of the modulation switch, U2A.

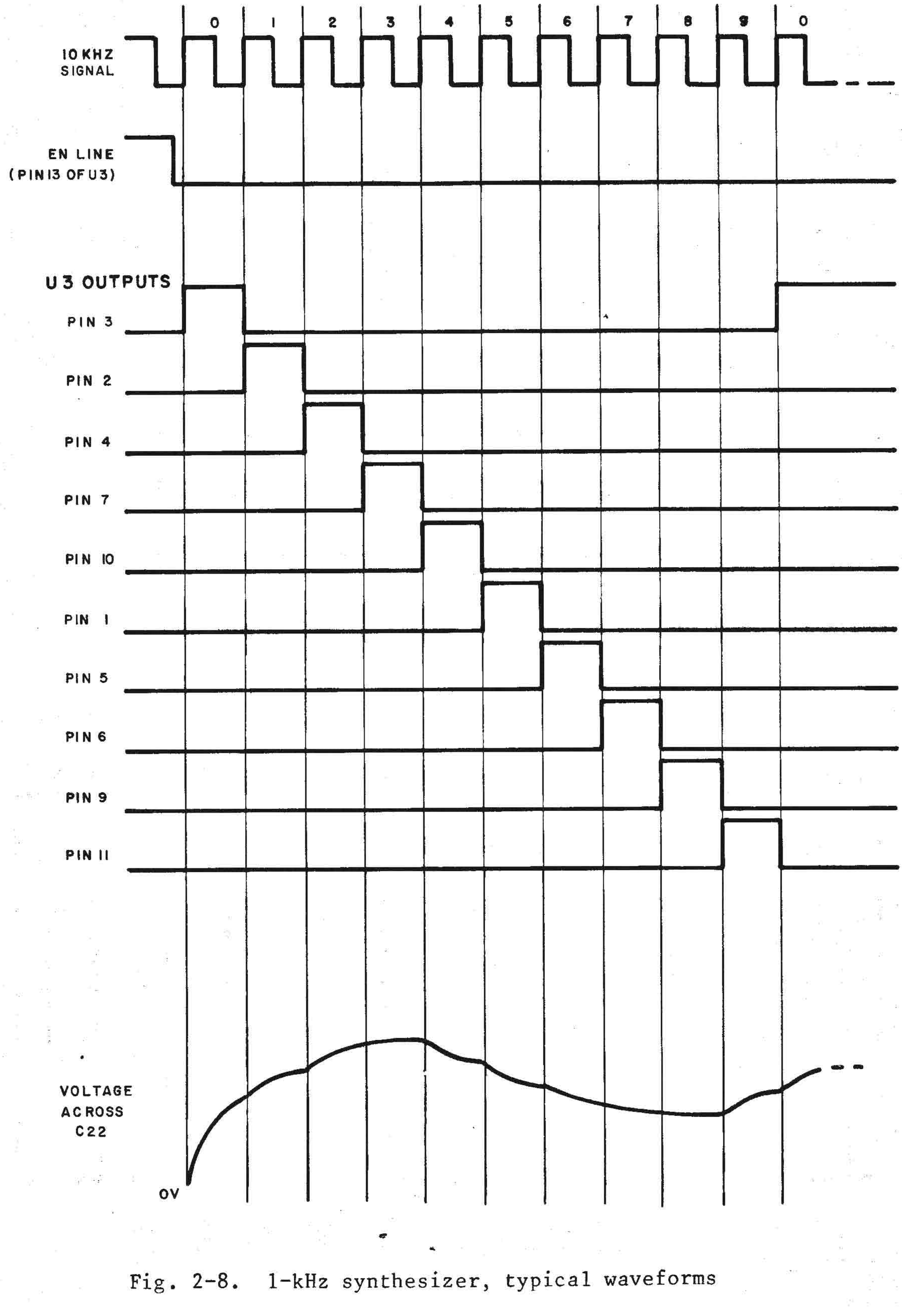


Fig. 2-8. 1-kHz synthesizer, typical waveforms

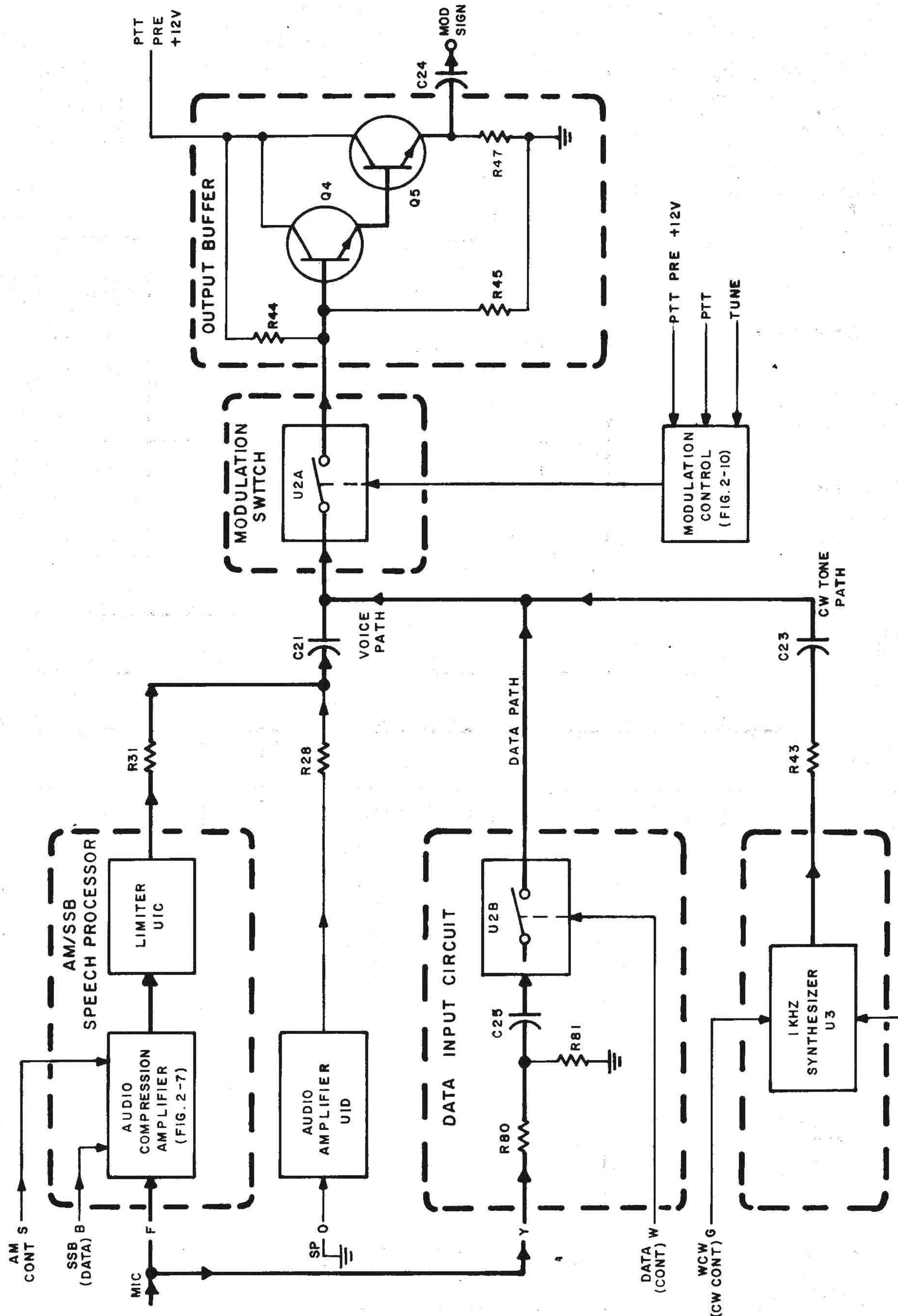


Fig. 2-9. Modulation signal selector, simplified circuit diagram

(a) Voice path. The microphone signal is allowed to pass to the modulation switch only when the AM/SSB speech processor, comprised of the audio compression and clipper amplifiers, is powered. Power to these circuits may be supplied either via the AM CONT line (pin S) or SSB (DATA) line (pin B). The output signal of the AM/SSB speech processor is applied to U2A via R31 and C21.

(b) Data path. When operating in the DATA mode, the AM/SSB speech processor does not operate. Instead, the incoming signal is applied through pin Y, through the attenuator comprised of R80 and R81 and capacitor C25, to the input of the analog switch U2B. In the DATA mode, a high level is received on the DATA (CONT) line (pin W) and U2A passes the signal to the input of U2A.

(c) CW tone path. When the WCW or NCW mode is selected, the 1-kHz synthesizer is turned following each activation of the PTT HANG line, and its output signal reaches U2A input via R43 and C23. All other paths are disabled during CW operation. The selected modulation signal passes the modulation switch U2A when operating in the transmit mode. During tuning, the modulation switch is turned off, thereby interrupting the modulation and sidetone signals (see (4) below).

(4) Control signal generation (fig. 2-6, 2-10).

(a) AM TUNE line (pin E). This line assumes a high level when the AM mode is selected (high level applied on the AM CONT line) and also during tuning, because the high level applied on the TUNE line (pin u) causes transistor Q6 to saturate and pull the AM TUNE line to a high level.

(b) AM TUNE TX line (pin J). This line assumes a high level when a carrier signal is required in the transmit mode. The high level is obtained by allowing the PTT PRE+12V voltage (appearing in the transmit mode) to pass through the analog switch U2D when the AM TUNE line is at a high level.

(c) Modulation switch control. Normally, in the transmit mode, the control line of modulation switch U2A is pulled up to the PTT PRE+12V voltage through R49 and the modulation switch is turned on. In the receive mode, the PTT PRE+12V voltage does not exist, the control line assumes a low level and the switch is turned off. However, the control line will also assume a low level in the following cases:

1. Tuning in process: when the TUNE line (pin U) is high, transistor Q7 saturates and pulls the control line to a low level.

2. Whenever the external PTT line is open. In this case, transistor Q8 saturates due to the bias current flowing through R54 and pulls the control line to a low level.

(5) PTT HANG line (pin I). This is the internal PTT line, which initiates transmission. This line behaves differently, according to the operation mode:

(a) AM, SSB and DATA modes (after tuning). In these modes, the CW (CONT) line is low, and transistor Q9 (in the HANG delay circuit) is cut off. The resulting constant high collector level is applied to pin 4 of NAND gate U4A.
Following tuning, when the external PTT line is grounded line TUNE remains low and the output of U4C is high. Therefore, all inputs of U4A are held at a high level, except the input controlled by the external PTT line via diode CR12 (pin 3). When the external PTT line is grounded, the output of U4A rises to a high level, which is then inverted by U4B and causes the PTT HANG line to assume a low level. Upon PTT release, the output of U4B rises after a 1-msec delay (caused by

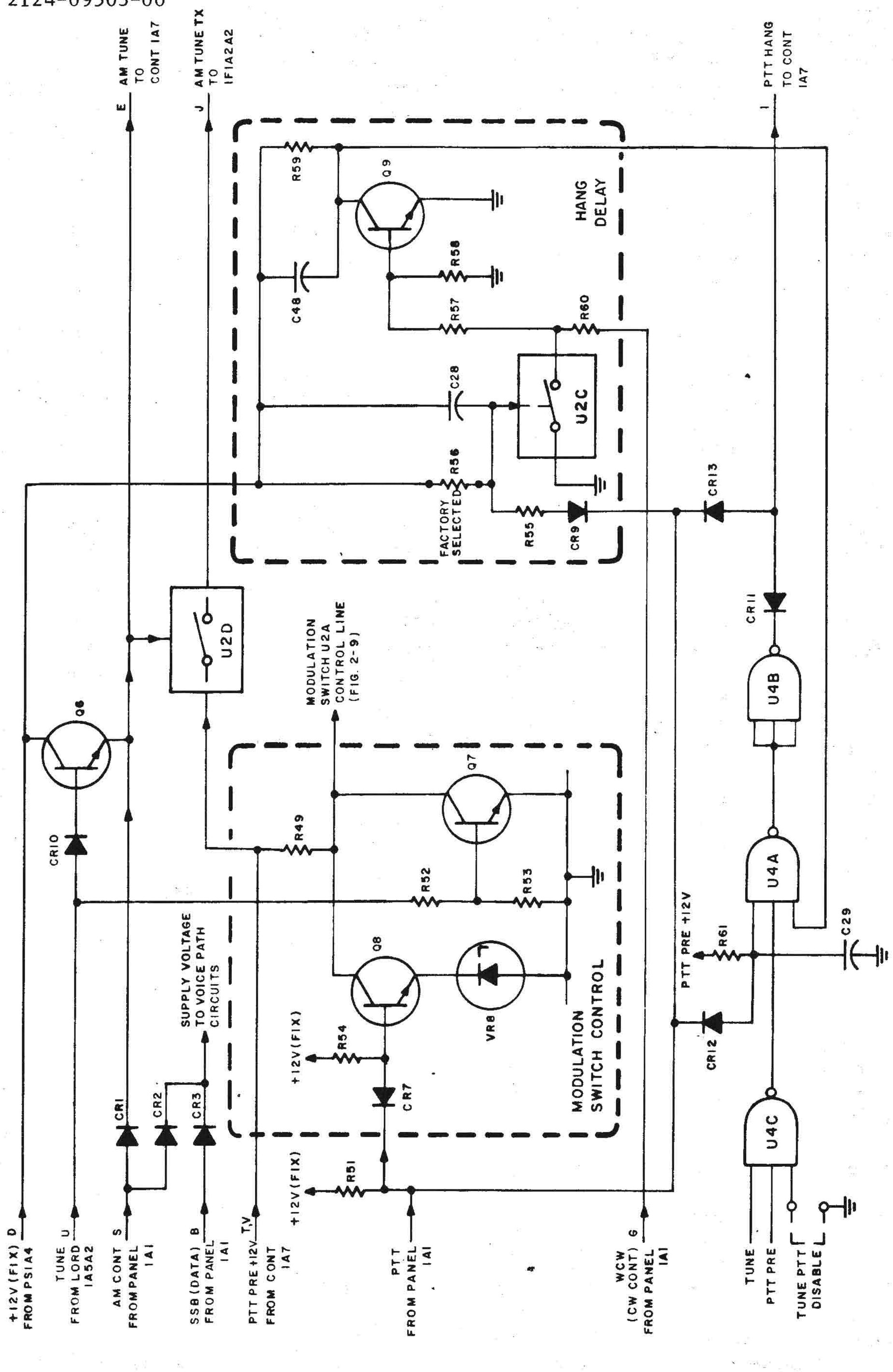


Fig. 2-10. Control signal generation, simplified circuit diagram

C29 and R61) to a high level, and so does the PTT HANG line. The PTT HANG line is pulled to +12V via two resistors (150 kohm and 10 kohm) located in module CONT 1A7. Diode CR13, however, pulls the PTT HANG line down whenever the external PTT line is grounded, irrespective of the condition of the gates.

(b) Tuning in the AM, SSB and DATA modes. During tuning, following the grounding of the external PTT line, the TUNE line rises to a high level. When the TUNE PTT DISABLE jumper is not installed, the other two inputs of U4C also receive high levels and U4C output assumes a low level. The output of U4A is thus forced to a high level until the tuning process is completed, irrespective of the condition of the external PTT line, and the PTT HANG line is therefore held low by the output of U4B, through CR11.

(c) WCW and NCW modes (after tuning). In these modes, a high level appears at pin G.
When the external PTT line is open, capacitor C28 eventually discharges through R56, a high level is applied to the control input of U2C and it turns on. Therefore, no bias is available for Q9 and it cuts off, exactly as in (a) above. When the external PTT line is grounded, the PTT HANG immediately assumes a low level, as explained in (a) above. While the PTT line is grounded, C28 charges rapidly to almost the full +12V supply voltage via CR9 and R55.
After C28 charges, the control input of U2C receives a low level, and U2C turns off. Bias current now flows into Q9 base and it saturates, thereby pulling pin 4 of U4A to a low level and forcing U4A output to a high level, irrespective of the condition of the external PTT line. Therefore, the PTT HANG remains at a low level even after the external PTT line is released, until Q9 cuts off again. Q9 cuts off after C28 discharges via the factory-selected HANG delay adjustment resistor R56· then the control input of U2C again receives a high level, U2C turns on and short-circuits the bias current to ground. Therefore, the return to the receive mode is delayed when operating in the WCW and NCW modes, to allow Morse operation without returning to the receive mode between Morse symbols and words. Note that the Morse symbols are generated by the switching action of U2A.

(d) Tuning in the WCW and NCW modes. The PTT HANG delay is also effective when tuning is initiated in these modes, however this is not significant because the tuning process is much longer. . See detailed analysis, see (b) above.

(6) RF preamplifier. This circuit receives the low-level RF signal generated by the MIXER 1A2A1 and amplifies it to a level of +20 dBm (100 mW), prior to its application to the power amplifier in module PA 1A6.
The RF signal, applied at pin R, is connected to the base of Q10 through C34. The DC bias to Q10 is supplied through the voltage divider comprised of resistors R65, R66. Resistors R67 and R68 stabilize the quiescent current of Q10[R68 is bypassed at RF by capacitor C35. Resistor R67 provides negative feedback in the emitter circuit.
Transformer T1 and capacitor C37 couple the second stage to the collector of Q10. The second stage, designed around Q11, is similar to the first, except for the negative feedback applied through C38 and R69. The third (power) stage, Q12, is driven from the collector of Q11 through transformer T2 and capacitor C41.
The bias voltage, derived from a voltage divider consisting of R74, R75 and temperature-compensation diode CR14, is fed to the base of Q12 through RF choke L6. Resistor R76 stabilizes the quiescent transistor current and is bypassed at RF by capacitor C50. The output voltage, developed across RF choke L7, is connected to output pin X through coupling capacitor C45. Negative feedback is applied via R77 and C44. Resistor R78 increases the loading on this stage, and protects it in case the external load is disconnected (e.g, when opera-

ting in the CBP mode or when module PA 1A6 is removed). The DC supply to the amplifier is +12V at a current of 300 mA. This power is supplied by the PTT PRE +12V line, which is active only during tuning and transmission. L5, L10, C36, C39, C43, C49 and C31 filter the supply voltage.

2-7. Module AUDIO 1A2A3 (fig. 2-11 thru 2-14)

Module AUDIO 1A2A3 contains the sidetone and receive path audio amplifier and the squelch control circuits.

a. Block Diagram Analysis (fig. 2-11, 2-12).

(1) Audio path in the normal receive mode. In the receive mode, the received audio signal arrives from the demodulators contained in module IF 1A2A2 (para. 2-8):

(a) At pin Y (SSB AUDIO) when operating in the SSB, DATA, WCW and NCW modes.

(b) At pin W (AM AUDIO) when operating in the AM mode.

The appropriate audio signal passes through the corresponding analog switch to the bandpass filter. The bandpass filter consists of a 350-Hz high-pass in series with a low-pass filter. The cut-off frequency of the low-pass filter is controlled by the DATA CONT line, from the front panel: in the DATA mode, the virtual cut-off frequency is 2400 Hz, in the other modes - it is 3500 Hz. The filtered signal passes through the open squelch gate to the electronic volume control circuit. The attenuation of the volume control is determined by the DC voltage arriving from the VOLUME control or a remote control device. The attenuated audio signal is amplified in the earphone amplifier and sent to the front panel connectors via the PHONE line (pin R). The audio signal appearing at the output of the squelch gate is also applied to an audio compression amplifier. This amplifier provides a constant average output voltage for the FIX AUDIO line, available in the CONTR connector. This audio output is not influenced by the setting of the VOLUME control, however it is controlled by the squelch gate when the SAVE mode is selected.

(2) Sidetone path in the transmit mode. The audio modulation signal provided by the PRE 1A2A4 module is also connected to pin T, and passes through an attenuator to the sidetone gate. The sidetone gate is an analog switch, controlled by the DC voltage appearing on the TX LEVEL line (see para. 2-14). This voltage is proportional to the RF output power of the RT-936/PRC-174. A peak sample-and-hold circuit "catches" the voltage peaks and stores them for a few seconds: this arrangement prevents changes in the gate control voltage caused by the instantaneous variations in the output power caused by the modulation. When the RF output power of the RT-936/-PRC-174 is sufficiently high, the gate control voltage provided by the peak sample-and-hold circuit exceeds the gate threshold, and the gate opens, letting the sidetone pass. When the RF output power decreases below allowable limits, the gate control voltage is too low to keep the gate open, and it closes, interrupting the sidetone signal. Therefore, the existence of a sidetone indicates that the transmit path is operational. The sidetone is however, unconditionally available at the input of the audio compression amplifier.

(3) Operational signaling path. Module CONT 1A7 (para. 2-26) provides various auditory signals which inform the operator of the RT-936/PRC-174 operational status. These signals arrive on the SIGNALING line (pin U) and pass directly to the input of the earphone amplifier.

(4) SAVE mode operation (fig. 2-12). In the SAVE mode, the squelch gate is controlled by the SAVE mode squelch circuits. These circuits are turned on and powered by the SAVE line arriving from the front panel.

The squelch circuits turn the squelch gate off, unless a speech signal is detected in the received signal. However, a special-purpose control line, SEC, allows to open the squelch gate

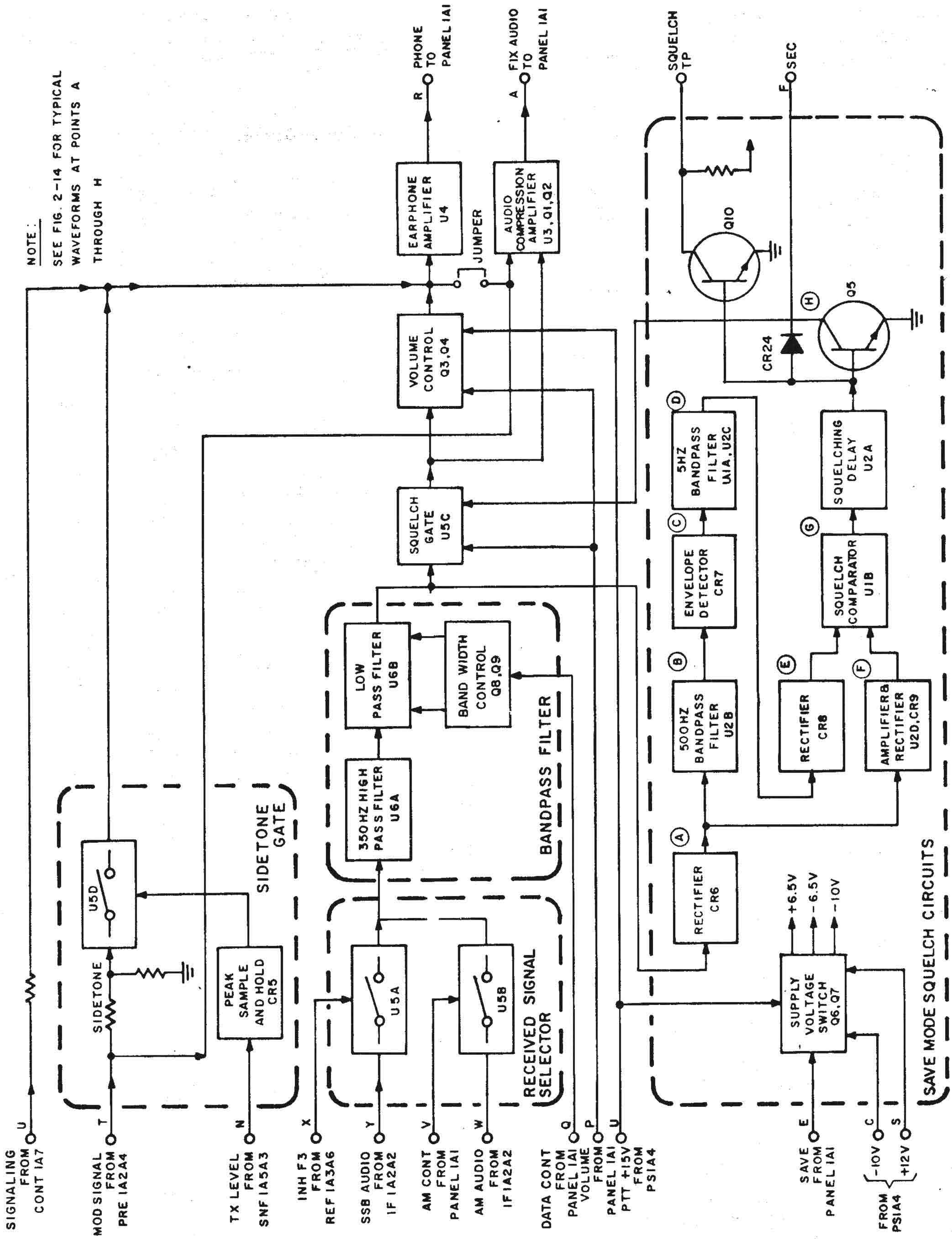


Fig. 2-11. Module AUDIO 1A2A3, block diagram

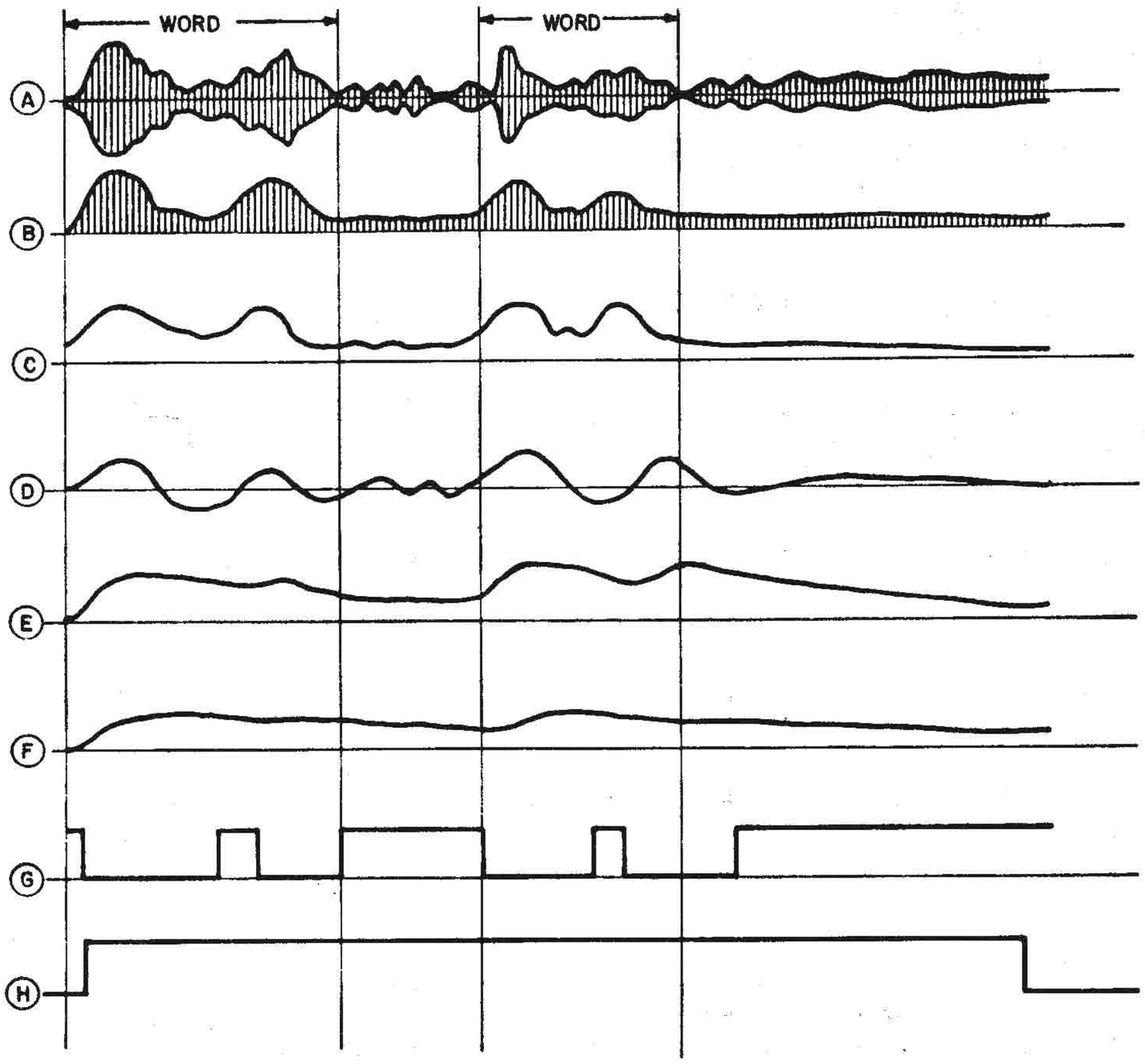


Fig. 2-12. Typical waveforms in the squelch circuit

even if the squelch circuits did not detect a voice signal. In order to detect the characteristic speech waveforms, the received signal is applied to two parallel paths, one processing the signal to extract the speech waveform, and another for setting an adaptive threshold.

(a) Signal processing path. The received signal is attenuated and then filtered by a 500-Hz bandpass filter. The filtered signal is rectified by an envelope detector, whose output is filtered again by a bandpass filter centered on 5 Hz. This filter passes the amplitude variations caused by the syllabes. The output filter of this bandpass filter is rectified and filtered, to obtain a DC voltage proportional to the syllabic modulation in the received signal. This DC voltage is applied to one of the squelch comparator inputs.

(b) Threshold generation. The rectified received signal is amplified and then rectified by a peak rectifier. The resulting DC signal is applied to the other input of the squelch comparator.

The squelch comparator turns the squelch gate on whenever the processed signal exceeds the threshold. However, to prevent gate chattering, a delay circuit delays the turn off of the gate for a short time, thereby bridging across short interruptions. This prevents interruption of the received signal between words. Fig. 2-12 shows typical waveforms in the squelch circuits.

b. Circuit Analysis (fig. 2-13, 2-14).

(1) Signal selector. The demodulated audio signals from module IF 1A2A2 (see para. 2-8) are applied at pin Y (for SSB, DATA, WCW and NCW ope-

ration) or pin W (for AM operation). The audio signal corresponding to the selected operation mode is passed by analog switch U5A or U5B, respectively. The control signals for these switches are applied at pin X (high for SSB and AM transmit operation) or pin V (high for AM operation).

(2) Bandpass filter. The selected audio signal is applied to the input of the active high-pass filter U6A, whose cutoff frequency is 350 Hz. Resistors R4, R5, R6, R7, R8 and capacitors C3, C4 determine the cutoff frequency. The pass band gain is determined by the ratio of R7 to R6. Resistors R4 and R5 determine the quiescent DC voltage at the output of the operational amplifier.
The output of U6A is coupled through C5 to the input of the active low-pass filter, built around U6B, whose cutoff frequency is determined by R9, R10, R11, R12, R13, R14, C8, C9, C43 and C44.

(a) When the DATA CONT line (pin Q) is high (function selector set to DATA), the gates of the FETs Q8 and Q9 receive +12V. The FETs are cut-off, and capacitors C8, C43 and C9, C44 are connected in series. This sets the cut-off frequency to 3500 Hz.

(b) When the DATA CONT (pin Q) is grounded, the FETs conduct and present a very low resistance. Capacitors C8 and C9 are short-circuited and the cut-off frequency decreases to approx. 2400 Hz.

Diode CR23 protects the source-gate junction of Q9 against forward-biasing by the output voltage of U6B.
The pass band gain is determined by the ratio of R14 to R13. Resistors R11 and R12 determine the quiescent DC voltage at the amplifier output. Together, the cascaded high-pass and low-pass filters provide a bandpass characteristic.

(3) Squelch gate. The filtered audio signal is transferred through the analog switch U5C to the FIX AUDIO audio compression amplifier (see (6) below), and to the electronic volume control. When transmitting, the PTT +15V line (pin O) is grounded and the squelch gate control line (pin 13 of U5C) is pulled to a low level via diode CR1. This turns off the squelch gate in the transmit mode.

(4) Electronic volume control (fig. 2-14). The electronic volume control is a voltage-controlled attenuator consisting of resistor R16 and the drain-source resistance of FET Q3, in parallel with R99. The FET resistance may be varied by the DC voltage arriving on the VOLUME line from the front panel (pin P) - thereby varying the attenuation ratio. Resistor R30 and coupling capacitor C10 reduce the distortion caused by Q3. The attenuated signal is buffered by FET Q4, which operates as a source follower. The output signal of Q4 is applied through C11 to the input of the earphone amplifier U4. In the transmit mode, the PTT +15V line (pin O) is grounded. The DC control voltage is thus shorted to ground via diode CR21, thereby neutralizing the influence of the VOLUME control. When Q3 receives nearly zero gate-source bias, it presents minimum resistance, yielding maximum attenuation. In conjunction with the closing of the squelch gate in the transmit mode, this arrangement further reduces the leakage of signals from module IF 1A2A2 to the earphone amplifier.

(5) Earphone amplifier. The earphone amplifier, U4, supplies the audio signal to the earphone (through pin R). The gain of U4 is determined by the ratio of R23 to R22. Resistors R20 and R21 determine the quiescent DC voltage at the amplifier output. Capacitor C14 reduces the DC gain to unity, while presenting a low reactance in the frequency range of interest.
The output signal is sent to the earphone via capacitors C12, resistor R24 and pin R.

(6) Audio compression amplifier. The signal appearing at the output of

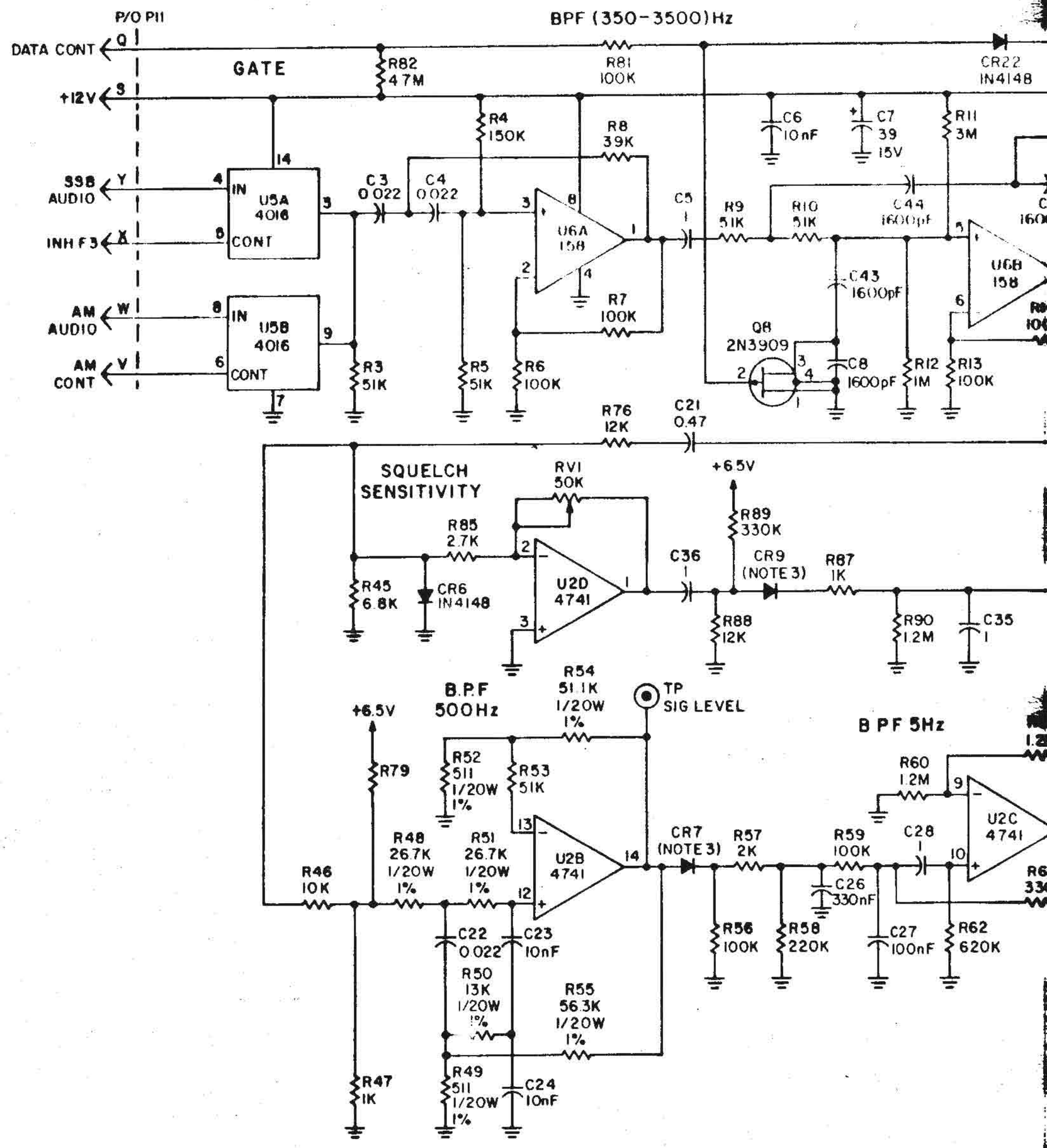
the squelch gate U5C is also coupled via capacitor C1 and R1 to the FIX AUDIO compression amplifier, built around operational amplifier U3.
The applied signal is attenuated by a voltage divider, consisting of resistor R1 and the drain-source resistance of FET Q1 in parallel with R31. The attenuated signal is amplified by U3 and sent, via an attenuator consisting of R80 and R38, to the FIX AUDIO output (pin A). A sample of the output voltage of U3 is applied via a voltage divider to the base of Q2. The divider comprises the fixed resistors R33, R37, R40 and the temperature dependent resistor R39. The resistance of R39 varies in a manner which stabilizes the output level of U3 against ambient temperature variations.
The collector of Q3 is connected through R32 to -10V. When no signal is detected, capacitor C2 charges to -10V. This causes the drain-to-source resistance of FET Q1 to be very high; thus, the attenuation introduced by the variable attenuator is negligible. When a sufficiently high-level signal appears, transistor Q2 starts to conduct. This causes C2 to discharge rapidly.
The decreased gate-source bias decreases the drain-source resistance of Q1, thereby increasing the attenuation of the speech signal, until the discharge of C2 through R22, Q2 and Q3 is balanced by the small charging current supplied through R32. The resulting output level of the compression amplifier is such that the speech peaks remain at a relatively constant level for a wide range of input signals.
The resulting FIX AUDIO level at pin AS is 220 mV. When speech stops or its level decreases, the voltage on capacitor C16 starts decreasing slowly, because of the very long charging time constant. This keeps the average level from changing during short interruptions (between words, etc); the circuit thus provides fast-attack, slow-release action.

(7) Sidetone path. The modulation signal arriving from module PRE 1A2A4 at pin T is applied, via resistor R96, to the input of the FIX AUDIO audio compression amplifier.
The modulation signal is also applied via a voltage divider comprised of R28 and R26, analog switch U5D and capacitor C13, to the input of the earphone amplifier. In the receive mode, the control input (pin 12) of U5D is at a low level and the sidetone gate is closed.
In the transmit mode, a varying DC voltage is received from the forward RF power detector in module SNF 1A5A3 on the TX LEVEL line (pin N). This voltage is proportional to the instantaneous output power. A peak sample-and-hold circuit, consisting of CR5, R97, R27 and C15, stores the peaks of the TX LEVEL voltage, thereby converting it to a relatively constant voltage, whose value is proportional to the peak RF output power. When the RF output power exceeds a certain minimum value, the voltage across C15 exceeds the gate threshold and the gate opens, allowing the sidetone signal to pass to the earphone. When the RF signal stops, C15 discharges slowly through R27. Diode CR5 becomes reverse-biased and prevents discharge through R97. Typically, the voltage across C15 will remain above the switching threshold of U5D for approximately 3 seconds; after this interval, U5D turns off and interrupts the sidetone. This arrangement ensures that the sidetone will be heard only when there is enough transmitter power.

(8) Signaling path. The signaling arriving from module CONT 1A7 at pin U is connected via resistor R25 to the input of the earphone amplifier. The signaling can be heard in the earphone in all operating modes; it can also be connected to the input of the audio compression amplifier by a jumper, thus making the signaling available at the FIX AUDIO output.

(9) Squelch circuits.

(a) Activation of squelch circuits. The squelch circuits are po-



NOTES :

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH 1A2A3.
2. UNLESS OTHERWISE SPECIFIED
   ALL RESISTORS ARE IN OHMS, 5%, 1/8W
   ALL CAPACITORS ARE IN MICROFARADS
3. CR7, CR8 AND CR9 ARE DIODES P/N 24-21122
4. R39 IS THERMISTOR P/N 24-11440.
5. THE JUMPER SHALL BE DISCONNECTED WHEN USED WITH MOTHERBOARD P/N 2124-32800 REV. E.
6. ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED
7. THE JUMPER SHALL BE CONNECTED WHEN SIGNALLING AT FIX AUDIO OUTPUT (PIN A) IS DESIRED
8. R18 IS SELECTED FROM 680 KOHM, 820 KOHM, 1 MOHM, 1.3 MOHM, 2.0 MOHM, AND 3.0 MOHM

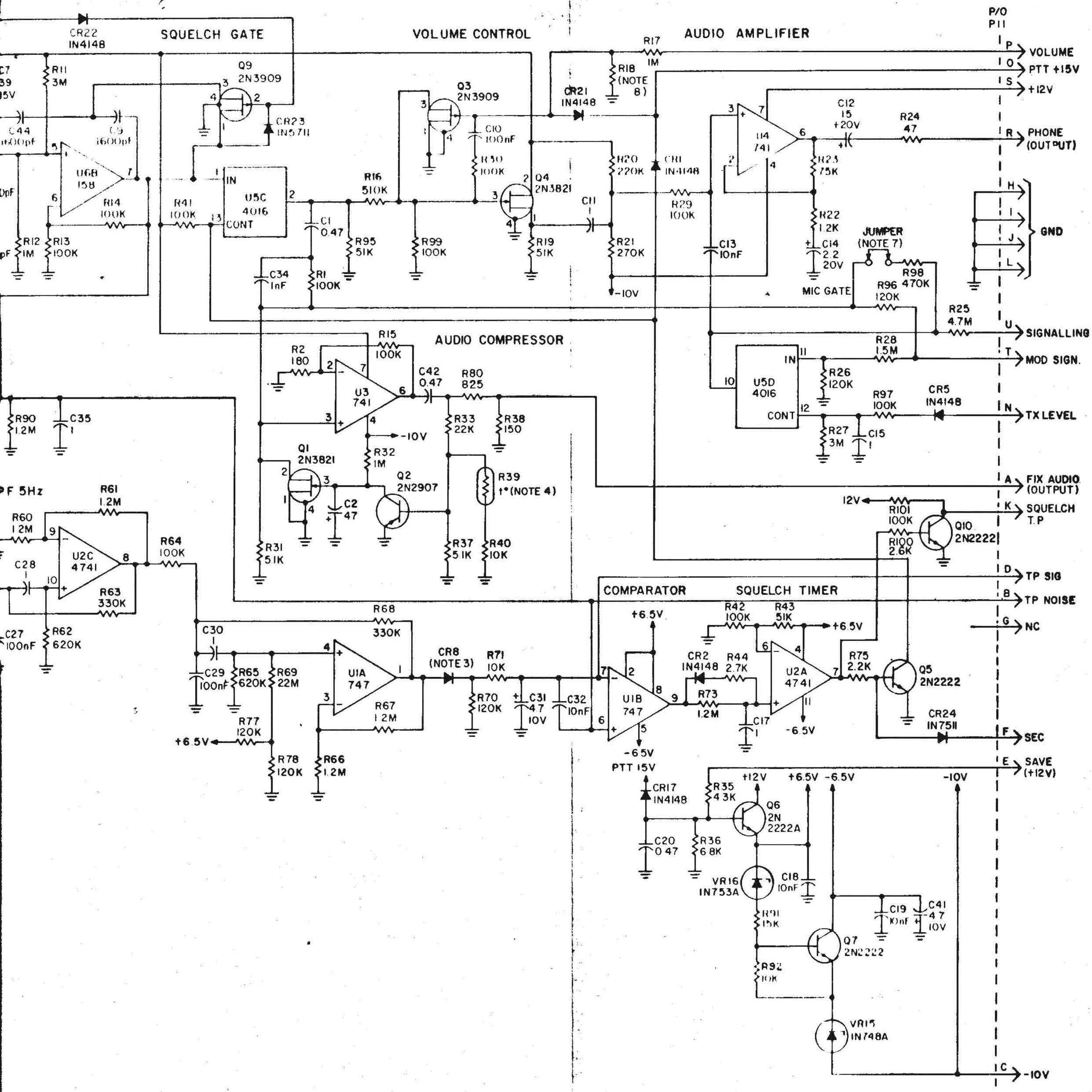


Fig. 2-13. Module AUDIO 1A2A3, schematic circuit diagram

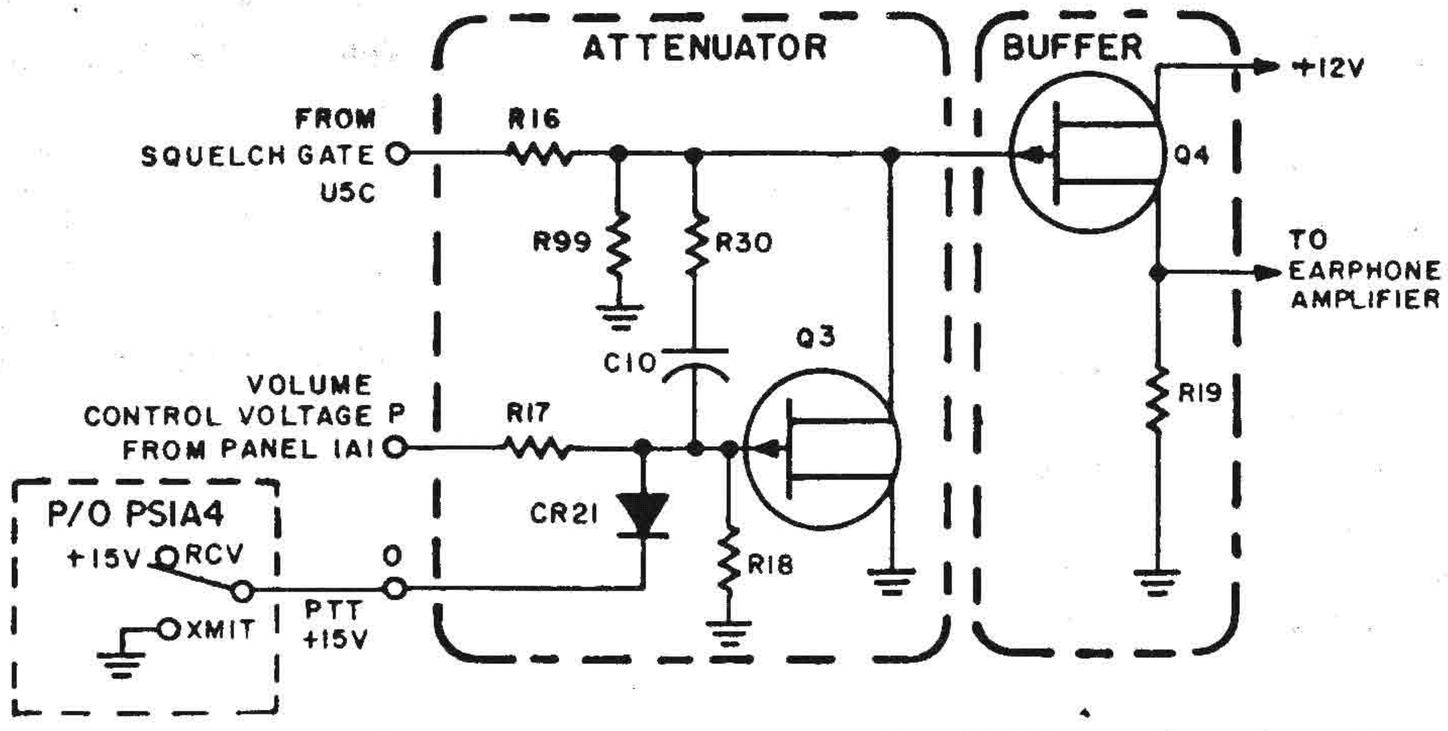


Fig. 2-14. Electronic Volume Control, Simplified Circuit Diagram

wered only in the SAVE mode. In this mode, a high level is received at pin E from the front panel. The high level causes Zener diodes VR15 and VR16 to break down, thereby allowing current to flow through both Q6 and Q7. The voltage divider comprised of R35 and R36 determines the voltage at the emitter of Q6: +6.5V. The voltage at the collector of Q7 is set to -6.5V by the breakdown voltage of VR15 and the saturation voltage of Q7. The +6.5V voltage appearing at the emitter of Q6 and the -6.5V voltage appearing at the collector of Q7 are used to power operational amplifiers U1 and U2 of the squelch circuit. When transmitting, the squelch circuits are disabled by means of the PTT +15V signal, to allow hearing the sidetone. In the transmit mode, the PTT +15V is grounded, thereby diverting the base current of Q6 to ground via diode CR17. In the receive mode, the +15V appearing on the PTT +15V line reverse-biases diode CR17, and the squelch circuits are enabled again.

(b) Squelch circuit operation (fig. 2-12). The filtered audio signal appearing at the output of U6B is applied through C21 and the voltage divider comprised of R76 and R45 to the rectifier diode CR6. At the anode of CR6, a negative half-wave rectified replica of the received signal appears, and is simultaneously applied to the inputs of the signal processing path and to the threshold-generation path.

1. Signal processing path. The input voltage passes through a voltage divider, composed of R46 and R47, and then filtered by a 500-Hz bandpass filter, built around U2B. The output signal of U2B (B in fig. 2-12) is applied to an envelope detector, built around CR7. A small forward bias is applied to this diode; this bias is developed by amplifying the small positive voltage applied via R79 across R47.
The rectified voltage (C in fig. 2-12) is filtered by a 5-Hz bandpass filter, comprised of U2C and U1A. The output voltage of U1A (D in fig. 2-12), which is the envelope of the received signal, is again rectified by CR8 and filtered by R71 and C31 (E in fig. 2-12). The voltage across C31 is applied to the inverting input (pin 7) of the squelch comparator, U1B.

2. Threshold generation. The rectified voltage appearing across CR6 is amplified by U2D and then coupled through capacitor C36 to a rectifier, built around CR9. A small forward bias is applied to CR9 from the voltage divider comprised of R88 and R89. The rectified voltage is filtered by R87 and C35, and the resulting DC voltage (F in fig. 2-12) is applied to the non-inverting input (pin 6) of the squelch comparator, U1B.
When the received signal does not contain speech, the voltage at the noninverting input of U1B exceeds that at its inverting input. Consequently, the output of U1B (G in fig. 2-12) ri-

ses to +6V, and capacitor C17 starts to charge slowly through R73. Eventually, the voltage across C17 exceeds the voltage applied to the inverting input of the squelching delay U2A (pin 6) via the voltage divider comprised of R42 and R43, and the output of U2A rises to +6V. Bias current then flows through R75 to the base of Q5, and it saturates, causing the control voltage (H in fig. 2-12) of the squelch gate U5C to fall to zero. The squelch gate closes, and the received signal cannot pass to the audio amplifiers.

When the received signal contains speech, the voltage applied to the inverting input of U1B exceeds the threshold voltage applied to its non-inverting input. Consequently, the output of U1B falls to -6V, rapidly discharging C17 through CR2 and R44. When the voltage across C17 decreases below the voltage at the inverting input of U2A, the output of U2A falls to -6V, causing Q5 to cut off. The control voltage of the squelch gate then rises to almost +12V, and the gate opens, allowing the received signal to pass to the audio amplifiers.

The transistor Q5 can also be turned off by applying a low level at pin F (SEC line), thereby forcing the squelch gate open. Transistor Q10 is connected in parallel with Q5 to the output of U2A, however it is not affected by the SEC line. The output of Q10 is available at contact K (SQUELCH TP).

The slow charging time constant of C17 ensures that short positive pulses appearing at the output of U1B do not change the state of the squelch gate.

2-8. Module IF 1A2A2 (fig. 2-15 through 2-19)

Module IF contains the modulator for the transmit path, an IF amplifier, demodulators for AM and SSB operation and AGC detectors.

a. Block Diagram Analysis (fig. 2-15).

(1) Transmit path. The transmit path is activated when the PTT PRE+12V line arriving from module CONT 1A7, rises to +12V. Concomitently, the receive path circuits are disabled, because the +6V supply voltage of the input IF amplifier is disconnected by the supply switch. The transmit path receives two input signals: the audio modulation signal from module PRE 1A2A4 and the 5.25-MHz carrier signal from module REF 1A3A6, which passes through the carrier switching circuit. The signals are applied to the double-balanced modulator. The resulting double-sideband 5.25-MHz signal is amplified in a buffer circuit and then sent to the MIXER 1A2A1 via module FILTER 1A2A5. In the AM mode, and also during tuning, the 5.25-MHz carrier reinsert amplifier is turned on by means of the AM TUNE TX line coming from module PRE 1A2A4 (para. 2-6.b(4)). The 5.25-MHz carrier signal appearing at its output is then applied to the buffer amplifier. In the buffer amplifier, the 5.25-MHz carrier signal is added to the double-sideband signal provided by the modulator, thereby reconstructing the AM signal.

(2) Receive path. The receive path is activated when the PTT PRE +12V line is grounded. This turns on the supply switch and +6V is supplied to the IF amplifier and AM audio output amplifier.

The receive path receives two signals: the received 5.25-MHz IF signal from module MIXER 1A2A1, and the 5.25-MHz carrier signal, which passes through the carrier switching circuit to the SSB demodulator. The 5.25-MHz IF signal is amplified by the IF amplifier and is then supplied to the SSB and AM demodulators. The output signal of the SSB demodulator is sent through a temperature compensated attenuator to pin E. The output signal of the AM demodulator (which is an envelope detector) is first amplified and then sent to pin W. An AGC detector provides two AGC voltages: AGCI for the local IF amplifier, and AGCII for module MIXER 1A2A1. The AGC voltage is also sent via the S METER line to module CONT 1A7, where it is measured and converted into a received-signal strength indication on the solid-state display.

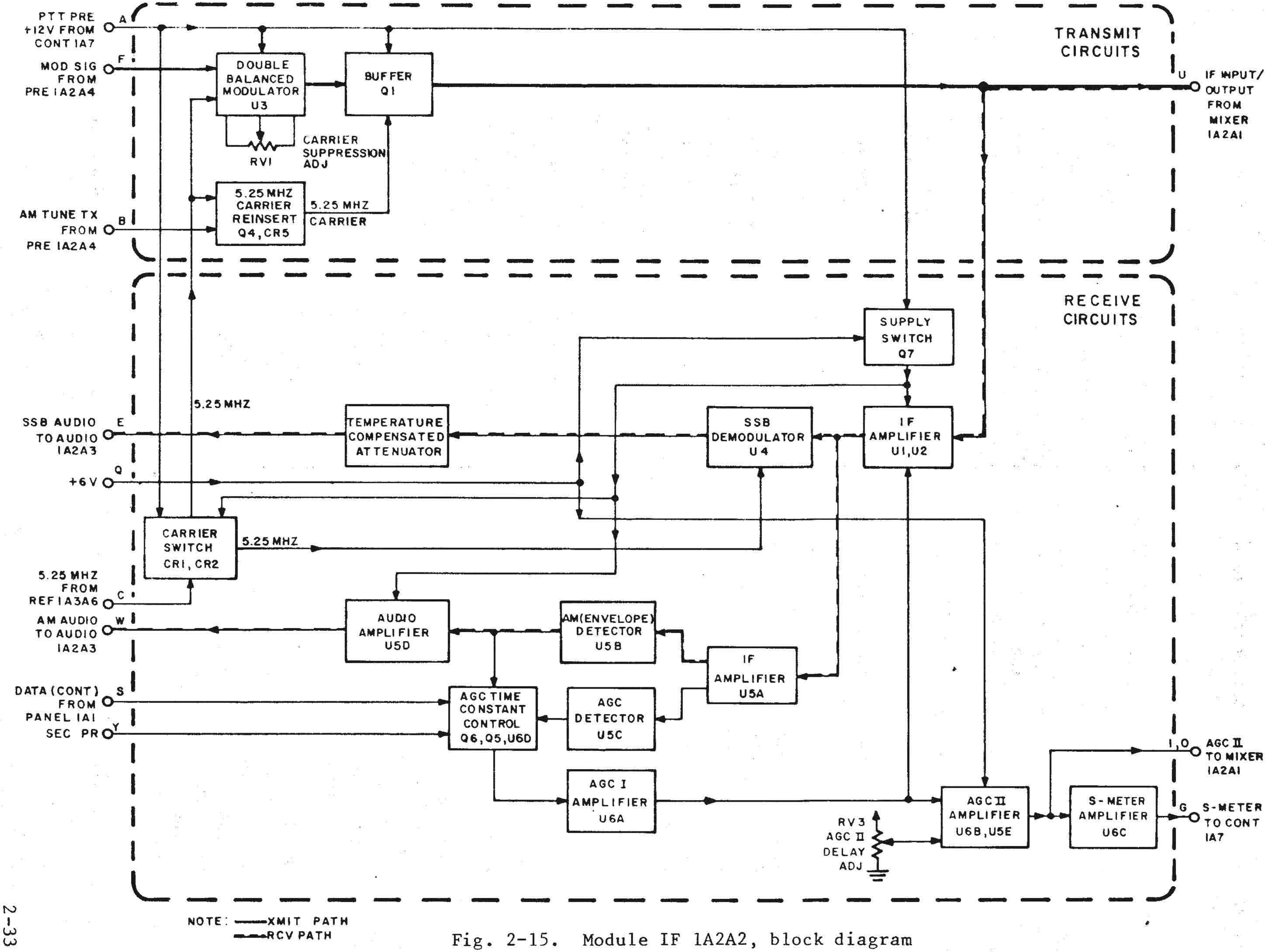


Fig. 2-15. Module IF 1A2A2, block diagram

MA 2124-09503-00

The AGC detector provides nearly zero AGC voltage for signals that do not exceed the internal noise of the receiver, to ensure maximum gain for feeble signals. The release time of the AGC circuit is decreased when the DATA operating mode is selected, to improve data transmission performance under fading conditions. The release time is changed by means of the DATA (CONT) control line arriving from the front panel, or by the SEC PR line (pin Y).

b. Transmit Path Circuit Analysis (fig. 2-17).

(1) SSB modulator. The SSB modulator, built around U3, is a double-sideband modulator which performs the modulation of the 5.25-MHz carrier in all operating modes.

The SSB modulator is powered when the PTT PRE +12V line rises to +12V. This provides bias voltages for all input and output terminals, except for V-: this voltage is obtained from the -10V supply voltage, via transistor Q2 and Zener diode VR4. Transistor Q2 turns on when the PTT PRE +12V line rises, due to the current which flows through Zener diode VR3 and resistor R24.

The carrier signal, arriving from module REF 1A3A6 to pin C, passes through the PIN switching diode CR1 to the carrier input (pin 7) of U3. Diode CR1 is forward-biased by the current flowing from the PTT PRE +12V line via resistor R23, the diode and resistor R7, and therefore presents a low resistance to the carrier signal. The voltage developed across R7 reverse-biases PIN diode CR2 and thus disconnects the carrier signal from the receive path circuits. Bias to the carrier input of U3 is provided by the voltage divider comprised of R16 and R9. The modulation signal, arriving from module PRE 1A2A4 at pin F, is applied to the signal input (pin 1).

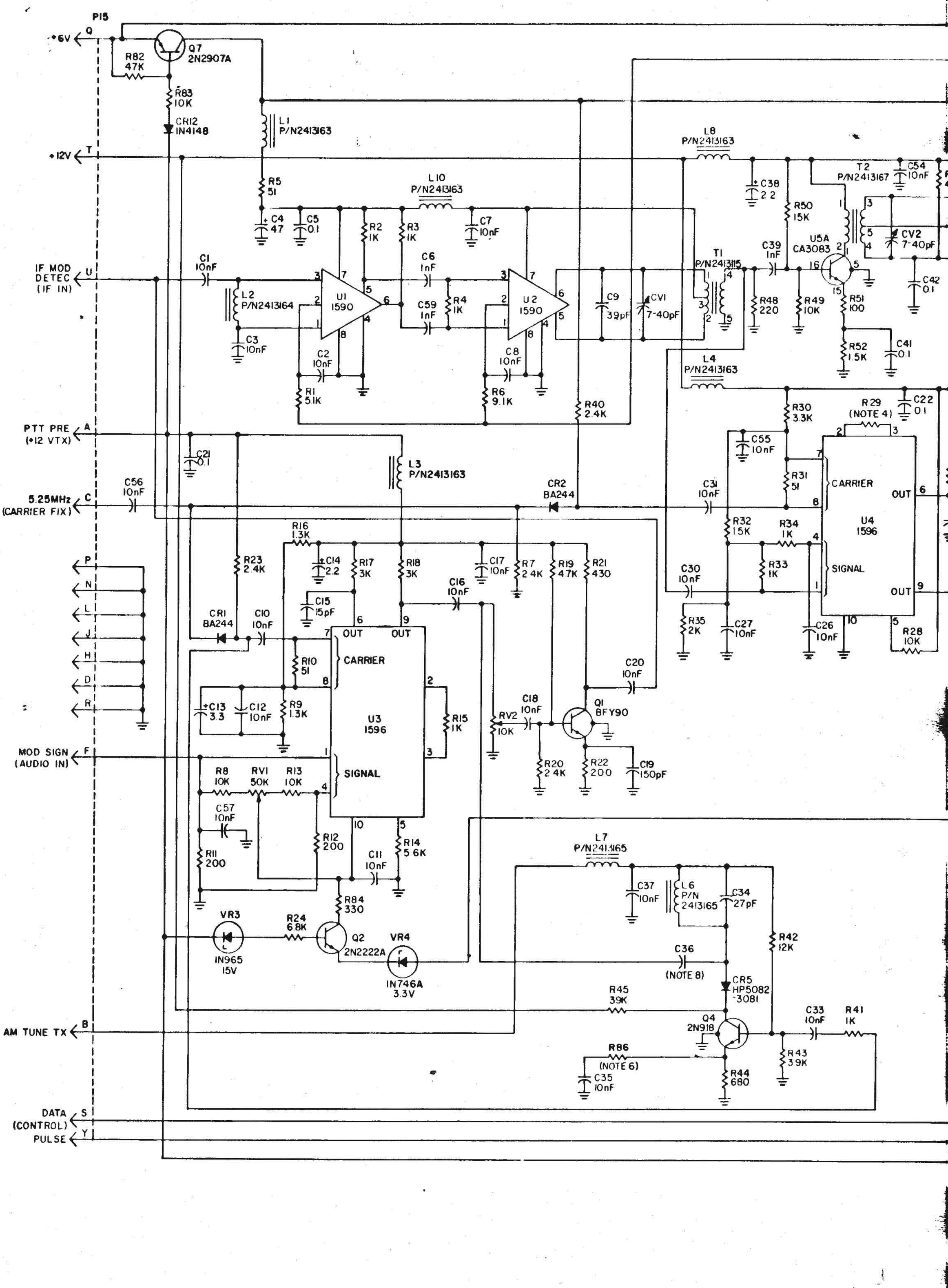
Bias to the signal input is applied through R11 and R12. The network comprised of R8, RV1, and R13 is used to apply a small offset voltage for obtaining maximum carrier suppression at the output of U3 (pin 9).

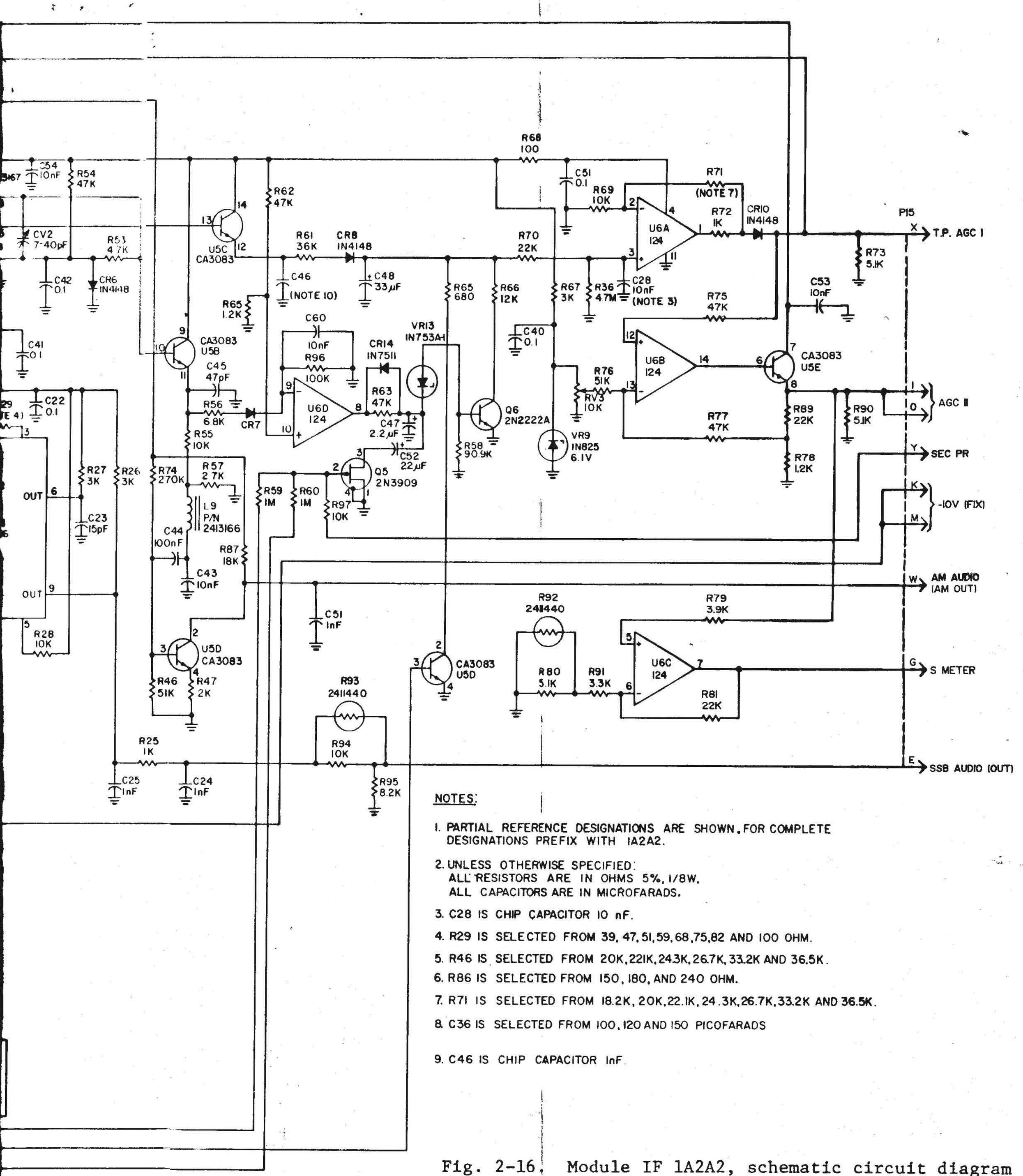
The gain of the modulator is determined by the ratio of the load resistor R18 and the gain-setting resistor R15.

The double-sideband signal appears across load resistor R18 and is coupled through capacitor C16 to potentiometer RV2.

(2) Output amplifier. The signal appearing at the moving contact of potentiometer RV2 is coupled via capacitor C18, to the base of Q1. Bias to Q1 is applied via resistors R19 and R20. The value of the collector load resistor R21 is selected to match the input impedance of the filters in module FILTER 1A2A5 (see para. 2-9). The output signal of Q1 is applied to module FILTER, via C20 and pin U.

(3) Carrier reinsert amplifier (fig. 2-16). This circuit is built around Q4. When transmit AM operation is selected, or tuning is in progress, the AM TUNE TX line (pin B) receives +12V from module PRE 1A2A4 (see para. 2-6.b.(4)). This supplies power to the carrier amplifier transistor Q4 and allows current to flow through the PIN diode CR5, which then presents negligible resistance to the carrier signal. R42 and R43 supply bias voltage to Q4. L6 and C34 form the tuned collector load of Q4. R86 determines the reinserted carrier level and is selected accordingly. L7 and C37 filter the supply voltage of Q1. The carrier signal is received from pin C, through the forward-biased PIN diode CR1, resistor R41 and capacitor C33. The amplified carrier signal, appearing at the collector of Q4, is connected via CR5 and C36 to the high end of RV2, thus reinserting a fixed level of carrier at the modulator output. Capacitor C36 is selected to obtain the correct phase relationship of the carrier to the double-sideband signal. When the AM TUNE TX line is low, there is no supply voltage for Q4. Diode CR5 is reverse-biased by the +12V voltage applied to its cathode through R45 and further attenuates carrier leakage through Q4.


P15
+6V
Q
Q7
2N2907A
R82
47K
R83
10K
CR12
IN4148
L1
P/N2413163
+12V
T
R5
51
C4
4.7
C5
0.1
L10
P/N2413163
R2
1K
R3
1K
C7
10nF
L8
P/N2413163
C38
22
R50
15K
T2
P/N2413167
C54
10nF
U5A
CA3083
CV2
7-40pF
C39
1nF
T1
P/N2413115
C42
0.1
IF MOD
DETEC
(IF IN)
U
C1
10nF
L2
P/N2413164
C3
10nF
U1
1590
C6
1nF
C59
1nF
R4
1K
U2
1590
C9
39pF
CV1
7-40pF
R48
220
R49
10K
R51
100
R52
1.5K
C41
0.1
C2
10nF
R1
5.1K
C8
10nF
R6
9.1K
R40
2.4K
L4
P/N2413163
R30
3.3K
R29
(NOTE 4)
C22
01
PTT PRE
(+12 VTX)
A
C21
0.1
L3
P/N2413163
C55
10nF
R31
51
C31
10nF
CARRIER
OUT
U4
1596
SIGNAL
OUT
5.25MHz
(CARRIER FIX)
C
C56
10nF
CR2
BA244
R32
1.5K
R34
1K
R33
1K
C30
10nF
R35
2K
C27
10nF
C26
10nF
R28
10K
P
N
L
J
H
D
R
R16
1.3K
R23
2.4K
C14
2.2
R17
3K
R18
3K
C17
10nF
R7
2.4K
R19
4.7K
R21
430
C16
10nF
C15
15pF
CR1
BA244
C10
10nF
OUT
OUT
CARRIER
R10
51
C20
10nF
C13
3.3
C12
10nF
R9
1.3K
U3
1596
R15
1K
C18
10nF
RV2
10K
Q1
BFY90
R20
2.4K
R22
200
C19
150pF
MOD SIGN
(AUDIO IN)
F
R8
10K
RV1
50K
R13
10K
SIGNAL
C57
10nF
R12
200
R14
5.6K
R11
200
C11
10nF
L7
P/N2413165
C37
10nF
L6
P/N
2413165
C34
27pF
R42
12K
R84
330
VR3
IN965
15V
R24
6.8K
Q2
2N2222A
VR4
IN746A
3.3V
C36
(NOTE 8)
CR5
HP5082
-3081
R45
39K
Q4
2N918
C33
10nF
R41
1K
AM TUNE TX
B
R86
(NOTE 6)
C35
10nF
R43
3.9K
R44
680
DATA
(CONTROL)
S
PULSE
Y



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH 1A2A2.
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS 5%, 1/8W.
   ALL CAPACITORS ARE IN MICROFARADS.
3. C28 IS CHIP CAPACITOR 10 nF.
4. R29 IS SELECTED FROM 39, 47, 51, 59, 68, 75, 82 AND 100 OHM.
5. R46 IS SELECTED FROM 20K, 22IK, 24.3K, 26.7K, 33.2K AND 36.5K.
6. R86 IS SELECTED FROM 150, 180, AND 240 OHM.
7. R71 IS SELECTED FROM 18.2K, 20K, 22.1K, 24.3K, 26.7K, 33.2K AND 36.5K.
8. C36 IS SELECTED FROM 100, 120 AND 150 PICOFARADS
9. C46 IS CHIP CAPACITOR 1nF.

Fig. 2-16. Module IF 1A2A2, schematic circuit diagram

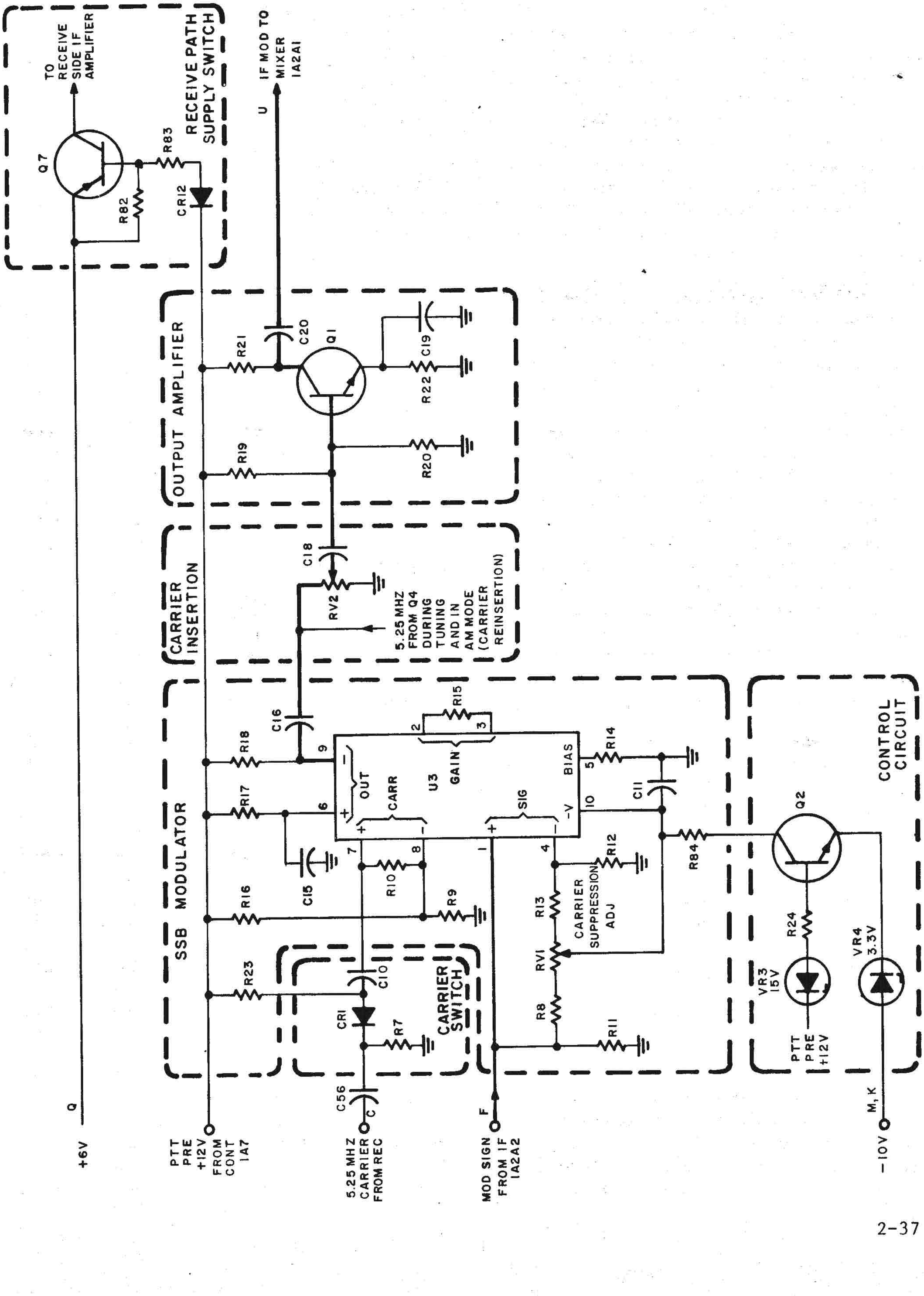


Fig. 2-17. Transmit path, simplified schematic diagram

c. Receive Path (fig. 2-18). The receive path is activated when the PTT PRE +12V line is grounded. Current then flows from the base of transistor Q7, R83 and CR12, and Q7 saturates. +6V is applied via Q7 to U1, U2, and via R40 to the PIN diode CR2. CR2 conducts and connects the 5.25-MHz carrier signal to the SSB demodulator (see (2) below). The voltage on R7 then reverse-biases CR1 and disconnects the carrier signal from the transmit path circuits.

(1) IF amplifier. The received 5.25 MHz IF signal arriving from module FILTER 1A2A5 to pin U is coupled through C1 to integrated circuit U1. U1 is a differential input differential output RF amplifier with AGC capability. C3 decouples the second input of U1, and L2 provides a bias path to pin 3. The gain of U1 is controlled by the AGCI voltage applied to pin 2. This voltage is decoupled by R1 and C2. R2 and R3 are load resistors. The output voltages appearing at pins 5 and 6 of U1 are coupled through C59 and C6 to amplifier U2, which is identical to U1. The output load of U2 is the tuned-primary transformer T1. Capacitor CV1 adjusts the resonance frequency to 5.25 MHz.

(2) SSB demodulator. The SSB demodulator is built around the double balanced modulator U4, which operates as a product detector.
The IF signal appearing at the secondary of T1 (approximately 35 mV) is coupled through C30 to the SIGNAL input of U4, and the 5.25-MHz signal - to its CARRIER input (through C56, CR2, C31). A voltage divider comprised of R30, R32, and R35, (bypassed by C27 and C55) provides bias voltages for U4 inputs. The bias voltages are applied via R31, R33 and R34.
The gain of U4 depends on the ratio of the load resistor to the gain-setting resistor R29. The value of R29 is selected to achieve the correct SSB demodulated audio level.
The audio output voltage developed across R26 is filtered by C25, R25 and C24, and is then sent via the temperature-compensated attenuator comprised of thermistor R93 and resistors R94 and R95, and pin E, to module AUDIO 1A2A3. The changes in the attenuation cancel temperature induced variations in the gain of U4.

(3) AM envelope detector and AM audio amplifier. The IF voltage appearing across the secondary of T1 is coupled through C39 to a buffer stage incorporating U5A (this is one of the five independent transistors contained in the integrated circuit U5). The output voltage of U5A is coupled through transformer T2 to the base of U5B, which performs envelope detection. The secondary of T2 is tuned to 5.25 MHz by CV2.
To improve detection linearity, the base of U5B receives a small forward bias, developed from the voltage drop across CR6, and connected to the base via the secondary of T2. C42 connects the low end of the secondary winding to ground.

The rectified voltage appearing at the emitter of U5B is attenuated by R55 and R57 and applied via the IF filter L9, C43, and coupling capacitor C44, to the base of the audio amplifier, U5D. The gain of U5D is determined by the ratio of R87 to R47. The output signal of U5D is connected to pin W (the AM AUDIO line) and applied to module AUDIO 1A2A3.

(4) AGCI voltage generation (fig. 2-16, 2-19). The AGC voltage is derived from the emitter voltage of transistor U5C. Transistor U5C receives part of the secondary voltage of T2, together with the small forward bias due to CR6. The peak-rectified signal appearing at its emitter is filtered by C46, R61, C48, R70 and C28. The voltage across C28 is amplified by the non-inverting amplifier U6A. The gain of U6A is determined by the ratio of R71 to R69, and can be adjusted by selecting the value of R71. The output voltage of U6A passes through CR10 to the AGCI line, used to

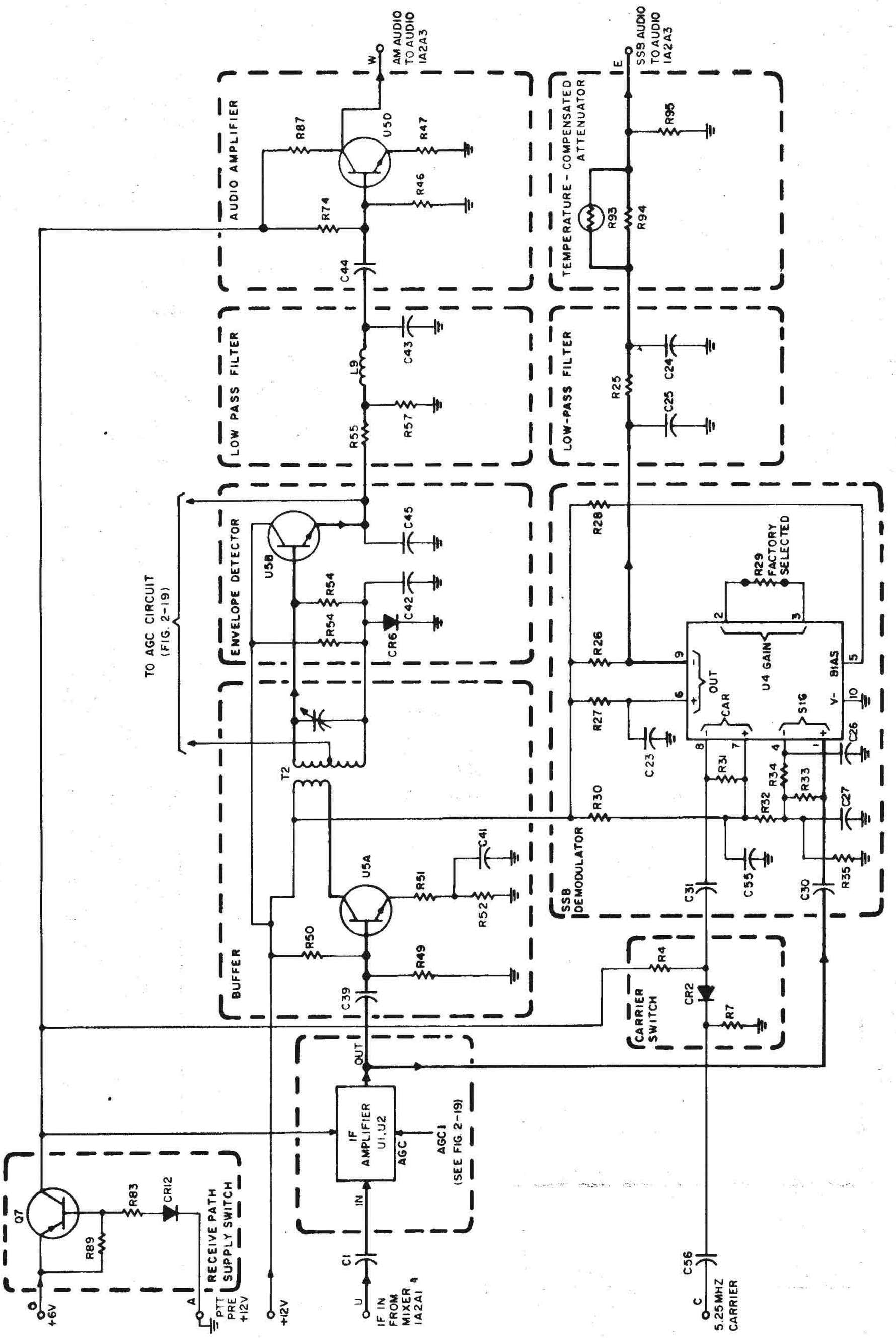


Fig. 2-18. Receive path, simplified schematic diagram

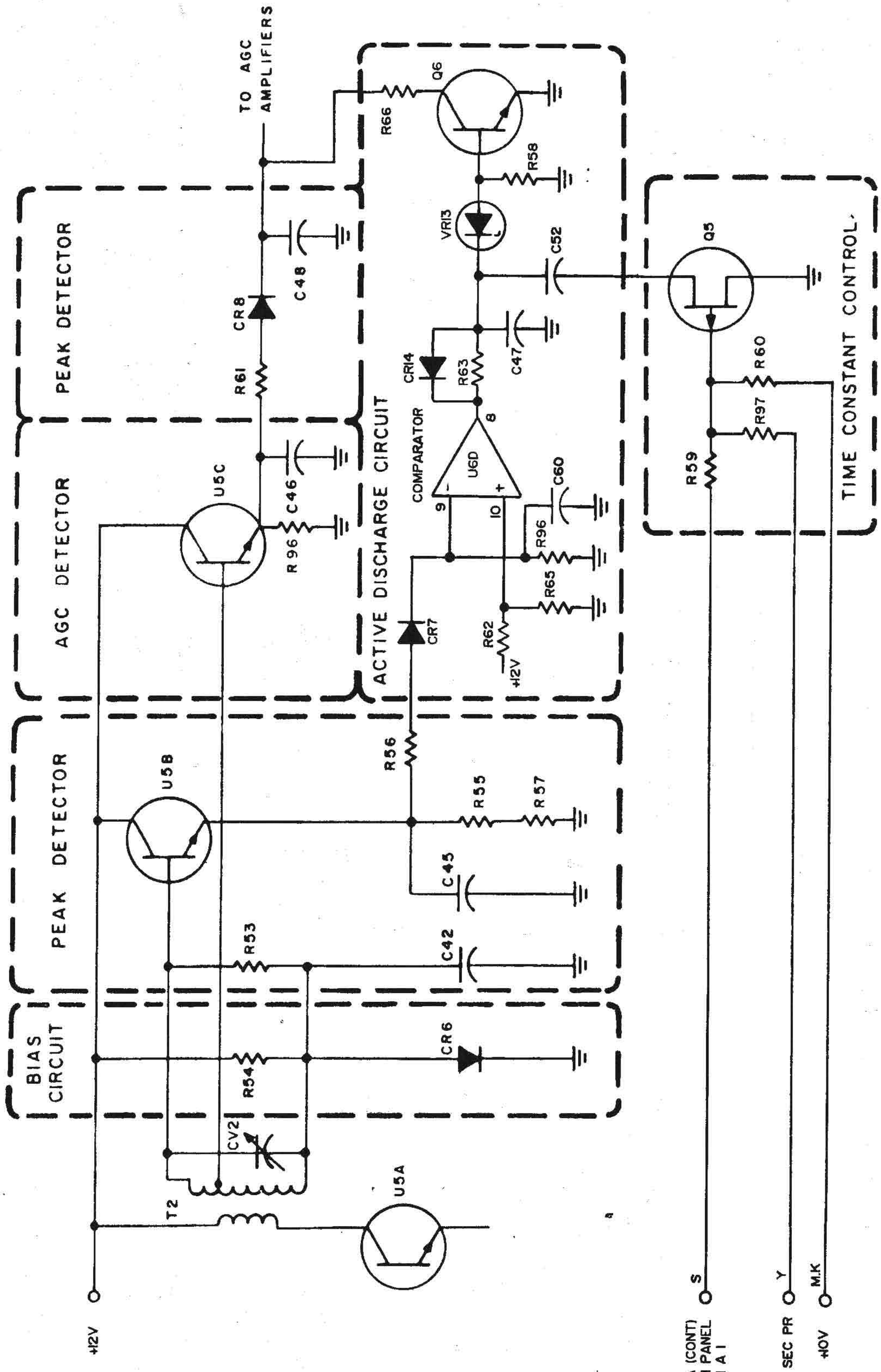


Fig. 2-19. AGC detector, simplified schematic diagram

control the gain of the IF amplifiers U1, U2 (see (1) above).

The active discharge circuit, comprising U6D and Q6, ensures that the AGC voltage due to internal noise, is close to zero. The inverting input of the comparator U6D receives the DC (AGC) voltage developing at the emitter of U5B via the peak holding network comprising R56, CR7, R96 and C60. The voltage across C60 is compared with the voltage applied to the non-inverting input of U6D via voltage divider R62, R65.

(a) As long as the AGC voltage does not exceed the voltage across R65, the output of U6D is high and capacitor C47 charges via R63. When the voltage across C47 exceeds the breakdown voltage of Zener VR13, transistor Q6 is biased into conduction and connects the resistor R66 across C48. This reduces the AGC voltage to nearly zero, because of the voltage divider R61,R66.

(b) When the AGC voltage rises (due to the reception of a useful signal) and exceeds the voltage at the non-inverting input of U6D, the output of U6D falls to zero volts, and capacitor C47 discharges rapidly via CR14. As a result, Q6 cuts off, and the AGC voltage can reach its normal values.

In the DATA mode, the release time of the active discharge circuit is decreased by disconnecting capacitor C52 in parallel with C47 with the FET Q5. The gate of Q5 is connected via R60 to the PTT PRE line, via R59 to the DATA CONT line, and via R97 - to the SEC PR line. In the transmit mode, the positive voltage applied via R60 holds Q5 cut off. The same is true in the receive mode when the DATA mode is selected (because the DATA CONT line is at nearly zero volt in all other modes). In the data mode, the DATA CONT line is high (+12V approx), Q5 is off and disconnects the capacitor C52 from ground. The SEC PR line, when grounded, holds Q5 on permanently.

(5) AGCII and S-METER voltage generation. The AGCI voltage appearing at the cathode of CR10 is applied to the non-inverting input of U6B (pin 12). A reference voltage, developed across the temperature-compensated Zener diode VR9 and adjusted by potentiometer RV3, is applied to the inverting input of U6B (pin 13). The gain of U6B (including the booster transistor U5E) is determined, essentially, by resistors R89 and R78. The delayed AGC voltage appearing at the emitter of U5E is sent via the AGCII line to the MIXER 1A2A1, where it is used to reduce the gain of the RF and IF stages where strong signals are received.
The AGCII voltage is also applied, via R79, to the non-inverting input of U6C (pin 5). The gain of U6C is determined by the ratio of R81 to the equivalent resistance of the temperature dependent resistor network R91, R92 and R80. The gain variations cancel the AGC voltage variations caused by temperature changes. The output voltage of U6C is sent to the CONT 1A7 module via the S-METER line (pin G), where it is converted to a relative indication of the received signal strength.

d. The +12V supply voltage is filtered by L8, C38, C54, R68, C51, L4, and C22.
The PTT PRE +12V line is filtered by C21, L3, C17, and C14. The AM TUNE TX line is filtered by L7 and C37.

2-9. Module FILTER 1A2A5 (fig. 2-20)

Module FILTER 1A2A5 contains three crystal filters, which provide the required receiver selectivity and band-limit the transmitter signal.

a. The SSB filter, FL1, passes the

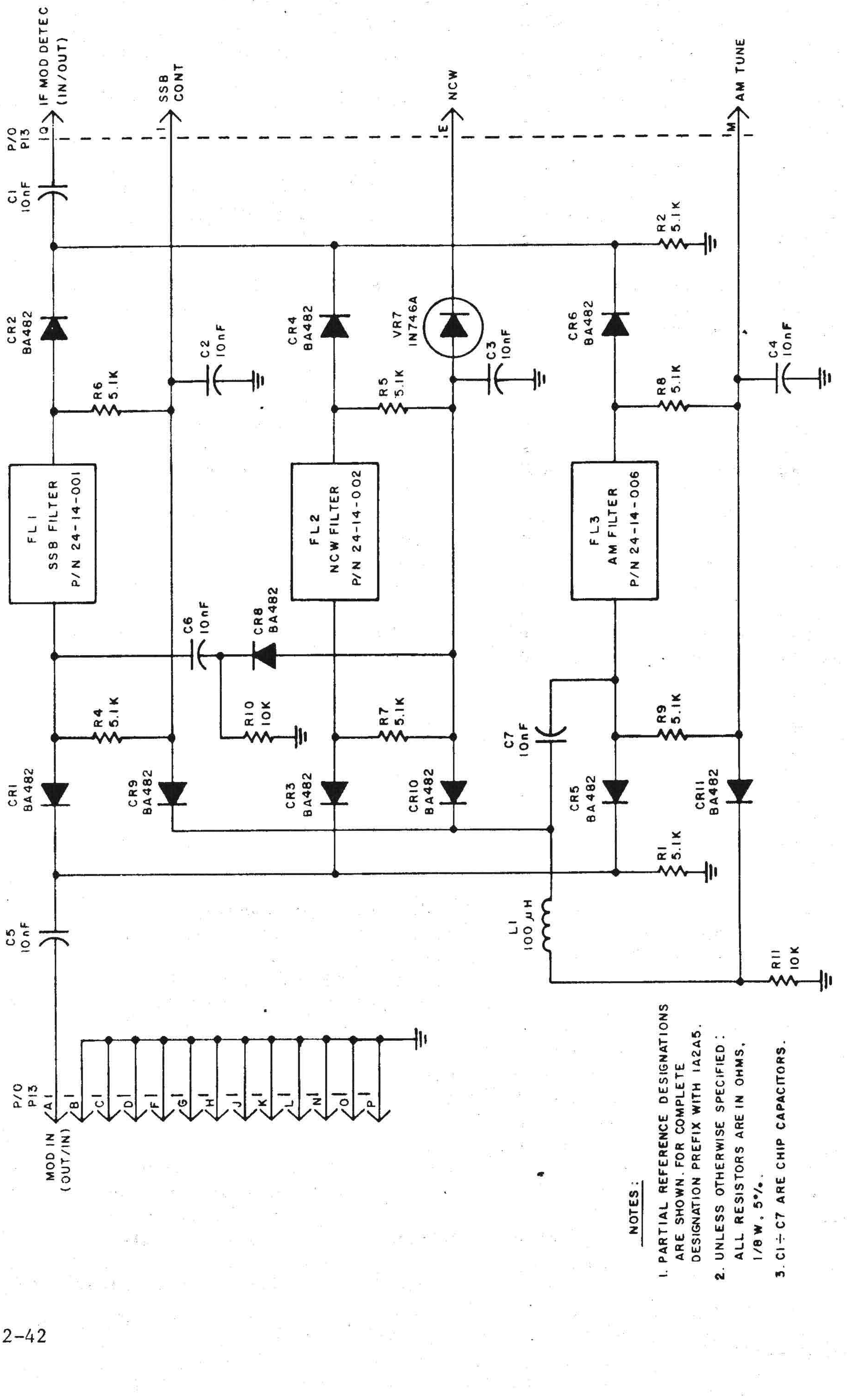


Fig. 2-20. Module FILTER 1A2A5, schematic circuit diagram

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A2A5.
2. UNLESS OTHERWISE SPECIFIED: ALL RESISTORS ARE IN OHMS, 1/8 W, 5%.
3. C1 ÷ C7 ARE CHIP CAPACITORS.

upper sideband of the 5.25-MHz IF signal (+350 to +3300 Hz above the IF frequency). This filter is inserted into the signal path when +12V is applied to pin I (SSB CONT line from module CONT 1A7) via resistor R17 located on the motherboard PCB. This causes DC current to flow through R4, CR1, R1 and through R6, CR2, and R2. The voltage appearing across R1 and R2 reverse-biases the remaining switching diodes, thereby blocking signal transfer through the other filters. Capacitor C2 shunts RF voltages, appearing across R4 and R6, to ground. DC current from pin I also flows through CR9, L1 and R11. The input of the AM filter is effectively shorted to ground through CR9, C7 and C2. This attenuates any RF voltages leaking into the input of the AM filter.

b. The NCW filter FL2 passes a band of 250 Hz, centered on a frequency of 5.25 MHz + 1 kHz. The filter is inserted into the signal path when a high level appears at pin E (NCW line from the function selector, mounted on panel 1A1).
This high level causes DC current to flow through VR7, R7, CR3, and R1, and through R5, CR4, and R2. DC current also flows through CR10, L1, and R11, and through CR8 and R10. Any voltages leaking into the input of the AM and SSB filters are attenuated, since their input is grounded through C7, C6 and C3. During tuning (see para. c below), the AM filter is inserted into the signal path. The signal path through the NCW filter is then blocked since Zener diode VR7 provides a lower voltage at the interconnection of R5, R7, and CR10, causing CR3 and CR4 to cut off.

c. The AM filter FL3 has a passband of ±3 kHz centered on 5.25 MHz. The filter is inserted into the signal path when a high level (generated by module PRE 1A2A4) appears at pin M, the AM TUNE line. The high level causes DC current to flow through R9, CR5, and R1, and R8, CR6, and R2; DC current from pin E also flows through CR11 and R11, thus blocking CR9 and CR10.

d. In the receiving mode, the IF signal arrives at pin A from module MIXER 1A2A1 (see para. 2-10), and the filtered signal appears at pin Q. In the transmitting mode, the signal flow through the filter module is reversed.

2-10. Module MIXER 1A2A1 (fig. 2-21 through 2-24)

Module 1A2A1 contains separate transmit and receive paths. Only one path is active at any time.

a. Block Diagram Analysis (fig. 2-21).

(1) Transmit path. The transmit path is activated by the appearance of +12V on the PTT PRE +12V line. Concomitantly, the supply voltage of the receive path is disconnected by the receive path supply switch, thereby disabling the receive path.

The transmit path receives the modulated and filtered 5.25-MHz signal via the MOD IN line from module FILTER 1A2A5. The input signal passes through an ALC amplifier, whose gain is varied by the ALC voltage arriving from module SNF 1A5A3 such as to maintain a constant peak RF output power. The output signal of the ALC amplifier is mixed with the F2 signal (104.1 MHz for LSB operation, 114.6 MHz for USB and AM operation), and up-converted to a frequency of 109.35 MHz. The F2 signal is received from module USB 1A3A3 and is amplified by an amplifier located in the MIXER 1A2A1 module[the amplified F2 signal is applied to the first transmit mixer via a PIN diode switch.

The 109.35-MHz output signal of the mixer passes through the contacts of relay K2 (energized in the transmit mode) to the 109.35-MHz crystal filter.

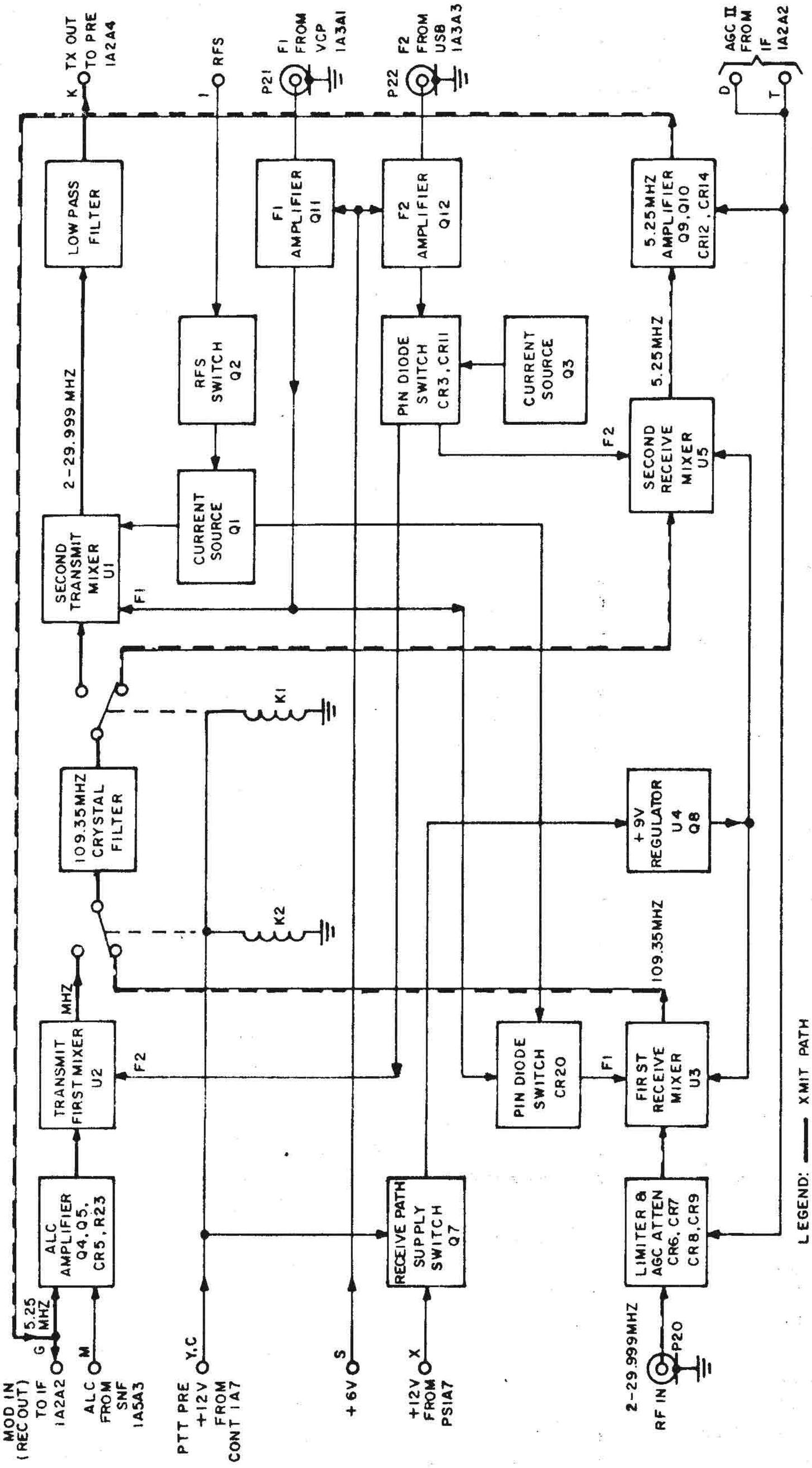


Fig. 2-21. Module MIXER 1A2A1, block diagram

The filtered signal appearing at the filter's output passes through the contacts of relay K1 (also energized in the transmit mode) to the second transmit mixer. In this mixer, the 109.35-MHz signal is mixed with the F1 signal (111.35 to 134.3499 MHz), to convert it to the final RF frequency. The F1 signal is received from module VCP 1A3A1 and is amplified by an amplifier located on the MIXER 1A2A1 module[the amplified signal is applied to the second transmit mixer. The mixer output signal is filtered by a low-pass filter, which allows only the difference frequency - in the 2.0 to 29.9999 MHz range - to pass. The filtered signal is sent through the TX (OUT) line to the RF preamplifier in module PRE 1A2A4.

Each mixer in the transmit path is an active mixer, which receives DC power from the PTT PRE +12V line. The DC operating current is determined by current sources. The current source used with the second transmit mixer can be turned off by a switch, controlled by the RFS line. This permits to interrupt the RF output signal during frequency changes, switching in the matching network, "no-match" condition, and also when the current drawn by the power amplifier in module PA 1A6 becomes excessive.

(2) Receive path. The receive path is activated when the PTT PRE +12V line is grounded. This turns on the receive path switch, and +12V are applied to the +9V regulator which provides power to the two receive mixers. The received RF signal is applied to the first receive mixer via a limiter and an AGC attenuator. The limiter protects the mixer input against excessive signals, and the AGC attenuator, which is controlled by the AGCII voltage provided by module IF 1A2A2, reduces the input signal level when the received signal strength is too high. In the first receive mixer, the received signal is up-converted to a frequency of 109.35 MHz by mixing it with the F1 signal. The mixer output signal passes through the contacts of relay K1 (unenergized in the receive mode) to the 109.35-MHz crystal filter.

The filtered signal passes through the contacts of relay K2 (also unenergized in the receive mode) to the second receive mixer, where it is mixed with the F2 signal. The resulting 5.25-MHz upper sideband IF signal is amplified by a tuned amplifier, whose gain is controlled by the AGCII voltage. The amplified signal is sent to the FILTER 1A2A5 module via the REC OUT line (pin G). The receive path mixers are active mixers, which receive DC power from the +9V regulator. The DC operating current of each mixer is determined by current sources.

(3) F1 and F2 amplifiers. The F1 and F2 amplifiers amplify the respective signals, received from module VCP 1A3A1 and USB 1A3A3. The amplified signals are connected by means of PIN diode switches to the mixers in the operative signal path.

b. Transmit Path Circuit Analysis (fig. 2-22, 2-23).

(1) ALC attenuator. The 5.25-MHz IF signal, arriving at pin G from module FILTER 1A2A5, is attenuated by a voltage-variable attenuator consisting of R23 and PIN diode CR5 and is then applied to the gate of Q5. The attenuation of the IF signal is controlled by the automatic level control (ALC) voltage applied to pin M. This voltage is generated in module SNF 1A5A3 (see para. 2-14) and applied to the PIN diode via resistor R24 and the choke L7. The DC current resulting from the ALC voltage controls the dynamic resistance of CR5, which decreases (thereby increasing the attenuation) when the ALC voltage increases. This action keeps the peak output power of the power amplifier in module PA 1A6 constant.

(2) Amplifier stage. FET Q5 and the resonant circuit comprised of L6, and CV6 operate as a tuned amplifier.

The DC current through Q5 is set by R21 and R22. Capacitor C21 by passes R22 at RF, so that only R21 causes degeneration in the source circuit.
The output of Q5 is buffered by Q4 and then applied to the second transmit mixer. The base bias to Q4 depends on the DC voltage drop across R20, generated by the DC current flowing through Q5. Capacitors C19, C23, and L5 filter the supply line to Q4 and Q5.

(3) First transmit mixer and associated current source. The amplified IF signal appearing at the emitter of Q4 is attenuated by potentiometer RV1 and is then applied, via R17 and C18, to the primary transformer T4. The transformer applies this signal to the gates of the two matched FET transistors contained in U2. The sources of the two FETs receive the F2 "fixed" frequency (104.1 MHz for LSB operation, 114.6 MHz for USB operation) from the collector of Q12, via the forward-biased PIN diode CR3. Diode CR11, used to apply the F2 signal to the receive path mixer, is reverse-biased by the positive voltage appearing at its cathode, and therefore does not allow the F2 signal to reach the receive path mixer. The DC current through both FETs is set by the current source Q3 (the same DC current also flows through the PIN diode switch CR3). The current flowing through Q3 is determined by the base voltage and the value of the emitter resistor. The base voltage is obtained from the +6V supply voltage via the voltage divider comprised of resistors R13 and R14, and the temperature-compensation diode CR4. The resistor emitter, R16, is connected via contacts 2, 3 of relay K2. C16 and C17 are by-pass capacitors. Both FET drains receive power from the PTT PRE +12V line, through the choke L3 and the two halves of T3 primary winding. C10 is a decoupling capacitor. The input transformer, T4, and capacitors C12 and C14 resonate at 5.25 MHz. Resistor R12, bypassed by C13, connects the center-tap of the transformer to ground.

The output transformer T3 is tuned to the 109.35-MHz signal appearing at the mixer output by capacitors C11 and CV2.

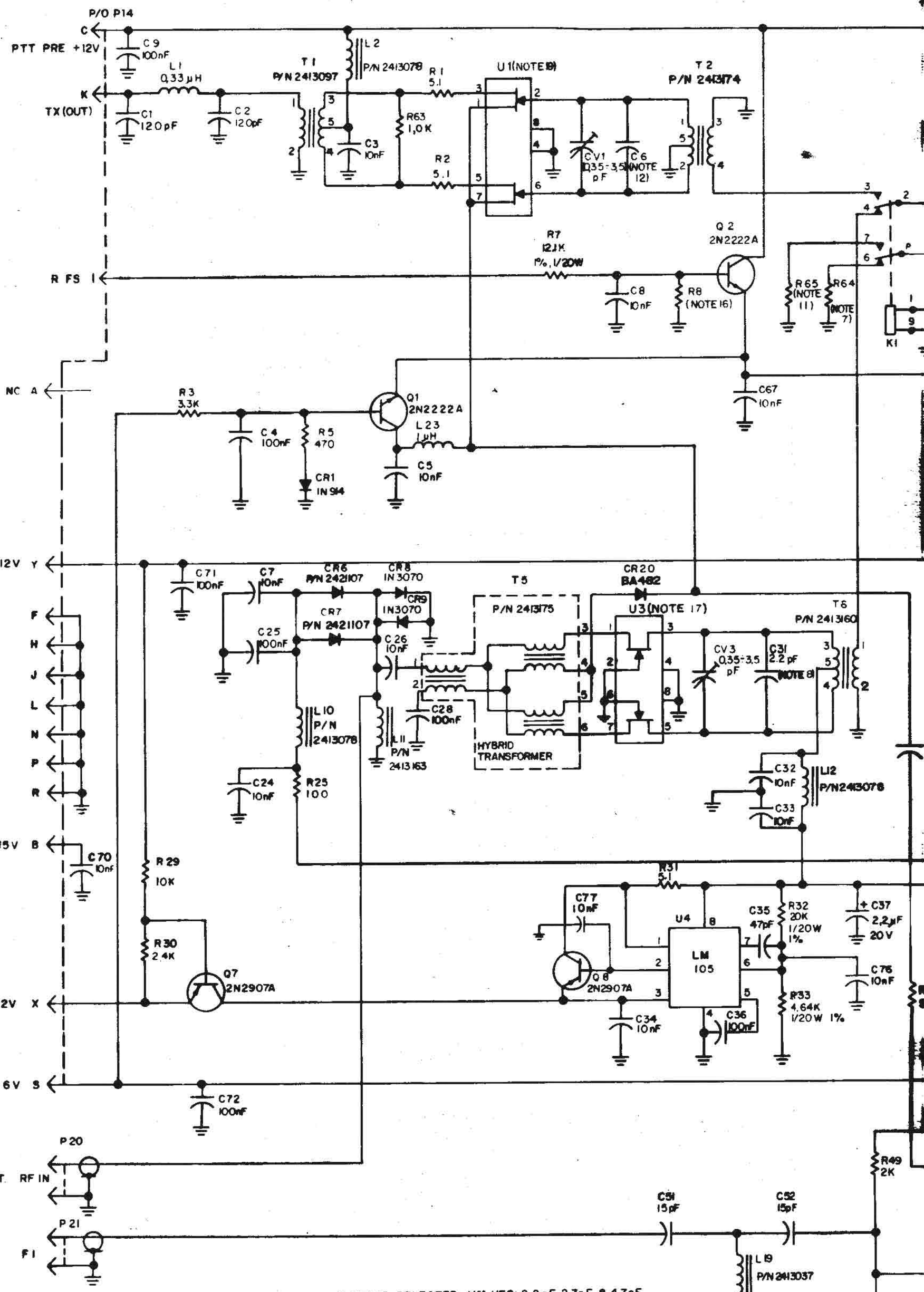
(4) Crystal filter. The 109.35 MHz output signal of the first transmit mixer passes through contacts 7, 8 of relay K2 (energized during transmission), to the crystal filter. The filtered signal passes through contacts 2,3 of relay K1 (also energized during transmission) to the input of the second transmit mixer.

(5) Second transmit mixer and associated current source. This mixer consists of two matched FETs contained in U1. The input signal is applied to the FET gates through the tuned-secondary transformer T2, whose resonance frequency is adjusted to 109.35 MHz by CV1. The F1 variable synthesizer frequency (111.35 to 139.3499 MHz), received from the collector of Q11, is directly applied to the FET sources.

The mixer output signal is coupled through transformer T1 to a low pass filter, comprised of C1, L1 and C2. The filter passes the difference signal, which is at the required operating frequency in the 2 to 29.9999 MHz band. The filtered RF signal passes through pin K (TX OUT line) to the RF preamplifier in module PRE 1A2A4.

The supply voltage for the FETs is obtained from the PTT PRE +12V line via choke L2, the two halves of the primary winding of transformer T1 and equalizing resistors R1 and R2. C3 is a decoupling capacitor.
The DC operating current of the FETs is determined by the current source built around Q1. This current source is similar to that used for the first transmit mixer (see (1) above. Resistor R65 is selected to obtain the proper DC current.

(6) RFS switch. The RFS line (pin I) is normally at a low level, therefore transistor Q2 is reverse-biased and does not affect the operation of Q1.



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATIONS PREFIX WITH 1A2-A1
2. ALL RESISTORS ARE IN OHMS, 5%, 1/8 W UNLESS OTHERWISE SPECIFIED.
3. C3, C5, C8, C 19, C23, C67, C69, C70, C73, C76 AND C77 ARE CHIP CAPACITORS 10nF.
4. C4, C9, C25, C28, C36, C71, C72, C74 AND C75 ARE CHIP CAPACITORS 100nF.
5. R15 IS SELECTED, VALUES 51, 100 AND 150.
6. R44 IS SELECTED, VALUES: 1.5 K, 4.75 K, 3.3 K & 6.25 K.
7. R64 IS SELECTED, VALUES: 75, 100 AND 150.
8. C31 IS SELECTED, VALUES: 2.2 pF, 2.7pF & 4.7pF
9. C38 IS SELECTED, VALUES: 4.7 pF, 6.8 pF AND 10pF.
10. R16 IS SELECTED, VALUES: 22, 33, 68, 398 47Ω.
11. R65 IS SELECTED, VALUES: 33, 39, 51, 68Ω.
12. C6 IS SELECTED, VALUES: 4.7pf, 5.6pF AND 8.2pF.
13. C11 IS SELECTED, VALUES: 2.2 pF, 3.3pF AND 4.7 pF.
14. C29, C30, C55, C57, C58 ARE CHIP CAPACITORS InF.
15. K1 AND K2 ARE RELAY M39016/15-031L.
16. R8 IS SELECTED, VALUES: 8.2, 9.1, 10, 12.1, 15, 1 K.
17. U3 IS U430 SELECTED P N 24-21240 (DN-1954)
18. R38 IS SELECTED, VALUES: 1K, 2K, 3.32K, 4.75K
19. U1, 2, 5 IS 430 P. N. 24-21041 (DN 1949)

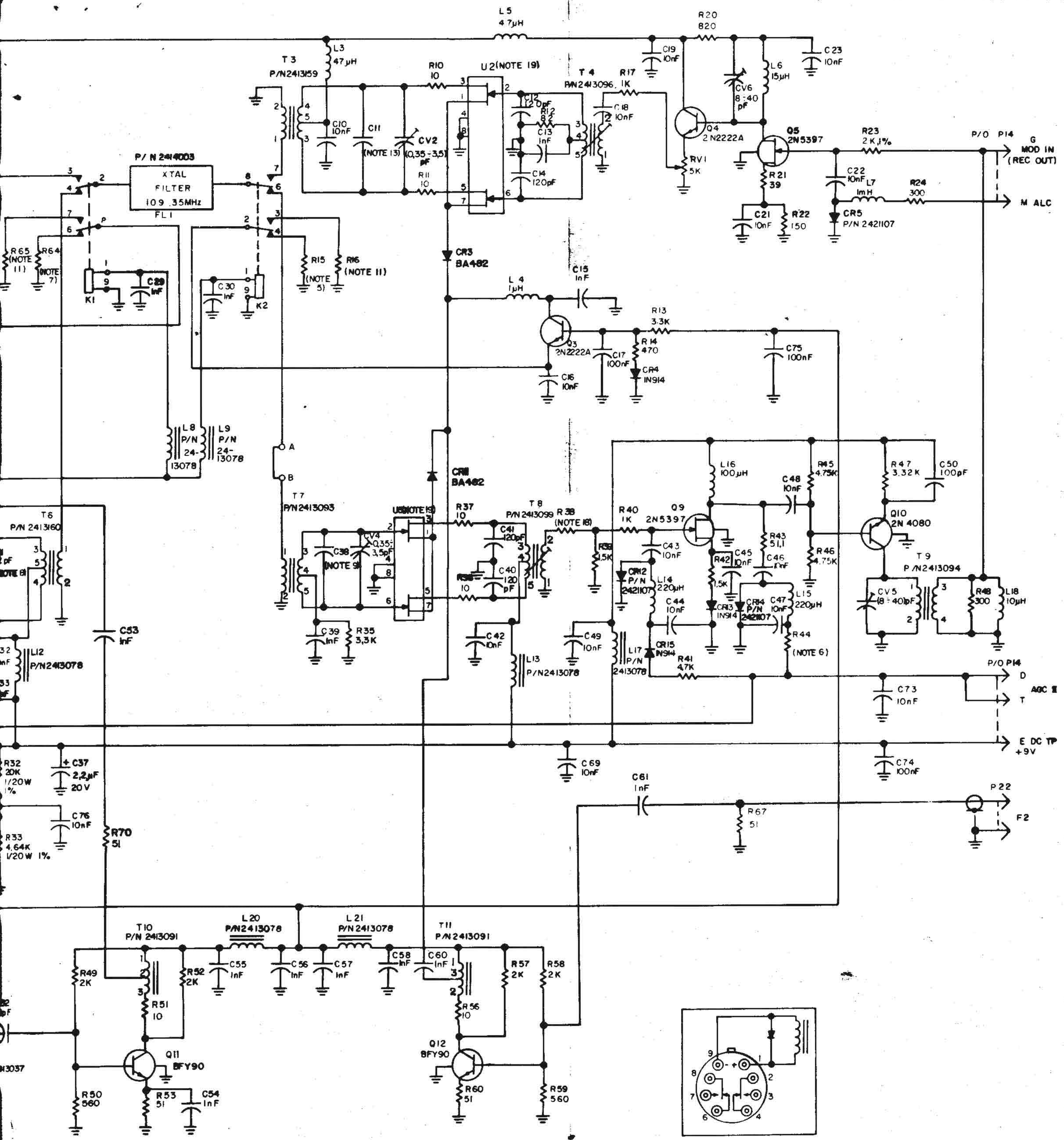
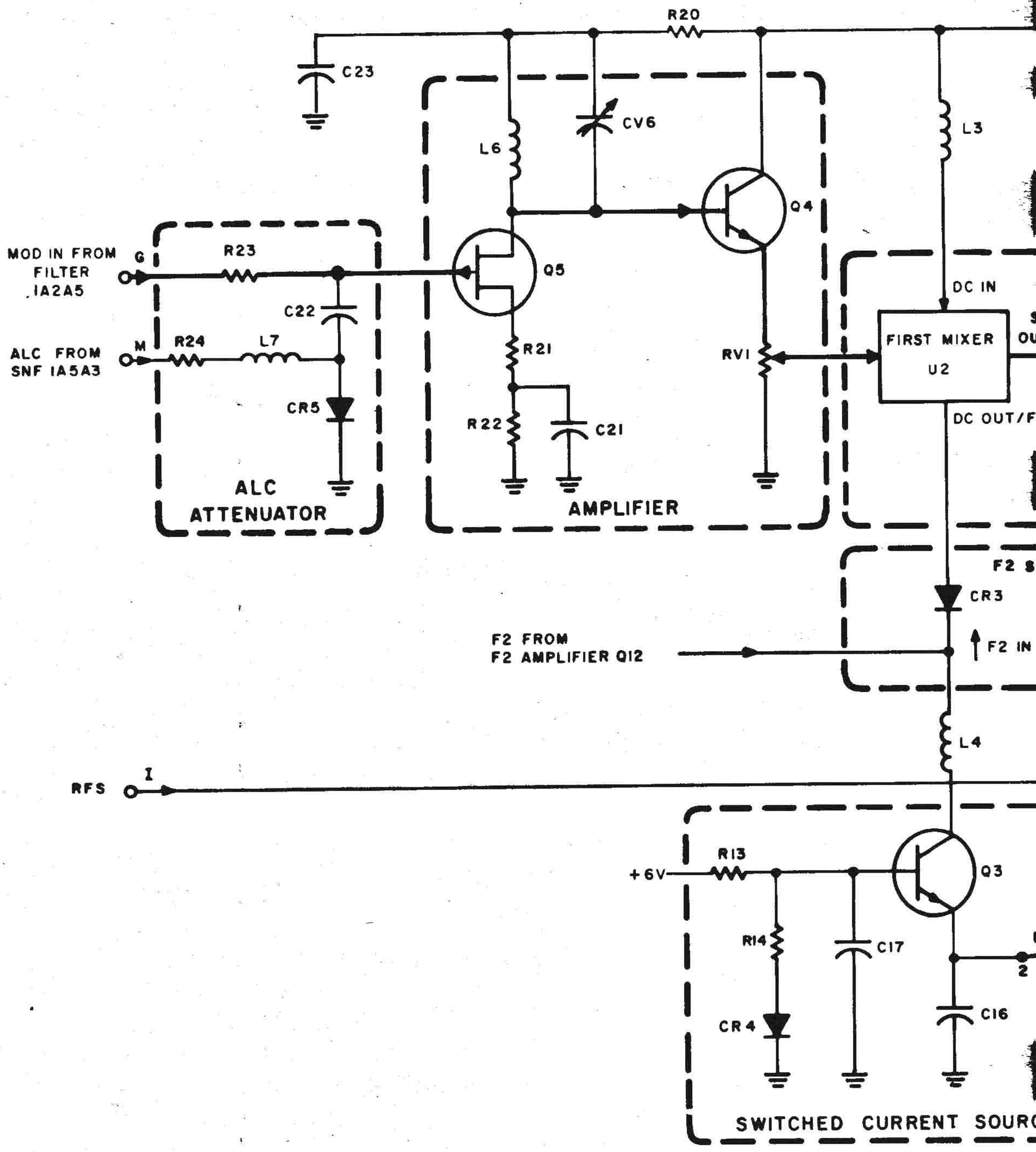


Fig. 2-22. Module MIXER 1A2A1, schematic circuit diagram


R20
C23
CV6
L6
L3
Q4
MOD IN FROM
FILTER
IA2A5
G
R23
Q5
C22
DC IN
FIRST MIXER
U2
ALC FROM
SNF IA5A3
M
R24
L7
R21
RV1
CR5
R22
C21
ALC
ATTENUATOR
AMPLIFIER
CR3
F2 FROM
F2 AMPLIFIER Q12
F2 IN
L4
RFS
I
R13
+6V
Q3
R14
C17
CR4
C16
SWITCHED CURRENT SOURC

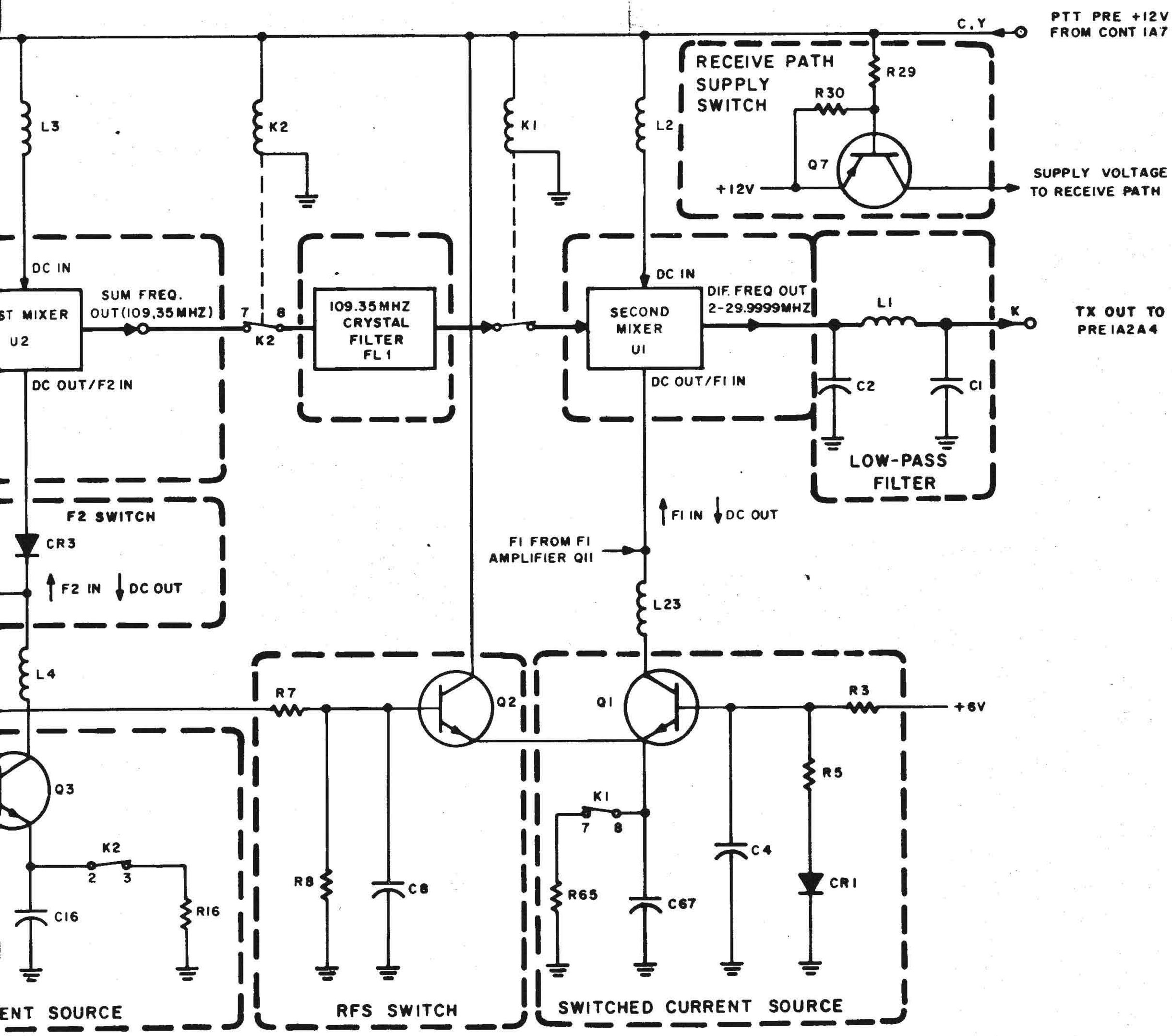
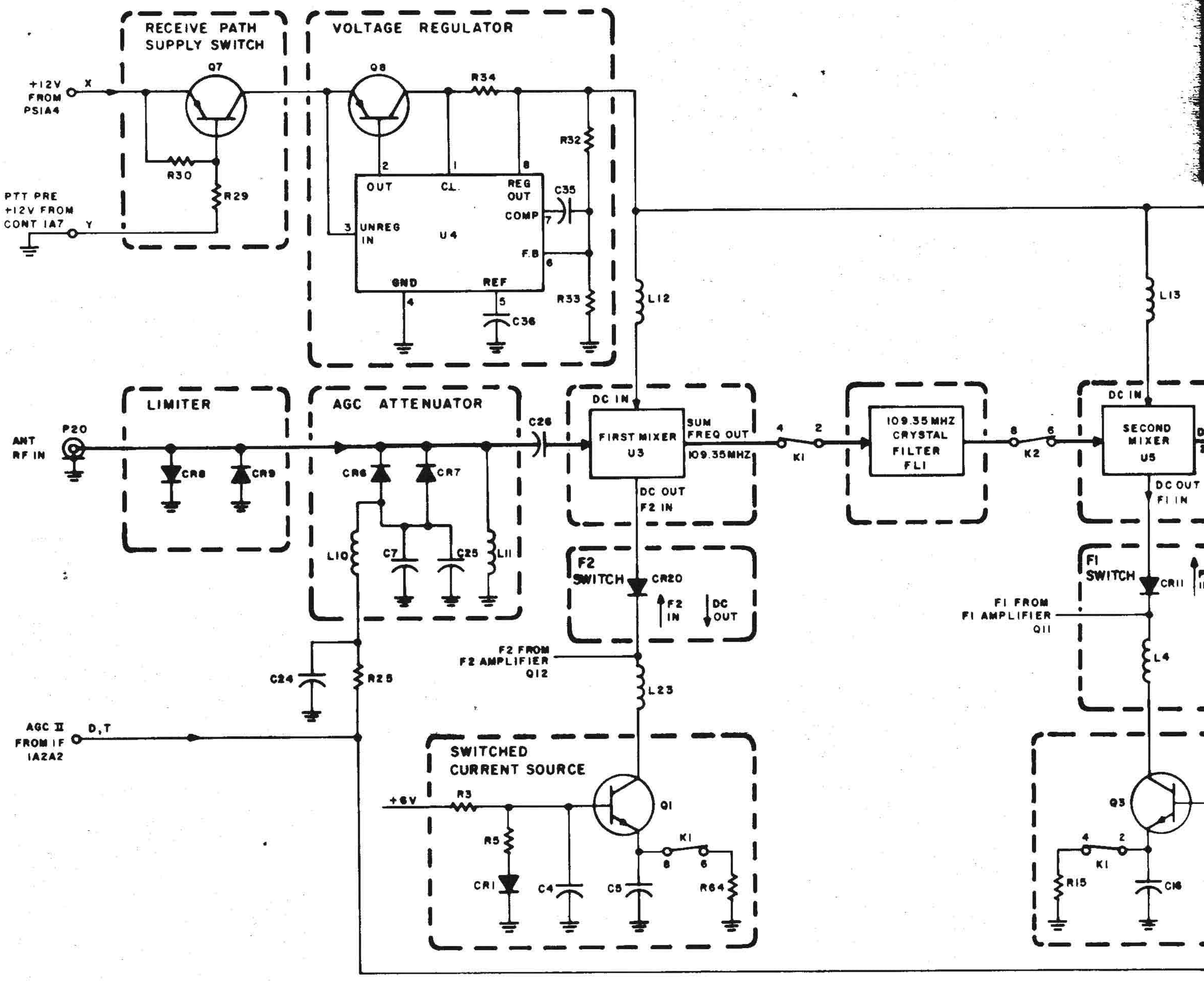


Fig. 2-23. Transmit path, simplified circuit diagram


RECEIVE PATH SUPPLY SWITCH
VOLTAGE REGULATOR
+12V FROM PSIA4
X
Q7
Q8
R34
R32
R30
R29
2
1
8
OUT
CL.
REG OUT
C35
PTT PRE +12V FROM CONT IA7
Y
3
UNREG IN
U4
COMP
7
F.B
6
GND
REF
4
5
C36
R33
L12
L13
LIMITER
AGC ATTENUATOR
DC IN
ANT RF IN
P20
C26
FIRST MIXER U3
SUM FREQ OUT
109.35MHZ
4
2
K1
109.35MHZ CRYSTAL FILTER FL1
8
6
K2
SECOND MIXER U5
DC OUT F2 IN
DC OUT F1 IN
CR8
CR9
CR6
CR7
L10
C7
C25
L11
F2 SWITCH
CR20
F2 IN
DC OUT
F1 SWITCH
CR11
F1 FROM F1 AMPLIFIER Q11
F2 FROM F2 AMPLIFIER Q12
C24
R25
L23
L4
AGC II FROM IF IA2A2
D,T
SWITCHED CURRENT SOURCE
+6V
R3
Q1
Q3
R5
K1
8
6
4
2
CR1
C4
C5
R64
R15
C16

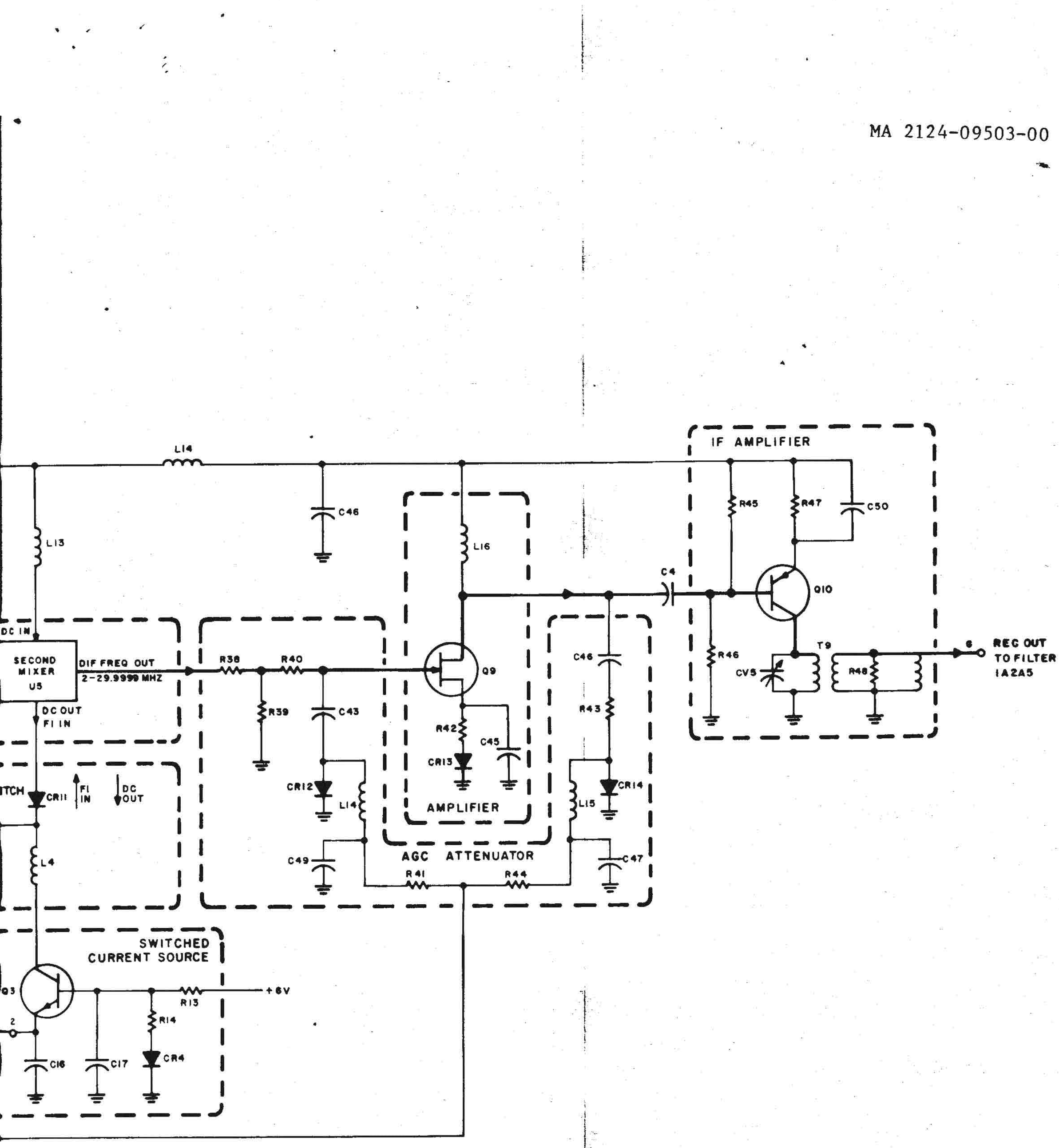


Fig. 2-24. Receive path, simplified circuit diagram

However, when it is necessary to interrupt the RF output signal while remaining in the transmit mode, the RFS line is pulled to approximately +12V by circuits external to module MIXER 1A2A1. When the RFS line voltage is pulled to a voltage above 4.5V (by module PS 1A4 or LORD 1A5A2), transistor Q2 becomes forward-biased and pulls the emitter of Q1 to a voltage higher than the base bias voltage applied through R3. Transistor Q1 becomes reverse-biased and cuts off, thereby causing the mixer FETs to also cut off. The output signal (at pin K) drops to 0. Likewise, the transmitter output power drops to 0.

c. Receive Path Circuit Analysis (fig. 2-22, 2-24).

(1) Receive path supply switch and voltage regulator. The receive path is activated when the PTT PRE +12V line is grounded. This allows bias current for Q7 to flow. Q7 saturates and the +12V voltage at pin X passes to the monolithic voltage regulator U4. This regulator supplies +9V for the operation of the two receive path mixers. The output voltage of U4 is set by the ratio of R32 to R33. Resistor R31 is the sensor resistor for the U4 internal current-limit circuit. Transistor Q8 is a current booster transistor. C35 is a compensation capacitor, and C36 is a filter capacitor for the internal reference voltage source.

(2) Limiter and AGC attenuator. The received signal arriving at the P20 coaxial connector from module SNF 1A5A3 (see para. 2-14) is applied to the input of the first receive mixer through a protection limiter and AGC attenuator. The limiter consists of diodes CR8 and CR9, which conduct and limit the input voltage when it exceeds their conduction threshold. The AGC attenuator consists of PIN diodes CR6 and CR7. These diodes receive the AGCII voltage (pins D, T) supplied by module IF 1A2A2 (see para. 2-9). The AGCII voltage is filtered by R25, C24, L10, C7, and C25. The dynamic resistance of CR6 and CR7 is determined by the current flowing through them as a result of the AGC voltage; it decreases when the AGC voltage increases, diode resistance decreases and the attenuation increases.

(3) First receive mixer and associated current source. The RF signal is applied, through a hybrid transformer, T5, to the sources of the two matched FETs contained in U3. The FETs form an active, wide dynamic rangemixer. The local oscillator signal is the F1 variable frequency, also connected to the FET sources through R70, T5 and PIN diode CR20. The drains of U3 are connected to the tuned transformer T6, whose primary is adjusted by CV3 to resonate at the 109.35-MHz frequency appearing at the output of this mixer.
The DC current through U3 is set by the current source Q1 (see b.(4) above). The selected resistor R64, connected via contacts 8,6 of relay K1, is used to adjust the current value to the requirements of the receive path mixer. A voltage of +9V is applied to the FET drains of U3, via filter C33, L12, C32, and T6.

(4) Crystal filter. The output of the first receive mixer is connected, via contacts 2, 4 of relay K1, to the 109.35-MHz bandpass crystal filter, which selects the difference frequency generated in the mixer. The filtered signal passes through contacts 8,6 of relay K2 to the input of the second mixer.

(5) Second receive mixer and associated current source. The second receive mixer, built around U5, is similar to the first transmit mixer (see b.(2) above) built around U2. Current source Q3 now supplies current to U5 through CR11, while CR3 is reverse-biased. The current supplied by Q3 to the receive path differs from that supplied to the transmit path. The change is made by the contacts of relay K2, which connect a different re-

sistor, R15, to the emitter of Q3.

(6) AGC attenuator and amplifier, and IF amplifier. The 5.25-MHz signal appearing at the output of T8 is applied to the base of FET amplifier Q9 through a fixed voltage divider, R38 and R39, followed by a voltage-controlled attenuator, comprised of R40 and PIN diode CR12. R38 is selected to obtain the required gain from the mixers. The AGC action is achieved by varying the dynamic resistance of PIN diode CR12 by the AGCII voltage. Increasing the AGC voltage increases the attenuation of the signal applied to the gate of FET Q9. The AGCII voltage is converted to a control current by R41. C44 and L14 prevent IF leakage to the AGC line.

The current through Q9 is determined by R42. Diode CR13 stabilizes the current against temperature changes. C45 is an RF bypass capacitor.

The output voltage of Q9, developed across the RF choke L16, is coupled via C48, to the base of the second amplifier, Q10. The equivalent drain load of Q9 is varied by the AGC voltage applied to PIN diode CR14, thus making to gain of Q9 inversely proportional to the AGC voltage magnitude.

The collector load of Q10 is the tuned transformer T9 (adjusted to resonance at 5.25 MHz by CV5) in parallel with R48. R48 determines the output resistance of the mixer and is chosen so that the crystal filters in module FILTER 1A2A5 (see para. 2-9) see the proper termination. L18 resonates with the parasitic capacitance of the connections to the module output (pin G).

d. F1 and F2 Amplifiers.

(1) F1 amplifier. This amplifier is built around Q11. The F1 signal (111.35 to 139.3499 MHz), arriving from module VCP 1A3A1 (para. 2-22) to the coaxial connector P21, is coupled through a high pass filter, consisting of C51, L19, and C52, to the base of Q11. The amplified signal, taken from a tap on transformer T10, passes via R70 and C53 to the operative mixer.

(2) F2 amplifier. This amplifier is built around Q12. The F2 signal arriving from module USB 1A3A3 (114.6 MHz in USB and AM mode, 104.1 MHz in LSB mode), at coaxial connector P22 is amplified by Q12 and connected to the operating mixer through switching diode CR11 or CR3.

(3) The supply voltage for Q11 and Q12 is +6V.

2-11. Module PA 1A6
(fig. 2-25, 2-26)

a. Block Diagram Analysis (fig. 2-25). Power amplifier module PA 1A6 receives the +20 dBm (100 mW) output of the RF preamplifier in module PRE 1A2A4 (para. 2-6.b) and linearly amplifies it to +45 dBm (30 W). There are two amplification stages: a driver stage and a power stage. The driver stage is powered by the primary DC voltage arriving from module PS 1A4 on the +26V (UNFIL) line.

The power stage is powered by the +34V provided by module PS 1A4 in the transmit mode.

Bias to the driver and power stages is derived from the PTT 6V, received from module CONT 1A7 in the transmit mode. The bias voltage for the driver stage is provided by a passive network, whereas the bias for the power stage is provided by an active bias regulator. The module is protected against overheating by a thermoswitch, connected in series with the supply line of the driver stage, which interrupts transmission if the internal temperature endangers the power stage. A fuse, F1, protects the power stage. In addition, the current drawn by the final stage is monitored in module PS 1A4. The RF drive signal provided by module MIXER 1A2A1 (para. 2-10.b.(5)) is interrupted if the current exceeds a

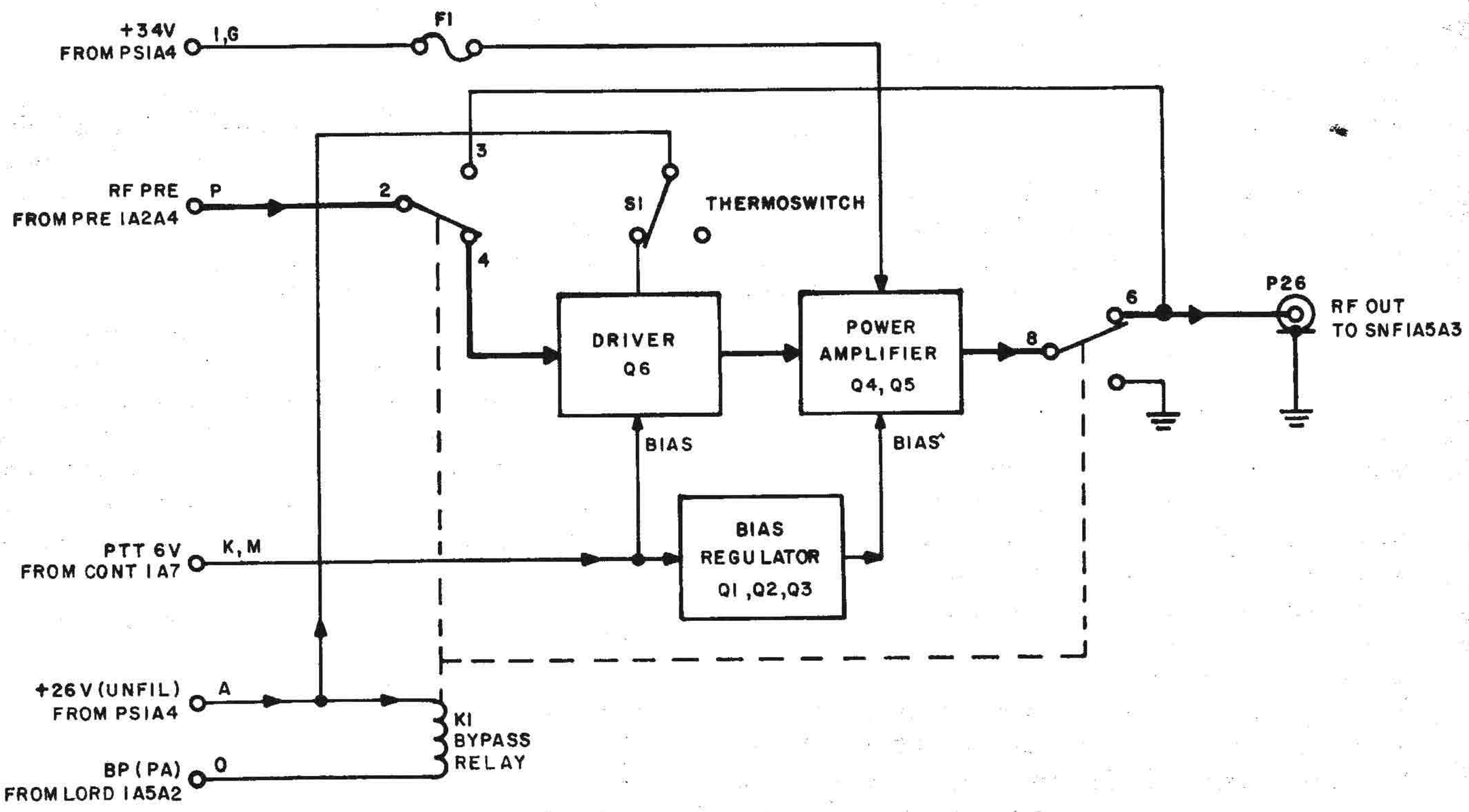


Fig. 2-25. Module PA1A6, block diagram

preestablished threshold (refer to para. 2-16).
A relay allows to bypass the RF amplification stages; this relay is controlled by the BP (PA) line. Then, the +20-dBm output of the RF preamplifier appears at the RF OUT connector.

b. Circuit Analysis (fig. 2-26).

(1) Driver stage. The RF signal, arriving from module PRE 1A2A4 at pin P, is connected, through the normally-closed contacts (2 and 4) of relay K1 (unenergized), to the input of the driver stage. The driver stage is built around the vertical MOS (VMOS) FET power transistor Q6. The RF input signal is applied to the gate of Q6 via an attenuator comprised of R1 and R2, a frequency compensation network comprised of R3, C1, R4 and L1, and DC-blocking capacitors C2 and C3. The gate bias voltage is applied through a voltage divider comprised of resistor R5 and potentiometer R6. L2, L3, C4 and C5 form a decoupling network.

Q6 operates in a common-source configuration. The RF output signal develops across L5 and is coupled through a matching network, comprised of C9, R15, C17, L6 and T1, to the bases of the power stage transistors, Q4 and Q5. C10 and C11 are DC blocking capacitors. Negative feedback is applied from the drain of Q6 to its gate, through R7, C6 and L4, to obtain con-stant gain and good linearity over the full operating frequency range. The +26V supply line for Q6 passes through the normally closed contacts of the thermostat switch and is filtered by C8 and C7.

The supply voltage for the driver stage is nominally +26V; this voltage is the unregulated radio set supply voltage, which may vary from 22 to 32 V. The thermoswitch S1 disconnects this voltage when the internal tempera-

ture in the module exceeds 110°.

(2) Power stage and associated bias regulator. The power stage is a Class AB push-pull amplifier consist- ing of Q4 and Q5. The RF drive for Q4 and Q5 is applied from the driver, Q6, through transformer T1, directly to their bases. The RF output signal is coupled through transformer T2 and the normally-closed contacts (8,6) of the bypass relay, K1 (unenergized) to the RF OUT connector. The bias regulator for the power stage consists of Q1, Q2 and Q3, and its function is to provide a temperature-varying output voltage which tracks the changes in the base-emitter voltages of Q4 and Q5 - thus ensuring a stable DC quiescent current. The bias current is supplied by the Darlington pair, Q1 and Q3, which receive bias current through R8. Negative feedback from the emitter of Q1 to the base of Q2 ensures a very low output resistance, and stabilizes the bias voltage to a value which depends mainly on the ratio of R8 and R9.
The bias current is filtered by C15, C16, C18, L7, L8. The bias regulator receives +6V from the PTT +6V line (from module CONT 1A7 - see para. 2-26). This voltage is only present when transmitting.
The supply voltage for the power stage is +34V; this is a regulated voltage, generated by the power supply module PS 1A4 (see para. 2-16) when the radio set is keyed. The supply line is filtered by C25, C26 and C29. Fuse F1 protects the power supply in case of transistor failure.

(3) Bypass mode.. The RF output power is connected through the normally closed contacts of relay K1 to the coaxial output connector. Relay K1 may be energized by the BP (PA) command applied at the REMOTE connector. In this case, the +20-dBm RF output of module PRE 1A2A4 is directly connected to the output connector. Usually, the power amplifier is bypassed when RT-936/PRC-174 serves as the exciter for an external power amplifier.

2-12. Automatic Matching System Operation (fig. 2-27)

The matching of various types of antennas is performed by a matching network (module MN 1A5A1) digitally controlled by the specialized tuning processor contained in module LORD 1A5A2 (see para. 2-15). This processor receives the frequency and antenna type information from the panel 1A1 and the whip sensor and load-character information from sensors in module SNF 1A5A3 (refer to para. 2-14), and varies the values of the matching network components according to a fixed algorithm.

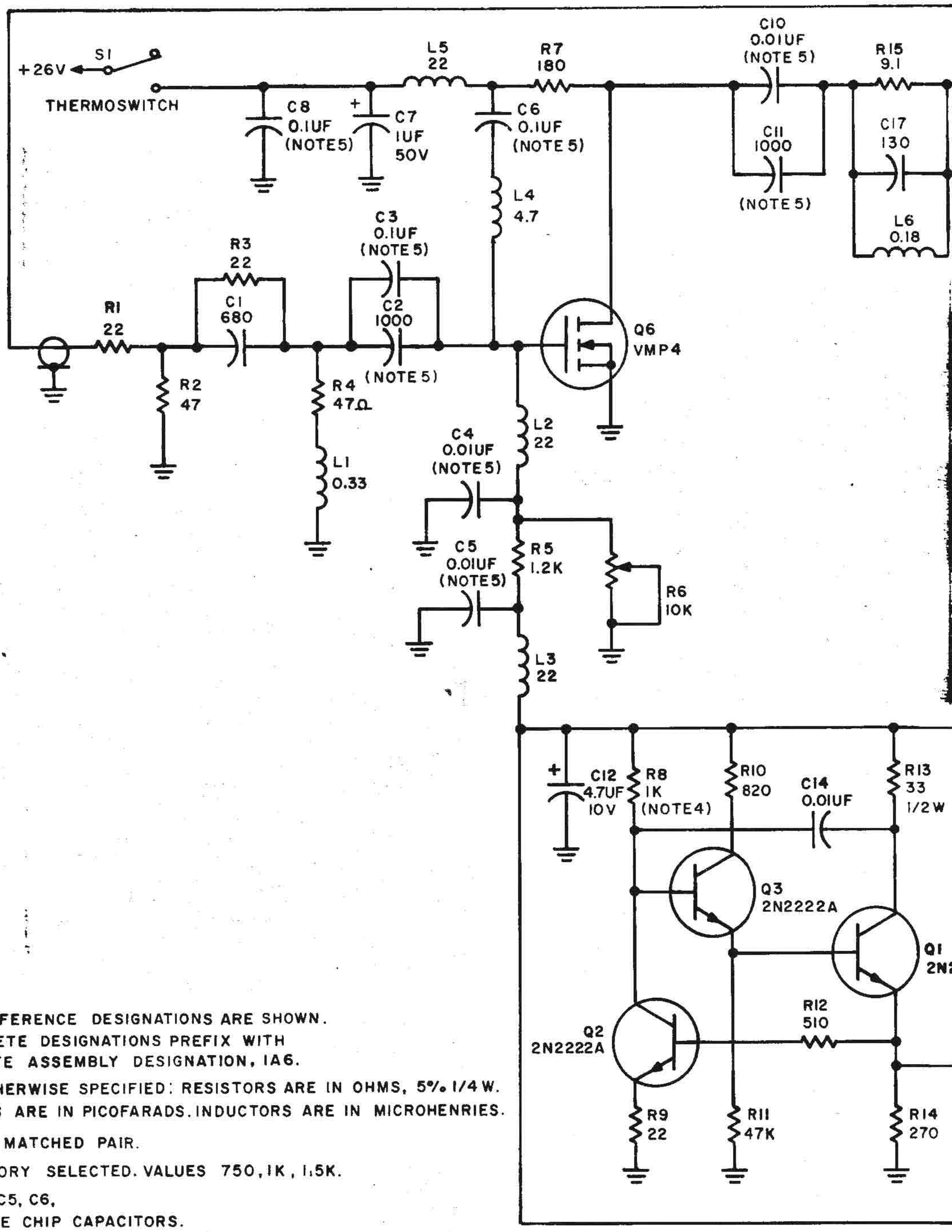
a. Initiation of the Matching Cycle. This is done by pressing the PTT after frequency change or equipment turn-on. The typical tuning time will be less than 1.5 seconds.

b. Termination of First Matching Cycle. This will happen when the load presented to the power amplifier results in a better than 1.5:1 voltage standing-wave ratio (VSWR).

c. Initiation of Second Matching Cycle. Asecond matching cycle will be automatically`carried out if the first attempt (para. b) fails.

d. Termination of Second Matching Cycle. The same as para. b above. The total maximum tuning time (if second cycle is successfully completed) is 5 seconds.
In case of failure, transmission is inhibited and a "no-matching" indication is provided on the solid state display and in the earphone (see para. 2-26).

e. Adaptation to Changing Antenna Impedance. With every PTT action (after matching is first achieved) the load presented to the power amplifier is evaluated; if the VSWR is higher than 3.0:1, retuning will be carried out. This typically lasts 0.2 seconds. The retuning will end when a VSWR better than 1.5:1 is attained.



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH APPROPRIATE ASSEMBLY DESIGNATION, 1A6.
2. UNLESS OTHERWISE SPECIFIED: RESISTORS ARE IN OHMS, 5%, 1/4 W. CAPACITORS ARE IN PICOFARADS. INDUCTORS ARE IN MICROHENRIES.
3. Q4, Q5 ARE MATCHED PAIR.
4. R8 IS FACTORY SELECTED. VALUES 750, 1K, 1.5K.
5. C2, C3, C4, C5, C6, C26, C27 ARE CHIP CAPACITORS.

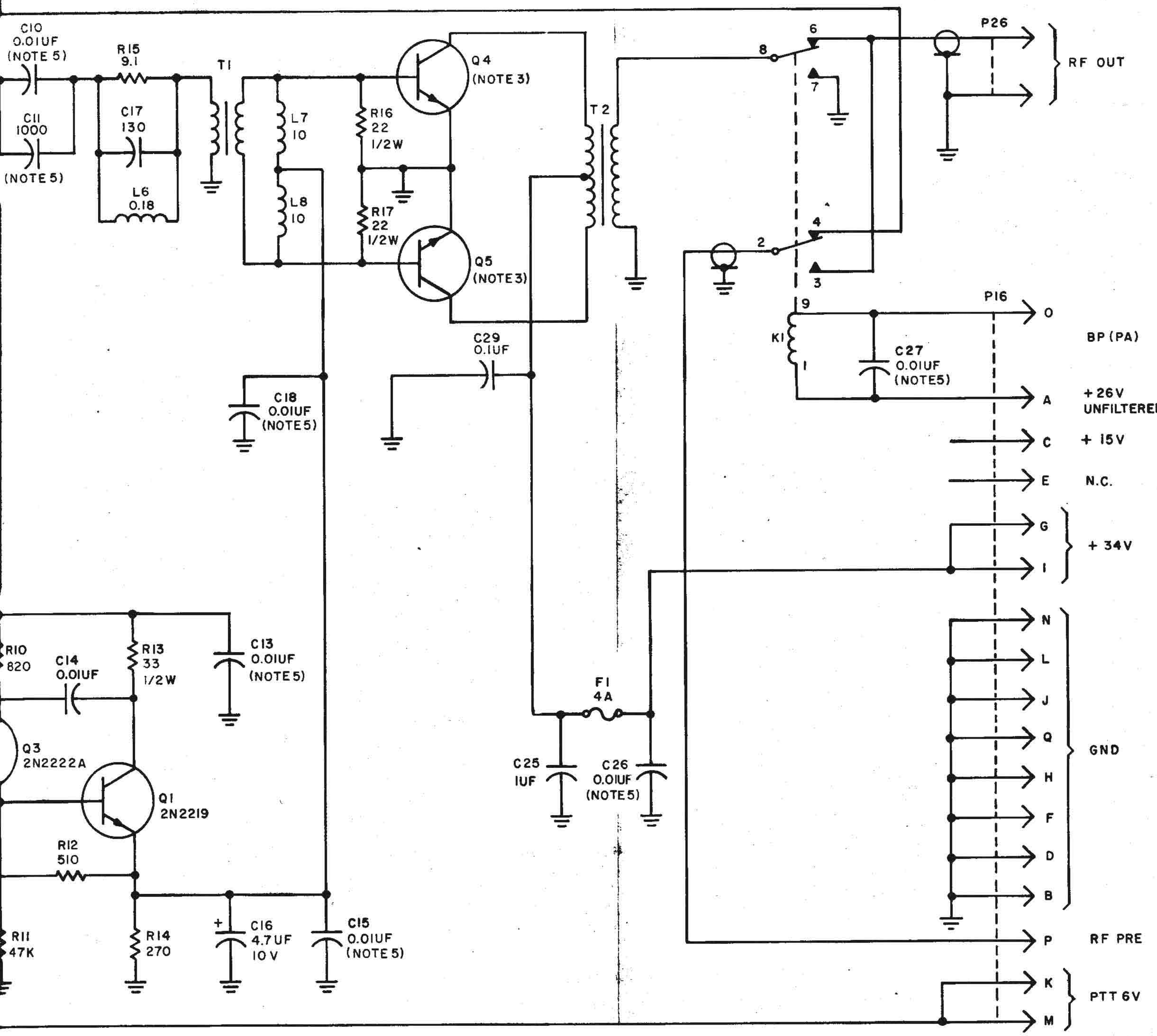


Fig. 2-26. Module PA1A6, schematic circuit diagram

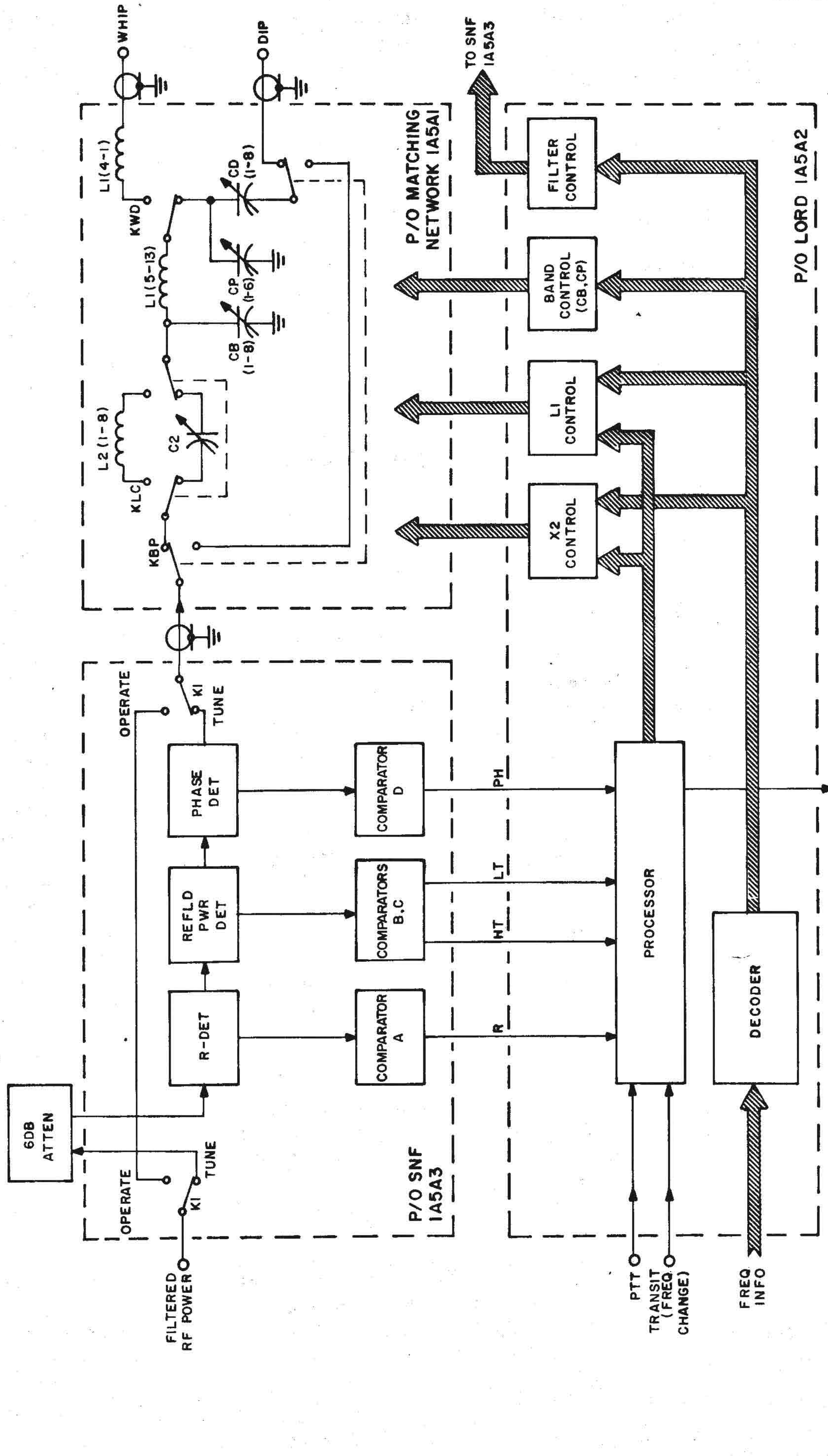


Fig. 2-27. Automatic matching system, block diagram

f. Matching Algorithm. See para 2-15 for a detailed description of the matching algorithm.

2-13. Module MN 1A5A1 (fig. 2-27, 2-28)

The matching network module contains the components of the T-network used for antenna matching, and the relays which control their values. The relay drivers are contained in module LORD 1A5A2 (see para. 2-15).

a. Reactance X2. This reactance is composed of coils L2-1 to L2-8 or capacitors C2-1 to C2-8. Relay KLC selects the type of component and the contacts of relays K2-1 to K2-8 short-circuit those component elements which are not required for tuning. The element values are binary weighted· the elements with the lowest value carry the number 8. Only 5 elements are actually used in any given frequency range.

b. Capacitor CB. This component is composed of eight capacitors (CB1 to CB8), inserted or disconnected by relays KB1 to KB8. The value of CB is selected according to the operating frequency band.

c. Inductance L1. L1 is composed of 13 coils; only eight are used in any given frequency range. Contacts of relays K1-13 to K1-1 short-circuit those coils which are not required for tuning (except for L1-3 through L1-6 which are disconnected when not used). The WHIP connector is connected directly to coil L1-1.

d. The DIPOLE connector is connected through the contacts of relay KBP to capacitors CD1 to CD8 and CP1 to CP6. Those components not required for dipole matching are neutralized by the second set of contacts of relays KB1 to KB8. These contacts short-circuit CD capacitors and disconnect CP capacitors. The output of the capacitor chain is connected to L1-5 by contacts of relay KWD, or to L1-7 by relays KB-8 and KWD. In the 21 to 30 MHz range, CD8 is connected between L1-6 and L1-7.

e. Relays K2-x, K1-x (except K1-1 and K1-2), KLC, KBP and KWD are latching relays. Such relays do not require continuous application of current to maintain the selected position.

f. When RT-936/PRC-174 is used as an exciter for a high-power amplifier or when testing, the output of the power amplifier in module PA 1A6 may be directly connected to the DIPOLE connector, by the contacts of relay KBP (this is called the BYPASS mode).

2-14. Module SNF 1A5A3 (fig. 2-27, 2-29, 2-30)

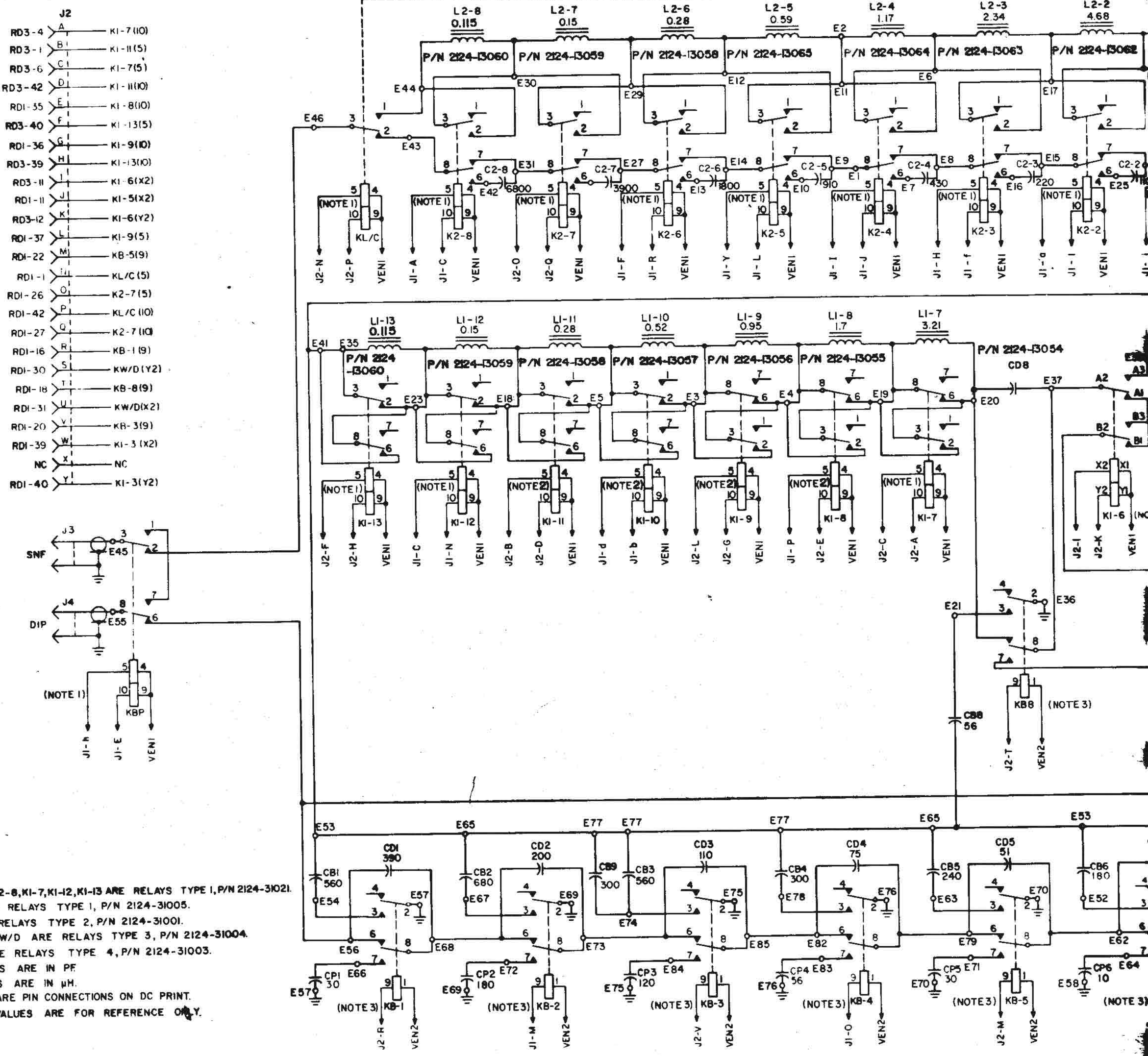
a. Block Diagram Analysis (fig. 2-27, 2-29). Module SNF 1A5A3 contains the receive-transmit relay, tune-operate relay, bandpass filters, load sensors, and TX LEVEL and ALC detectors.

In the tuning mode, the transmit signal arriving from module PA 1A6 passes through the contacts of the transmit/receive relay (energized in this mode) and through the selected bandpass filter to the TX LEVEL and ALC forward power detectors.

From these detectors, the transmit signal passes through the contacts of the tune/operate relay (energized in this mode) to the 6-dB attenuator located on the chassis, and then to the load sensors:

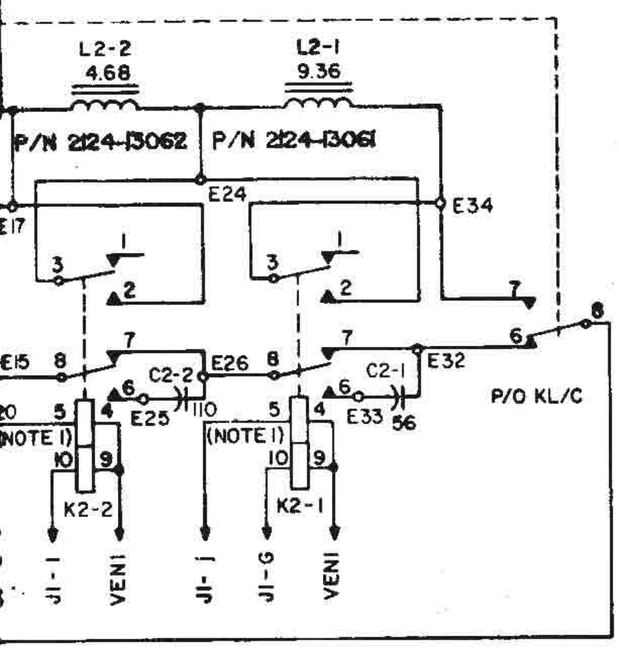
(1) Load resistance detector (R-DET). This detector provides an output signal depending only on the resistive component magnitude. Comparator A transforms this output to either a low or a high level, according to the load resistance (smaller or greater than 50 ohms, respectively).

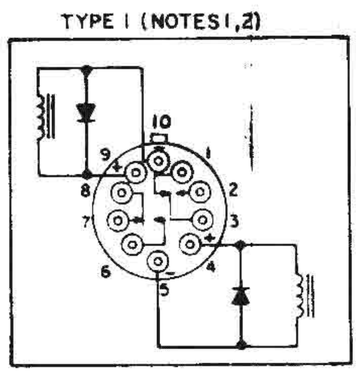
(2) Reflected power detector. This detector produces an output voltage proportional to the power reflec-



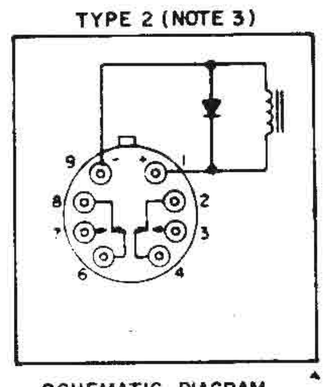
NOTES:

1. KBP, KLC, K2-1 ÷ K2-8, KI-7, KI-12, KI-13 ARE RELAYS TYPE 1, P/N 2124-31021.
2. KI-8 ÷ KI-11 ARE RELAYS TYPE 1, P/N 2124-31005.
3. KB1 ÷ KB8 ARE RELAYS TYPE 2, P/N 2124-31001.
4. KI-3 ÷ KI-6 & KW/D ARE RELAYS TYPE 3, P/N 2124-31004.
5. KI-1 & KI-2 ARE RELAYS TYPE 4, P/N 2124-31003.
6. ALL CAPACITORS ARE IN PF.
7. ALL INDUCTORS ARE IN μH.
8. E91, E92 & E93 ARE PIN CONNECTIONS ON DC PRINT.
9. INDUCTANCES VALUES ARE FOR REFERENCE ONLY.

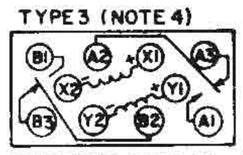




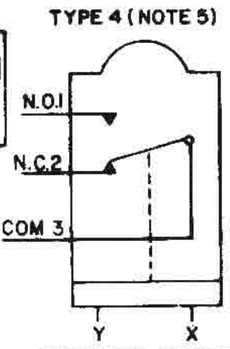
SCHEMATIC DIAGRAM
(PINS 4,5 LAST
ENERGIZED BOTTOM VIEW)



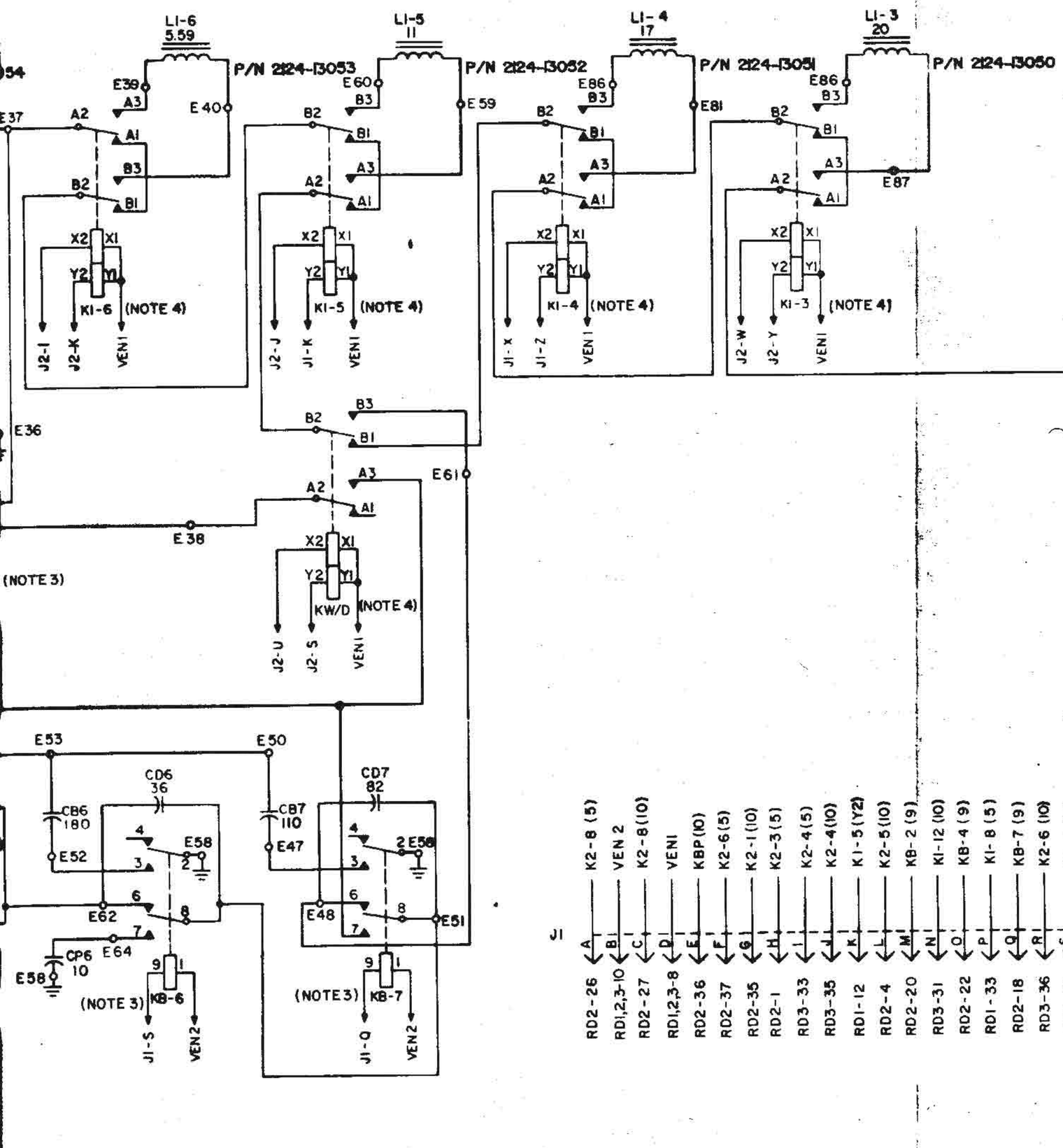
SCHEMATIC DIAGRAM
(UNENENERGIZED POSITION-
BOTTOM VIEW)



SCHEMATIC DIAGRAM
(Y1 AND Y2 LAST
ENERGIZED-BOTTOM
VIEW)



SCHEMATIC DIAGRAM
(UNENERGIZED POSITION-
SIDE - VIEW)



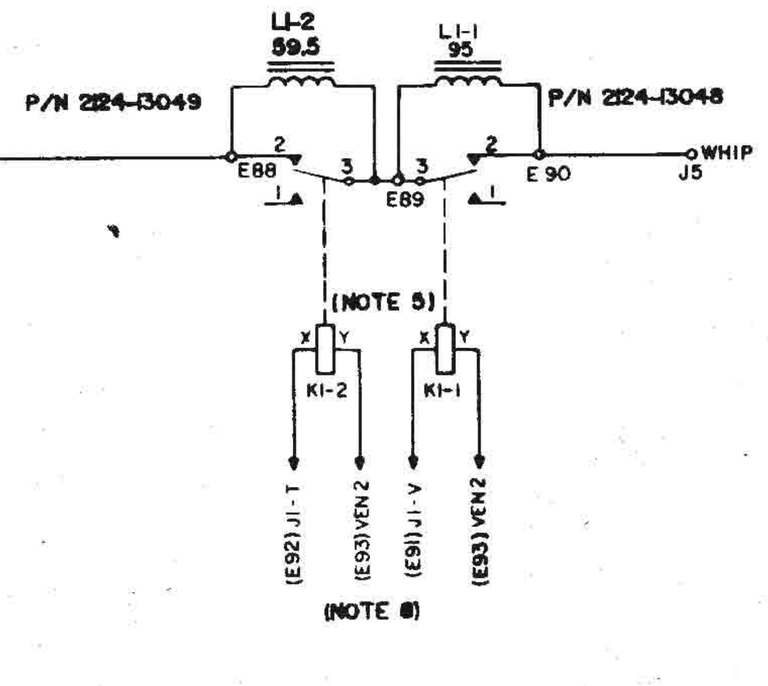
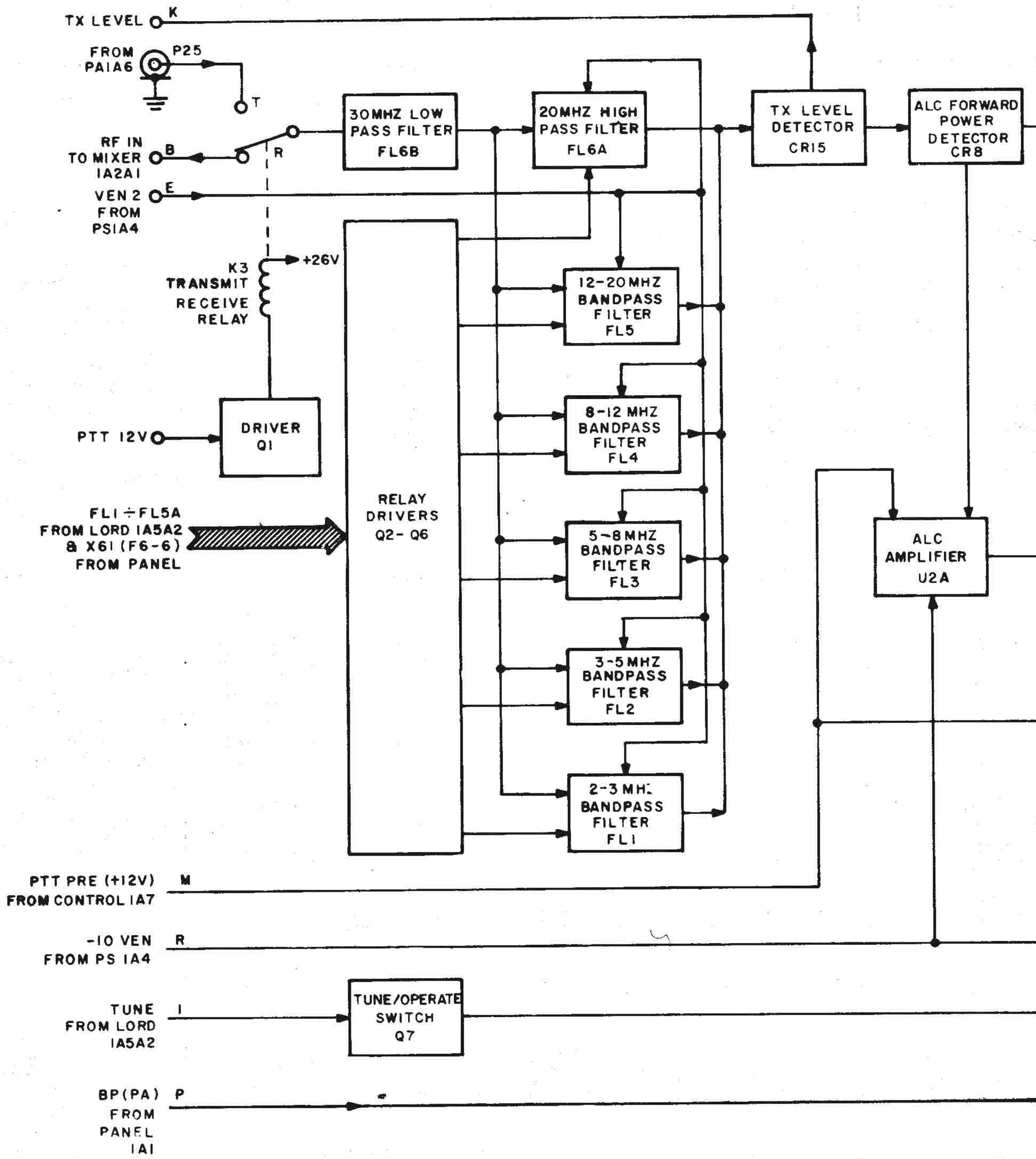


Fig. 2-28. Module MN 1A5A1, schematic circuit diagram


TX LEVEL
K
FROM PA1A6
P25
T
RF IN TO MIXER 1A2A1
B
R
VEN 2 FROM PS1A4
E
K3 TRANSMIT RECEIVE RELAY
+26V
PTT 12V
DRIVER Q1
FL1 ÷ FL5A FROM LORD 1A5A2 & X61 (F6-6) FROM PANEL
RELAY DRIVERS Q2- Q6
30MHZ LOW PASS FILTER FL6B
20MHZ HIGH PASS FILTER FL6A
12-20MHZ BANDPASS FILTER FL5
8-12 MHZ BANDPASS FILTER FL4
5-8MHZ BANDPASS FILTER FL3
3-5MHZ BANDPASS FILTER FL2
2-3 MHZ BANDPASS FILTER FL1
TX LEVEL DETECTOR CR15
ALC FORWARD POWER DETECTOR CR8
ALC AMPLIFIER U2A
PTT PRE (+12V) FROM CONTROL 1A7
M
-10 VEN FROM PS 1A4
R
TUNE FROM LORD 1A5A2
I
TUNE/OPERATE SWITCH Q7
BP(PA) FROM PANEL 1A1
P

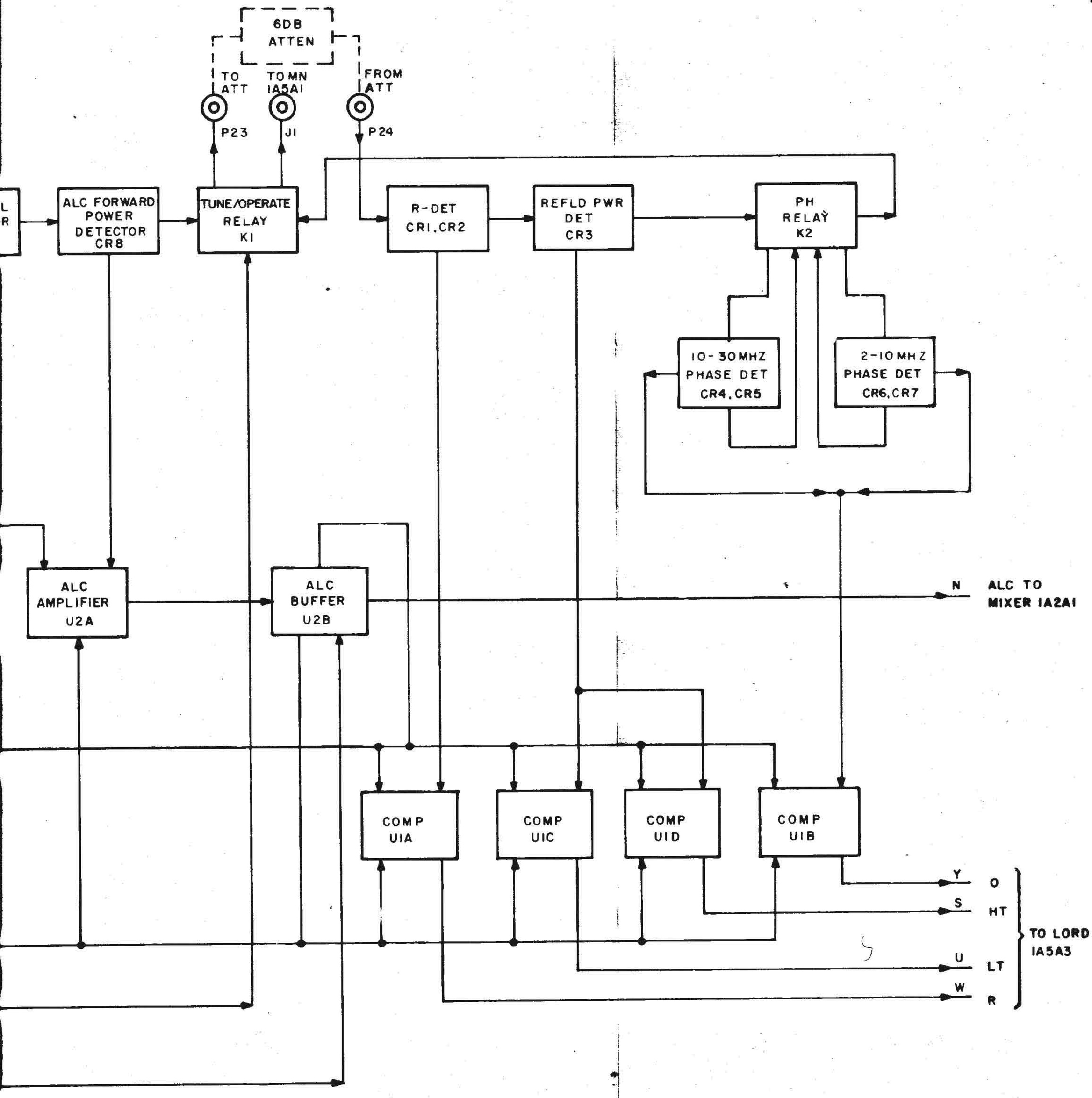
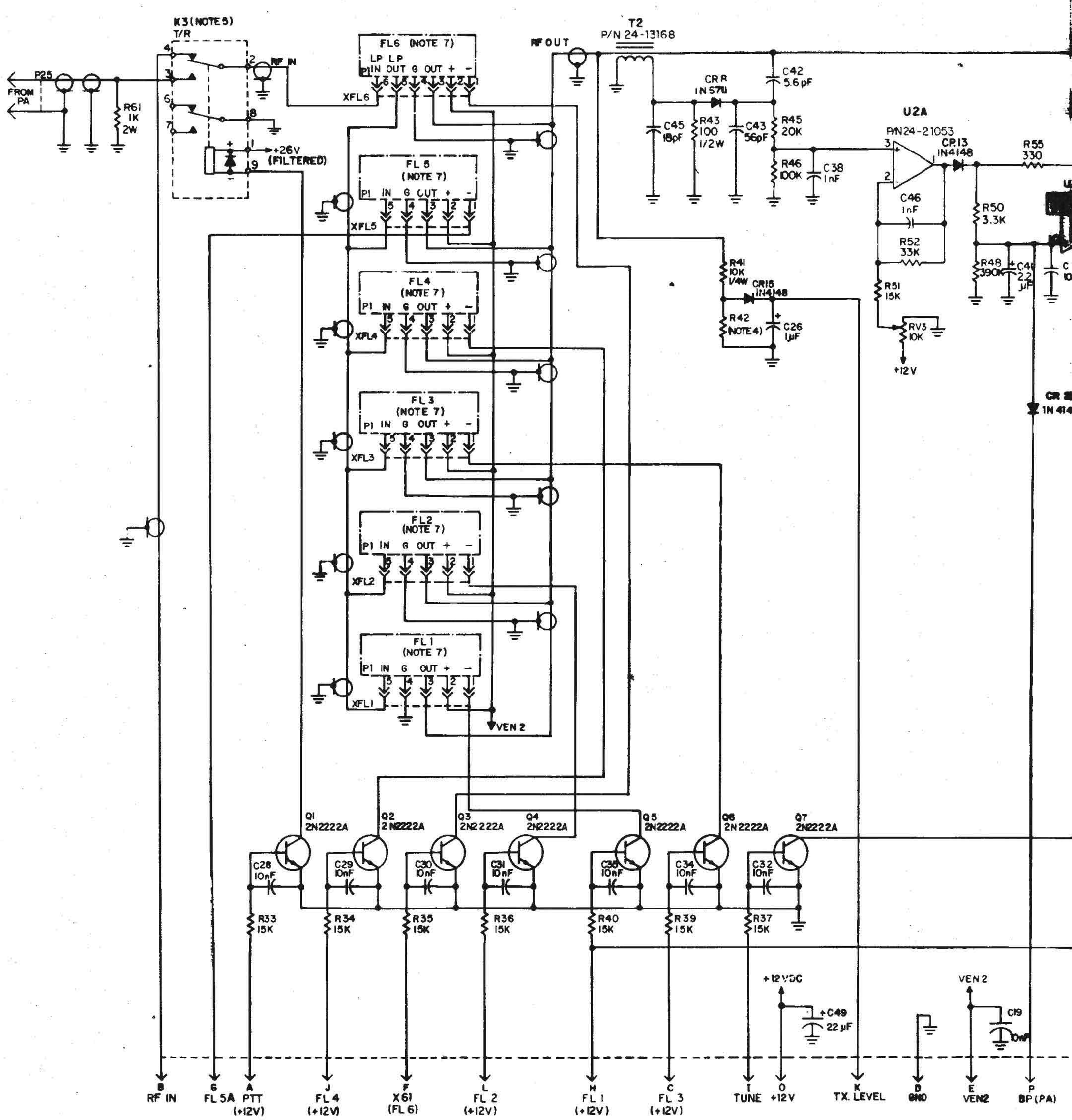
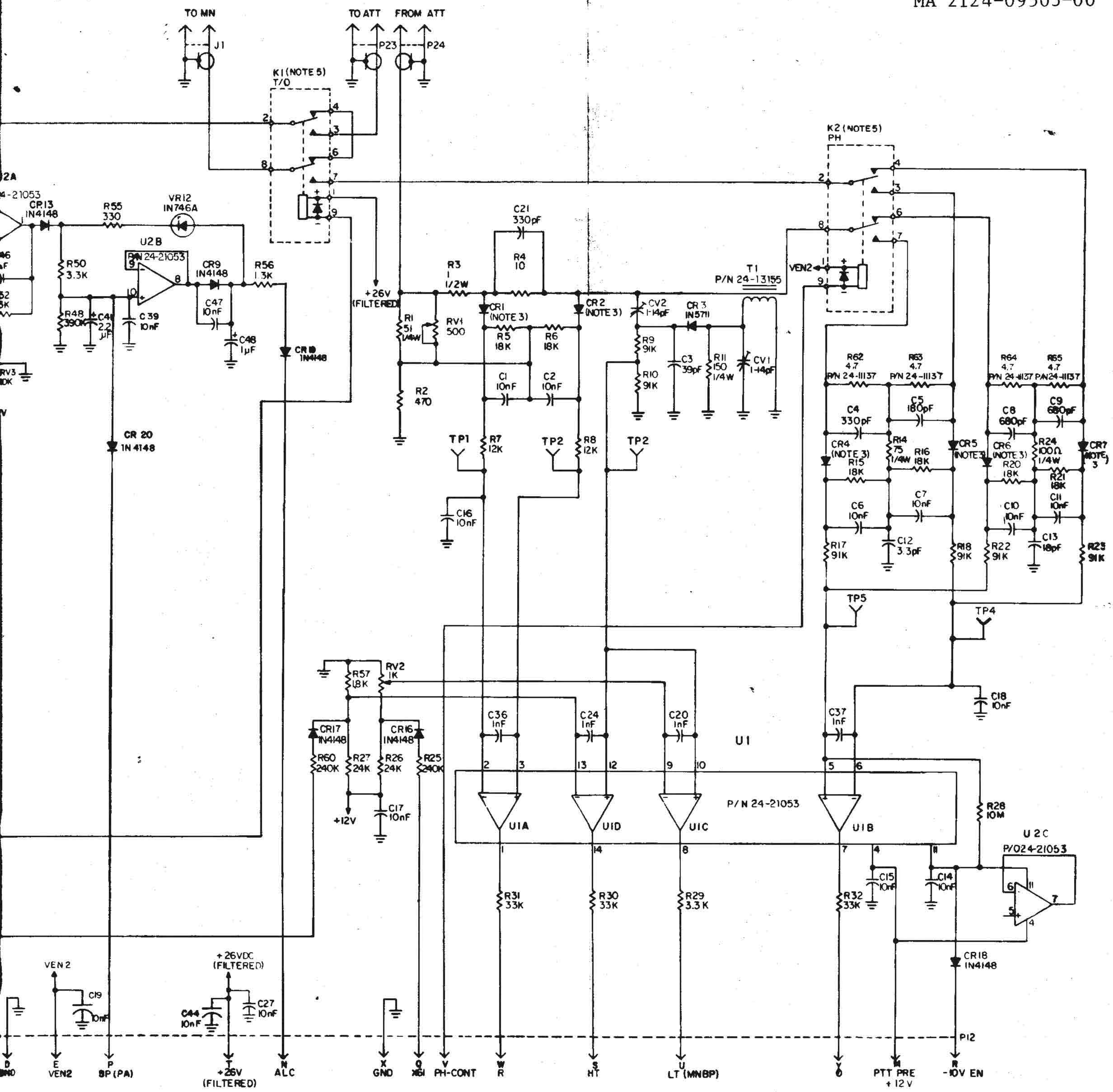


Fig. 2-29. Module SNF 1A5A3, block diagram

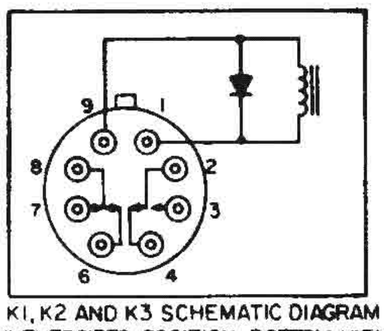


NOTES:

1. PARTIAL REFERENS DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH 1A5A3.
2. ALL RESISTORS ARE IN OHMS, 1/8 W, 5% UNLESS OTHERWISE SPECIFIED.
3. CR1 & CR2, CR4 & CR5, CR6 & CR7 ARE MATCHED PAIRS P/N 24-21091.
4. R42 IS SELECTED VALUES 2.21KΩ & 2.43KΩ & 2.67KΩ, 1/20W, 1 %.
5. K1, K2 AND K3 ARE RELAYS M39016/15-033L P/N 24-31001.
6. CAPACITORS C14, C15, C17÷C19, C20, C24, C27÷C32, C34÷39, C44÷C46, C47 ARE CHIP CAPACITORS.
7. FOR SCHEMATIC DIAGRAM SEE DWG: FL-1 - 24-91540-58, FL-2 - 24-91550-58, FL-3 - 24-91560-58, FL-4 - 24-91570-58, FL-5 - 24-91580-58, FL-6 - 24-91590-58
8. PARTIAL PART NO. ARE SHOWN, FOR COMPLETE P/N PREFI

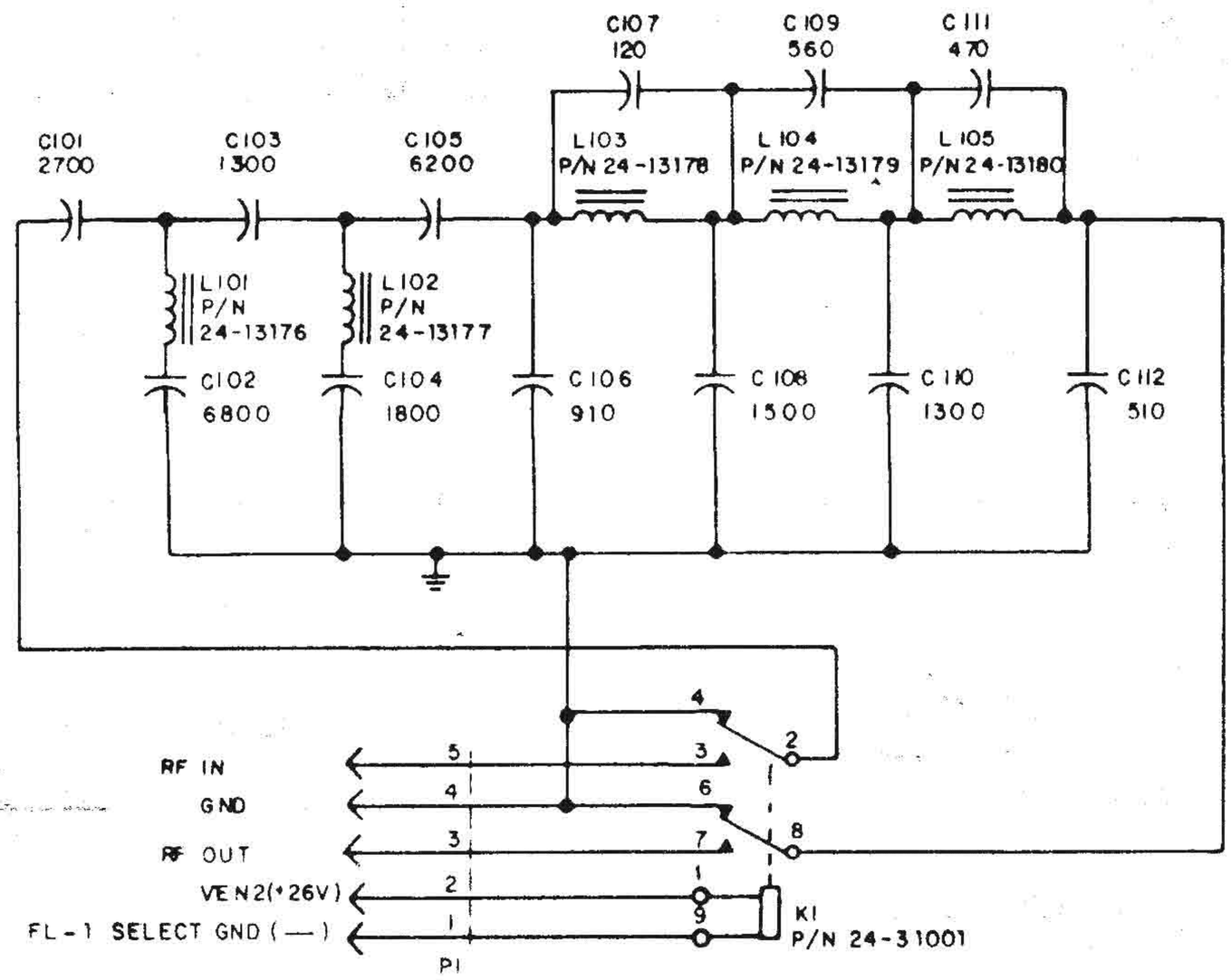


N, FOR COMPLETE P/N PREFIX WITH 21.



K1, K2 AND K3 SCHEMATIC DIAGRAM (SEE NOTE 5)
(UNENERGIZED POSITION-BOTTOM VIEW)

Fig. 2-30.A. Module SNF 1A5A3, schematic circuit diagram (sheet 1 of 7)



NOTES

1 PARTIAL PART NUMBERS ARE SHOWN FOR COMPLETE P/N PREFIX WITH 21

2. ALL CAPACITORS ARE IN PICOFARADS.

3 COILS INDUCTANCE AS FOLLOWS (FOR REFERENCE ONLY):

CATALOG P/N	INDUCTANCE VALUE (μH)
24-13176	3,70
24-13177	7,00
24-13178	3,18
24-13179	2,45
24-13180	2,30

4 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH 1A5A3FL1.

K 1 SCHEMATIC DIAGRAM
(DEENERGIZED POSITION BOTTOM VIEW)

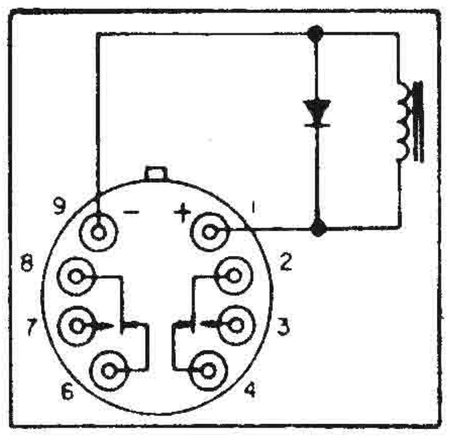
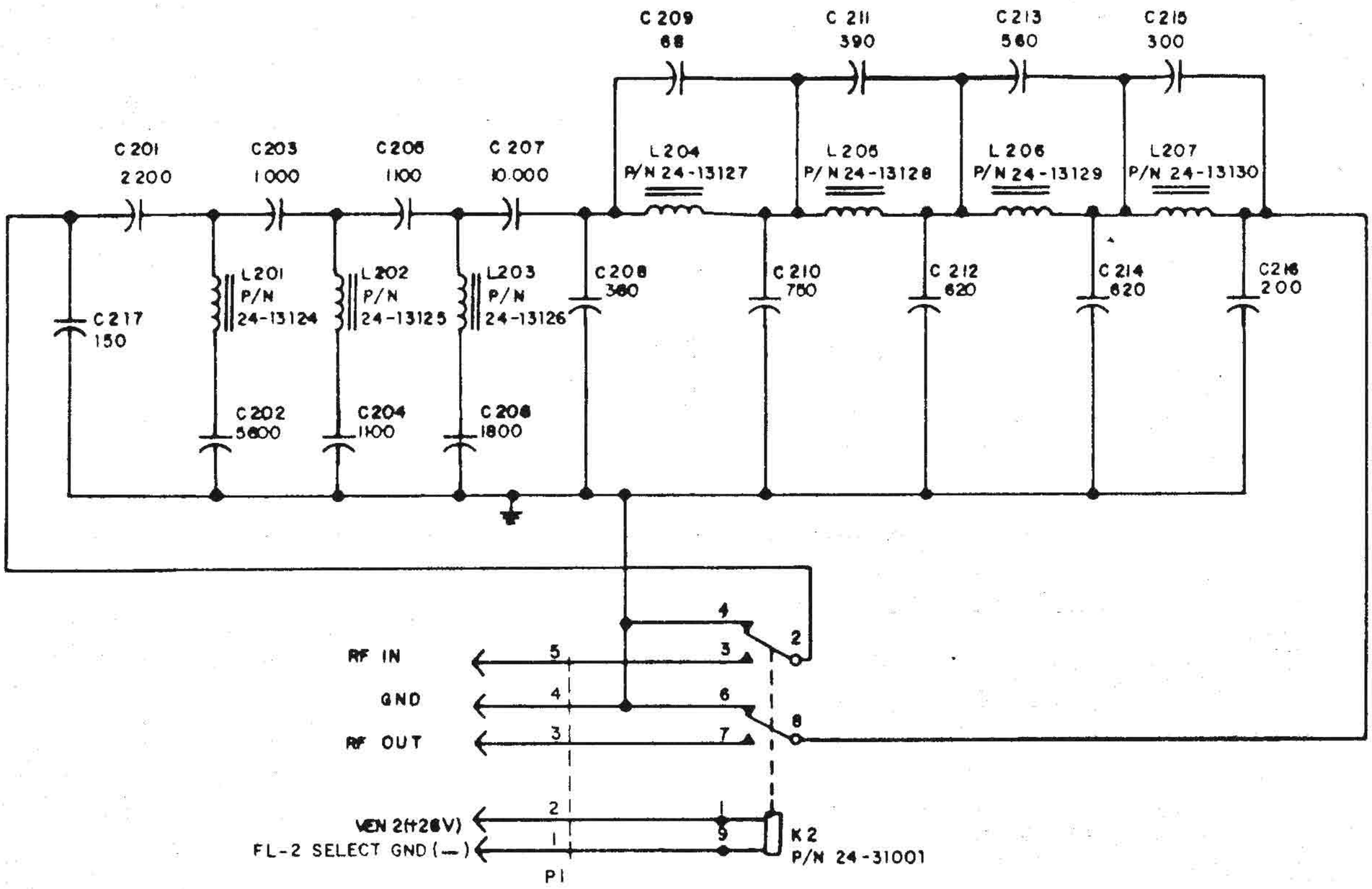


Fig. 2-30.B. Module SNF 1A5A3, schematic circuit diagram (sheet 2 of 7)



NOTES:

1. PARTIAL PART NUMBERS ARE SHOWN. FOR COMPLETE P/N PREFIX WITH 21.
2. ALL CAPACITORS ARE IN PICOFARADS
3. COILS INDUCTANCE AS FOLLOWS (FOR REFERENCE ONLY):

CATALOG P/N	INDUCTANCE VALUE (μH)
24-13124	2,52
24-13125	4,05
24-13126	3,90
24-13127	1,90
24-13128	1,46
24-13129	1,15
24-13130	1,23

4 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH 1A5A3FL2

K 2 SCHEMATIC DIAGRAM
(DE ENERGIZED POSITION BOTTOM VIEW)

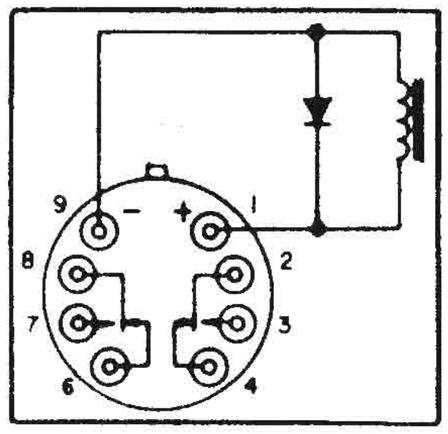
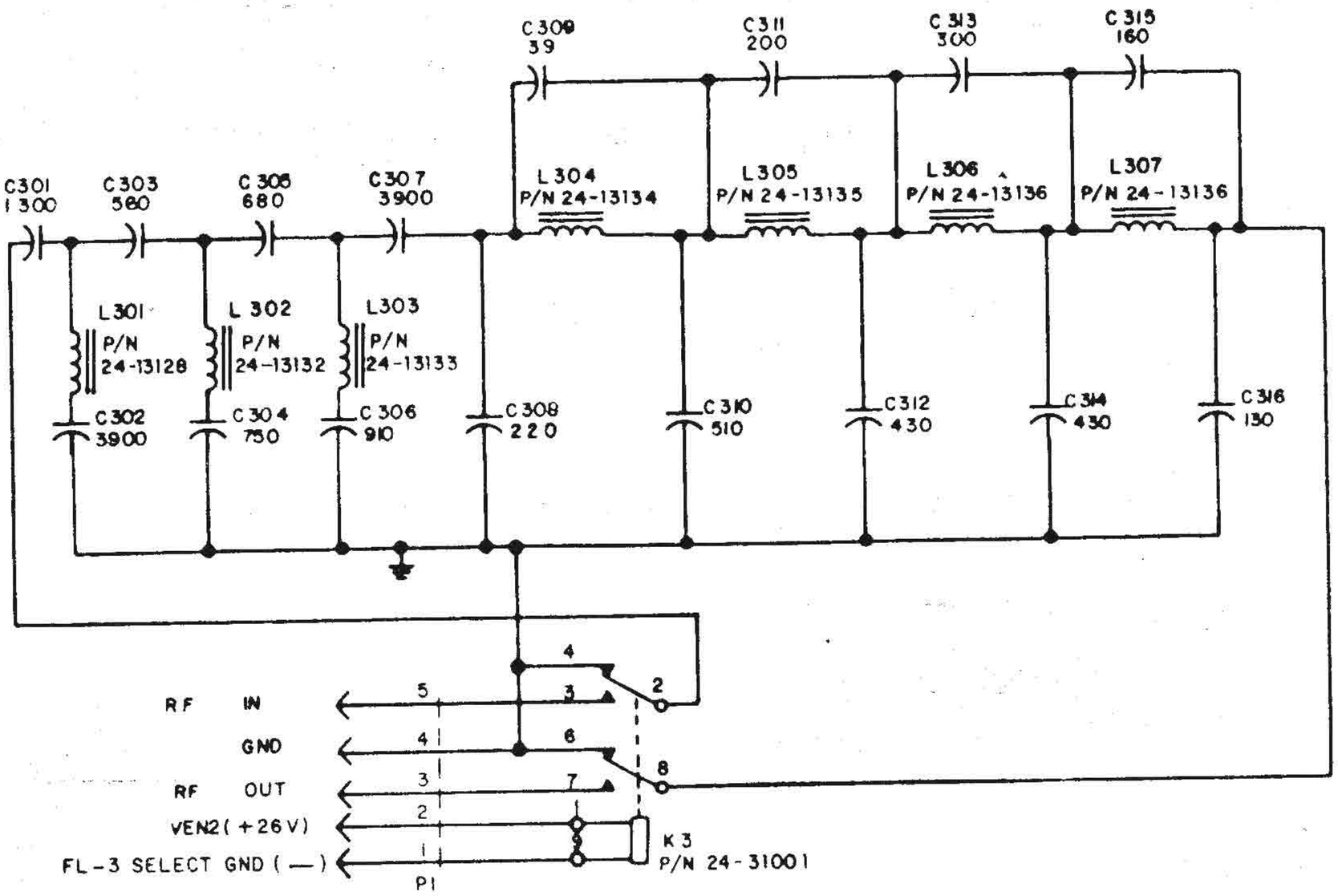


Fig. 2-30.C. Module SNF 1A5A3, schematic circuit diagram (sheet 3 of 7)



NOTES:

1. PARTIAL PART NUMBERS ARE SHOWN. FOR COMPLETE P/N PREFIX WITH 21.
2. ALL CAPACITORS ARE IN PICOFARADS.
3. COILS INDUCTANCE AS FOLLOWS (FOR REFERENCE ONLY):

CATALOG P/N	INDUCTANCE VALUE (μH)
24-13128	1,45
24-13132	2,10
24-13133	2,44
24-13134	1,20
24-13135	1,01
24-13136	0,87

4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH 1A5A3FL3

K 3 SCHEMATIC DIAGRAM
(DEENERGIZED POSITION BOTTOM VIEW)

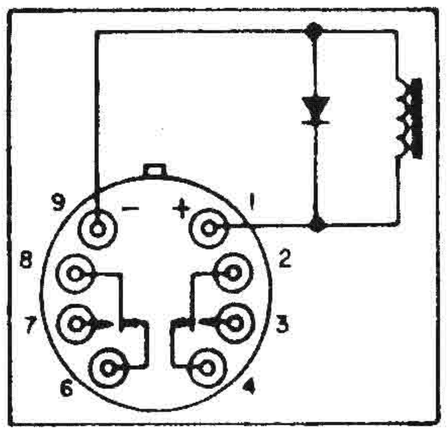
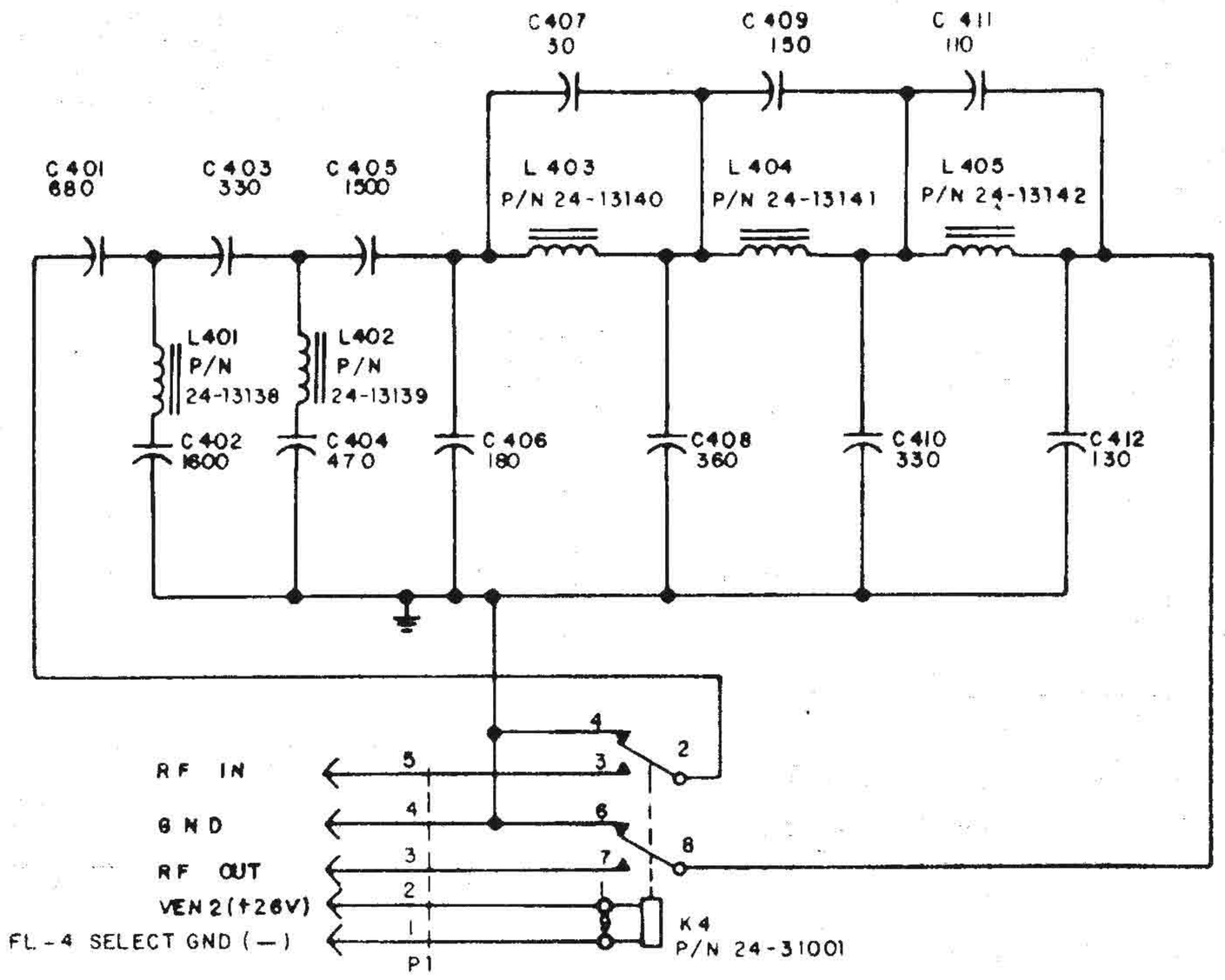


Fig. 2-30.D. Module SNF 1A5A3, schematic circuit diagram (sheet 4 of 7)



NOTES:

1. PARTIAL PART NUMBERS ARE SHOWN. FOR COMPLETE P/N PREFIX WITH 21.
2. ALL CAPACITORS ARE IN PICOFARADS
3. COILS INDUCTANCE AS FOLLOWS (FOR REFERENCE ONLY):

CATALOG P/N	INDUCTANCE VALUE (μH)
24-13138	0,94
24-13139	1,54
24-13140	0,83
24-13141	0,66
24-13142	0,61

4 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH 1A5A3FL4.

K 4 SCHEMATIC DIAGRAM
(DEENERGIZED POSITION BOTTOM VIEW)

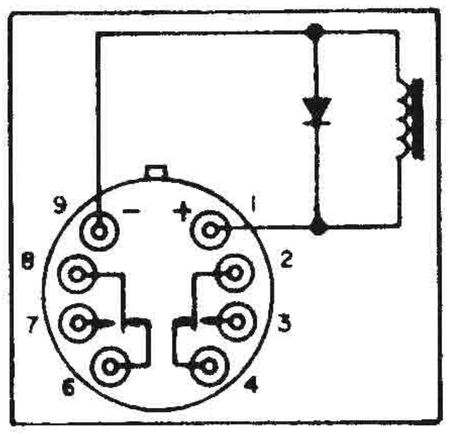
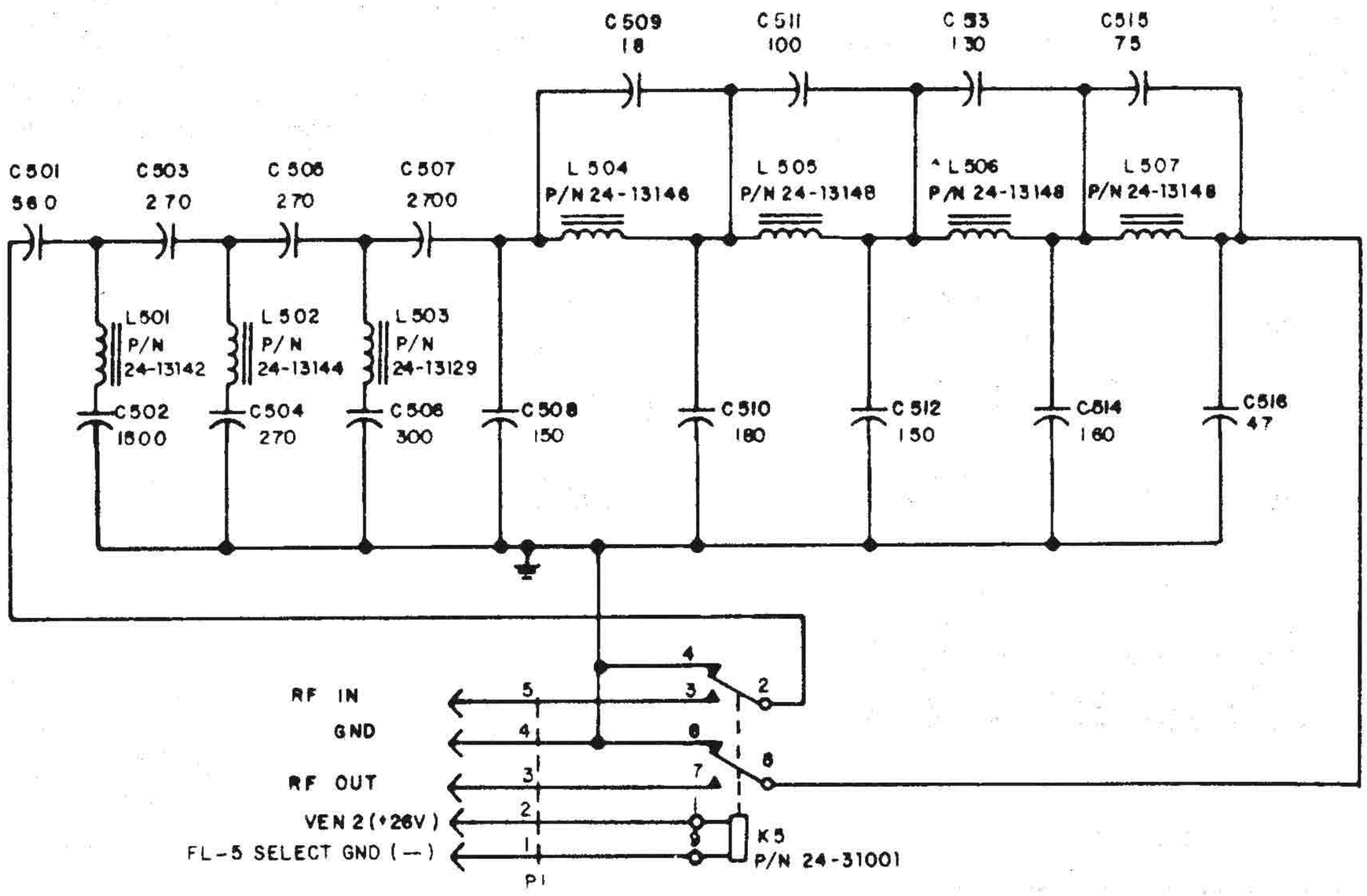


Fig. 2-30.E. Module SNF 1A5A3, schematic circuit diagram (sheet 5 of 7)



NOTES.

1. PARTIAL PART NUMBERS ARE SHOWN. FOR COMPLETE P/N PREFIX WITH 21.
2. ALL CAPACITORS ARE IN PICOFARADS.
3. COILS INDUCTANCE AS FOLLOWS (FOR REFERENCE ONLY):

CATALOG P/N	INDUCTANCE VALUE (μH)
24-13142	0,62
24-13144	0,98
24-13129	1,13
24-13146	0,47
24-13148	0,33

4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH 1A5A3FL5.

K5 SCHEMATIC DIAGRAM
(DEENERGIZED POSITION BOTTOM VIEW)

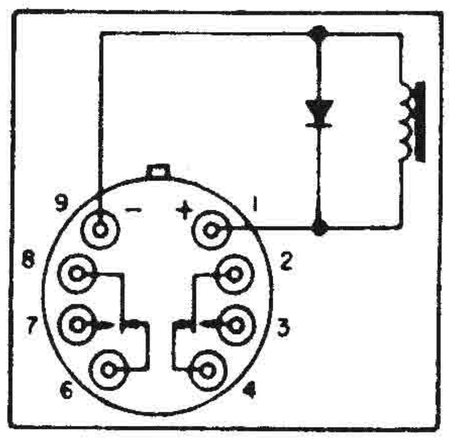
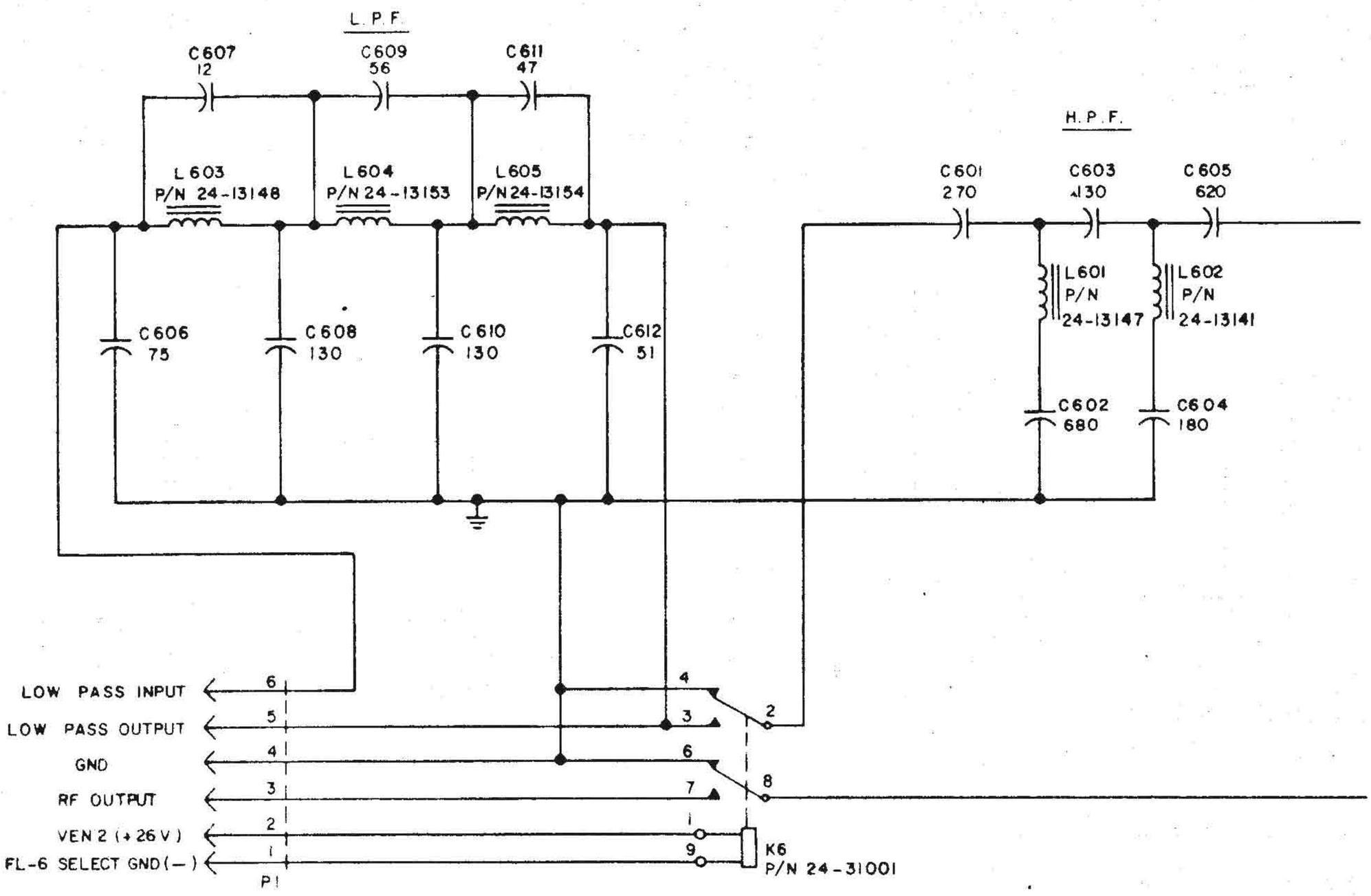


Fig. 2-30.F. Module SNF 1A5A3, schematic circuit diagram (sheet 6 of 7)



NOTES

1. PARTIAL PART NUMBERS ARE SHOWN FOR COMPLETE P/N PREFIX WITH 21.
2. ALL CAPACITORS ARE IN PICOFARADS
3. COILS INDUCTANCE AS FOLLOWS (FOR REFERENCE ONLY):

CATALOG P/N	INDUCTANCE VALUE (μH)
24-13147	0.37
24-13141	0.66
24-13148	0.33
24-13153	0.26
24-13154	0.24

4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH 1A5A3FL6.

K6 SCHEMATIC DIAGRAM
(DEENERGIZED POSITION BOTTOM VIEW)

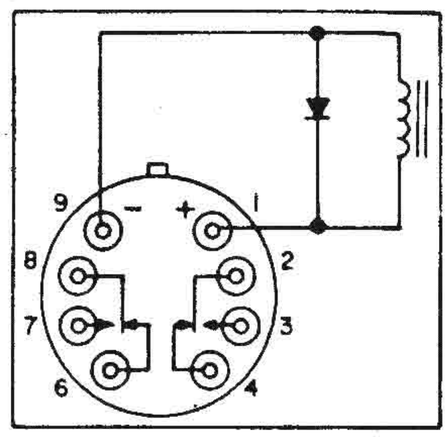


Fig. 2-30.G. Module SNF 1A5A3, schematic circuit diagram (sheet 7 of 7)

ted from the load. Comparators B, C transform this output to logic levels:

(a) A high level is generated at the output of comparator B (UIP) (HT-high threshold line) if the reflected power is higher than that corresponding to a load VSWR of 3.0:1.

(b) A high level is generated at the output of comparator C (UIC) (LT-low threshold line) if the reflected power is higher than that corresponding to a load VSWR of 1.5:1.

(3) Load phase detectors (PH-DET). These detectors provide an output voltage proportional to the load phase angle. There are two detectors, one for the lower frequency range (2 to 10 MHz) and the second for the 10 to 30-MHz range. The appropriate detector is connected in the signal path by the contact of relay K2. The detector outputs are applied to comparator D (UIB), which generates a low level when the reactance is capacitive and a high level when it is inductive.

From the load sensors, the transmit signal passes through the contacts of the tune/operate relay to module MN 1A5A1. In the regular transmit mode, transmit signal passes through the contacts of the energized transmit/receive relay and through the selected bandpass filter to the TX LEVEL and ALC detectors. From these detectors, the transmit signal passes through the contacts of the unenergized tune/operate relay to module MN 1A5A1. The comparators and the ALC amplifiers are powered only in the transmit mode (from the PTT PRE +12V and -10VEN lines).

In the receive mode, the received signal arriving from module MN 1A5A1 passes through the unenergized contacts of the tune/operate relay and through the TX LEVEL and ALC detectors (which do not influence the received signal) to the selected bandpass filter. The filtered signal passes through the contacts of the unenergized transmit/receive relay to module MIXER 1A2A1.

b. Receive Path Circuit Analysis (fig. 2-30).

(1) Signal path. The signal arriving from module MN 1A5A1 at coaxial connector J1, passes via the contacts 2,4 and 8,6 of the tune/operate relay K1 (unenergized) and transformer T2 of the ALC detector to the bandpass filters. The signal passes through the bandpass filter, corresponding to the operating frequency and is applied through contacts 2 and 4 of receive/transmit relay K3 (shown in fig. 2-30.A in the RECEIVE position) to pin B.

(2) Bandpass filters (fig. 2-30.B through 2-30.G). Each one of the blocks designated FL1 - FL6 contains a bandpass filter and a relay. The relay contacts insert the filter into the signal path when the relay coil is grounded by the corresponding driver transistor, Q2 through Q6 (the driver transistor for FL5 is contained in module LORD 1A5A2). The frequency range of each filter is:

(a) FL1 - 2.0 to 2.9999 MHz.
(b) FL2 - 3.0 to 4.9999 MHz.
(c) FL3 - 5.0 to 7.9999 MHz.
(d) FL4 - 8.0 to 11.9999 MHz.
(e) FL5 -12.0 to 19.9999 MHz.

(f) In the frequency range of 20 to 30 MHz, the bandpass filter is composed of FL6B (a low pass filter with a cutoff frequency of 30 MHz) and of FL6A (a 20-MHz high pass filter).

FL6B is always inserted in the signal path.

c. Transmit Path Circuit Analysis (fig. 2-30).

(1) Signal path. The RF transmit signal arriving from module PA 1A6 at connector P25 is connected through contacts 3, 2 of relay K3 (energized), lowpass filter FL6B, and the selected bandpass filter to the ALC and TX LEVEL

detector. From the ALC detector, the signal is coupled through contacts 2, 4 and 6, 8 of relay K1 (unenergized) to the matching network.

(2) TX LEVEL detector. The TX LEVEL detector consists of diode CR15, which rectifies a sample of the RF output voltage through R41 and R42. The rectified voltage is filtered by C26 and connected to pin K.

(3) ALC detector. The ALC detector is a directional detector, responsive only to the power flowing to the load. Current transformer T2 provides a voltage proportional to the load current, and capacitive divider C42, C43 provides a sample of the load RF voltage. Diode CR8 rectifies the voltage resulting from the vectorial summing of these voltages. The resulting DC voltage, which is proportional to the forward power, is reduced by R45, R46 and filtered by C38 before application to U2A.
U2A amplifies the difference between the rectified voltage across C38 and the reference voltage determined by RV3. C46 prevents noise from appearing at the output of U2A.
The output voltage of U2A is applied via CR13 and R50 to capacitors C41 and C39. Their charge time is very fast, while the discharge (via R48) is much slower. Therefore, C41 stores the positive peaks of the rectified voltage. The voltage on C41 is buffered by U2B, and applied to pin N (the ALC line) via R56, CR9 and CR19.
Due to the action of CR9 and C48, the voltage at pin N is proportional to the peak output. When sudden, large changes in the ALC voltage occur (e.g. during tuning) the buffer U2B is bypassed through R55 and VR12; this provides fast response despite the use of a large capacitance for C48.
When the power amplifier in module PA 1A6 is bypassed (BP (PA) line grounded), the input of U2B is also grounded through CR20. This ensures a zero ALC voltage in the bypass mode while maintaining the circuit under power; this arrangement prevents transients upon return to transmit mode.

d. Tuning Path Circuit Analysis (fig. 2-30.A).

(1) Signal path. The tuning path is identical to the transmit path up to the tune/operate relay K1. When the tuning cycle begins, relay K1 operates and its contacts connect the PA signal, appearing at pin 2, to pin 3 (see also para. 2-12). The signal is attenuated by 6 dB in the hybrid attenuator located on the chasis, and returned, via a coaxial connector, to the three load sensors.

(2) R-DET (CR1, CR2). A sample of the RF voltage, provided by R1, RV1 and R2, is added to the current sample (the voltage drop across R4) and rectified by the diodes CR1 and CR2. C1, C2, R7, R8, C16, and C36 filter the resulting differential voltage, which is then applied to comparator U1A. The rectified voltage on TP2 will be higher than that on TP1 when the load resistive component is smaller than 50 ohms and comparator U1A output (R line) will be high (about +10V). The output of U1A will be low if the load resistive component is greater than 50 ohms.

(3) Reflected power detector. This circuit is identical to that of the ALC (forward power) detector, except that the polarity of the voltage supplied by T1 is reversed (relative to that provided by T2). The detector's output is connected to comparators B (U1D) and C (U1C) (see para. 2-12.f). Reference voltages are applied to the comparators by the voltage dividers R57 and R27, R26, and RV2 respectively. The reference voltage for comparator B is increased when operating in the frequency bands 2 to 3 MHz (by R60 and CR17). The reference voltage for comparator C is increased when operating in the frequency bands 20 to 30 MHz (by CR16 and R25), by using the high levels appearing on lines FL1 and X61.

(4) Load phase detectors. Two load phase detectors are used - one for the frequency range of 2 to 10 MHz

(CR6, CR7) and one for frequency range 10 to 30 MHz (CR4, CR5). The contacts of relay PH K2 connect the appropriate phase detector. Relay PH K2 is controlled by module LORD 1A5A2 through the PH CONT line, pin V. The load phase detector output is connected to comparator D (U1B). Analysis of the 10-30 MHz phase detector is presented below (the second phase detector is identical, except for the component values).

The diodes CR4 and CR5 rectify the vectorial sum of the voltage drops across the current sensing resistors R62 and R63, respectively, and the sample of the RF voltage appearing across R14. This sample is phase-shifted by +90°, relative to the voltage across the load, since the current through R14 is determined mainly by C12 reactance. When the load reactance is zero, its current and voltage are in-phase and the phase detector output is zero. Phase shift between the load current and voltage causes the rectified voltage at the output of one of the phase detector arms to increase, while the second will decrease. Therefore, an output voltage is generated, whose polarity depends on the phase shift. Comparator U1B senses this output and converts it to high or low levels.

2-15. Module LORD 1A5A2 (fig. 2-31 through 2-42)

a. General Description (fig. 2-31).

Module LORD 1A5A2 contains a special-purpose processor which controls the antenna matching process.

The LORD is comprised of seven microelectronic modules and one erasable, programmable read-only memory (EPROM), which contains the operating program. The microelectronic modules are:

(1) Logic controller A1: contains logic circuits and decoder which provide control signals for L1 and for the band capacitors in module MN 1A5A1.

(2) Decoder A2: contains logic circuits and decoders which provide control signals for the bandpass filters and phase detector selection relay in module SNF 1A5A3, and frequency range information to the logic controller, A1.

(3) Processor A3: contains the special-purpose processor.

(4) Timer A4: provides timing signals and controls the second variable series element, X2, in module MN 1A5A1, using information provided by the decoder A2.

(5) Relay drivers, RD (three microelectronic modules): convert the logic-level signals provided by the other microelectronic modules to drive signals appropriate for driving the controlled relays in modules SNF 1A5A3 and MN 1A5A1.

b. LORD Interface (fig. 2-31).

(1) The LORD receives the following control lines:

(a) PTT LORD from module CONT 1A7. A high level on this line indicates that the PTT line was grounded.

(b) TRANSIT from the front panel frequency controls. A positive or negative-going pulse on this line indicates that the frequency was changed.

(c) 12V supply line. Although this line is used to power the LORD circuits, it should also be considered a control line, which indicates that the RT-936/PRC-174 was turned on.

(2) The LORD receives the following information lines:

(a) DIP from the whip sensor.
(b) Operating frequency (in

BCD representation): X61, X60 (10-MHz digit), X53, X52, X51, X50 (1-MHz digit), X43, X42 (the two most significant bits of the 0.1 MHz digit).

(c) Φ line from module SNF 1A5A3.

(d) R line from module SNF 1A5A3.

(e) LT line from module SNF 1A5A3.

(f) HT line from module SNF 1A5A3.

(3) The LORD provides the following control lines:

(a) Drive lines for the relays of module MN 1A5A1.

(b) Control lines for the drivers of the bandpass filters in module SNF 1A5A3.

(c) PH CONT control line for the phase detector selection relay in module SNF 1A5A3.

(d) RFS line to module MIXER 1A2A1 - for turning off the RF output of the transmitter while relays are switched under LORD control, or after matching failed.

(e) EN CONT to module PS 1A4, for turning on the supply voltage for the relays in the SNF 1A5A3 and MN 1A5A1, when relays are switched under LORD control.

(f) Bypass relay drive line - to module MN 1A5A1.

(g) SF pulse to module CONT 1A7. This is a positive-going pulse which is triggered by the TRANSIT pulse or equipment turn-on.

(4) The LORD provides the following indication lines:

(a) NM line. A high level on this line indicates that the matching process failed.

(b) FO UNLOCK. A high level on this line indicates that the selected frequency is outside the 2 to 29.9999 MHz range.

(c) TUNE and $\overline{\text{TUNE}}$ indicate that matching is being performed.

(5) The LORD receives the following supply lines:

(a) 12V for powering its internal circuits.

(b) -10V EN - for providing -5V to the EPROM and level-shifting circuits during the matching process.

(c) VEN1 and VEN2 - to the relay drivers.

c. Matching Algorithm (fig. 2-32). This paragraph provides a short description of the matching algorithm. For full details, follow the flow chart in fig. 2-32.

(1) Start and initial checks. The matching algorithm starts upon turn-on, start of transmission, or reception of TRANSIT pulse (para. c.).

(a) After program execution starts, the LORD checks PTT LORD line state.
If PTT LORD=0 (receive mode), the LORD brings the matching network components in module MN 1A5A1 to the optimal setting, as provided by microelectronics modules A1 and A2, then the execution of the program is ended. When the dipole antenna is used, the LORD activates the bypass relay, which bypasses the whole matching network.
If PTT LORD=1 (transmit mode), the LORD checks whether this is the first transmission following a frequency change or PRC-174 turn-on.

1. If not, it is assumed that matching was achieved during the previous transmission and the existing matching network condition should be retained. However, when the dipole is

connected, the LORD first tries to bypass the matching network, because a properly installed dipole antenna is well-matched to the PRC-174 output impedance. If antenna VSWR is less than 1.5:1, the LORD assumes that matching exists and the execution of the program is ended. If the VSWR is more than 1.5:1, and the dipole is used, the bypassing is cancelled; if now the VSWR is less than 3:1, it is accepted. Otherwise a full matching cycle is started (point A).

2. If the LORD finds that the present transmission is the first one, it still checks for matching, but this time it requires a VSWR less than 1.5:1. If the VSWR occurs to be less than 1.5, matching is declared and program execution ends. If the VSWR is more than 1.5:1, a full matching cycle is started (point A).

(2) First matching trial. The matching process starts at point A. The matching process consists of two parts.

(a) In the first one, the value of L1 is changed while X2 is kept at zero. L1 is changed in the same direction until the VSWR decreases below 1.5:1 (LT line assumes a low level) or until the load resistance sensor (the R-sensor in module SNF 1A5A1) indicates that the load resistance has passed through the 50-ohm value (i.e. from a value higher than 50 ohms to a lower value, or vice-versa; this is indicated by a level change on the R-line). This change means that the load resistance seen by the power amplifier is close to 50 ohms.

(b) The second part is reached when the VSWR remains greater than 1.5:1, but the load resistance is close to 50 ohms. To reduce the VSWR, the load reactance must be tuned out, by changing the value of X2. X2 can be either a coil (L2) or a capacitor (C2), according to the position of relay KLC (controlled by the TLC line). During the second part, X2 is changed while L1 is kept fixed. X2 is changed in the same direction, until the VSWR decreases below 1.5:1 (LT line assumes a low level) or the load phase detector in module SNF 1A5A3 indicates that the phase changed sign (i.e. the load reactance changes from capacitive to inductive, or vice-versa.
This is indicated by a level change on the Φ-line). This change means that the load impedance is now nearly 50 ohms.

The first matching trial ends successfully only when the VSWR is less than 1.5:1. If during the matching trial level changes were obtained on either the R or Φ-lines without obtaining a VSWR less than 1.5:1, the matching process described in (a) and (b) above is repeated once more.

(3) Second matching trial. The second matching trial (point B) is automatically started when one of the two variable components reached its extreme value, without achieving a VSWR less than 1.5:1 or obtaining at least a level change on either the R- or Φ-line. When the second trial starts (point B), the appropriate component of the matching network is brought to the home condition (the other extreme value, i.e. if the previous matching trial ended with minimum L2 inductance, the second matching trial starts with L2 at maximum inductance). If matching is not obtained in this condition, the program returns to point A and the operations described in (2) above are repeated.
The second matching trial ends successfully only when the VSWR is less than 1.5:1, or level changes where obtained on both the R and Φ lines.

(4) No-match condition. If the second matching trial fails, the no-match (NM) condition is declared. Transmission is then inhibited and an alarm indication is generated.

d. LORD Processor Operation (fig. 2-31).

(1) The LORD processor is activated by the start pulse, $\overline{PP}$, provided by circuits in microelectronic module A4. This pulse is generated when either of the following events occur:

(a) The PTT LORD line rises to a high level, and triggers the start pulse monostable, which then provides a pulse on the PP line.

(b) A TRANSIT pulse is received from the front panel frequency controls. This pulse triggers the SF pulse monostable. The resulting pulse causes a pulse of similar length to appear on the $\overline{PP}$ line.

(c) The RT-936/PRC-174 is turned on. The rise of the +12V supply voltage is detected by the supply voltage monitor, which then triggers the SF pulse monostable (see (b) above).

(2) The $\overline{PP}$ pulse sets the start/stop flipflop in microelectronic module A3. In response, the TUNE line rises to a high level and the $\overline{TUNE}$ line falls to a low level. The low level on the $\overline{TUNE}$ line also enables the EPROM and starts the clock oscillator in the microelectronic module A3.
In addition, the $\overline{PP}$ pulse resets the address latch, also located in microelectronic module A3, which then applies the address of the first instruction on the address bus. This completes the start-up procedure.

(3) The output signal of the clock oscillator is processed by the state clock control circuit. This circuit generates three clock signals: a command clock, an address clock and a state clock. The command clock is applied to the state latch and command decoder, whereas the address clock is applied to the address latch. The state clock is applied to the least significant bit (LSB) input of the EPROM address port, therefore, when the state clock line falls to a low level, an even-numbered memory location is addressed, whereas when the state clock line rises to a high level, an odd-numbered memory location is addressed. The EPROM contents are organized such that odd-numbered addresses contain the information required to obtain the next address, whereas even-numbered addresses contain a command. Therefore, the alternation of high/low pulses on the state clock line provides the alternate retrieval of addresses and commands, which is essential for the proper operation of any computer system.

(4) The contents of the addressed EPROM location appear on the data bus. A level shifter ensures compatibility between the EPROM output levels and those used in the microelectronic module A3.

(5) During an address cycle, the data appearing on the data bus is latched into the address latch, whereas in a command cycle, the data is latched into the state latch and the command decoder. Both the state latch and the command decoder hold the received data bits steady at their outputs, until new bits are retrieved from the EPROM. The functions initiated by these bits are described in detail in (7) and (8) below.

(6) In principle, the purpose of a command cycle is to control circuits external to the LORD, e.g. to change the position of relays in module MN 1A5A1, whereas the purpose of an address cycle is to check the conditions reached after performing the last command cycle, and cause the retrieval of the commands required to complete the matching process. Therefore, in an address cycle, it may be necessary to check the conditions of the external control and information lines as well as the present system states (indicated by the bits appearing at the output of the state latch). This check is carried out by means of an input selector, whose output participates in the formation of the next address (in

P/O TIMER A4

+12V

SUPPLY VOLTAGE MONITOR

SF PULSE MONOSTABLE

TRANSIT (FROM FREQUENCY CONTROLS)

START PULSE ($\overline{PP}$) MONOSTABLE

$\overline{PP}$

S START/ST
FLIP-FLO
R

PTTLORD (FROM CONTROL MODULE)

+12V

CS

DATA PORT

LEVEL SHIFTE

EPROM

LSB

ADDRESS PORT

ADDRESS

VEN1

VEN2

FROM SNF MODULE

Ø

R

LT

HT

LIM

LI

-10V EN

-5V REGULATOR

-5V

FREQUENCY INFORMATION

10MHZ

X61

X60

1MHZ

X53

X52

X51

X50

0.1MHZ

X43

X42

DIP.

DECODER

DL21

DL22

F6-F8

PH CON

DECODER A2

PROCESSOR A3

S
R
START/STOP FLIP-FLOP
TUNE
$\overline{\text{TUNE}}$
CLOCK CONTROL
CLOCK OSCILLATOR
STATE CLOCK CONTROL
STATE LATCH
BP
NM
T
U
COMMAND CLOCK
P/O TIMER A4
RFSC
LEVEL SHIFTER
DATA BUS
COMMAND DECODER
LS1
CNT1
PST
LS2
CNT2
LSB
STATE CLOCK
ADDRESS BUS
P/O TIM
RESET ADDRESS LATCH
INPUT SELECTOR
ADDRESS CLOCK
$\overline{\text{LIM2}}$
U
T
$\overline{\text{W}}$
$\overline{\text{LIM1}}$
DL21
DL22
F6-F8
PH CONT.

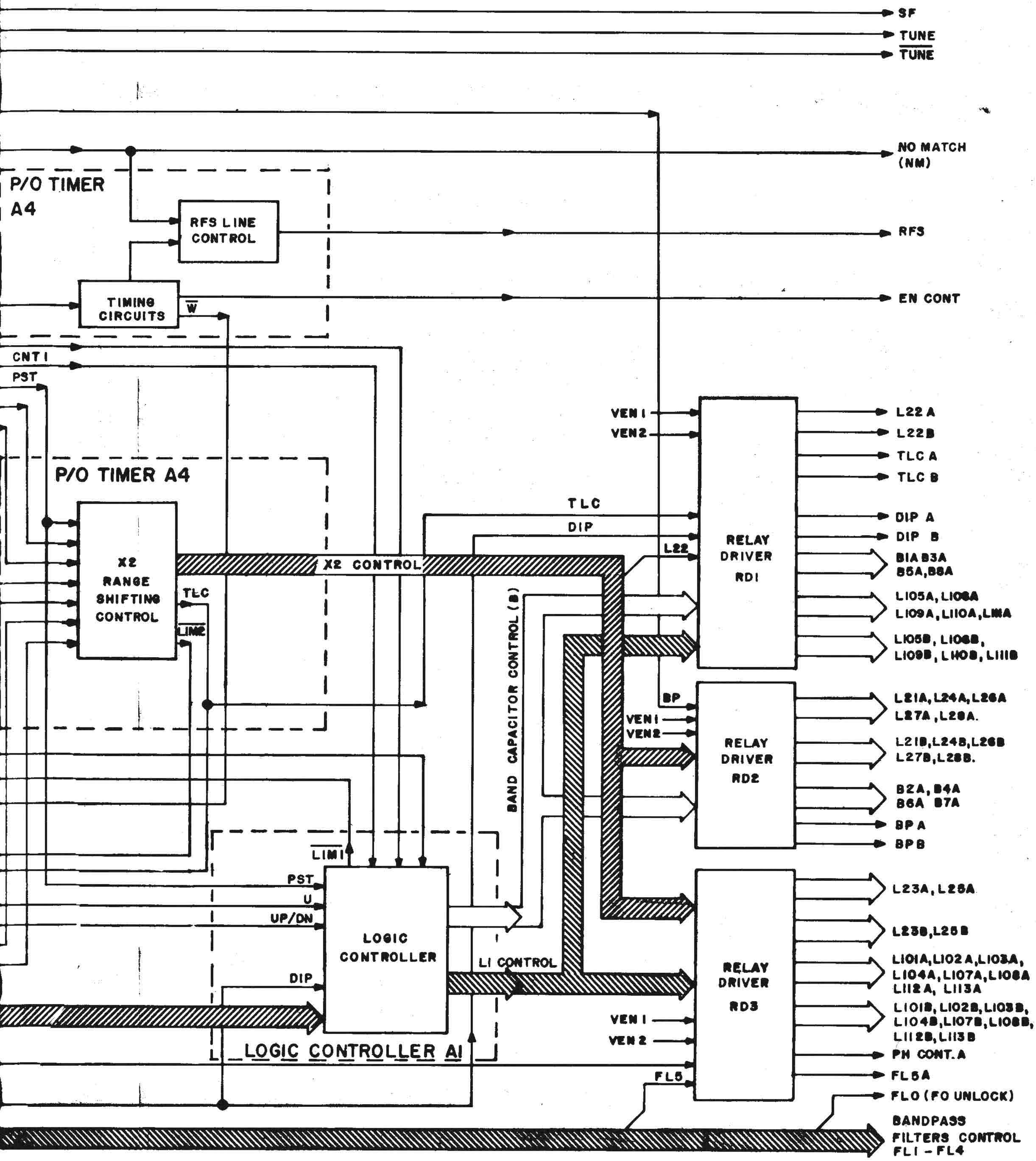


Fig. 2-31. Module LORD 1A5A2, block diagram

the address latch). The input selector is controlled by several of the data bus lines. The binary code appearing on these lines is used to select the appropriate input line (see fig. 2-31), and this line is connected to the address latch. In the address latch, the selected line is combined with the partial address appearing on the other data bus lines and the new address is formed.
The address-forming process described above allows the LORD processor to ask questions and branch to the instruction appropriate for dealing with the new system conditions.

(7) The bits appearing at the output of the state latch are:

(a) BP - controls the bypass relay in MN 1A5A1.

(b) T - a high level indicates that the LORD executes the second part (cycle) of a matching trial (see para. e).

(c) U - a high level indicates that the LORD executes the second matching trial.

(d) NM (NO MATCH) - a high level indicates that the matching process failed.

(8) The bits appearing at the output of the command decoder are:

(a) RFSC - controls the RFS timing circuits in the microelectronic module A4: when the RFSC line rises to a high level, an RFS pulse is generated.

(b) LS1, CNT1 - control the operation of microelectronic module A1.

(c) LS2, CNT2 - control the operation of microelectronic module A4.

(d) PST - controls loading of information from microelectronic modules A1 and A4.

e. Control of External Circuits (fig. 2-31). The LORD processor interfaces the external circuits via circuits contained in microelectronic modules A1, A2, and part of A4. Several of the control lines exiting from these microelectronic modules are buffered by driver circuits contained in the three relay driver microelectronic modules, i.e. RD1, RD2 and RD3. This paragraph analyzes the operation of these circuits, and their interaction with the LORD processor.

(1) RFS line control - microelectronic module, A4. The RFS line is controlled by the LORD processor via circuits contained in microelectronic module A4.

(a) During the matching process, i.e. when the NM line is held at a low level, the state of the RFS line depends only on the RFSC output line (from the command decoder in microelectronic module A3). The RFSC line rises to a high level each time the relays controlled by the LORD must change position (cold switching). Following the rise of the RFSC line, a high pulse is applied on the RFS line. During this pulse, the following events occur:

1. The RF power is turned off.

2. After the RF power is turned off, a high level pulse is applied to the EN CONT line. This pulse turns on the relay supply voltage, and they change position according to the commands issued by the A1 and A2 microelectronic modules. The EN CONT pulse is long enough to allow the relays to settle down in their new position.
The RFS and EN CONT pulses end simultaneously. To halt processor operation while relays change position, the timing circuits in microelectronic module A4 apply a pulse on the $\overline{W}$ line. This pulse starts when the RFSC line

rises to a high level and ends a few milliseconds after the end of the RFS and EN CONT pulse. This additional interval allows the RF output power to reach its normal level, and the SNF sensor outputs to settle, before the LORD processor samples them.

(b) In the event that matching fails, and the NM line rises to a high level, the RFS line is forced to assume high level.

(2) Frequency band decoding - microelectronic module A2. The decoder A2 receives the 10-MHz, 1-MHz and 0.1-MHz frequency data and provides three frequency-band lines, designated F6, F7 and F8, which are used by the logic controller, A1, to calculate the optimum initial setting of L1 in module MN 1A5A1, and to select the appropriate band capacitor in the same module.

(3) PH CONT line - microelectronic module A2. The PH CONT line passes from the decoder A2, via relay driver RD3, to the phase detector selection relay in module SNF 1A5A3.

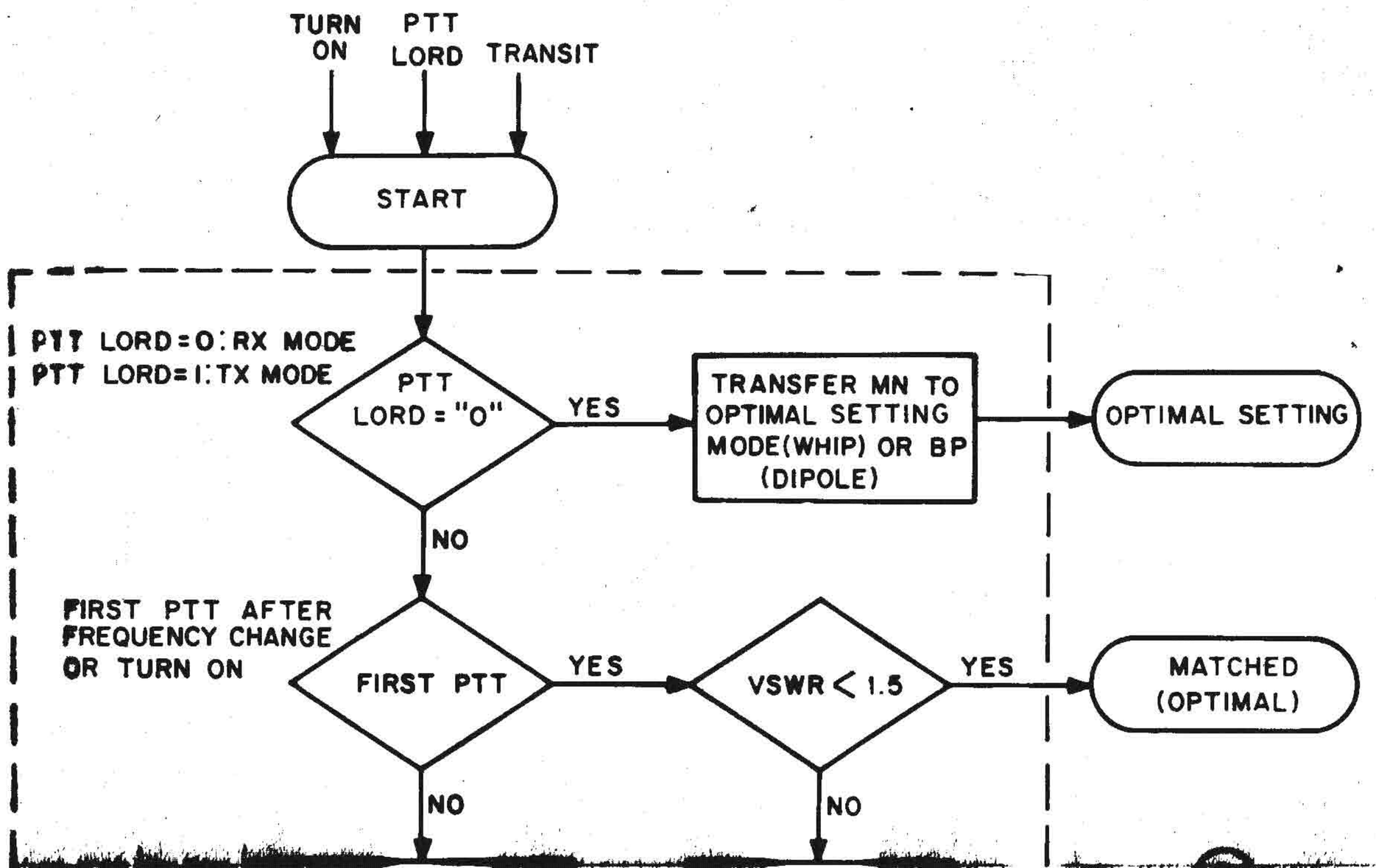
(4) Bandpass filter control lines, FL1 thru FL5 - microelectronic module A2. The decoder A2 provides the control signals -lines FL1 through FL5- which select the appropriate bandpass filter in module SNF 1A5A3. The FL5 line passes through relay driver RD3; the other lines are routed directly to module SNF 1A5A3. See Chapter 2, para. 2-14.

5) FLO (FO UNLOCK) control line - microelectronic module A2. This line indicates that the selected frequency is outside the 2-29.9999 MHz range.

(6) Control of X2 components - microelectronic modules A2, A4. The DL21 and DL22 control lines of microelectronic module, A2 provide a binary code, which is used to calculate the settings of the X2 (L2 or C2) component in module MN 1A5A1. This code is sent to the X2 range shifting control circuit in the timer A4, where it is converted, under control of the processor A3, to relay switching commands. The conversion is required because only five out of the eight possible X2 components are actually used in the matching process, at any given frequency.

The five components are selected according to the operating frequency. The processor controls the conversion of the code received from the decoder A2, and also dynamically changes the selected X2 components, by means of the control signals PST, LS2 and CNT2 appearing at the command decoder outputs, and clock signal SHC. The X2 range shifting control circuit also provides a control line for the KLC relay in module MN 1A5A1.

(7) Control of L1 components - microelectronic module A1. The three-bit frequency band code (F6 - F8) provided by microelectronic module A2 is converted in the logic controller A1 to commands which determine the initial setting of the L1 component in module MN 1A5A1. After a frequency change or equipment turn-on, and before the first PTT activation, the A1 provides an initial setting, which is optimized for best receiver sensitivity. The setting provided when the whip is installed is called "optimal setting". When the dipole is used, the initial setting comprises by-passing and resetting the matching network. After the PTT is depressed for the first time, the A1 provides another initial setting (dependent on the antenna type), which is used in the first matching trial (see para. e.); starting from it, the value of L1 is dynamically changed under control of the processor A3. The changes are controlled by means of control lines UP/DN, PST, and CNT1 provided by the command decoder in A3. When the second matching trial starts, the initial setting is changed to zero, under control of line U provided by the command decoder. When L1 reaches one of its limits, the logic controller A1


TURN ON
PTT LORD
TRANSIT
START
PTT LORD=0: RX MODE
PTT LORD=1: TX MODE
PTT LORD = "0"
YES
TRANSFER MN TO OPTIMAL SETTING MODE(WHIP) OR BP (DIPOLE)
OPTIMAL SETTING
NO
FIRST PTT AFTER FREQUENCY CHANGE OR TURN ON
FIRST PTT
YES
VSWR < 1.5
YES
MATCHED (OPTIMAL)
NO
NO

FREQUENCY CHANGE
OR TURN ON

FIRST PTT

YES

VSWR < 1.5

YES

MATCHED
(OPTIMAL)

NO

NO

TRANSFER MN TO BP
FOR DIPOLE OR LAST
STATE FOR WHIP

TRANSFER MN TO
INITIAL
SETTING

B

VSWR < 1.5

YES

MATCHED

YES

VSWR < 1.5

NO

NO

REMOVE BP
(WHEN DIPOLE
IS USED)

INITIAL CHECKS
AND PRESETTING

VSWR < 3

YES

MATCHED

NO

A

INCREMENT
L1

YES

R< 50Ω

NO

DECREMENT
L1

MATCHED

YES

VSWR<1.5

L1
ADJUSTMENT

VSWR<1.5

YES

MATCHED

NO

NO

YES

L1 AT
UPPER LIMIT

L1 AT
LOWER LIMIT

YES

NO

NO

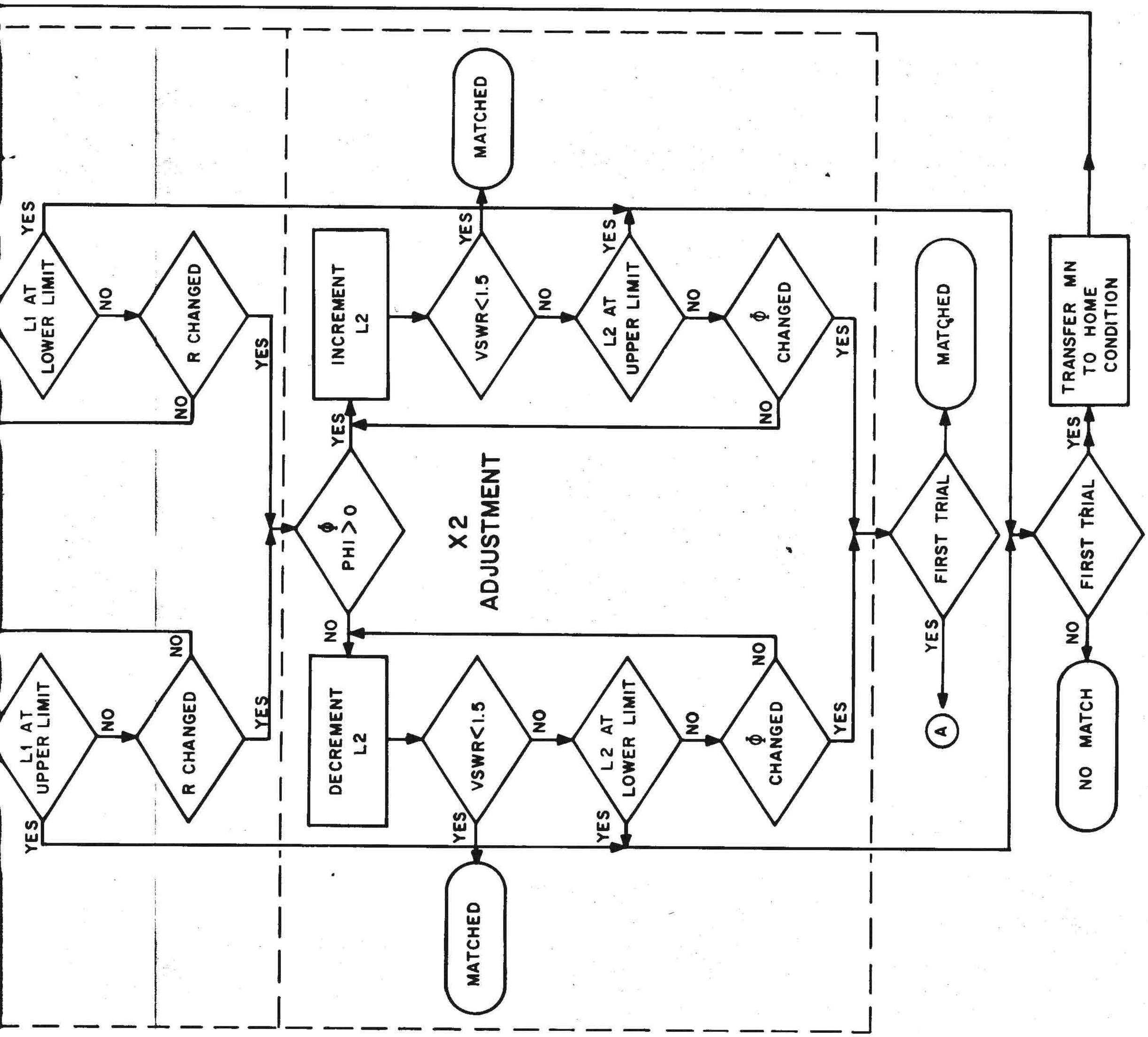


Fig. 2-32. Matching algorithm flowchart

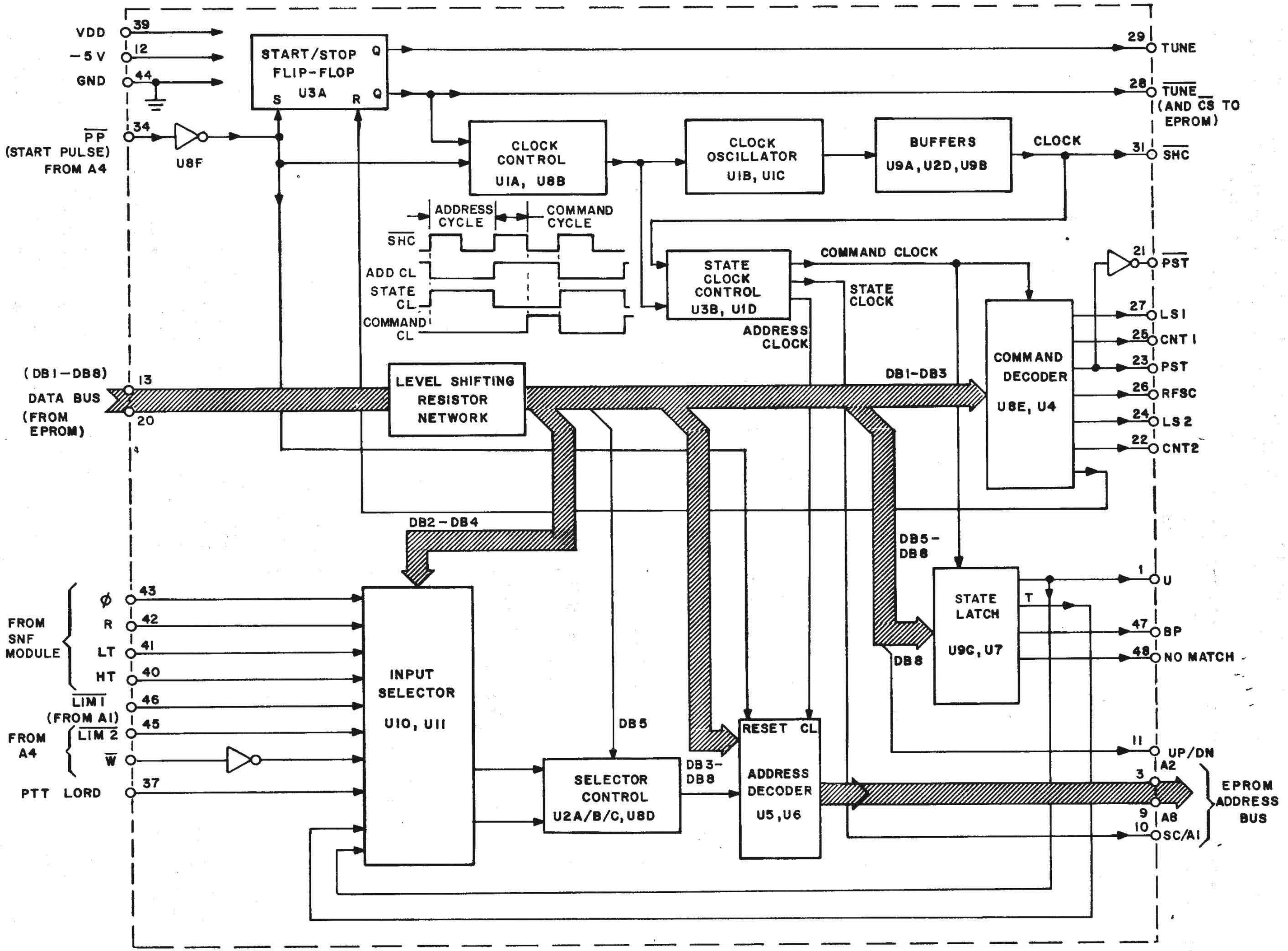


Fig. 2-33. Processor A3, block diagram

MA 2124-09503-00

sends an indication to the processor A3 via the LIM1 line (see para. e.).

(8) Band capacitor control - microelectronic module A1. The value of the band capacitor in module MN 1A5A1 is determined by microelectric module A1, according to the three-bit frequency band code (F6 - F8) provided by microelectronic module A2. The band capacitor value depends on the frequency band, therefore it is not changed during the matching process.

f. Processor Microelectronic Module A3 (fig. 2-33, 2-34). See fig. 2-33 for the functional designations of the various circuits. Refer to para. c. for block diagram analysis.

(1) Start-stop flip-flop and clock circuits.

(a) Halted state. The $\overline{PP}$ line (pin 34) is normally held at a high line and a low level exists at the output of U8F. Flip-flop U3A is in the reset state (pin 1 - the TUNE line - at a low level, and pin 2 - the $\overline{TUNE}$ line - at a high level). The high level on the $\overline{TUNE}$ line forces a high level at the output of U8B, and the clock oscillator, comprised of U1B and U1C, is inhibited.

(b) Start-up. The processor starts when the $\overline{PP}$ line momentarily falls to a low level. The resulting high level pulse appearing at the output of U8F sets U3A. Line TUNE rises to a high level and line $\overline{TUNE}$ falls to a low level. The low level of the $\overline{TUNE}$ line enables the EPROM. After the $\overline{PP}$ pulse ends, the output of U8B falls to a low level and the clock oscillator is enabled.

(c) Clock oscillator. The clock oscillator is an astable multivibrator, comprised of U1B and U1C. The oscillator provides a square wave signal with a period of 5 to 7 microseconds. The clock signal passes through U9A, U2D and U9B and appears at pin 31 of the microelectronic module, designated $\overline{SHC}$.

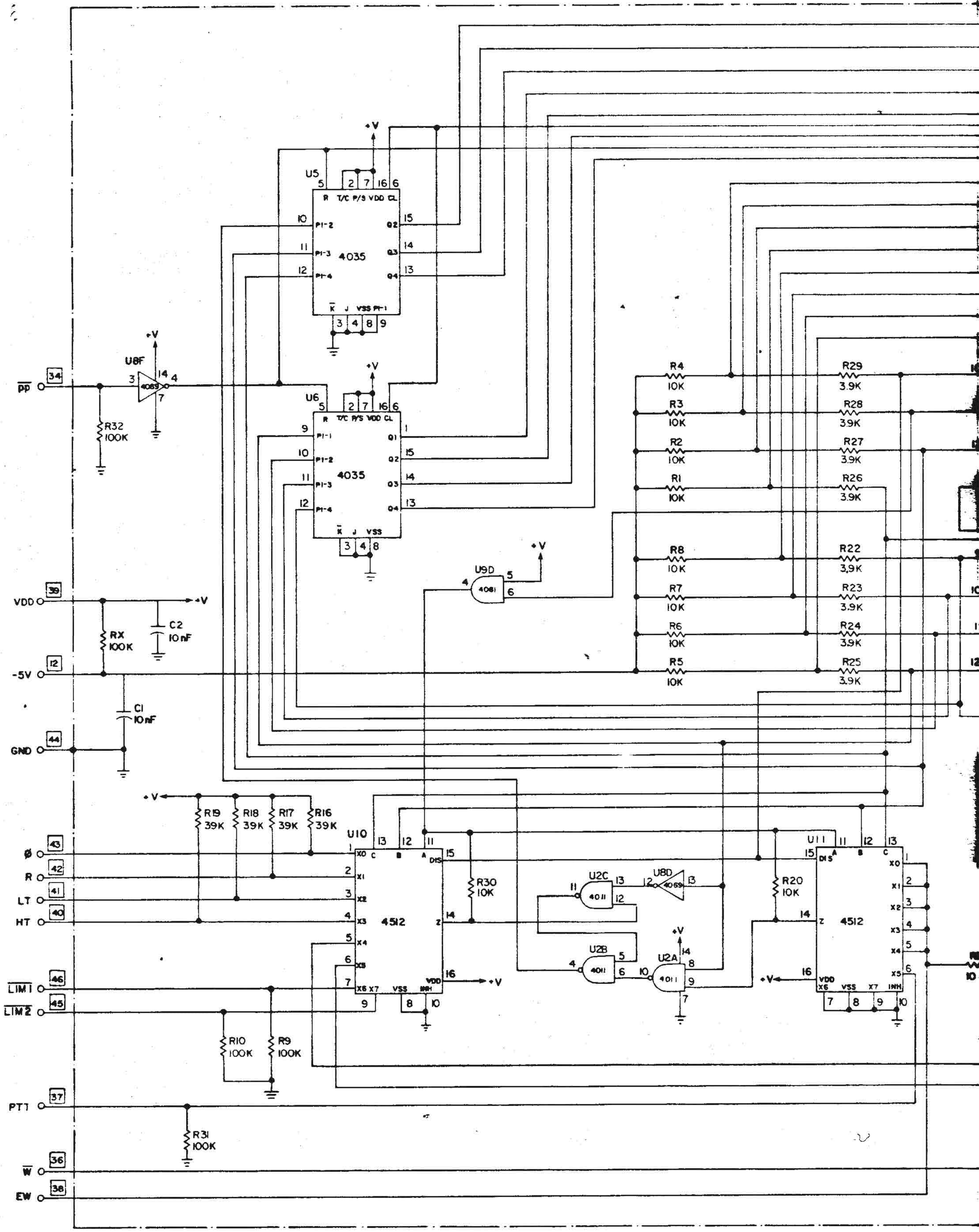
(d) State clock control. The state clock is obtained by dividing by 2 the frequency of the $\overline{SHC}$ clock signal in flip-flop U3B. The state clock appearing at pin 13 of U3B is combined with the original clock signal in gate U1D. The signal appearing at the output of U1D is termed the command clock, because it assumes a high level during command cycles. The output signal appearing at pin 12 of U3B is termed the address clock because it rises to a high level during address cycles.
The high level normally existing at the output of U8B (see (a) above) holds U3B in the reset state, therefore the state clock signal is not available until the end of the PP* pulse (when the output of U8B falls to a low level).

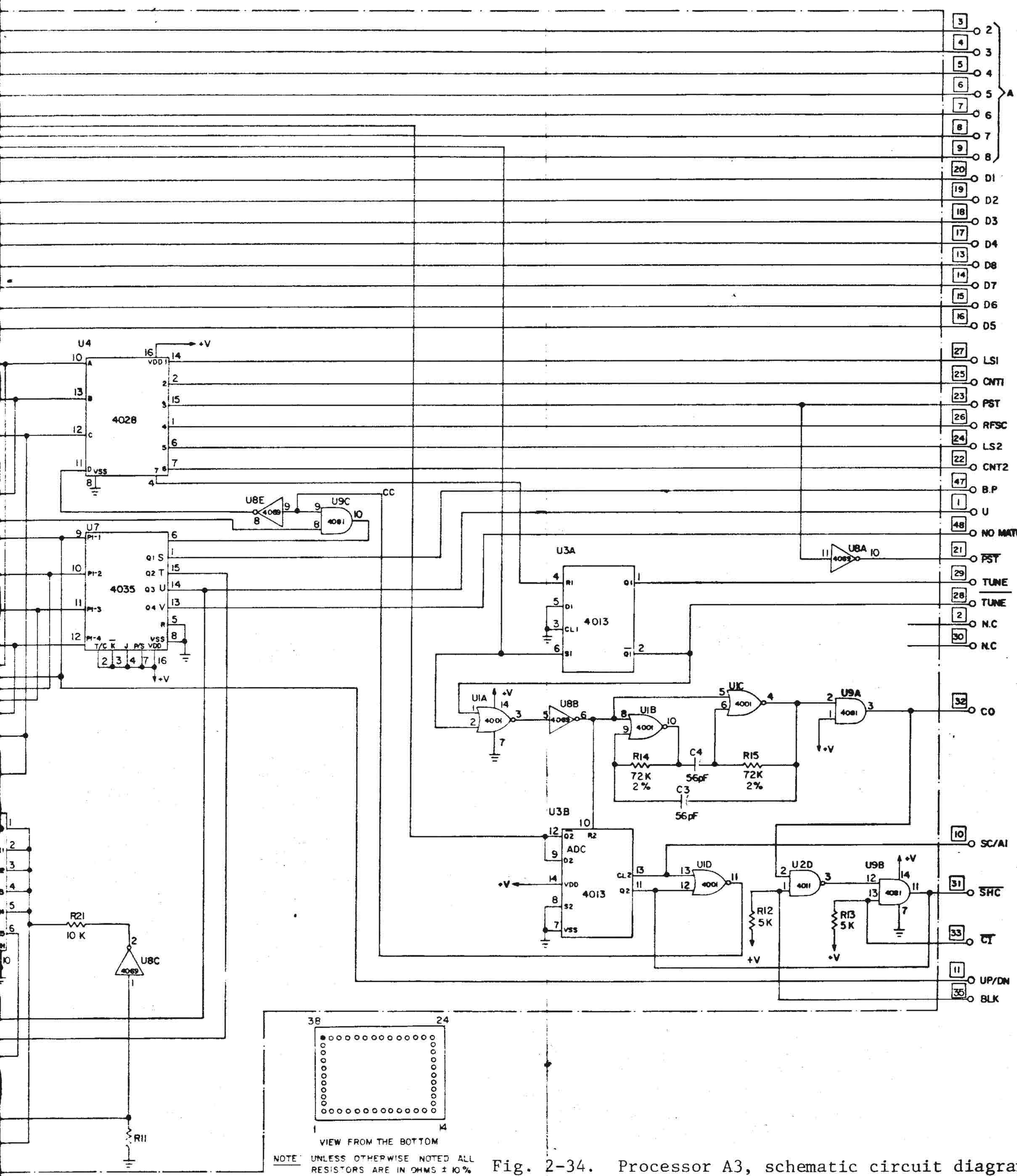
(2) Command decoder. When the command clock is at a high level, the output of U8E assumes a low level. This level is applied to the most significant bit (MSB) input of the command decoder, U4. U4 is an 1-of-10 decoder, which is used as an 1-of-8 decoder, with the MSB input (pin 11) serving as a disable input. When the MSB=0 (low input level), a high level appears at the output whose number equals the binary value of the word appearing on the DB1, DB2 and DB3 data bus lines; the other outputs remain at low levels. When the MSB=1 (high input level), all seven outputs of U4 assume low levels.

The outputs of U4 are designated LS1, CNT1, PST, RFSC, LS2 and CNT2; the seventh U4 output is used to reset U3A when the matching process ends.

(3) State latch. The state latch, U7, is a synchronous parallel-in, parallel-out shift register. The data appearing on the DB5-DB8 lines is clocked into U7 and appears at its outputs when the command clock rises to a high level, provided that line DB4 is at a high level.

(4) Input selector and associated circuits. The sensor output lines arriving from module SNF 1A5A3, the


U5
U6
4035
U8F
4069
U9D
4081
U10
U11
4512
U2C
4011
U8D
U2B
U2A
R4 10K
R3 10K
R2 10K
R1 10K
R8 10K
R7 10K
R6 10K
R5 10K
R29 3.9K
R28 3.9K
R27 3.9K
R26 3.9K
R22 3,9K
R23 3.9K
R24 3.9K
R25 3.9K
R32 100K
RX 100K
C2 10nF
C1 10nF
R19 39K
R18 39K
R17 39K
R16 39K
R30 10K
R20 10K
R10 100K
R9 100K
R31 100K
+V
VDD
-5V
GND
PP
Ø
R
LT
HT
LIM1
LIM2
PT1
W
EW



NOTE: UNLESS OTHERWISE NOTED ALL RESISTORS ARE IN OHMS ± 10%

Fig. 2-34. Processor A3, schematic circuit diagram

$\overline{LIM1}$ and $\overline{LIM2}$ lines from microelectronic modules A1 and A2, and the T and U lines from the state latch are applied to an eight-input multiplexer, U10. The multiplexer connects the input line whose number equals the binary value of the word appearing on the DB2-DB4 data bus line's to the output (pin 14). The multiplexer output is enabled only when the DB1 line assumes a low level. When the DB1 line assumes a high level, the output impedance becomes very high, and then the DB2 data bus line is effectively connected via R30 to pin 12 of U2C.

A second multiplexer, U11, is used to sample the PTT LORD and $\overline{W}$ lines; its output is similarly controlled by the DB2 line. Pin 14 of U11 is connected to pin 9 of U2A. U8D, U2A, U2B and U2C form a selector circuit, which operates as a single pole, double-throw switch controlled by the DB5 data bus line. When the DB5 line falls to a low level, the output signal of U11 appears at the output of U2B; when the DB5 line rises to a high level, the output signal of U11 appears at the output of U2B.

(5) Address decoder. The address decoder is composed of two identical synchronous parallel-in-parallel-out registers, U5 and U6. The registers are clocked by the address clock. When the address clock rises to a high level, the data appearing on the DB2-DB8 data bus line and the output signal of U2B are applied on the address bus. The output of U2B serves as the MSB address line. The address bus is connected to the EPROM address port.

(6) Logic truth tables. The truth tables given below complement the information presented in para a. thru e. above.

Table 2-1. Command Decoder Outputs as a Function of DB1-DB3 Data Bus Lines

DB1 (LSB)	DB2	DB3 (MSB)	LS1	CNT1	PST	RFSC	LS2	CNT2	$\overline{PST}$
0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	1
0	1	0	0	1	0	0	0	0	1
1	1	0	0	0	1	0	0	0	0
0	0	1	0	0	0	1	0	0	1
1	0	1	0	0	0	0	1	0	1
0	1	1	0	0	0	0	0	1	1

Table 2-2. State Latch Outputs as a Function of DB5-DB8 Lines (Following Low-to-High Transition on DB4)

DB5	DB6	DB7	DB8	BP	U	NM
1 0	1 0	1 0	1 0	1 0	1 0	1 0

Table 2-3. Address Decoder-Partial Truth Table

NOTE: Correct data appears at A3-A8 outputs, two $\overline{SHC}$ clock pulses later.

DB3	DB4	DB5	DB6	DB7	DB8	A3	A4	A5	A6	A7	A8
0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1	1	1

Table 2-4. Input Selector and Address Decoder Truth Table - Part I.

NOTES:

1. Correct data appears at A3-A8 outputs, two $\overline{SHC}$ clock pulses later.
2. When DB1=1, outputs assume high-impedance state.

DB5	DB4	DB3	DB2	$\overline{LIM2}$	$\overline{LIM1}$	HT	LT	R	Φ	A2
0	0	0	0	*	*	*	*	*	1	1
0	0	0	0	*	*	*	*	*	0	0
0	0	0	1	*	*	*	*	1	*	1
0	0	0	1	*	*	*	*	0	*	0
0	0	1	0	*	*	*	1	*	*	1
0	0	1	0	*	*	*	0	*	*	0
0	0	1	1	*	*	1	*	*	*	1
0	0	1	1	*	*	0	*	*	*	0
0	1	0	0	*	*	*	*	*	*	1
0	1	0	1	*	*	*	*	*	*	1
0	1	1	0	*	1	*	*	*	*	1
0	1	1	0	*	0	*	*	*	*	0
0	1	1	1	1	*	*	*	*	*	1
0	1	1	1	0	*	*	*	*	*	0

* - "Don't care" condition

Table 2-4. Input Selector and Address Decoder Truth Table - Part II.

NOTE

When DB1=1, outputs assume high-impedance state.

DB5	DB4 (MSB)	DB3	DB2 (LSB)	$\overline{W}$	OTT	$\overline{EW}$	A2
1	0	0	0	*	*	1	1
1	0	0	*	*	*	0	0
1	0	1	0	0	*	+	1
1	1	0	0	1	*	+	0
1	1	0	1	*	1	*	1
1	1	0	1	*	0	*	0

* - "Don't care" condition + - Open-circuit condition

g. Timer Microelectronic Module A4 (fig. 2-35, 2-36, 2-37, 2-38). Refer to fig. 2-35 for the functional designations of the various circuits. Refer to para. c. for block diagram analysis.

(1) SF pulse generation (fig. 2-37). The SF pulse is generated by the monostable multivibrator U7, when triggered by the high level pulse appearing at the output of U2D when the output level of U2C changes. The output level of U2C depends only on the output level of U2B, because both U2A inputs are internally connected to ground (via resistors).
Normally, the output of U2B is low; it rises to a high level in either of the following cases:

(a) At turn-on, the collector voltage of transistor Q1 (in the supply voltage monitor) remains at a high level, until capacitor C1 charges to a sufficiently high voltage; then Q1 saturates and its collector voltage falls to a low level. The output level of U2B follows the collector voltage of Q2.

(b) When the frequency is changed, a low level pulse appears on the TRANSIT line. Assuming that the pulse appears after the collector voltage of Q1 falled to a low level, the TRANSIT pulse causes a similar pulse to appear at the output of U2B.
The duration of the SF pulse is 200 to 350 msec.

(2) $\overline{PP}$ pulse generation (fig. 2-37). The $\overline{PP}$ pulse appears at the output of U1C in the following cases:

(a) The PTT LORD line rises to a high level and triggers the monostable multivibrator U12A. The multivibrator provides a 20-to-30 microsecond high level pulse, which is then inverted by U1C, and applied on the PP* line.

(b) When a SF pulse is generated. The SF pulse is inverted by U1C and the resulting low level pulse is applied on the $\overline{PP}$ line.

(3) RFS, EN CONT and W pulse generation. The RFS, EN CONT and $\overline{W}$ pulses are generated by a multivibrator chain, comprised of U12B, U6 and U5, and gates U8A, U8B, U8C and U8D. The first multivibrator, U12B, is reset when a $\overline{PP}$ pulse is generated. The multivibrator chain is triggered by the rising edge of the RFSC signal, arriving from the processor A3.

Fig. 2-37 shows the pulse timing diagram.

(4) Range shifting control circuit.

(a) The two-bit DL21,DL22 control code provided by the decoder A2 is applied to the preset inputs of the four-bit binary up/down counter, U11. The preset information is loaded into the counter on the rising edge of the LS2 pulse provided by the processor A3. After the LS2 pulse ends, the counter starts to count down at the rate of the $\overline{SHC}$ clock provided by the processor A3. The $\overline{SHC}$ clock reaches the clock input (pin 15) of U11 through U1D. When the count of 0000 is reached, the terminal count output of U11 (pin 7) falls to a low level. The output of U1A then rises to a high level and U1D blocks the transfer of the $\overline{SHC}$ clock.
The number of $\overline{SHC}$ clock pulse which pass U1D is therefore equal to the numerical value of the DL21, DL22 code applied to U11.

(b) The four-bit binary up/down counters U9 and U10 are connected in cascade. The counters are preset to 1100000 when the processor A3 sends a PST pulse. The counters count up when a high level is applied by the processor A3 on the UD/DN line, and count down for a low level. The counters count the CNT2 pulses, sent by the processor A3. The binary codes appearing at the counter outputs are applied to the parallel inputs of the U3 and U4 shift registers.
The relative timing of the $\overline{SHC}$, LS2 and CNT2 pulses is shown in fig. 2-38.

(c) The shift registers U3 and U4 are reset to zero when the PST pulse appears. The registers are loaded with the output word of the counters U9 and U10 each time a LS2 pulse is received. After the LS2 pulse ends, the information loaded into the registers is shifted, according to the number of clock pulses passing through U1D (see (a) above). Therefore, the binary word put out by the counters U9 and U10 is shifted across U3 and U4 outputs, by a number equal to the binary value of the code sent by the decoder A2. This permits to use only five out of the eight possible X2 components.

(d) The most significant bit of the counter formed by U9 and U10 (pin 14 of U10) is applied on the $\overline{LIM2}$ line, to notify the processor A3 that all X2 components have already been inserted into the circuit.

(e) The Q2-output of U10 controls the KLC relay in module MN 1A5A1, via the TLC line.

(f) Tables 2-7 and 2-8 present the truth table of the X2 range shifting control. The following definitions are used:

1. "B" is a binary word consisting of the L21 to L28 bits, where L28 is MSB and L21 is LSB as shown below:

B = $\underline{L28}$,L27,L26,L25,L24,L23,L22,$\underline{L21}$
MSB.....LSB

2. "C" is one group of pulses, as defined in fig. 2-38. To obtain the results shown in the tables, a high level pulse must be applied on the PST line before and after each pulse group.

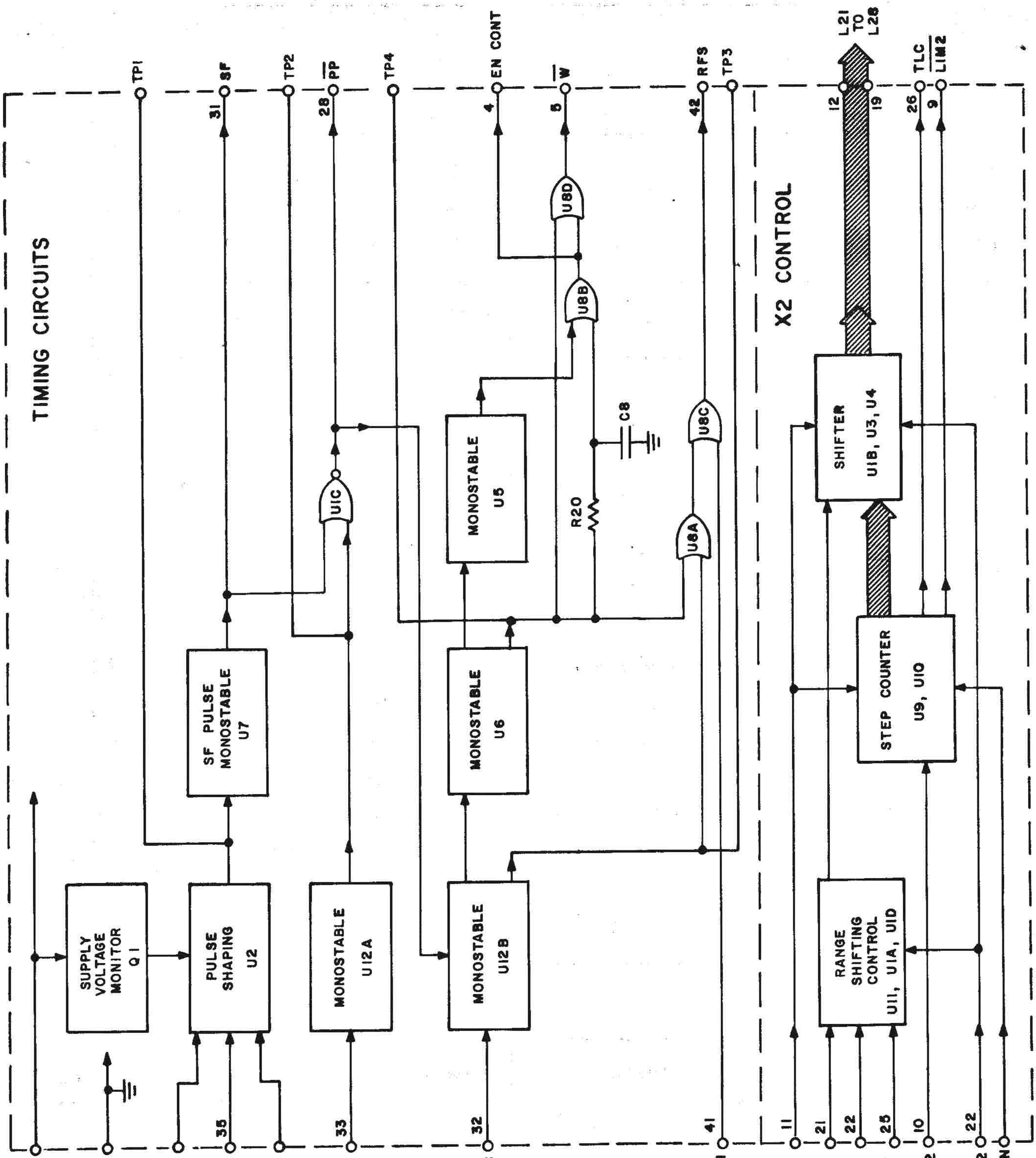


Fig. 2-35. Timer A4, block diagram

Table 2-5. X2 Range Shifting Control Truth Table - UP/DN Line at High Level

NUMBER OF C GROUPS	DL21	DL22	B COUNTS UP		TLC	$\overline{\text{LIM2}}$
			FROM	TO		
0-31	0	0	0 0 0 0 0 0 0 0	0 0 0 1 1 1 1 1	1	1
32-33	0	0	0 0 0 1 1 1 1 1	1 1 1 0 0 0 0 0	0	0
0-31	1	0	0 0 0 0 0 0 0 0	0 0 1 1 1 1 1 0	1	1
0-31	0	1	0 0 0 0 0 0 0 0	0 1 1 1 1 1 0 0	1	1
0-31	1	1	0 0 0 0 0 0 0 0	1 1 1 1 1 0 0 0	1	1

Table 2-6. X2 Range Shifting Control Truth Table - UP/DN Line at Low Level

NUMBER OF C GROUPS	DL21	DL22	B COUNTS DOWN		TLC	$\overline{\text{LIM2}}$
			FROM	TO		
0-31	0	0	1 1 1 1 1 1 1 1	1 1 1 0 0 0 0 0	0	1
31-32	0	0	1 1 1 0 0 0 0 0	0 0 0 1 1 1 1 1	1	0
0-31	1	0	1 1 1 1 1 1 1 1	1 1 0 0 0 0 0 1	0	1
0-31	0	1	1 1 1 1 1 1 1 1	1 0 0 0 0 0 1 1	0	1
0-31	1	1	1 1 1 1 1 1 1 1	0 0 0 0 0 1 1 1	0	1

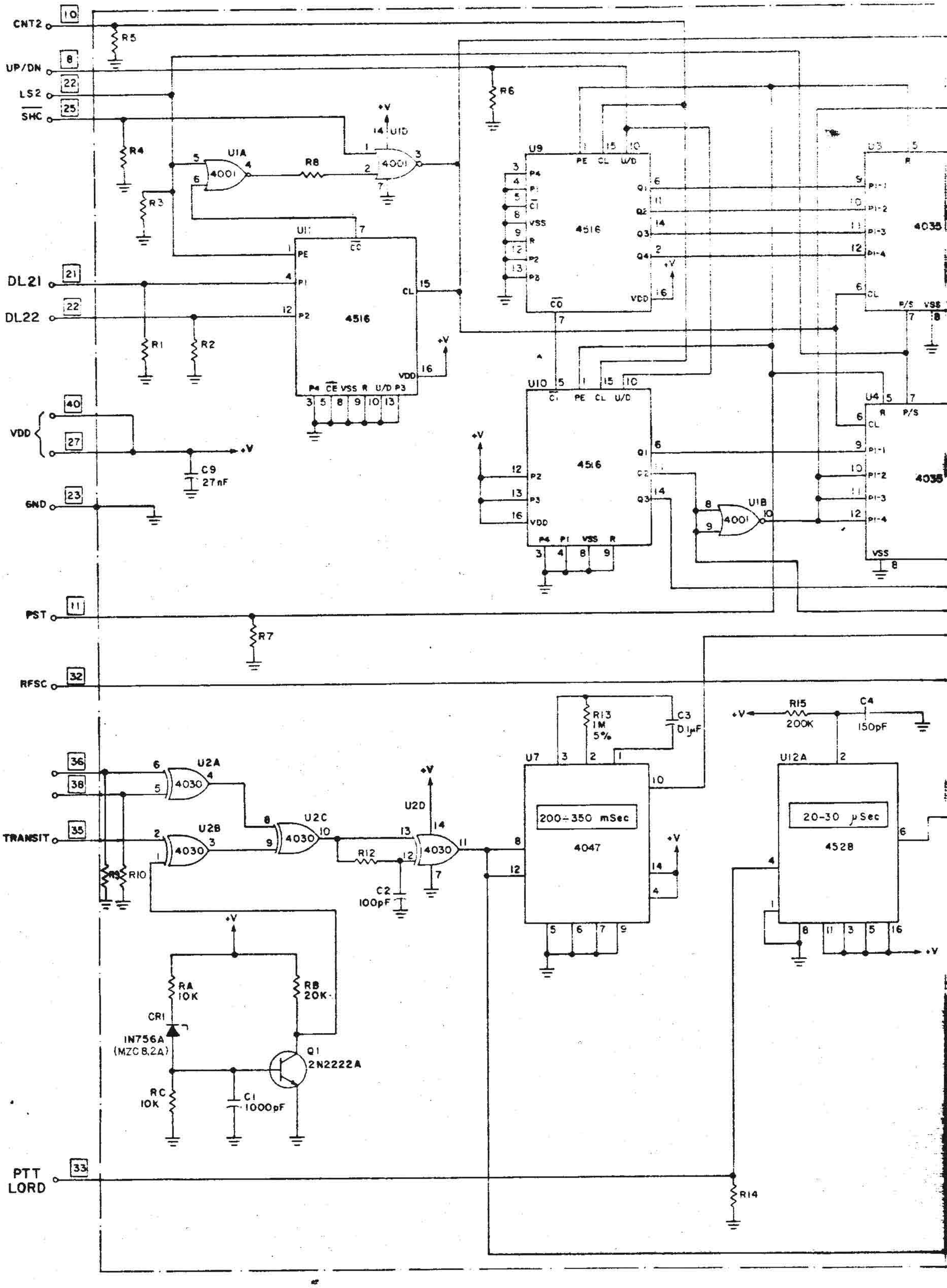
h. Decoder A2 (fig. 2-39). Refer to para c. for block diagram analysis.

(1) Decoder operation. The decoder A2 contains a custom LSI circuit, which decodes the frequency data. The decoder is activated when the TUNE line rises to a high level.

(a) The frequency data applied to the decoder inputs is used to generate a three-bit frequency band code, F6, F7 and F8. Table 2-10 below gives the decoder truth table. In Table 2-10, "B" is a binary word, consisting of the following bits: X61, X60, X53, X52, X51, X43 and X42. X61 is the MSB, and X42 is the LSB:

B = $\overline{\text{X61}}$ X60 X53 X52 X51 X50 X43 $\overline{\text{X42}}$

$\overline{\text{MSB}}$.....$\overline{\text{LSB}}$


CNT2
10
R5
UP/DN
8
LS2
22
SHC
25
R4
R3
U1A
4001
R8
U1D
4001
+V
14
R6
U9
4516
PE CL U/D
P4 P1 CI VSS R P2 P3
Q1 Q2 Q3 Q4
VDD
CO
U3
4035
P1-1 P1-2 P1-3 P1-4
P/S VSS
CL
U11
4516
PE CO
P1 P2
CL
VDD
P4 CE VSS R U/D P3
DL21
21
DL22
22
R1
R2
U10
4516
P2 P3 P4 P1 VSS R
VDD
U4
4035
U1B
4001
40
VDD
27
C9
27nF
23
GND
11
PST
R7
32
RFSC
36
38
35
TRANSIT
U2A
U2B
U2C
U2D
4030
R9
R10
R12
C2
100pF
U7
4047
200-350 mSec
R13
1M
5%
C3
0.1μF
U12A
4528
20-30 μSec
R15
200K
C4
150pF
RA
10K
RB
20K
CR1
IN756A
(MZC 8.2A)
Q1
2N2222A
RC
10K
C1
1000pF
33
PTT
LORD
R14

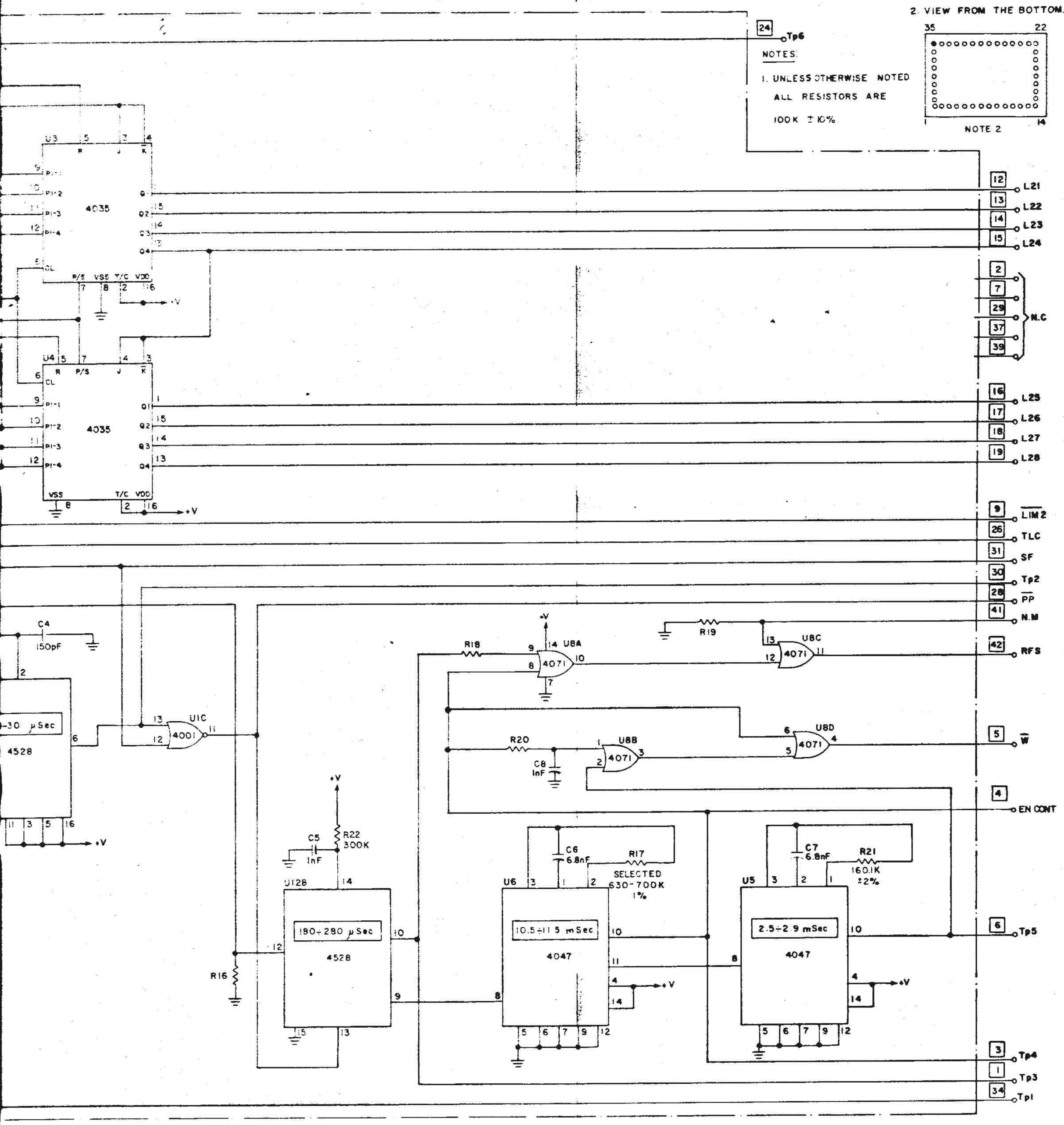


Fig. 2-36. Timer A4, schematic circuit diagram

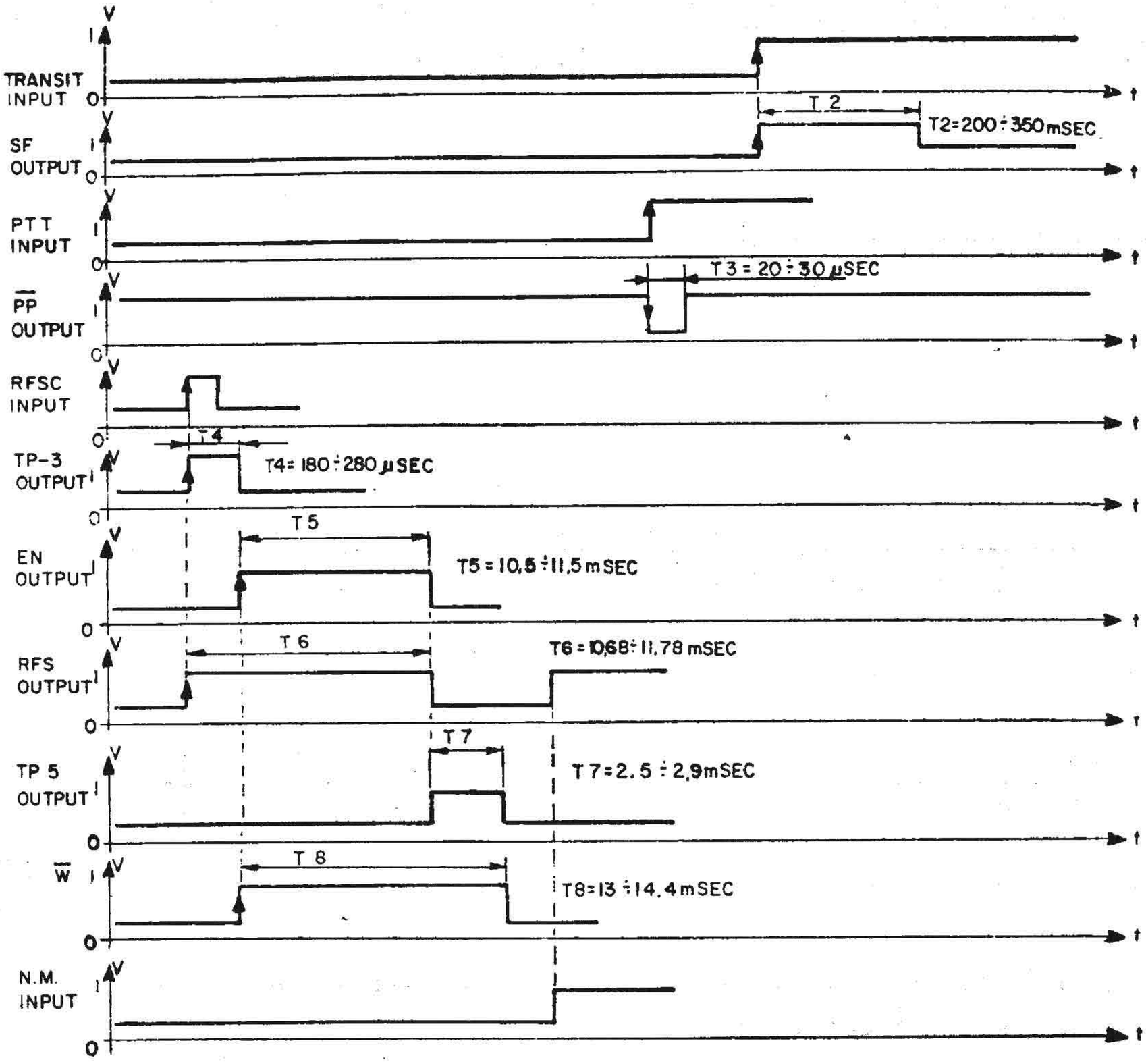
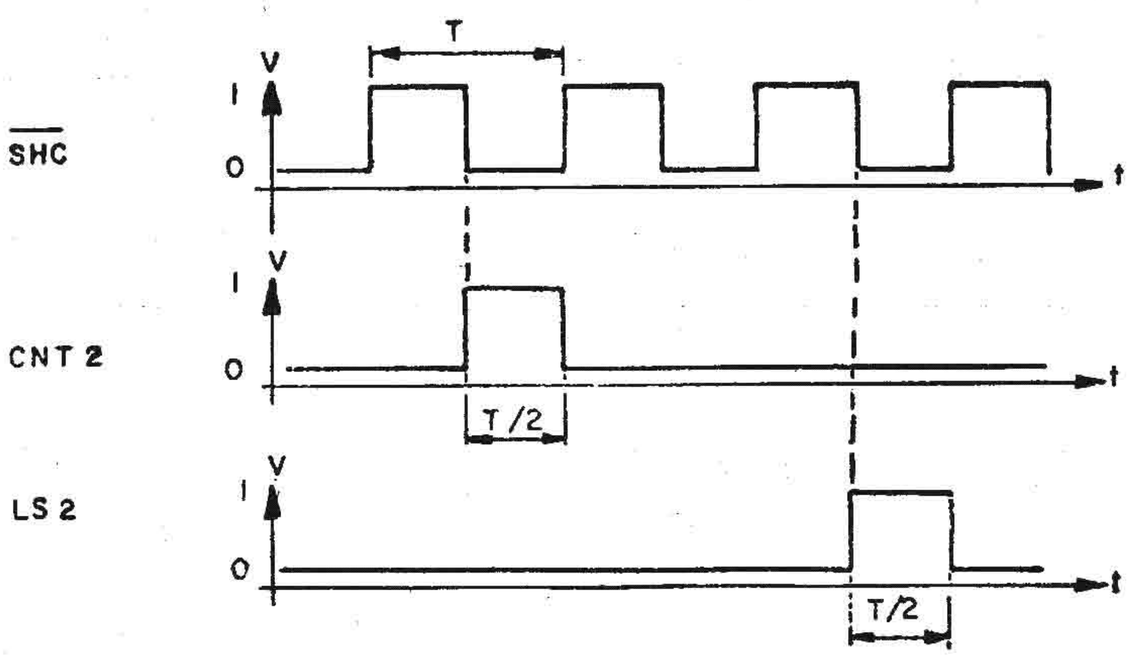


Fig. 2-37. Timer A4, output signals timing diagram



T = 5-7µSEC 40% TO 60% DUTY CYCLE

Fig. 2-38. Relative timing os SCH*,LS2 and CNT2 signals

Table 2-7. F6, F7, F8 Truth Table

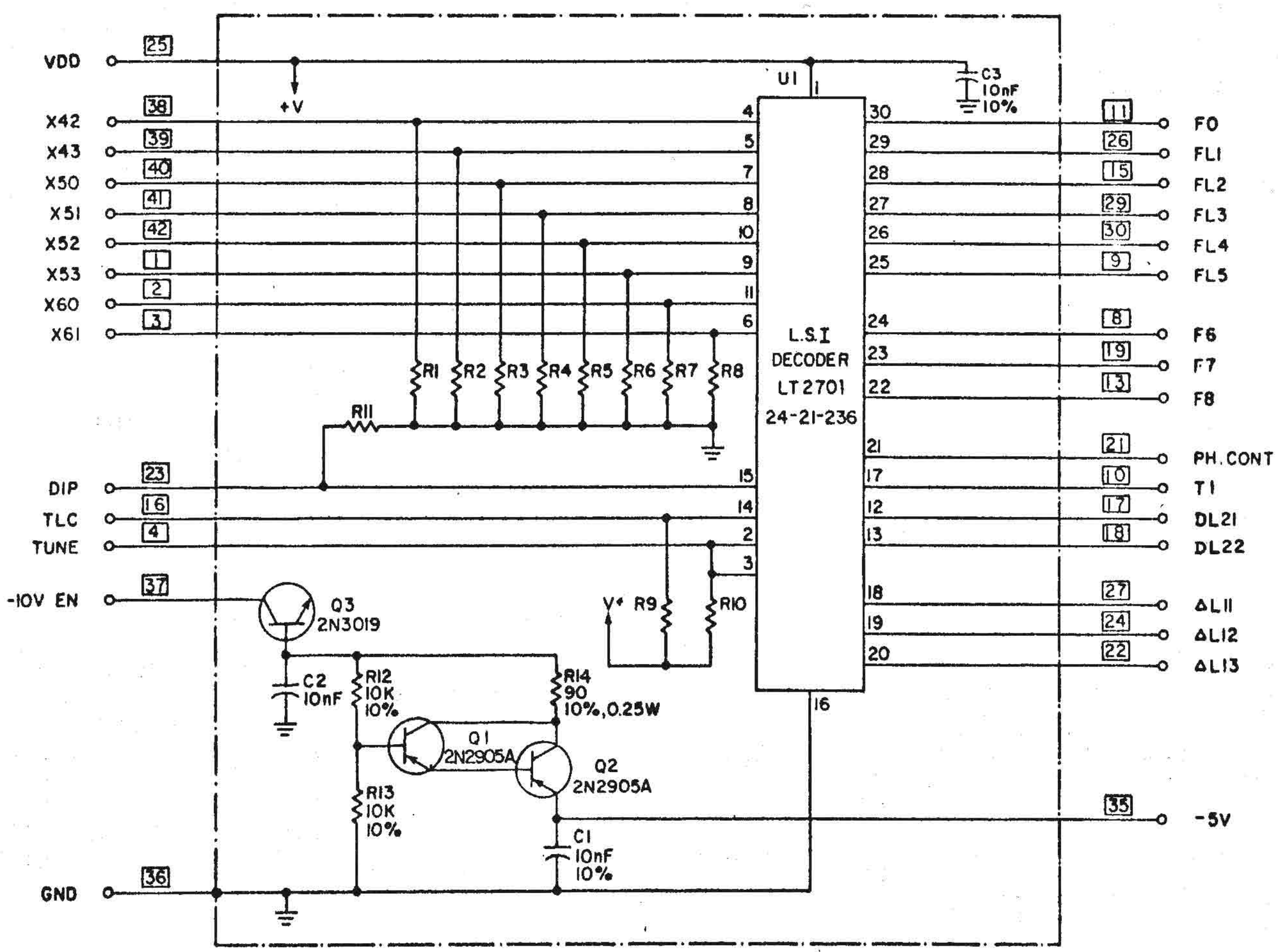
"B" INPUT CHANGES																OUTPUTS		
FROM								TO								F8	F7	F6
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
0	0	0	0	1	0	0	1	0	0	0	0	1	1	0	0	0	0	1
0	0	0	0	1	1	0	1	0	0	0	1	0	0	0	1	0	1	0
0	0	0	1	0	0	1	0	0	0	0	1	1	0	1	0	0	1	1
0	0	0	1	1	1	0	0	0	0	1	0	0	1	1	0	1	0	0
0	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	0	1
0	1	0	1	0	0	0	1	1	0	0	0	0	0	1	0	1	1	0
1	0	0	0	0	1	0	0	1	0	1	0	0	1	1	0	1	1	1

(b) The decoder also provides a control signal, designated PH CONT, for the phase detector selection relay in module SNF 1A5A2. Table 2-8 gives the PH CONT truth table.

Table 2-8. Truth Table for PH CONT Line

"B" INPUT CHANGES																$\overline{\text{TUNE}}$	PH CONT
FROM								TO									
0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0
0	1	0	0	0	0	0	0	1	0	1	0	0	1	1	0	0	1
0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0
0	1	0	0	0	0	0	0	1	0	1	0	0	1	1	0	1	0

(c) The decoder sends a two-bit code to the X2 range shifting control in microelectronic module A4. Table 2-9 gives the truth table for this code.



NOTES:

1. UNLESS OTHERWISE NOTED ALL RESISTORS ARE 100K $^{+30\%}_{-10\%}$
2. VIEW FROM THE BOTTOM.

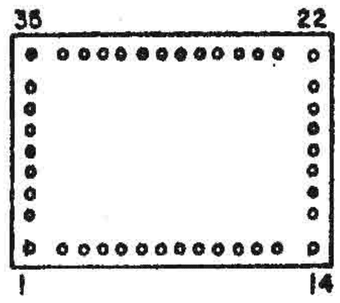


Fig. 2-39. Decoder A2, schematic circuit diagram

Table 2-9. DL21, DL22 Truth Table

"B" INPUT CHANGES																TLC	OUTPUTS	
FROM								TO									DL21	DL22
0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1
0	0	0	0	1	1	0	1	0	0	0	1	1	0	1	0	0	1	0
0	0	0	1	1	1	0	0	0	1	0	1	0	0	0	0	1	0	1
0	0	0	1	1	1	0	0	0	1	0	1	0	0	0	0	0	1	0
0	1	0	1	0	0	0	1	1	0	1	0	0	1	1	0	0	1	1
0	1	0	1	0	0	0	1	1	0	1	0	0	1	1	0	1	0	0

(d) The decoder provides control lines (FL1 through FL5) to the bandpass filters in module SNF 1A5A3, and an out-of-range output, FL0 (FO UNLOCK). Table 2-10 presents their truth table.

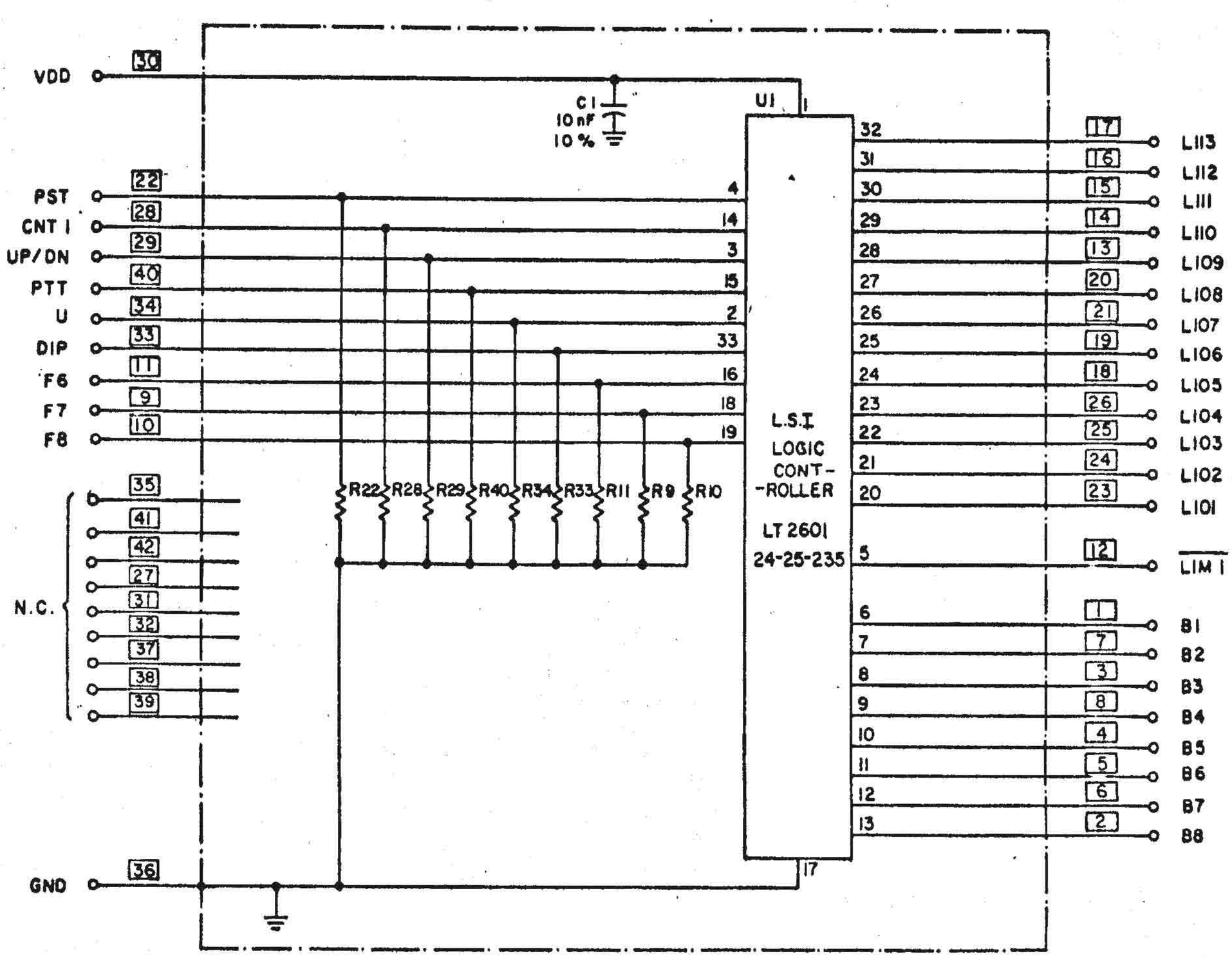
Table 2-10. FL0-FL5 Truth Table

"B" INPUT CHANGES																OUTPUTS					
FROM								TO								FL0	FL1	FL2	FL3	FL4	FL5
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	0	0	0
0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0
0	0	0	0	1	1	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0
0	0	0	0	1	1	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0
0	0	0	1	0	1	0	0	0	0	0	1	1	1	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0	1	0
0	1	0	0	1	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	1

(2) -5V EPROM regulator. The decoder A2 contains a regulator which reduces the -10V EN voltage to -5V. The -5V is used by the EPROM and the level shifter circuit in the processor A3. The regulator is comprised of Q1, Q2 and Q3.

h. Logic Controller A1 (fig. 2-40). Refer to para. c. for block diagram analysis.

(1) The operation of the logic controller is described by the truth tables given in Tables 2-11 through 2-13.



NOTE :

1. UNLESS OTHERWISE NOTED ALL RESISTORS ARE 100K $\pm^{30}_{10}$ %.

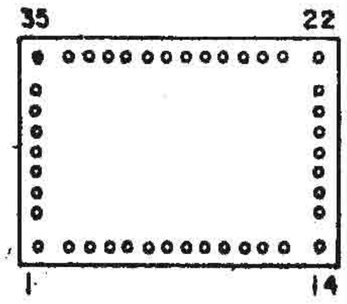


Fig. 2-40. Logic controller A1, schematic circuit diagram

Table 2-11. B1-B8 Lines Truth Table

F8	F7	F6	B1	B2	B3	B4	B5	B6	B7	B8
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Table 2-12. L101 and LIM1 Truth Table
(Following Low-to-high Transition on PST Line)

NOTE: L is a binary word consisting of the following bits:
$\underline{L113}$, L112, ...$\underline{L101}$
MSB .....LSB

F8	F7	F6	PTT LORD	DIP	U	UP/DN	L	$\overline{LIM1}$
0	0	0	0	0	0	0	1101100100000	1
0	0	1	0	0	0	0	0100110100000	1
0	1	0	0	0	0	0	0001111001000	1
0	1	1	0	0	0	0	0000101100100	1
1	0	0	0	0	0	0	0000001111001	1
1	0	1	0	0	0	0	0000001011001	1
1	1	0	0	0	0	0	0000000001001	1
1	1	1	0	0	0	0	0000000001001	1
0	0	0	1	0	0	0	0101100000000	1
0	0	1	1	0	0	0	0000100000000	1
0	1	0	1	0	0	0	0000101000000	1
0	1	1	1	0	0	0	0000001100000	1
1	0	0	1	0	0	0	0000000110000	1
1	0	1	1	0	0	0	0000000011000	1
1	1	0	1	0	0	0	0000000000000	1
1	1	1	1	0	0	0	0000000000000	1
*	*	*	*	1	0	0	0000000000000	1
*	*	*	*	0	1	1	0000000000000	1

* - "Don't care" condition

Table 2-13. Dynamic Operation Table

F6	F7	F8	DIP	UP/DN	BINARY WORD	DIRECTION	FINAL STATE	$\overline{\text{LIM1}}$ FINAL STATE
0	0	1	0	1	E	UP	ALL ONES	0
0	0	1	0	0	E	DOWN	ALL ZEROS	1
0	1	0	0	1	D	UP	ALL ONES	0
0	1	0	0	0	D	DOWN	ALL ZEROS	1
0	1	1	0	1	C	UP	ALL ONES	0
0	1	1	0	0	C	DOWN	ALL ZEROS	1
1	0	0	0	1	A	UP	ALL ONES	0
1	0	0	0	0	A	DOWN	ALL ZEROS	1
0	0	1	1	1	B	UP	ALL ONES	0
0	0	1	0	0	B	DOWN	ALL ZEROS	1
0	1	0	0	1	B	UP	ALL ONES	0
0	1	0	0	0	B	DOWN	ALL ZEROS	1
0	1	1	1	1	A	UP	ALL ONES	0
0	1	1	0	0	A	DOWN	ALL ZEROS	1

NOTES: 1. A,B,C,D, and E are binary words, defined as follows:

A = L101, L102, L103, L104, L105, L106, L107, L108
B = L102, L103, L104, L105, L106, L107, L108, L109
C = L103, L104, L105, L106, L107, L108, L109, L110
D = L104, L105, L106, L107, L108, L109, L110, L111
E = L106, L107, L108, L109, L110, L111, L112, L113

2. After a low-to-high transition on the PST input line, the binary words A-E shall change by 1 for each pulse applied to the CNT1 line. The direction of change and the final value are defined in the table.

Table 2-14. LORD 1A5A2 Interconnection Table

No.	A1	A2	A3	A4	Type (Note 4)	A5	A6	A7	MN	(DC)	MB	TEST	Function	Notes
				36,		RD1	RD2	RD3	J1	J2	J3	J4		
1	36	36	44	23,38		9.24	9	9.24		x	k	A	GND	
2	33	23	-	-	A	28					g	-	D I P	
3	-	-	-	-	B	30				S	-	-	D I P-A	KW/D
4	-	-	-	-	C	31				U	-	-	D I P-B	NOTE 1
5	31	-	21	-	-	-	-	-	-	-	-	-	$\overline{\text{PST}}$	
6	34	-	1	-	-	-	-	-	-	-	-	-	U	
7	32	-	31	25	-	-	-	-	-	-	-	-	$\overline{\text{SHC}}$	

Table 2-14. LORD 1A5A2 Interconnection Table

No.	A1	A2	A3	A4	Type (Note 4)	A5 RD1	A6 RD2	A7 RD3	MN J1	(DC) J2	MB J3	TEST J4	Function	Notes
8	40	-	37	33	-	-	-	-	-	-	m,e	-	PTT LORD	
9	12	-	46	-	-	-	-	-	-	-	-	-	$\overline{\text{lim 1}}$	
10	29	-	11	8	-	-	-	-	-	-	-	-	UP/DN	
11	22	-	23	11	-	-	-	-	-	-	-	-	P S T	
12	13	-	-	-	A	14	-	-	-	-	-	-	L 109	K1-5
13	-	-	-	-	B	12	-	-	K	-	-	-	L 109-A	
14	-	-	-	-	C	11				J	-	-	L 109-B	
15	14	-	-	-	A	7	-	-	-	-	-	-	L 110	K1-4
16	-	-	-	-	B	6	-	-	Z	-	-	-	L 110-A	
17	-	-	-	-	C	4		-	X	-	-	-	L 110-B	
18	15	-	-	-	A	41	-	-	-	-	-	-	L 111	K1-3
19	-	-	-	-	B	40	-	-	-	Y	-	-	L 111-A	
20	-	-	-	-	C	39	-	-	-	W	-	-	L 111-B	
21	16	-	-	-	A		-	17	-	-	-	-	L 112	K1-2
22	-	-	-	-	B		-	18	T	-	-	-	L 112-A	
23	17	-	-	-	A		-	19	-	-	-	-	L 113	K1-1
24	-	-	-	-	B		-	20	V	-	-	-	L 113-A	
25	18	-	-	-	A	38	-	-	-	-	-	-	L 105	K1-9
26	-	-	-	-	B	37	-	-	-	L	-	-	L 105-A	
27	-	-	-	-	C	36	-	-	-	G	-	-	L 105-B	
28	19	-	-	-	A	32	-	-	-	-	-	-	L 106	K1-8
29	-	-	-	-	B	33	-	-	P	-	-	-	L 106-A	
30	-	-	-	-	C	35	-	-	-	E	-	-	L 106-B	
31	27	-	27	-	-	-	-	-	-	-	-	-	L S I	

Table 2-14. LORD 1A5A2 Interconnection Table (Cont'd.)

No.	A1	A2	A3	A4	Type (Note 4)	A5	A6	A7	MN	(DC)	MB	TEST	Function	Notes
				36,		RD1	RD2	RD3	J1	J2	J3	J4		
1	36	36	44	23,38		9.24	9	9.24		x	k	A	GND	
32	21	-	-	-	A	-	-	7	-	-	-	-	L 107	
33	-	-	-	-	B	-	-	6	-	C	-	-	L 107-A	K1-7
34	-	-	-	-	C	-	-	4	-	A	-	-	L 107-B	
35	20	-	-	-	A	-	-	14	-	-	-	-	L 108	
36	-	-	-	-	B	-	-	12	-	K	-	-	L 108-A	K1-6
37	-	-	-	-	C	-	-	11	-	I	-	-	L 108-B	
38	23	-	-	-	A	-	-	41	-	-	-	-	L 101	
39	-	-	-	-	B	-	-	40	-	F	-	-	L 101-A	K1-13
40	-	-	-	-	C	-	-	39	-	H	-	-	L 101-B	
41	24	-	-	-	A	-	-	28	-	-	-	-	L 102	
42	-	-	-	-	B	-	-	30	W	-	-	-	L 102-A	K1-12
43	-	-	-	-	C	-	-	31	N	-	-	-	L 102-B	
44	25	-	-	-	A	-	-	3	-	-	-	-	L 103	
45	-	-	-	-	B	-	-	1	-	B	-	-	L 103-A	K1-11
46	-	-	-	-	C	-	-	42	-	D	-	-	L 103-B	
47	26	-	-	-	A	-	-	25	-	-	-	-	L 104	
48	-	-	-	-	B	-	-	26	d	-	-	-	L 104-A	K1-10
49	-	-	-	-	C	-	-	27	b	-	-	-	L 104-B	
50	28	-	25	-	-	-	-	-	-	-	-	-	CNT 1	
51	39	27	-	-	-	-	-	-	-	-	-	-	DL 11	
52	38	24	-	-	-	-	-	-	-	-	-	-	DL 12	
53	37	22	-	-	-	-	-	-	-	-	-	-	DL 13	
54	-	11	-	-	-	-	-	-	-	-	o	-	FO UNLOCK	
55	-	26	-	-	-	-	-	-	-	-	R	-	FL 1	
56	-	15	-	-	-	-	-	-	-	-	M	-	FL 2	
57	-	29	-	-	-	-	-	-	-	-	j	-	FL 3	
58	-	30	-	-	-	-	-	-	-	-	h	-	FL 4	
59	-	9	-	-	A'	-	-	15	-	-	-	-	FL 5	
60	-	-	-	-	B'	-	-	16	-	-	f	-	FL 5-A	
61	11	8	-	-	-	-	-	-	-	-	-	-	F 6	
62	9	19	-	-	-	-	-	-	-	-	-	-	F 7	
63	10	13	-	-	-	-	-	-	-	-	-	-	F 8	

Table 2-16. LORD 1A5A2 Interconnection Table (Cont'd.)

No.	A1	A2	A3	A4	PROM U1	Type Note	A5	A6	A7	MN	(DC)	MB	TEST	Function	Notes
				36,			RD1	RD2	RD3	J1	J2	J3	J4		
1	36	36	44	23,38		(4)	9.24	9	9.24		x	k	A	GND	
64	1	-	-	-		A'	15	-	-	-	-	-	-	B 1	
65	-	-	-	-		B'	16	-	-	-	R	-	-	B 1-A	KB-1
66	7	-	-	-		A'	-	19	-	-	-	-	-	B 2	
67	-	-	-	-		B'	-	20	-	M	-	-	-	B 2-A	KB-2
68	3	-	-	-		A'	19	-	-	-	-	-	-	B 3	
69	-	-	-	-		B'	20	-	-	-	V	-	-	B 3-A	KB-3
70	8	28	-	-		A'	-	21	-	-	-	-	-	B 4	
71	-	-	-	-		B'	-	22	-	0	-	-	-	B 4-A	KB-4
72	4	20	-	-		A'	21	-	-	-	-	-	-	B 5	
73	-	-	-	-		B'	22	-	-	-	M	-	-	B 5-A	KB-5
74	5	-	-	-		A'	-	15	-	-	-	-	-	B 6	
75	-	-	-	-		B'	-	16	-	S	-	-	-	B 6-A	KB-6
76	6	-	-	-		A'	-	17	-	-	-	-	-	B 7	
77	-	-	-	-		B'	-	18	-	Q	-	-	-	B 7-A	KB-7
78	2	-	-	-		A'	17	-	-	-	-	-	-	B 8	
79	-	-	-	-		B'	18	-	-	-	T	-	-	B 8-A	KB-8
80	30	25	39	27, 40	12,13 15,22 23	-	-	-	-	-	-	L	Q	+12V	NOTE 5/6
81	-	37	-	-	-	-	-	-	-	-	-	W	-	-10 VEN	
82	-	35	12	-	24	-	-	-	-	-	--	-	-	-5V	NOTE 6
83	-	-	-	4	-	-	-	-	-	-	-	F	-	EN, CONT	
84	-	-	-	-	-	-	8	8	8	D	-	P	-	VEN1	NOTE 2
85	-	-	-	-	-	-	10	10	10	B	-	A	-	VEN 2	
85a	30	25	-	-	-	-	-	-	-	-	-	-	-	VDD	NOTE 7
86	-	-	29	-	-	-	-	-	-	-	-	E	-	TUNE	
87	-	4	28	-	14,16	-	-	-	-	-	-	O	-	TUNE	
88	-	10	-	-	-	A	-	14	-	-	-	-	-	T'	
89	-	-	-	-	-	B	-	12	-	o	-	-	-	T' - A)	NOTE 2,3
90	-	-	-	-	-	C	-	11	-	n	-	-	-	T' - B)	
91	-	21	-	-	-	A'	-	-	21	-	-	-	-	PH CONT	
92	-	-	-	-	-	B'	-	-	22	-	-	I	-	PH-A	K-2
93	-	16	-	26	-	A	3	-	-	-	-	-	-	TLC	
94	-	-	-	-	-	B	1	-	-	-	N	-	-	TLC - A)	KL/C
95	-	-	-	-	-	C	42	-	-	-	P	-	-	TLC - B)	

Table 2-14. LORD 1A5A2 Interconnection Table (Cont'd.)

No.	A1	A2	A3	A4	PROM U1	Type (NOTE 4)	A5 RD1	A6 RD2	A7 RD3	MN J1	(DC) J2	MB J3	TEST J4	Function	Notes
1	36	36	44	36, 23,38			9.24	9	9.24		x	k	A	GND	
96	-	-	-	12	-	A	-	25	-	-	-	-	-	L 21	
97	-	-	-	-	-	B	-	26	-	A	-	-	-	L 21-A	K2-8
98	-	-	-	-	-	C	-	27	-	C	-	-	-	L 21-B	K2-8
99	-	-	-	13	-	A	25	-	-	-	-	-	-	L 22	
100	-	-	-	-	-	B	26	-	-	-	O	-	-	L 22-A	K2-7
101	-	-	-	-	-	C	27	-	-	-	Q	-	-	L 22-B	K2-7
102	-	-	-	14	-	A	-	-	38	-	-	-	-	L 23	
103	-	-	-	-	-	B	-	-	37	F	-	-	-	L 23-A	K2-6
104	-	-	-	-	-	C	-	-	36	R	-	-	-	L 23-B	K2-6
105	-	-	-	15	-	A	-	7	-	-	-	-	-	L 24	
106	-	-	-	-	-	B	-	6	-	Y	-	-	-	L 24-A	K2-5
107	-	-	-	-	-	C	-	4	-	L	-	-	-	L 24-B	K2-5
108	-	-	-	16	-	A	-	-	32	-	-	-	-	L 25	
109	-	-	-	-	-	B	-	-	33	I	-	-	-	L 25-A	K2-4
110	-	-	-	-	-	C	-	-	35	J	-	-	-	L 25-B	K2-4
111	-	-	-	17	-	A	-3	-	-	-	-	-	-	L 26	
112	-	-	-	-	-	B	-1	-	-	H	-	-	-	L 26-A	K2-3
113	-	-	-	-	-	C	42	-	-	f	-	-	-	L 26-B	K2-3
114	-	-	-	18	-	A	28	-	-	-	-	-	-	L 27	
115	-	-	-	-	-	B	30	-	-	a	-	-	-	L 27-A	K2-2
116	-	-	-	-	-	C	31	-	-	1	-	-	-	L 27-B	K2-2
117	-	-	-	19	-	A	32	-	-	-	-	-	-	L 28	
118	-	-	-	-	-	B	33	-	-	j	-	-	-	L 28-A	K2-1
119	-	-	-	-	-	C	35	-	-	G	-	-	-	L 28-B	K2-1
120	-	-	-	35	-	-	-	-	-	-	-	n	-	TRANSIT	
122	-	-	-	31	-		-	-	-	-	-	k	-	SF	
123	-	-	-	42	-	-	-	-	-	-	-	H	-	RFS	
124	-	-	26	32	-	-	-	-	-	-	-	-	-	RFSC	
125	-	-	36	5	-	-	-	-	-	-	-	-	-	$\overline{W}$	
126	-	-	45	9	-	-	-	-	-	-	-	-	-	$\overline{\text{lim 2}}$	
127	-	-	24	22	-	-	-	-	-	-	-	-	-	LS 2	
128	-	-	22	10	-	-	-	-	-	-	-	-	-	CNT 2	
129	-	-	(47)	-		(A)	-	38	-	-	-	-	-	BP	NOTE 1

Table 2-14. LORD 1A5A2 Interconnection Table (Cont'd.)

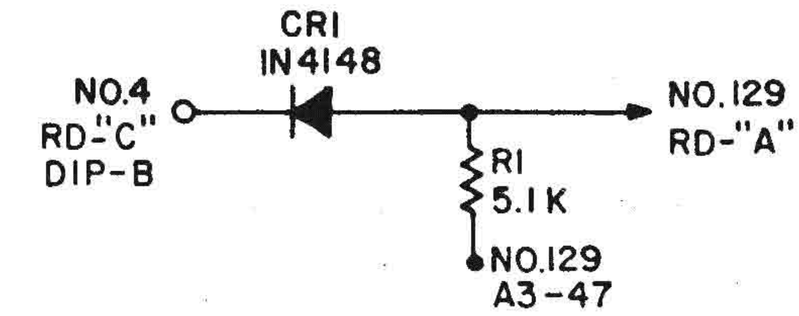
No.	A1	A2	A3	A4	PROM U1	Type (NOTE 4)	A5 RD1	A6 RD2	A7 RD3	MN J1	(DC) J2	MB J3	TEST J4	Function	Notes
1	36	36	44	36, 23,38			9.24	9	9.24		x	k	A	GND	
130	-	-	-	-	-	B	-	37	-	h	-	V	-	BP-A)	KBP
131	-	-	-	-	-	C	-	36	-	E	-	-	-	BP-B)	KBP
132	-	-	43	-	-	-	-	-	-	-	-	C	-	Φ	
133	-	-	42	-	-	-	-	-	-	-	-	G	-	R	
134	-	-	41	-	-	-	-	-	-	-	-	B	-	LT	
135	-	-	40	-	-	-	-	-	-	-	-	D	-	RT	
136	-	-	48	41	-	-	-	-	-	-	-	S	-	NO MATCH	
137	-	17	-	21	-	-	-	-	-	-	-	-	-	DL21	
138	-	18	-	20	-	-	-	-	-	-	-	-	-	DL22	
139	-	-	34	28	-		-	-	-	-	-	-	-	PP	
140	-	38	-	-	-	-	-	-	-	-	-	Y	-	X42	
141	-	39	-	-	-	-	-	-	-	-	-	z	-	X43	
142	-	40	-	-	-	-	-	-	-	-	-	x	-	X50	
143	-	41	-	-	-	-	-	-	-	-	-	J	-	X51	
144	-	42	-	-	-	-	-	-	-	-	-	i	-	X52	
145	-	1	-	-	-	-	-	-	-	-	-	Q	-	X53	
146	-	2	-	-	-	-	-	-	-	-	-	b	-	X60	
147	-	3	-	-	-	-	-	-	-	-	-	d	-	X61	(FL 6)
148	-	-	9		17	-	-	-	-	-	-	-	H	A8	
149	-	-	7		19	-	-	-	-	-	-	-	I	A6	
150	-	-	6		20	-	-	-	-	-	-	-	J	A5	
151	-	-	5		21	-	-	-	-	-	-	-	D	A4	
152	-	-	4		1	-	-	-	-	-	-	-	G	A3	
153	-	-	3		2	-	-	-	-	-	-	-	B	A2	
154	-	-	8		18	-	-	-	-	-	-	-	K	A7	
155	-	-	38		-	-	-	-	-	-	-	-	P	EW	
156	-	-	35		-	-	-	-	-	-	-	-	N	BLK	
157	-	-	33		-	-	-	-	-	-	-	-	M	ci	
158	-	-	32		-	-	-	-	-	-	-	-	O	CO	
159	-	-	10		3	-	-	-	-	-	-	-	F	A1	
160	-	-	20		4	-	-	-	-	-	-	-	-	TP1	
161	-	-	19		5	-	-	-	-	-	-	-	-	TP2	
162	-	-	18		6	-	-	-	-	-	-	-	-	TP3	
163	-	-	17		7	-	-	-	-	-	-	-	-	TP4	
164	-	-	16		8	-	-	-	-	-	-	-	-	TP5	

Table 2-14. LORD 1A5A2 Interconnection Table (Cont'd.)

No.	A1	A2	A3	A4	PROM U1	Type Note	A5	A6	A7	MN	(DC)	MB	TEST	Function	Notes
				36,			RD1	RD2	RD3	J1	J2	J3	J4		
1	36	36	44	23,38		(4)	9.24	9	9.24		x	k	A	GND	
165	-	-	15		9	-	-	-	-	-	-	-	-	TP6	
166	-	-	14		10	-	-	-	-	-	-	-	-	TP7	
167	-	-	13		11	-	-	-	-	-	-	-	-	TP8	

NOTE 1:

Point 31 of A5 (line 4) is connected to point 38 of A6 (line 129) via diode CR.1. Point 47 of A3 (line 129) is connected to point 38 of A6 at the same line via R1.



NOTE 2:

Chip - capacitors 10 F (C2,3,4,5) are connected between points 11, 12 of A6 (lines 90,89) 11,12 of A-7 (lines 37, 36) and points 8 of A-6,7 (line 84).

NOTE 3:

LORD functions T'A and T'B are not used in the MN 1A5A1.

Not applicable

NOTE 4:

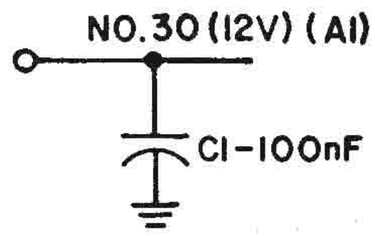
See drawing No. 24-27-050-1A.

NOTE 5:

Capacitor C1 is connected between point 39 of A3 (line 80: +12V) to GND.

NOTE 6:

Resistor R2 is connected between point 12 of A3 (line 82) and point 39 of A3 (line 80: +12V).



NOTE 7:

Resistor R3 is connected between point 25 (line 85a) and point 40 of A4 (line 80).

i. Relay Driver RD (fig. 2-41). Three relay drivers are used in the LORD 1A5A2. Each relay driver has 12 driver circuits. Four of them consist of a single transistor, with a protection diode connected from its collector to the VEN2 line. The other eight drivers consist of two transistors, each one having a protection diode connected from its collector to the VEN1 line. The collector of the first transistor drives the base of the second one, therefore, when one transistor saturates, the other cuts off, and vice-versa.

The single-transistor drivers are used to drive regular relays, whereas the dual transistor drivers are used to drive latching relays.

j. Interconnection Table. Table 2-16 provides the interconnections for the LORD PCB.

2-16. Power Supply Module PS 1A4 (fig. 2-42 through 2-49)

The power supply module contains the ON/OFF relay, a fuse, switching regulators for +34V, +15V, +12V, +6V, and -10V, and several control and switching circuits. The module consists of two PC boards, connected together through the J1 and P1 connectors.

a. Block Diagram Analysis (fig. 2-42). The primary DC voltage, normally supplied from the RT-936/PRC-174 battery, arrives at pins N, L, K of the module, and passes through a protection fuse to the ON/OFF relay. A diode provides protection against reversal of primary voltage polarity.
The ON/OFF relay is a latching relay, controlled by the front panel function selector, which is used to connect the primary DC voltage to the power supply circuits. The primary unregulated voltage, controlled by the relay, is sent to the PA 1A6; the same voltage is filtered and sent to the CONT 1A7, USB 1A3A3 and SNF 1A5A3 modules.
The primary DC voltage is also applied to the +15V, +12V, +6V, -10V and +34V switching regulators. All regulators operate continuously, except the +34V regulator, which is turned on when the PTT +15V line is grounded (transmit mode). All regulators have internal current limiting, for protection against excessive load current and short-circuit. In addition, the output current of the +34V regulator is monitored; should the current exceed the maximum allowable value (indicating excessive output power, overloading or power amplifier failure), the current limiting circuit takes control of the RFS line (see para. 2-10), reducing or even turning off completely the RF output power.

The RFS line is also controlled by the $\overline{\text{TUNE}}$ line: when this line rises to a high level, following completion of tuning, its rising edge is differentiated and the resulting pulse is used to momentarily shut the RF output voltage.

In addition to the primary DC voltage and the regulated voltage, module PS 1A4 provides three voltages:

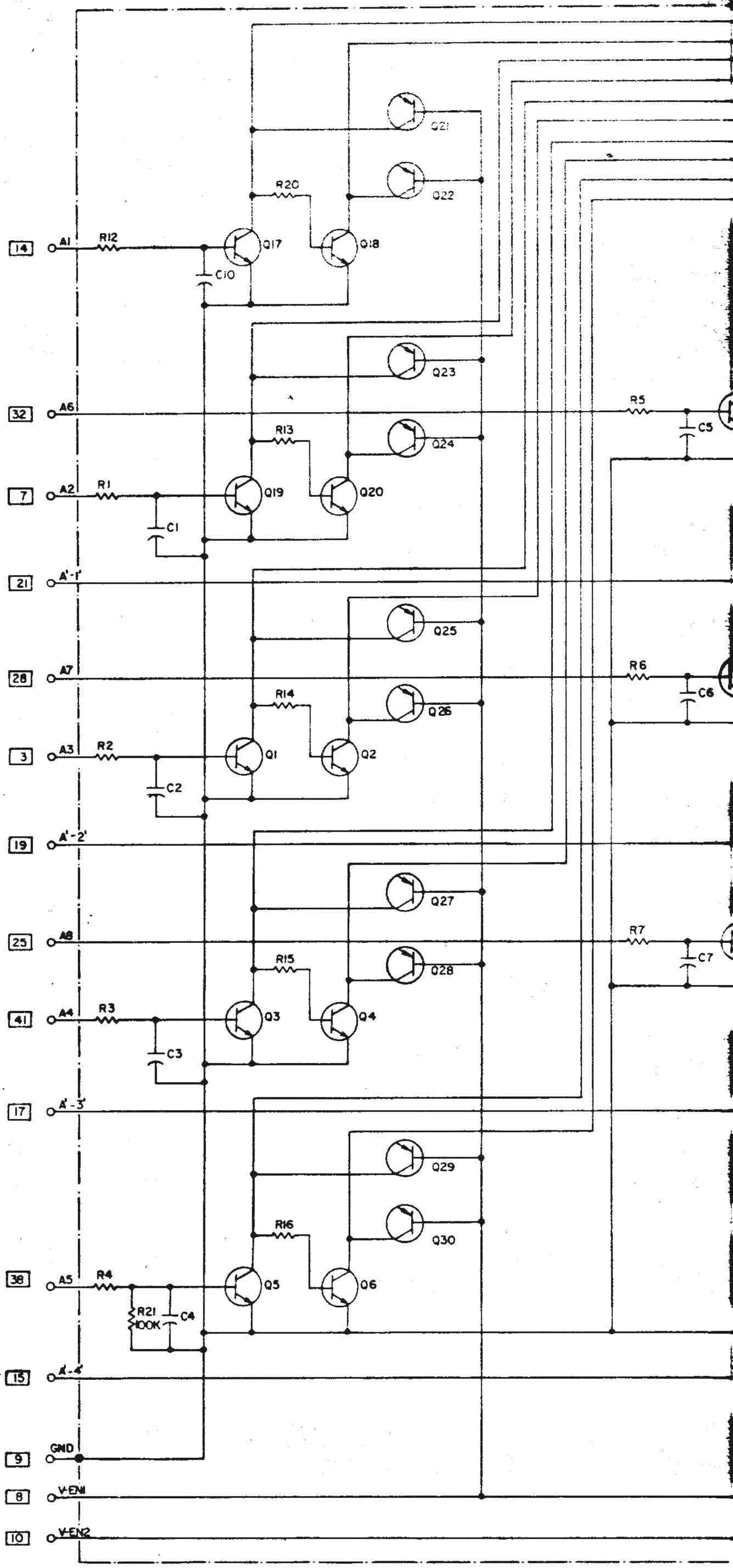
(1) VEN1 for the relay driver in module LORD 1A5A2. This is the primary DC voltage, turned on when the EN CONT line rises to a high level while matching network components are switched.

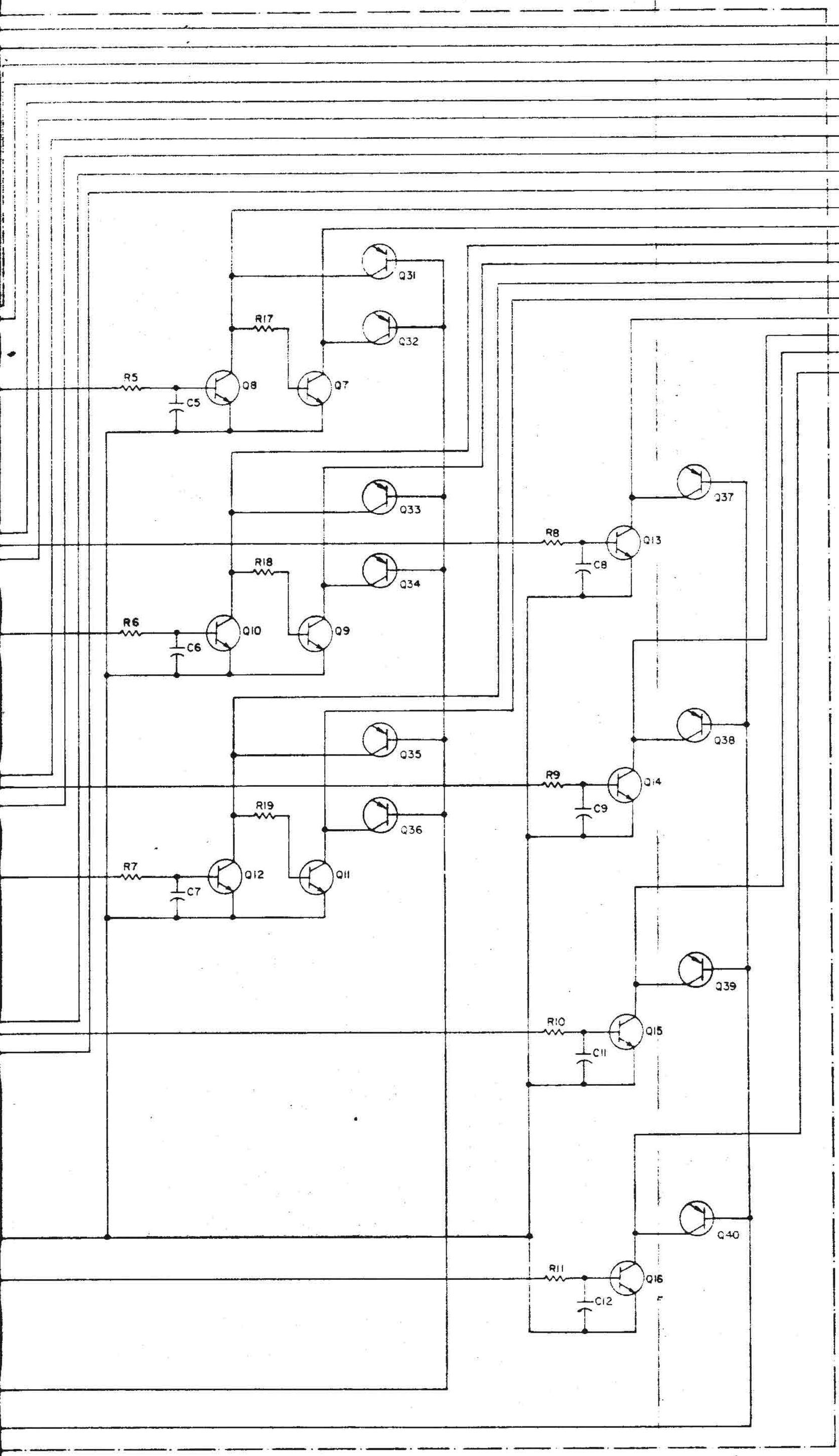
(2) VEN2 for the relay driver in module LORD 1A5A2 and the relays in module SNF 1A5A2. Normally, VEN2 is derived through a diode, from the +15V voltage; when the EN CONT line rises to a high level, the VEN2 line is connected to the primary DC voltage.

(3) -10VEN. This voltage is used in the tuning mode (under control of the $\overline{\text{TUNE}}$ line), to power circuits in modules LORD 1A5A2 and SNF 1A5A3.

b. Circuit Analysis (fig. 2-43 through 2-49).

(1) Input circuit (fig. 2-43, 2-44). The primary DC voltage, arri-


14
A1
R12
Q17
Q18
C10
Q21
Q22
R20
32
A6
R5
C5
Q23
Q24
R13
7
A2
R1
Q19
Q20
C1
21
A'-1'
Q25
28
A7
R6
C6
Q26
R14
3
A3
R2
Q1
Q2
C2
19
A'-2'
Q27
25
A8
R7
C7
Q28
R15
41
A4
R3
Q3
Q4
C3
17
A'-3'
Q29
Q30
R16
38
A5
R4
Q5
Q6
R21
100K
C4
15
A'-4'
9
GND
8
V-EN1
10
V-EN2



NOTES:

1. RESISTORS R1 TO R12 ARE 18K. ±10%.
2. RESISTORS R13 TO R20 ARE 39K. ±10%.
3. CAPACITORS C1 TO C12 ARE 10nF ± 20%.
4. TRANSISTORS Q1 TO Q20 ARE 2N3019
5. TRANSISTORS Q21 TO Q40 ARE 2N2905 A.
6. VIEW FROM THE BOTTOM.

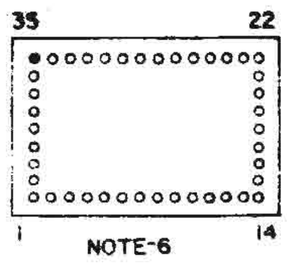


Fig. 2-41. Relay driver RD, schematic circuit diagram

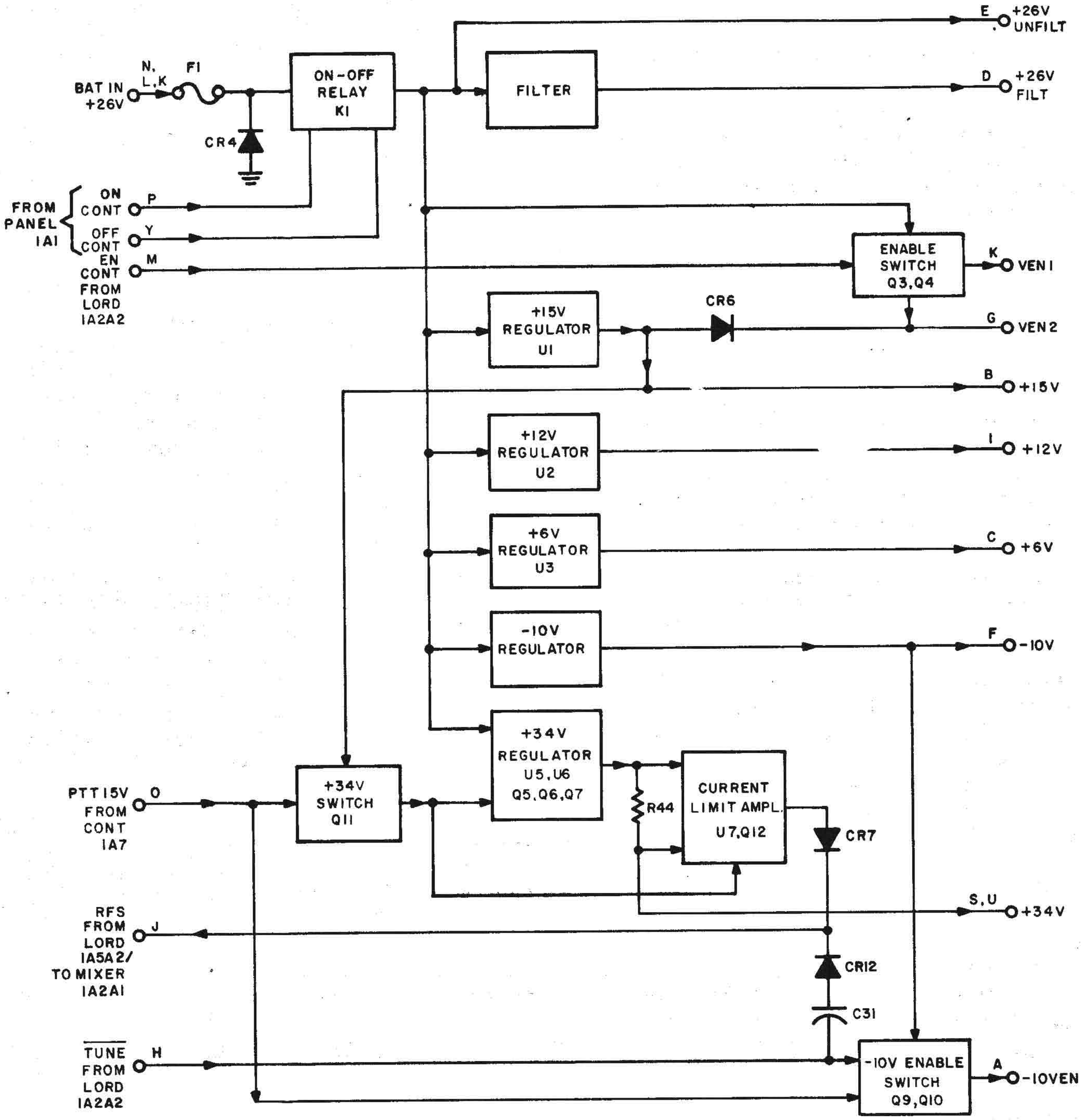


Fig. 2-42. Module PS1A4, block diagram

ving at pins L, N, X, passes through fuse F1 to the contacts of the ON/OFF relay, K1. Diode CR4 conducts when the polarity of the input voltage is reversed, and blows out fuse F1.
Relay K1 - the ON/OFF relay - is controlled by the front panel function switch. Assuming for the moment that K1 is at the OFF position (as shown in fig. 2-44), line OFF CONT is grounded and line ON CONT is open-circuited. Capacitor C1 eventually charges to the full primary DC voltage value through contacts B2, B3 of K1 and resistor R7. When the RT-936/PRC-174 is turned on, the ON CONT line is grounded and the OFF CONT line is open-circuited. Capacitor C1 discharges through the ON coil (X1-X2) and the contacts switch connecting the +26V UNFIL line to the BAT IN line. The BAT IN voltage is also filtered by C12, L3 and C3 and applied on the +26V FIL line. Capacitor C2 now charges through R8 to the BAT IN voltage, therefore when the function switch is returned to OFF (OFF CONT line grounded), C2 discharges through the OFF coil (X1-X2) and the contacts switch again, this time disconnecting the BAT IN line.

(2) VEN1 and VEN2 voltages (fig. 2-44). The VEN1 voltage is obtained from the +26V UNFIL voltage. When the EN CONT line from module LORD 1A5A2 rises to a high level, transistors Q4 and Q3 saturate, and the +26V UNFIL voltage passes through resistor R67 and transistor Q3 to the VEN1 line. When the EN CONT is at a low level, Q4 and Q3 cut off, and the VEN1 line is open-circuited.
When the EN CONT line is low, the +15V voltage passes through CR6 to the VEN2 line, whereas when the EN CONT line is high, the higher VEN1 voltage passes through CR14 to the VEN2 line, and diode CR6 is reverse-biased.

(3) +15, +12V and +6V regulators (fig. 2-43, 2-45). These are high efficiency switching regulators, designed around hybrid circuits U1, U2 and U3. All regulators are identical, except the values of the components which determine the output voltages. The operation of the +15V regulator is analyzed below, using the simplified circuit diagram shown in fig. 2-45.

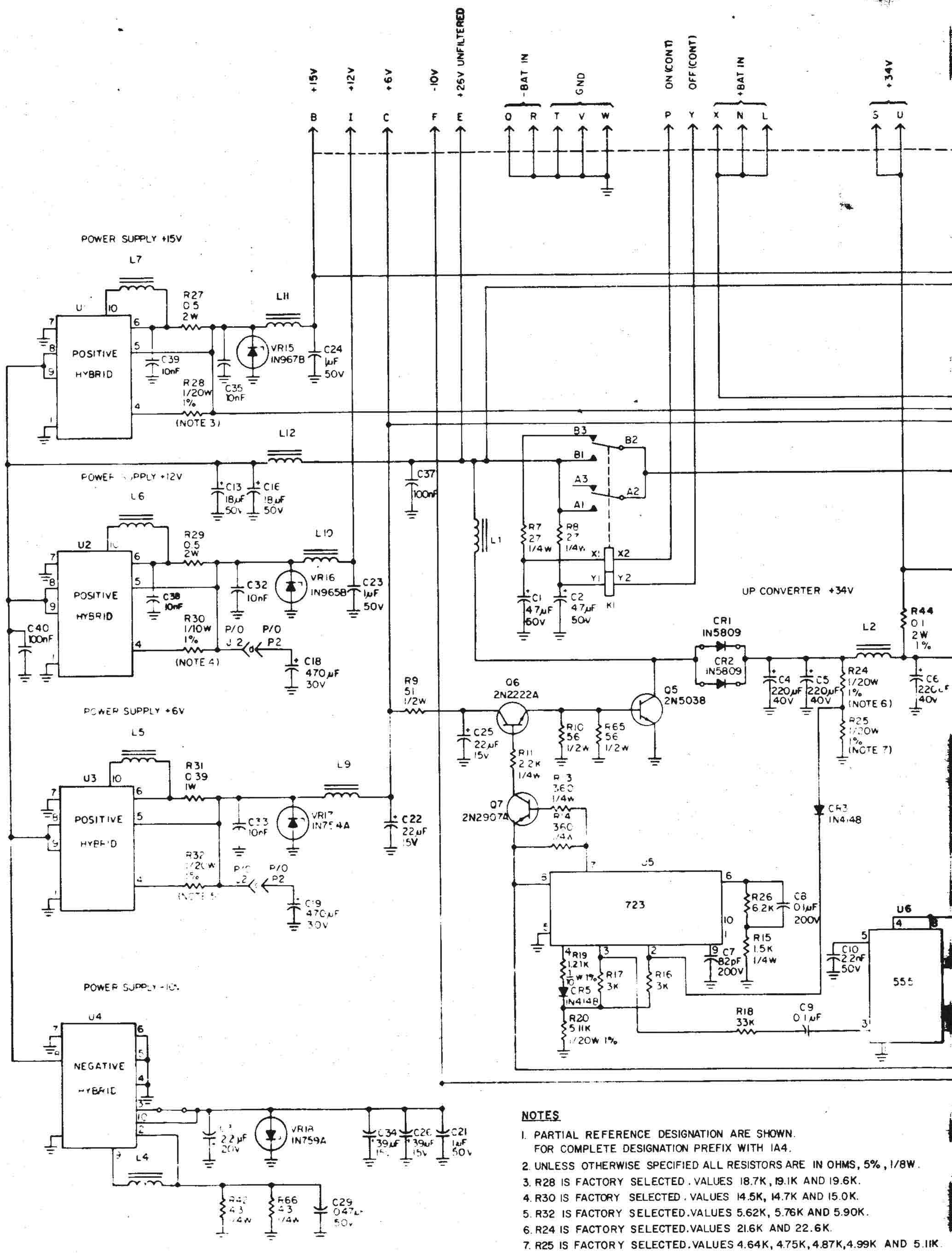
(a) The input voltage is filtered by L12, C13, and C16, and then applied to pins 8 and 9 of U1. The internal series switching transistor, U1Q3, conducts and connects pin 10 to pins 8,9. The current through L7 and R27 begins to increase and the voltage on capacitors C39 and C35 also increases.

(b) The output voltage, appearing on C35, is applied via R28 to the inverting input of the internal comparator, U1U1. The non-inverting input of the internal comparator receives an accurate reference voltage from an internal source. When the output voltage rises above the reference voltage, the internal transistor switches off U1Q3, and L7 now supplies current to the load, from the energy stored during the ON interval. The current path now closes through diode U1Q2.

(c) The OFF (discharge) interval ends when the voltage at pin 4 of U1 drops below the internal reference voltage. Then the internal transistor conducts again, and the cycle repeats itself. The switching frequency is several tens of kHz.

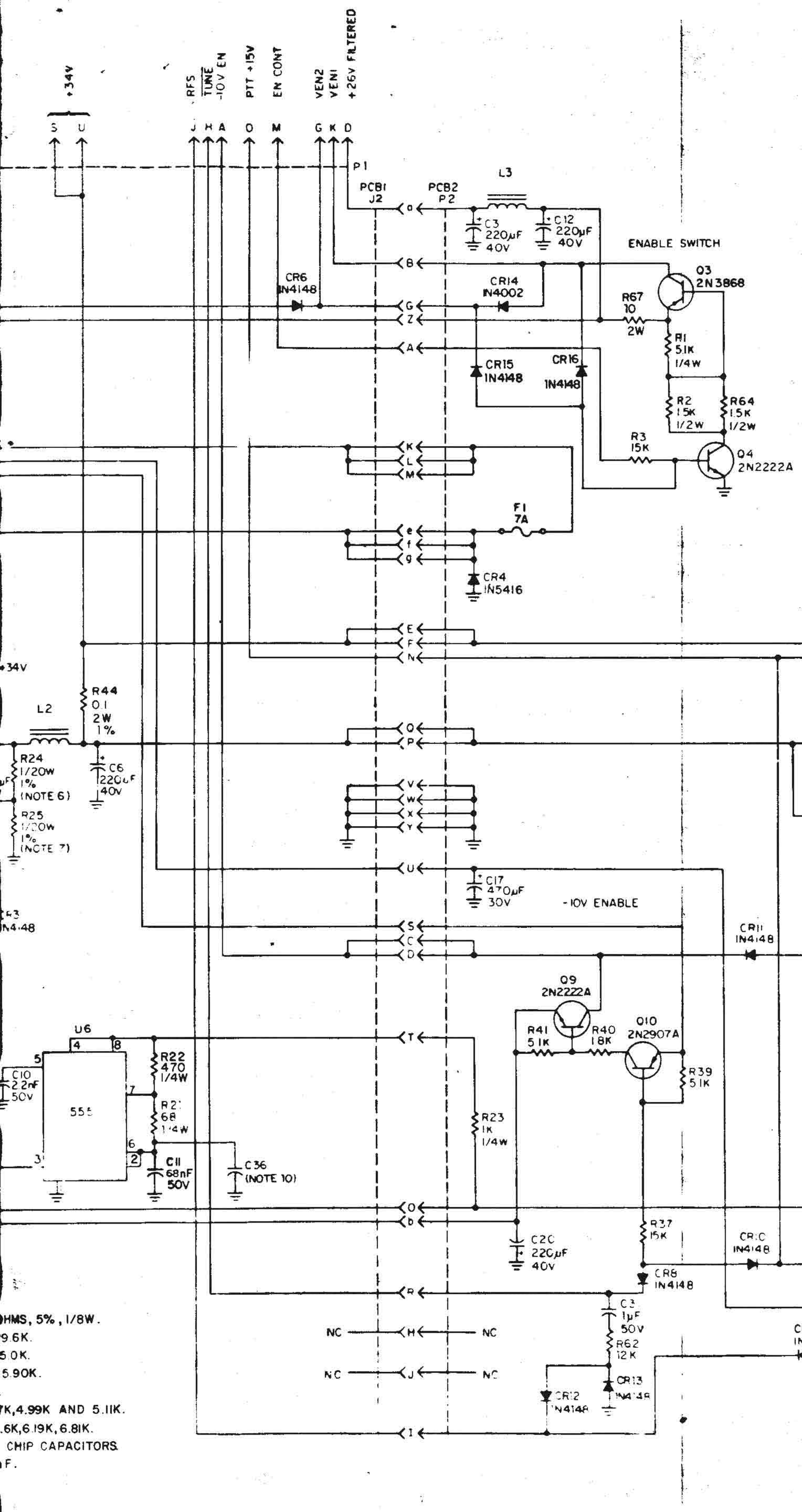
(d) The output voltage is regulated (to within the inherent ripple required for proper operation of the switching regulator) to a value determined by the selected resistor R28 (which is the external part of a voltage divider), and the internal reference voltage.

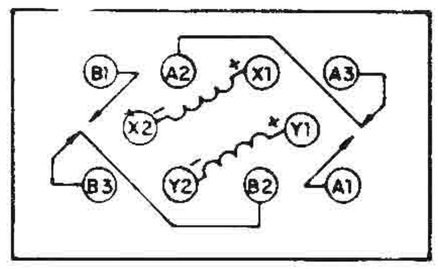
(e) The regulator's output current flows through the current sense resistor R27. The voltage across R27 is applied across the base-emitter junction of the current limiting sense transistor, U1Q7. If the voltage drop across R27 becomes too high, transistor U1Q7 turns on, and provides base bias current to transistor U1Q6. U1Q6 pulls up the inverting



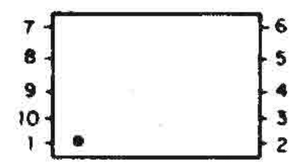
NOTES

1. PARTIAL REFERENCE DESIGNATION ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A4.
2. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE IN OHMS, 5%, 1/8W.
3. R28 IS FACTORY SELECTED. VALUES 18.7K, 19.1K AND 19.6K.
4. R30 IS FACTORY SELECTED. VALUES 14.5K, 14.7K AND 15.0K.
5. R32 IS FACTORY SELECTED. VALUES 5.62K, 5.76K AND 5.90K.
6. R24 IS FACTORY SELECTED. VALUES 21.6K AND 22.6K.
7. R25 IS FACTORY SELECTED. VALUES 4.64K, 4.75K, 4.87K, 4.99K AND 5.11K.
8. R58 IS FACTORY SELECTED VALUES 3.9K, 4.7K, 5.1K, 5.6K, 6.19K, 6.81K.
9. C32, C33, C35, C36, C37, C38, C39, AND C40 ARE CHIP CAPACITORS.
10. C36 OPTIONALLY ADDED CHIP CAPACITOR. VALUE 10nF.





K1 SCHEMATIC DIAGRAM
(UNENERGIZED POSITION BOTTOM VIEW)



POSITIVE & NEGATIVE
POWER SUPPLY HYBRID
(UP VIEW POSITION)

Fig. 2-43. Module PS1A4, schematic circuit diagram

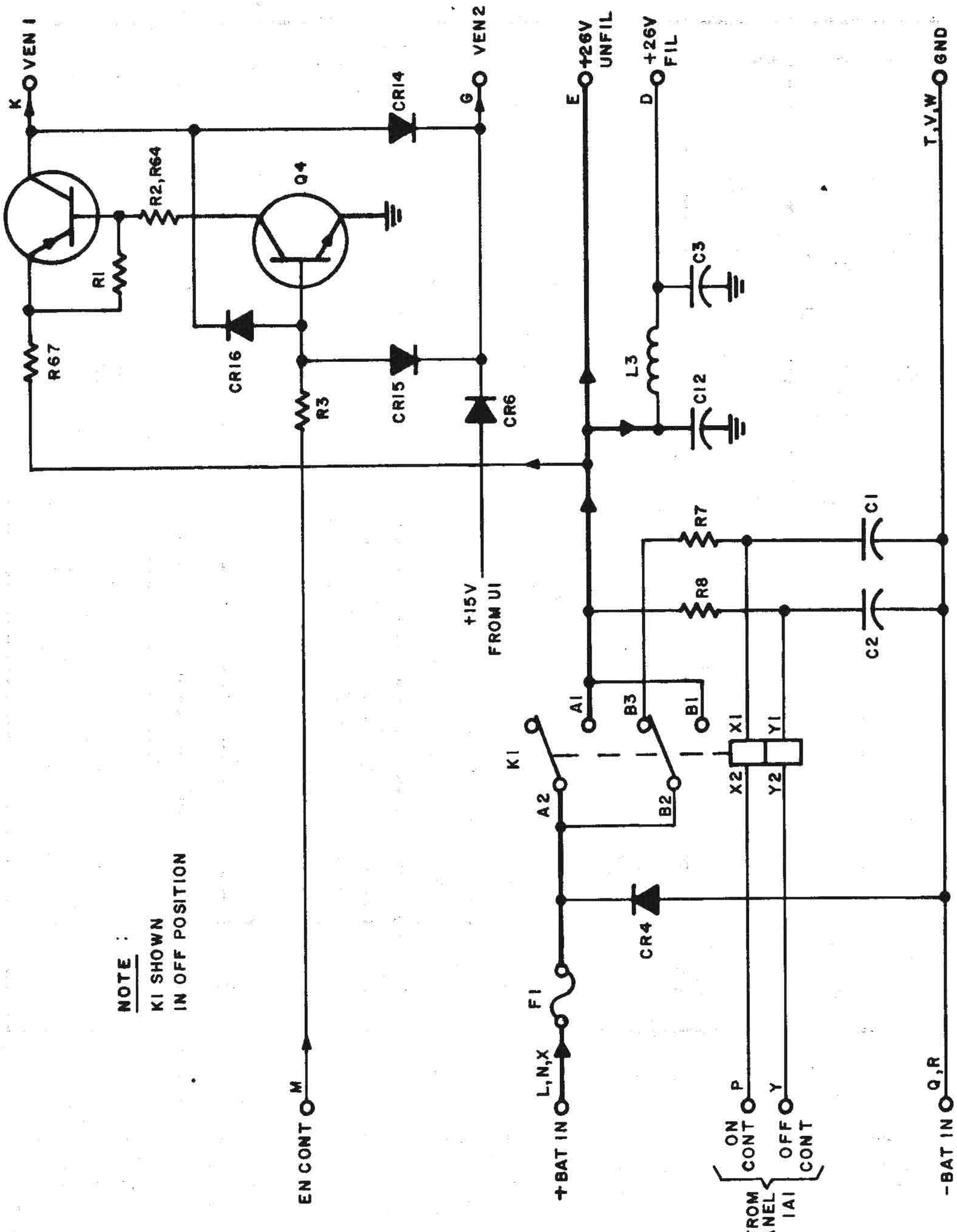


Fig. 2-44. Input circuit, simplified circuit diagram

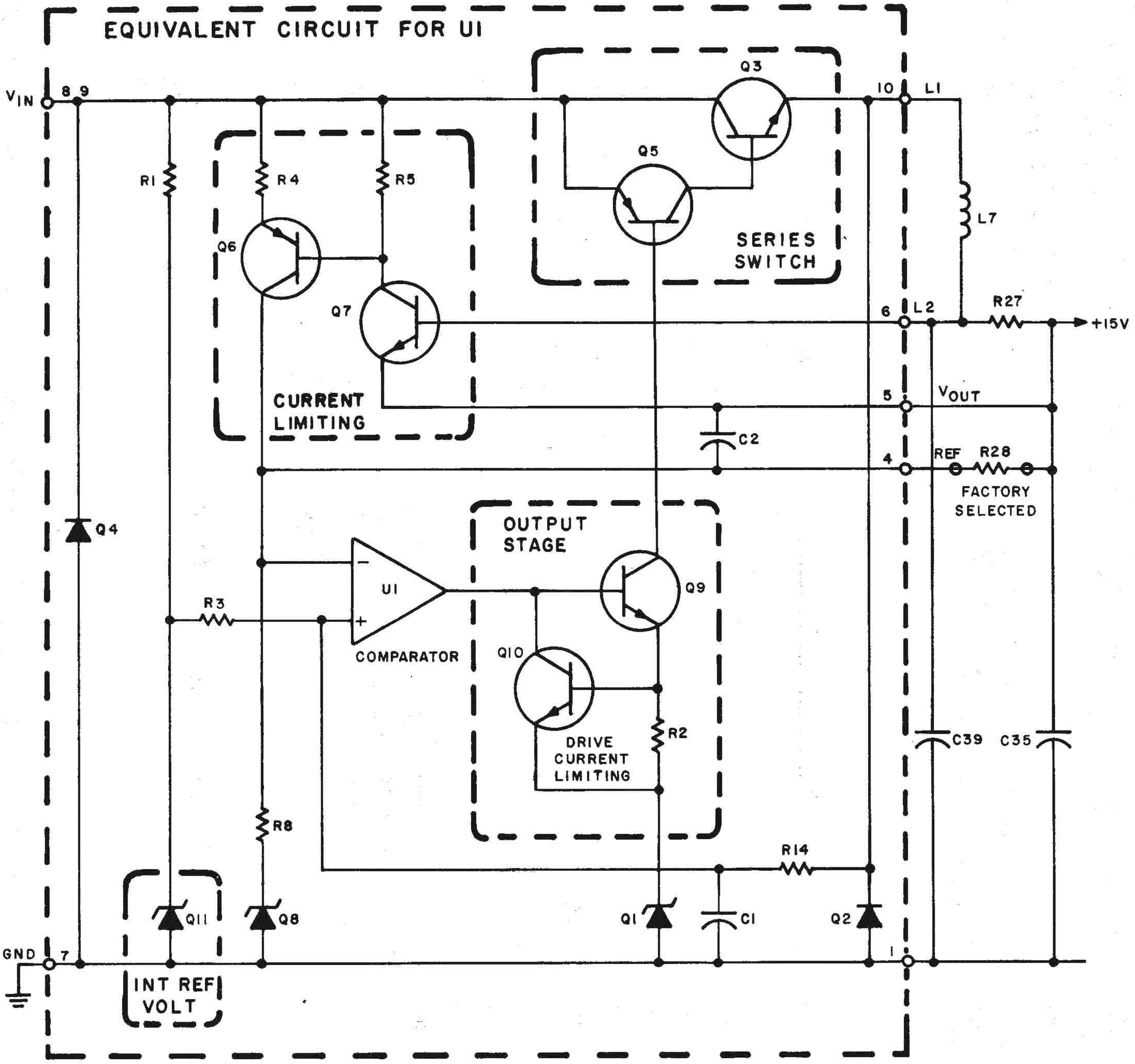


Fig. 2-45. +15V regulator, simplified circuit diagram

input of the internal comparator, U1U1, thereby turning off the switch transistor U1Q3 until the output voltage decreases and the current returns to an acceptable value. Thus the output voltage falls to a low value and regulator operation is inhibited, thereby protecting it against overload and short circuits.

(f) The +15V, generated by U1, is filtered by L11 and C24 and connected to pin B. Zener diode VR15 protects the regulator and the circuits connected to it against accidental application of a higher voltage to its output, or failure of the internal circuits.

(g) The regulators for +12V and +6V are identical. The +12V is connected to pin I, and the +6V to pin C.

(4) -10V regulator (fig. 2-46). This regulator is designed around hybrid circuit U4.

(a) The input voltage is applied to pin 8. The operating frequency of the regulator is determined by a multivibrator, which drives an internal transistor, U4Q8, connected between pins 8 and 9. The transistor conducts and drives current through L4 (which is effectively connected to ground through R42 and R66). Energy is stored in L4 during the conduction interval. An internal diode, U4Q10, connected between pins 9 and 10, prevents the positive voltage across L4 from appearing at the output (pin 10).

(b) When the current cycle ends, the internal transistor, U4Q8, cuts off. The voltage across L4 changes polarity (pin 9 becomes negative with respect to ground) and therefore passes via the internal diode, U1Q10, to the output. Capacitors C21, C26, C30 and C34 filter this voltage.

(c) The DC output voltage is determined by the breakdown voltage of the Zener diode U4Q3. The output voltage varies the current generated by the current source comprised of U4Q12 and U4Q3. This current controls the conduction time of U1Q8 through the current-controlled multivibrator, and the energy stored in L4, such that the output voltage is held at the desired value (-10V).

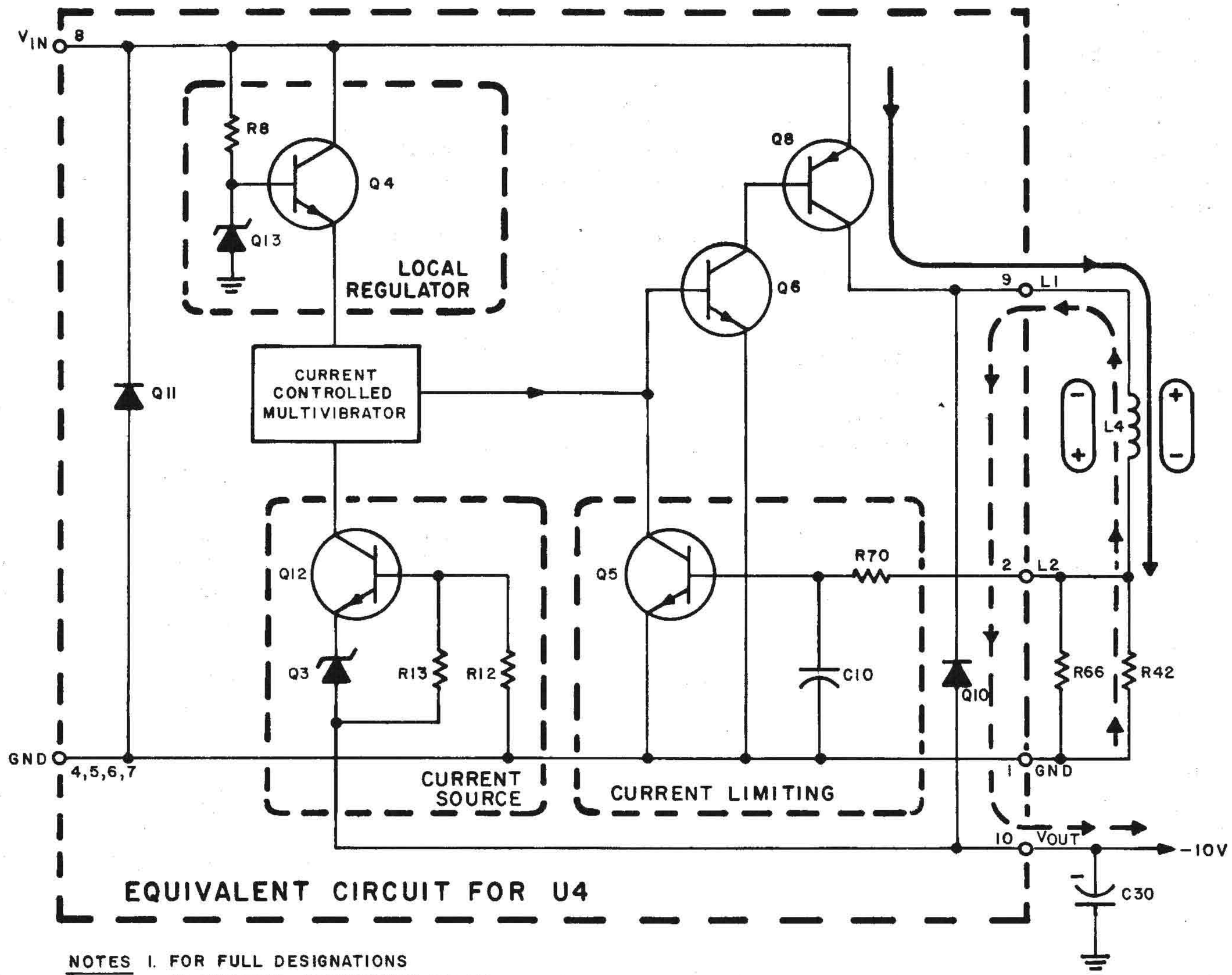
(d) The DC current through L4 (which is equal to the load current) flows through current sense resistors R42 and R66. The DC voltage, developing across them is applied across the base-emitter junction of current limiting transistor U4Q5. When the load current becomes excessive, U4Q5 turns on and shunts the drive current of U4Q6 and U4Q8 to ground, thereby interrupting regulator operation. This protects the regulator against overload and short circuits.

(e) The -10V output voltage is applied to pin F. Output overvoltage protection is provided by Zener diode VR18.

(5) -10VEN generation (fig. 2-47). During tuning, module LORD 1A5A2 applies a low level to the TUNE* line (pin H). This allows bias current to flow via CR8 and R37, into Q10. The emitter of Q10 is connected to +6V; therefore, Q10 saturates and supplies bias current to Q9 (through R40). Q9 also saturates and connects the -10V to pin A (-10VEN line).
Similar operation occurs during transmission, when the PTT 15V (pin 0) is grounded, connected through CR10, and R37 to the base of Q10.

(6) +34V regulator (fig. 2-48). The +34V regulator is a switching regulator, comprises of U6, U5, Q5, Q6, and Q7, which supplies power to the final stage of PA 1A6.

(a) The regulator operates only during transmission, when line PTT 15V is grounded. Transistor Q11



NOTES 1. FOR FULL DESIGNATIONS OF INTERNAL COMPONENTS OF U4, PREFIX THE PARTIAL DESIGNATIONS SHOWN BY U4
2. —— DENOTES CHARGING PATH
– – DENOTES DISCHARGE PATH

Fig. 2-46. -10V regulator, simplified circuit diagram

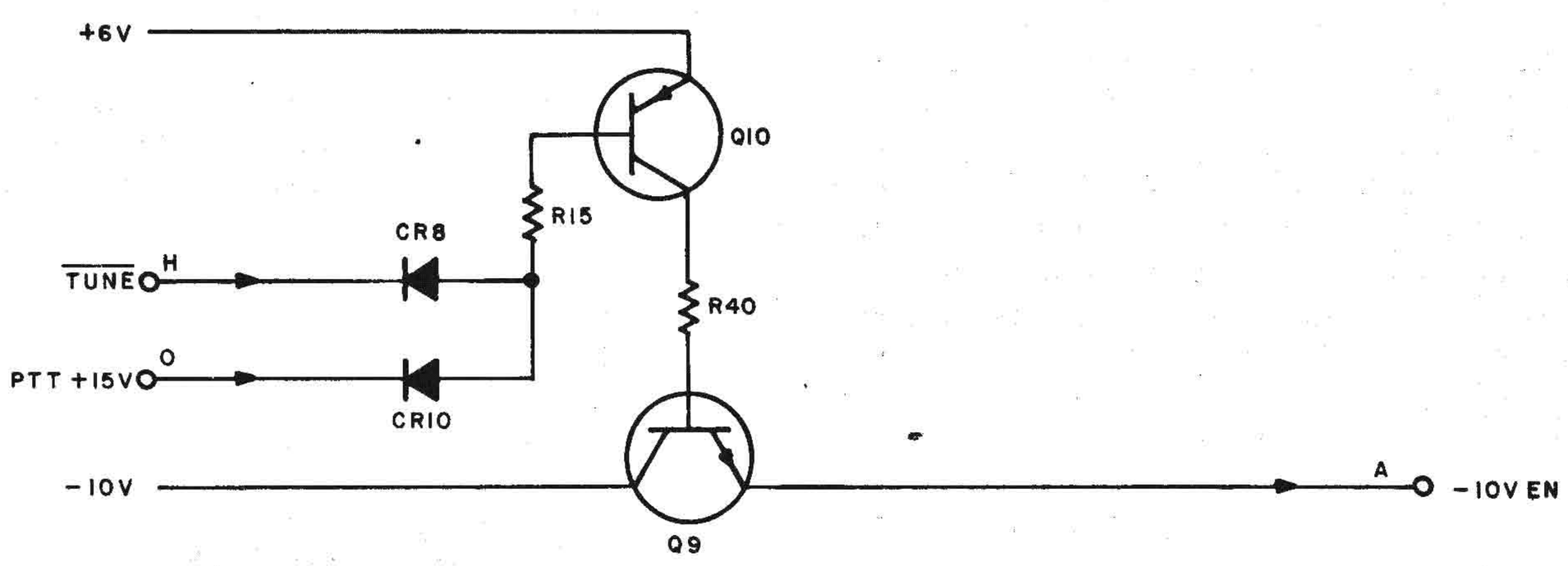


Fig. 2-47. -10V enable switch

saturates and supplies the +15V to the multivibrator U6, to the regulator integrated circuit U5, and to the drive transistor Q7.

(b) U6 oscillates at 35 to 40 kHz. The oscillation frequency is determined by R22, R21, and C11. The square wave output of U6 (pin 3) is applied to the non-inverting input of the internal error amplifier of U5, via R18 and C9. Its purpose is to determine the conduction interval of the parallel switch transistor, Q5.

(c) The output voltage of the regulator is the sum of the battery voltage and the voltage on L1. When Q5 conducts, energy is stored in L1. During this period, diodes CR1 and CR2 are reversed-biased by the higher output voltage stored on the output capacitors C4 and C5, and these discharge, supplying current to the load. When Q5 cuts off (under control of U5), the voltage drop across L1 changes polarity and adds to the battery voltage. This causes the diodes CR1 and CR2 to conduct and pass current, thereby recharging C4, C5 and supplying current to the load.

(d) A small ripple voltage is superimposed on the average DC voltage appearing across capacitors C4 and C5. A sample of this voltage is applied, via R24, R25 and CR3, to the inverting input of the error amplifier in U5. When this voltage rises above that existing at the non-inverting input, the voltage at pin 7 of U5 rises and Q7 cuts off. Transistors Q5 and Q6 remain cut off and current flows through L1. During this period, the load current is supplied by the output capacitors.

When the output capacitors discharge sufficiently, the voltage at the inverting input of U5 drops below that at the other input, Q5 cuts off, L1 recharges C4, C5, and the cycle repeats itself.

(7) PA current monitoring and RFS control (fig. 2-49). The regulated +34V output voltage is filtered by L2, C6 and passed to pins S, U via the current sensing resistor R44. The voltage drop across R44 is applied to the emitters of the matched transistor pair contained in Q12. These transistors are turned on when line PTT +15V is grounded (transmit mode). The amplified voltages appearing at the collectors of Q12, is applied to the non-inverting input of U7 (pin 3) through the voltage dividers comprised of R56, R57 and R55, R58, and to the inverting input (pin 2) through the voltage divider comprised of R52 and R53 and R54.
The output of U7, which is proportional to the current through R44, is applied on the RFS line via CR7 and R60. When the regulator output current is too large, the voltage applied on the RFS line reduces, or even shuts off completely, the RF signal generated by the MIXER 1A2A1. The value of current at which this occurs is determined by the value of the selected resistor R58.
Resistor R60 and capacitor C28 filter the RFS signal, thereby preventing activation of the protection circuit on modulation peaks.

Note that when the $\overline{\text{TUNE}}$ line returns to the high level, a positive pulse will be coupled via C31, R62, and CR12 to the RFS line. The pulse duration is determined by the charging time of C31.

2-17. Module REF 1A3A6
(fig. 2-50, 2-51, 2-52)

Review para. 2-4, which analyses the synthesizer block diagram, before reading the circuit analysis of the module.

a. Block Diagram Analysis (fig. 2-50). Module REF 1A3A6 provides the various reference frequencies required for the various RT-936/PRC-174 circuits. The source for these signals is a 3.5-MHz temperature compensated

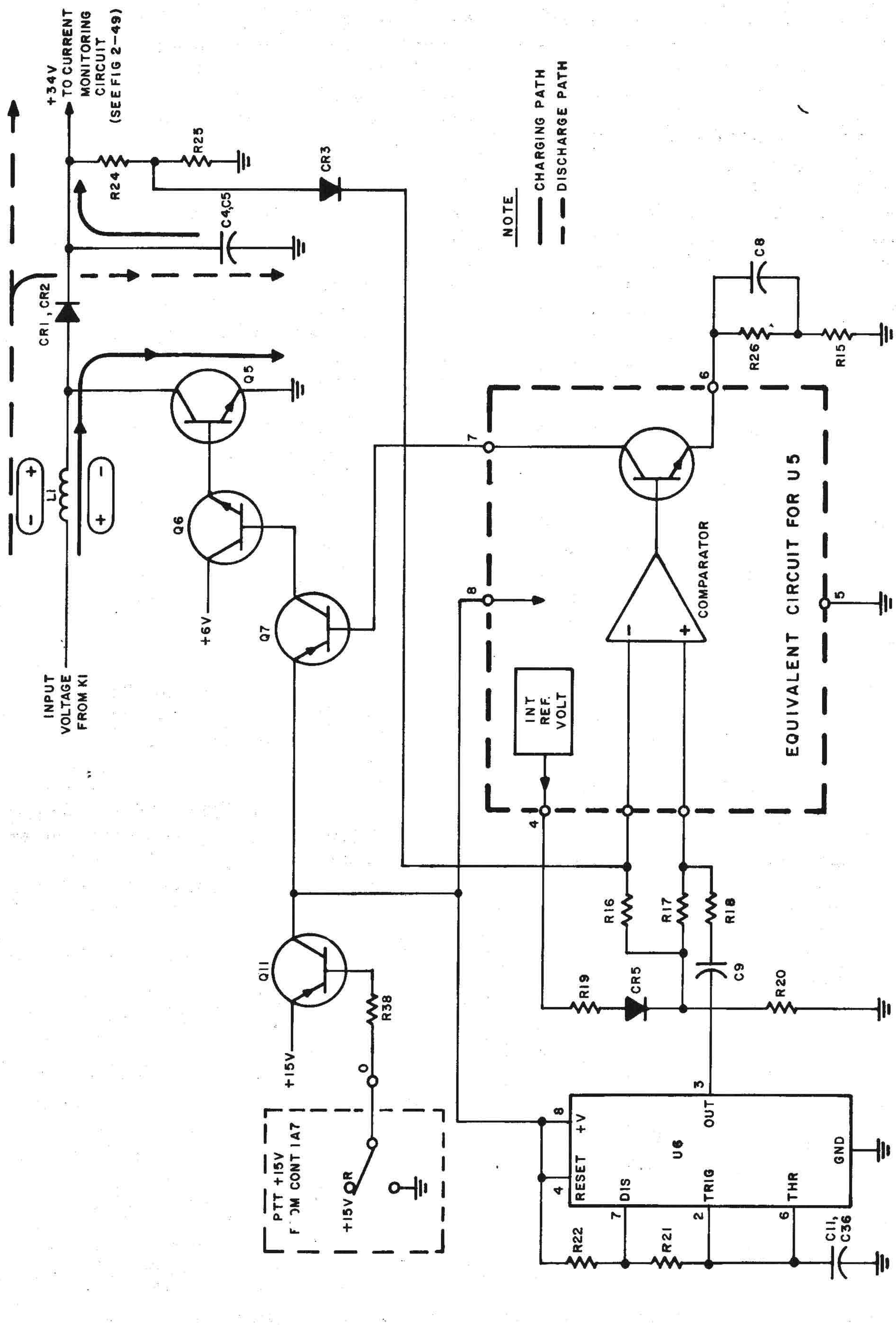


Fig. 2-48. +34V regulator, simplified circuit diagram

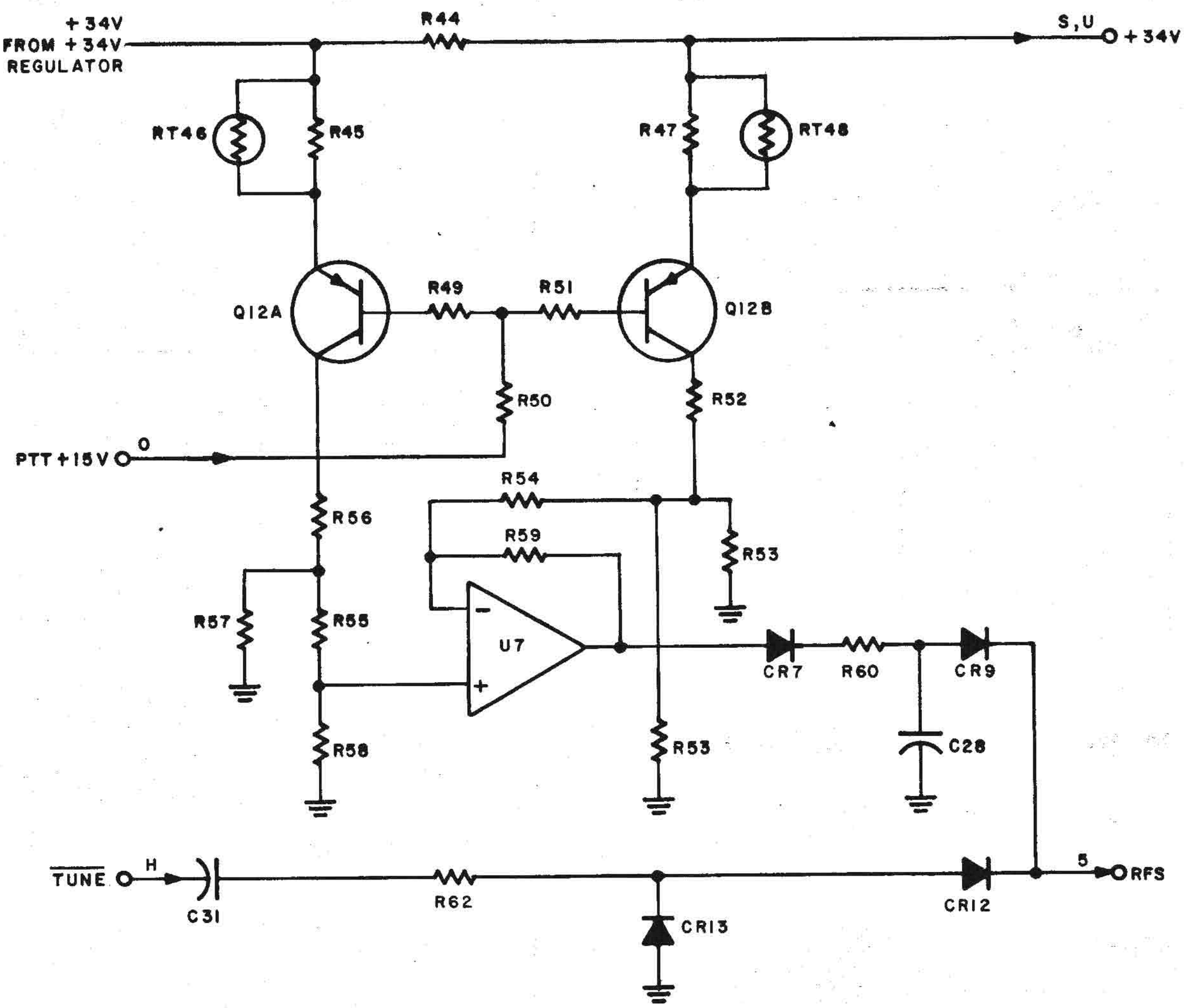


Fig. 2-49. PA current monitoring and RFS control, simplified circuit diagram

crystal oscillator (TCXO), which is powered from the +15V line via a separate voltage regulator. The frequency of the TCXO output signal is tripled to obtain the 10.5-MHz signal; divided by 2 and then tripled to obtain the 5.25-MHz carrier signal; divided by 175 to obtain the 20-kHz reference signal, and then by 2 and 4 to obtain the 10-kHz and 5-kHz signals, respectively.

(1) In the AM receive mode, the divider-by-2 in the 5.25-MHz path is disabled by the INH F3 line from module CONT 1A7, thereby interrupting the 5.25-MHz carrier.

(2) The 10-kHz signal is allowed to pass to module PRE 1A2A4 only during the WCW and NCW modes. This is obtained by controlling gate U5C by means of the WCW (CW) line.

b. Circuit Analysis (fig. 2-51, 2-52).

(1) 3.5-MHz TCXO (fig. 2-51). The reference for the synthesizer circuits is a 3.5-MHz TCXO, supplied by U7 with a +10.6-V regulated voltage. U7 is an integrated circuit regulator, whose output voltage is determined by the ratio of R20 to R21. Resistor R19 is the current-sense resistor, which provides protection by current limiting. The TCXO output is connected to the other frequency generation circuits through gate U4A.

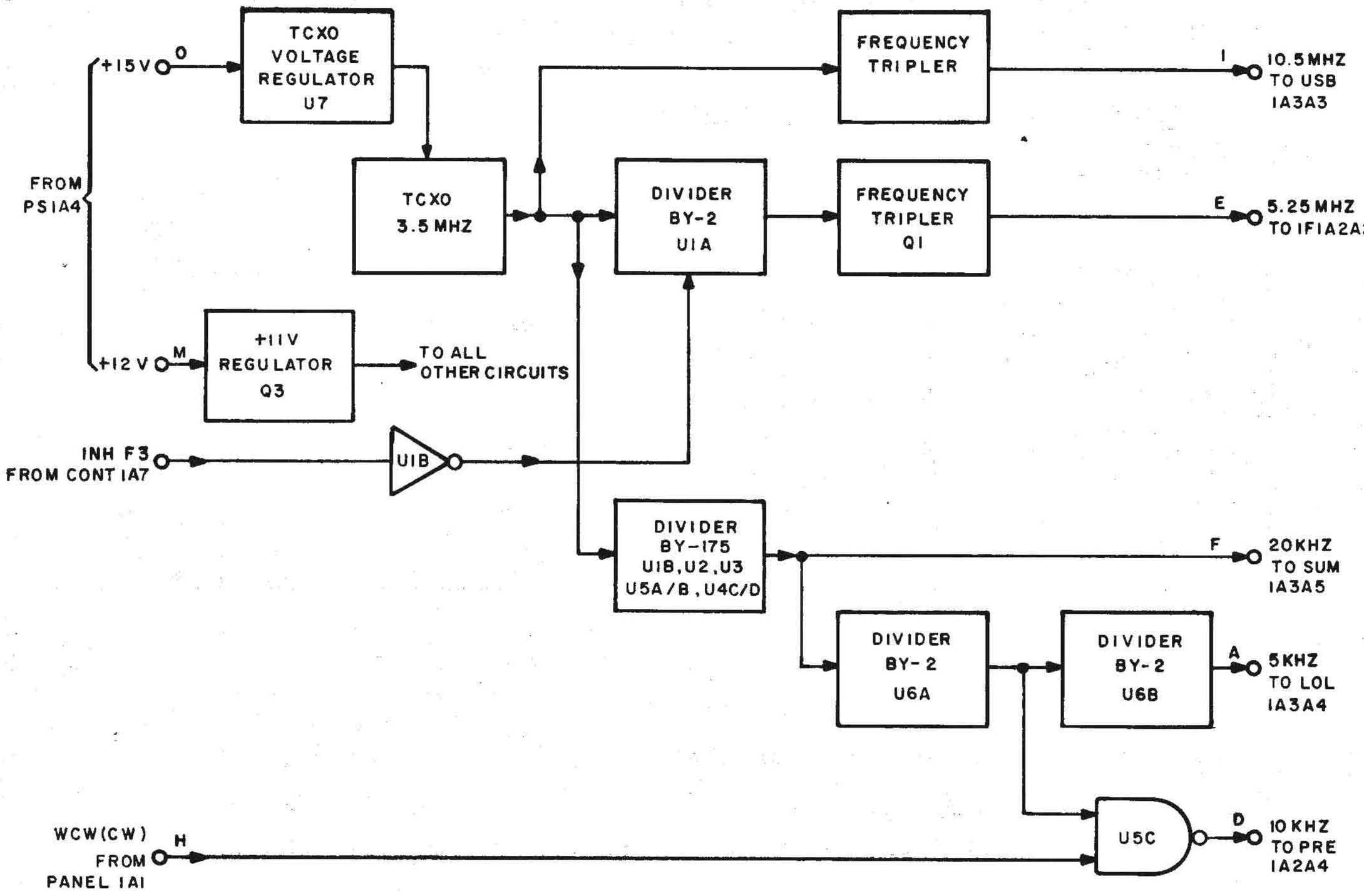
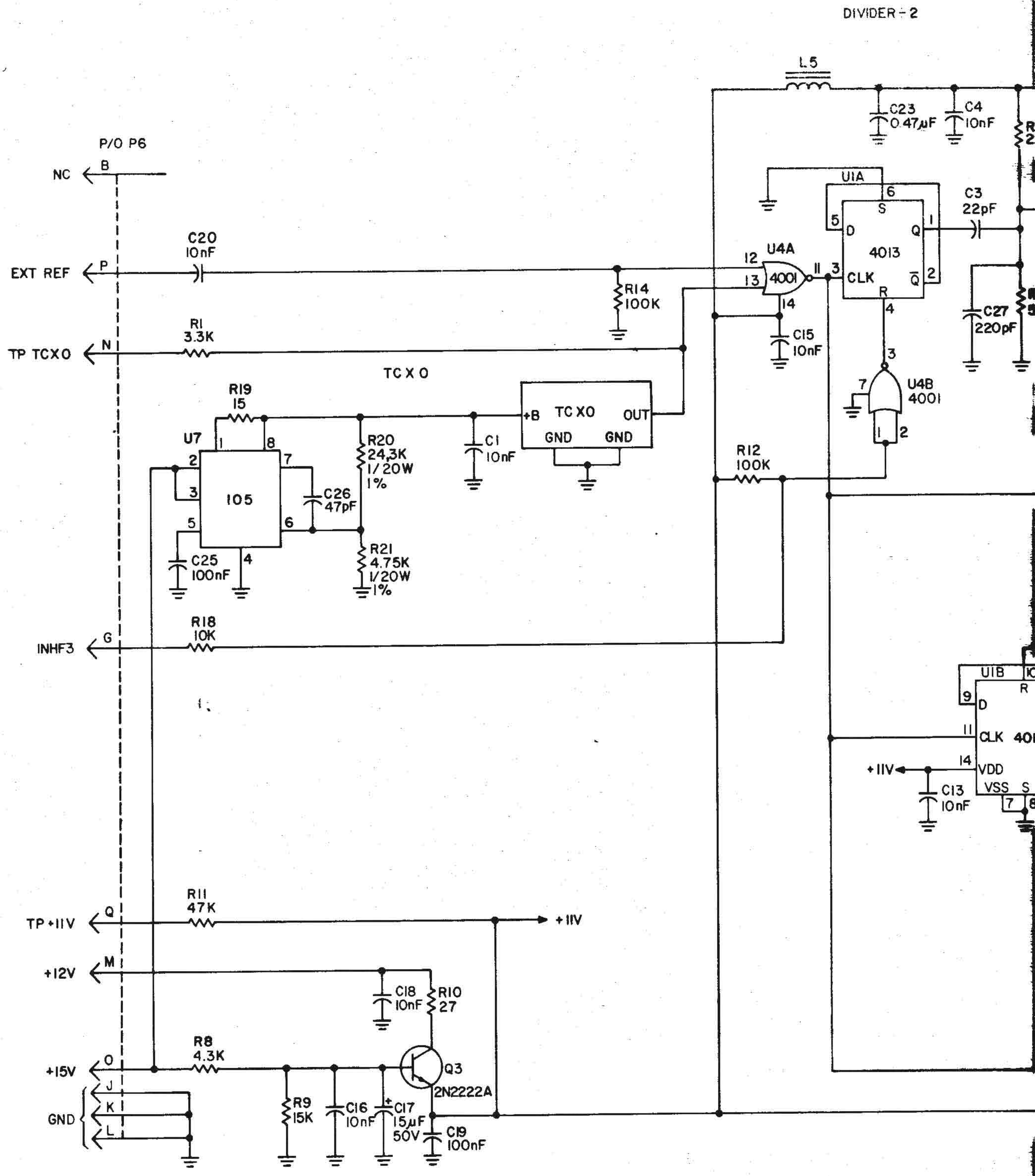


Fig. 2-50. Module REF 1A3A6, block diagram

(2) 10.5-MHz signal (fig. 2-51). The 3.5-MHz signal is applied, via C8, to the tripler circuit consisting of transistor Q2. The collector tuned circuit, comprised of T2 and C10, resonates at the third harmonic of the input signal, 10.5 MHz. The third-harmonic component of the current flowing through the transistor is enhanced by the series resonant circuit comprised of L3 and C12. The output signal is taken from a tap of T2 and connected to pin I. The supply voltage for this stage is supplied by module USB 1A3A3 when operating in the USB mode. Resistors R5, R6 supply



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A3A6:
2. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE IN OHMS, 5%, 1/8W.
3. R15 IS FACTORY SELECTED, VALUES 180, 240 & 390.
4. C22 IS FACTORY SELECTED, VALUES 3.3pF, 5.6pF & 8.2pF.

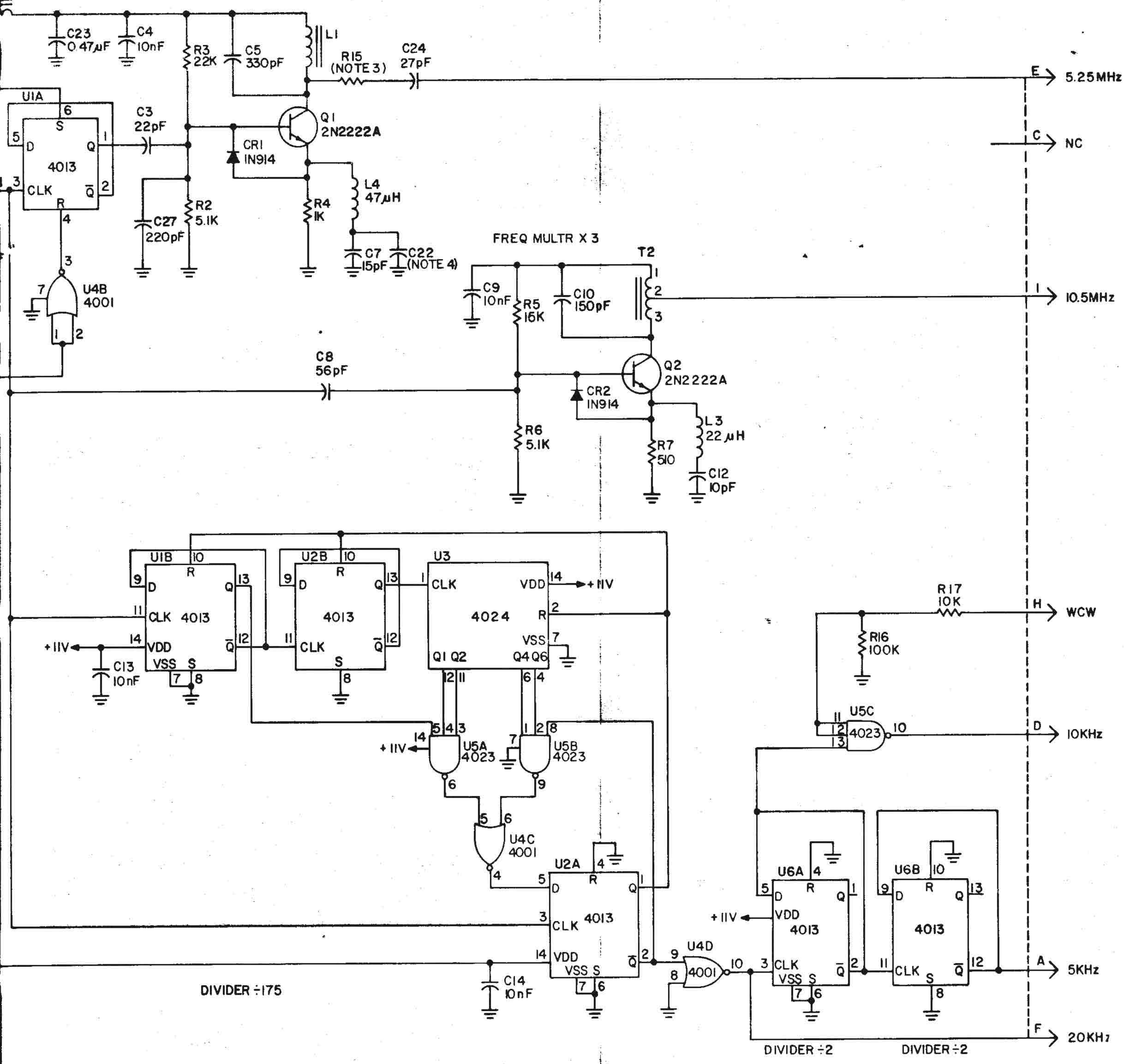


Fig. 2-51. Module REF 1A3A6, schematic circuit diagram

bias current. CR2 protects Q2 base-emitter junction against reverse voltage.

(3) 5.25-MHz carrier (fig. 2-51). The frequency of the TCXO output signal is divided by 2 by flip-flop U1A, and the resulting 1.75 MHz signal is applied to a tripler circuit built around Q1. The tripler circuit is similar to that used for 10.5-MHz generation. The DC supply voltage of Q1 is filtered by L5, C4, and C23.
The operation of divider U1A can be inhibited by a low level applied at pin G (INH F3 line). This level is inverted by U4B and applied to the reset input of U1A. The low level at pin G appears during AM receive operation, when the 5.25 MHz is not required.

(4) 20-kHz reference (fig. 2-51, 2-52). This signal is derived by dividing the frequency of the 3.5-MHz signal by 175, by means of frequency dividers U1B, U2, U3, U5A, B and U4C, C. U1B and U2B are D-flipflops, connected as dividers-by-2. U3 is a seven-stage binary counter: Q1 is the output of the first stage and Q6 is the output of the sixth stage. The 3 counters, U1B, U2B and U3, are connected as a binary ripple up-counter.
Figure 2-52 presents typical waveforms. Assuming that a division cycle just ended, the counters U1B, U2 and U3 start counting up, until the counter outputs reach the state 10101101 (this represents the state of the divider outputs, output Q6 of U3 being the most significant digit). This state is the binary representation of the decimal number 173. Reaching this number means that 173 input pulses were received; after this number of input pulses, the output of gate U4C rises to the high level. On the 174-th input pulse, this level is transferred to the Q-output of D-flip-flop U2A and immediately resets all counters to 0.....0. Simultaneously, the fall of $\overline{Q}$ output of U2A causes the output of U4C to return to the low level. On the 175th input pulse, this level appears at the Q output of U2A and releases the reset line. The counter is then ready for the next division cycle. The negative pulse appearing at the output of U2A is inverted by U4D and appears at pin F.

(5) 10-kHz reference (fig. 2-51). The frequency of the 20-kHz signal is halved by D-flipflop U6A, which is connected as a divide-by-2. The resulting 10-kHz signal is applied to the U5C input. The signal will be transferred to pin D only when WCW (CW) control line (pin H) is high (this occurs in CW operation).

(6) 5-kHz reference (fig. 2-51). The frequency of the 10-kHz signal is divided by U6B, and the resulting 5-kHz signal appears at pin A.

(7) Transistor Q3 supplies DC power to the 5.25-MHz multiplier and to the division circuits. Its output voltage (+11V) is determined by the ratio of R8 to R9. C19 filters the output voltage.

2-18. Module LOL 1A3A4 (fig. 2-53 through 2-56)

Review para. 2-4, for an analysis of the synthesizer block diagram.

a. Block Diagram Analysis (fig. 2-53). Module LOL 1A3A4 contains a phase-lock loop which provides the low frequency reference signal (LOF) for module SUM 1A3A5. The LOF signal frequency may be varied in 100-Hz increments in the frequency range of 30.0 to 49.9 kHz, according to the digital frequency information provided by selecting the 10-kHz, 1-kHz, and 100-Hz digits. The reference frequency used by this module is 5 kHz.

The 5-kHz reference is applied to a phase detector, together with the signal derived by dividing the VCO output frequency by the programmable frequency divider. In normal operation (locked mode), the phase detector provides a control voltage proportional to the phase difference between its two

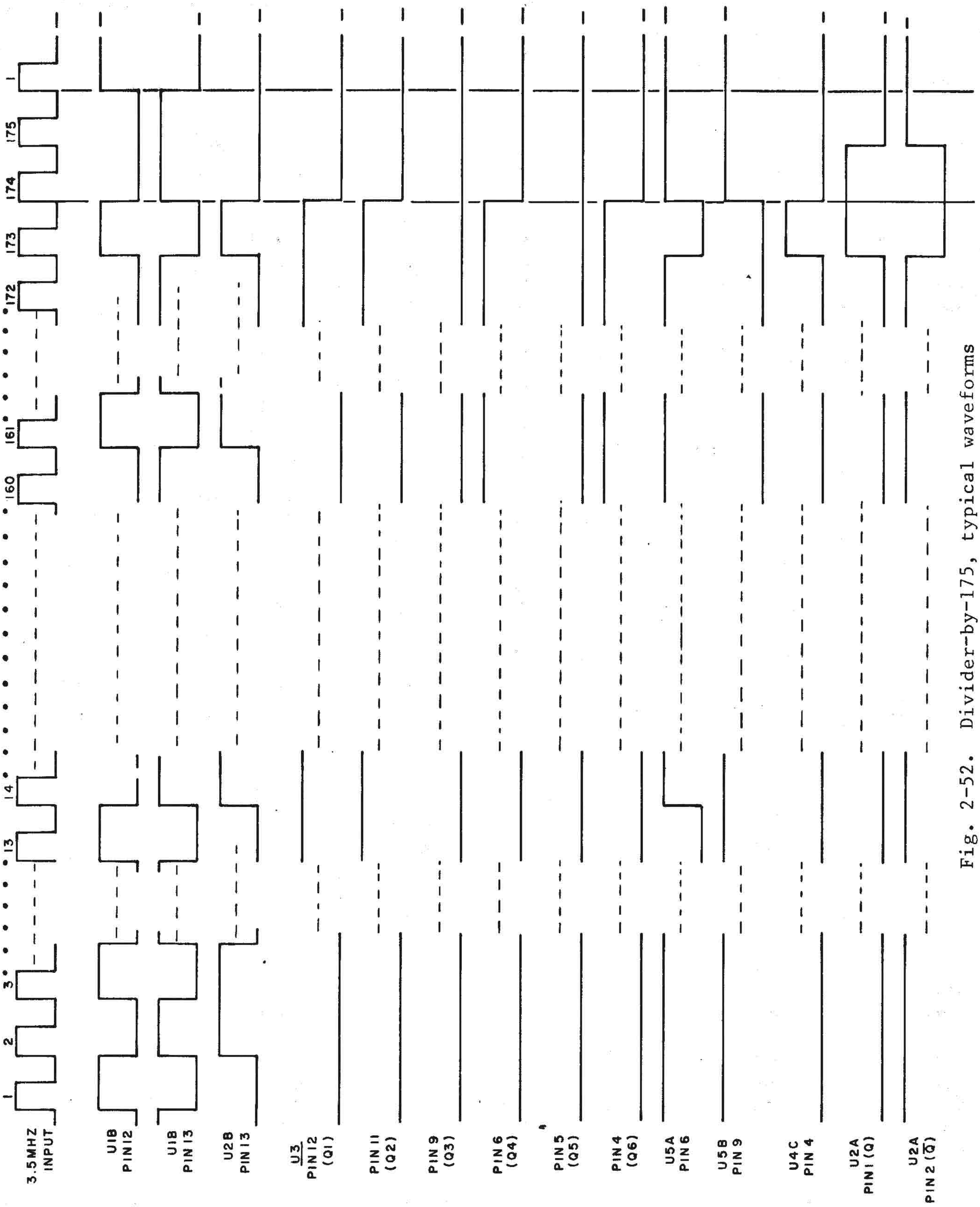


Fig. 2-52. Divider-by-175, typical waveforms

aforementioned input signals. The control voltage is filtered by the loop filter and then applied through a buffer to the control input of the VCO. In case lock is lost, the phase detector provides a constant output level (high or low, according to the frequency difference between the input signals), which causes the VCO frequency to sweep toward the desired frequency. After the VCO frequency is sufficiently close to the desired frequency, the detector returns to the normal mode and the resulting control voltage locks the VCO at the desired frequency.

The VCO output frequency (within the 1.5 to 2.495 MHz range) is divided by 50 and the resulting 30-to-49.9 kHz signal, called LOF, is sent to the SUM 1A3A5 module.

The VCO output frequency is also divided by the programmable frequency divider. The division ratio, K, depends on the 100-Hz, 1-kHz, and least significant bit (LSB) of the 10-kHz frequency information lines: the ratio thus varies between 300 and 499, according to the following relationship:

$$K = N_{100} + 10N_1 + 100(3 + X30)$$

where:

- N_{100} - the 100-Hz digit
- N_1 - the 1-kHz digit
- X30 - the LSB of the 10-kHz digit.

The circuits contained in module LOL 1A3A4 are powered by +11V, provided by a local voltage regulator.

b. Circuit Analysis (fig. 2-54, 2-55, 2-56).

(1) Phase detector (fig. 2-54, 2-55). The phase detector is U6. U6 is a monolithic phase lock loop, which contains a digital phase/frequency detector; the other circuits contained in U6 are not used.
The digital phase/frequency detector senses the time (phase) difference between the rising edges of the divider output waveform and that of the 5-kHz reference, applied to pin A.
If the reference signal rises before the divided signal, positive pulses (+10V) appear at pin 13 of U6. The pulse width is equal to the time difference between the rising edges of the signals. Low pulses (shorts to ground) appear if the divided VCO signal rises before the reference signal. When both input signals switch simultaneously, the output (pin 13) assumes a high-impedance state. This is the normal (phase detector) operation mode, which continues as far as the regular interleaved sequence of input pulses is not disrupted, that is, between each two consecutive pulses of the 5-kHz reference appears one pulse from the divider, and vice-versa. If two consecutive pulses appear on one line without having a pulse on the other line, the phase detector switches to the frequency mode, and its output remains at a high or low level, until the normal sequence appears at the phase detector input.
Fig. 2-55 shows typical waveforms.

(2) Loop filter and buffer. The phase detector output is filtered by R10, R11, R12, C9 and C10, and then applied to the gate of the FET source-follower, Q2. The source voltage is applied to the emittter follower, Q3. The voltage appearing at the emitter of Q3 is the VCO control voltage.
The control voltage increases when the 5-kHz reference signal precedes the divider output pulse.

(3) VCO circuit (fig. 2-54). The voltage-controlled oscillator (VCO) of the LOL is a Hartley oscillator, built around Q1. The oscillation frequency is determined by the resonant frequency of the tuned circuit formed by transformer T1 and the equivalent capacitance of the series-connected variable capacitance diodes CR1 and CR2. The oscillation frequency may be varied between 1.5 and 2.495 MHZ

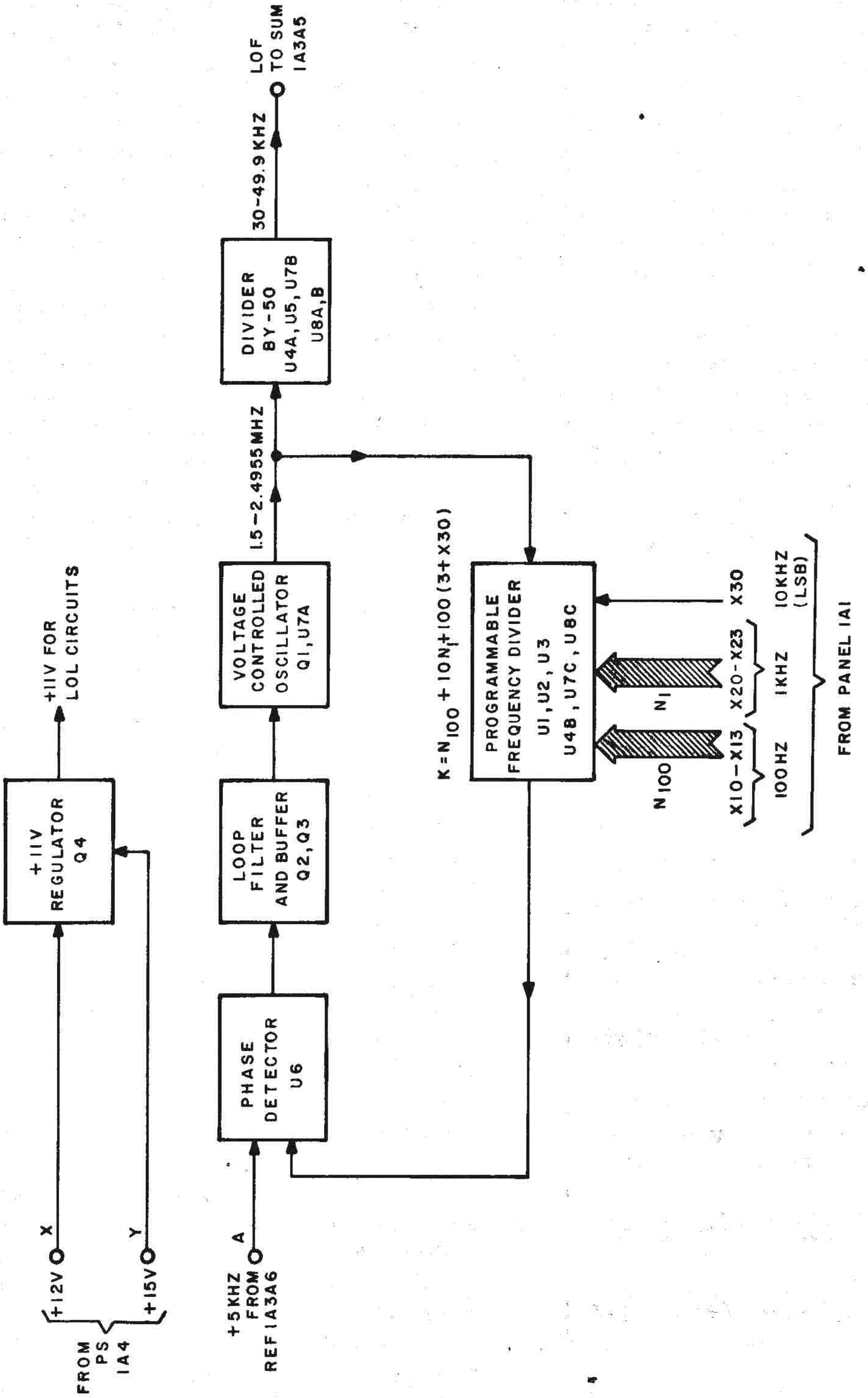
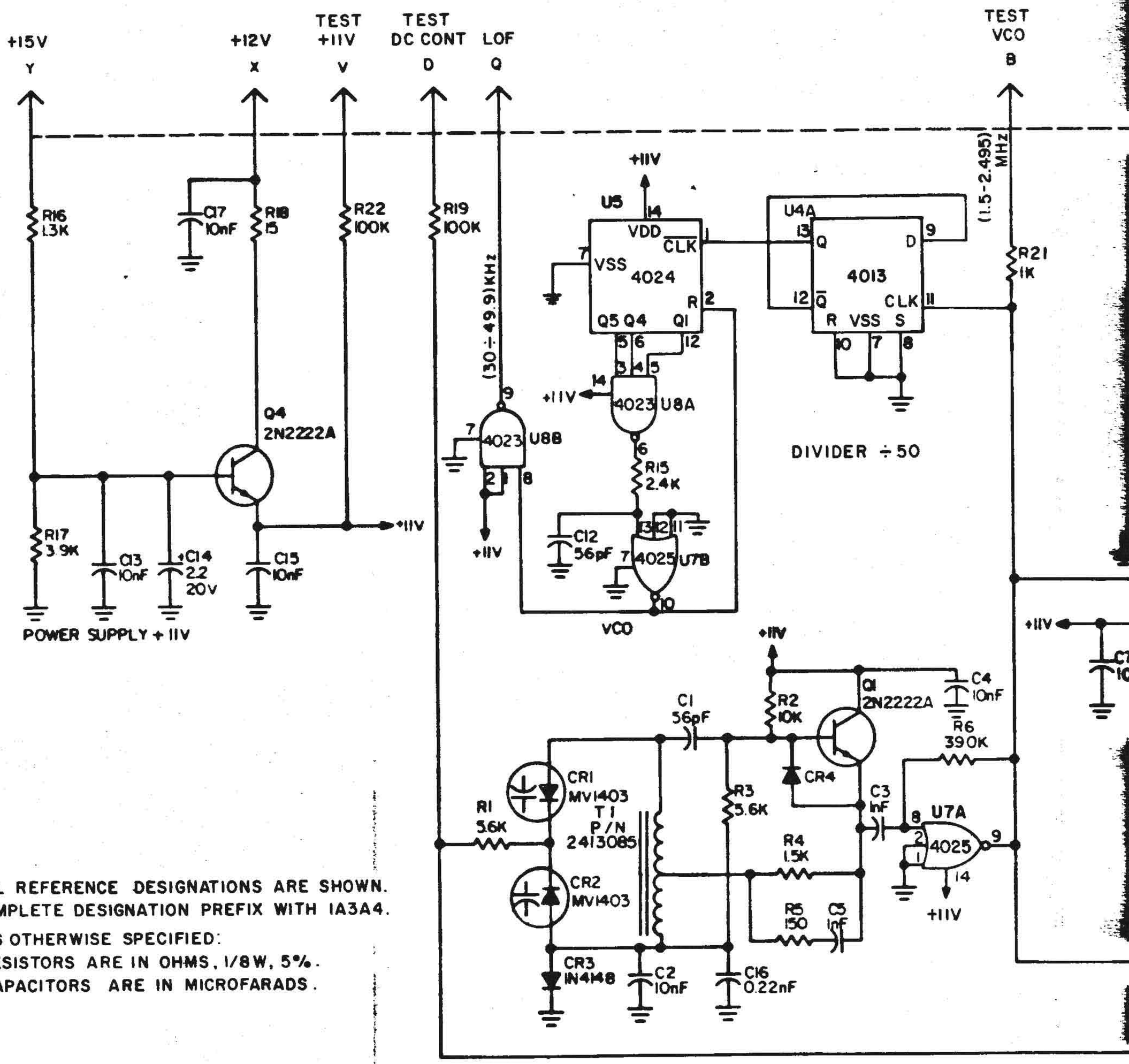


Fig. 2-53. Module LOL 1A3A4, block diagram



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A3A4.
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, 1/8W, 5%.
   ALL CAPACITORS ARE IN MICROFARADS.

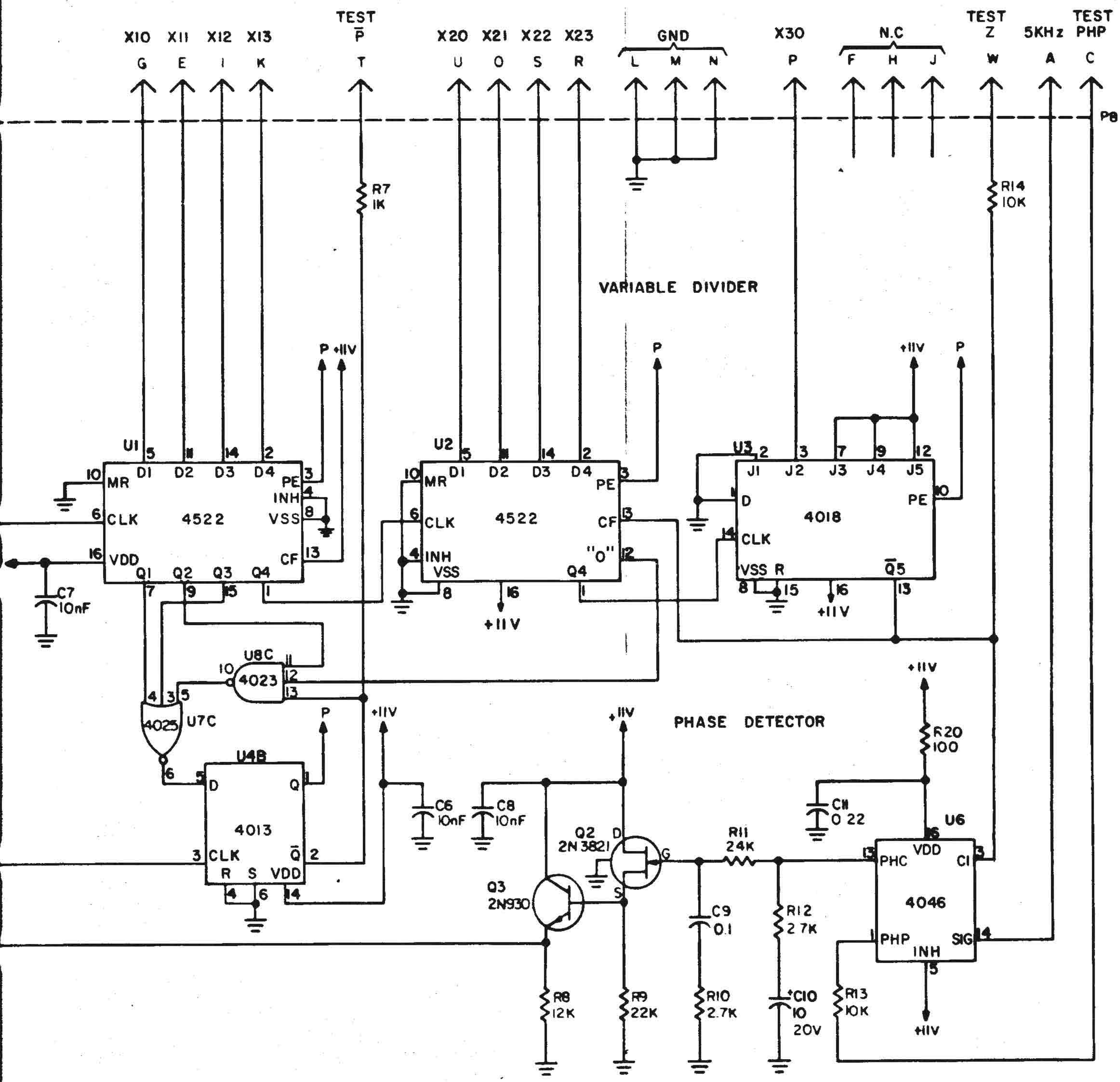


Fig. 2-54. Module LOL 1A3A4, schematic circuit diagram

by varying the control voltage applied to the variable capacitance diodes CR1 and CR2.

For example, assuming as in (2) above that the phase detector output voltage increases, the capacitance of variable capacitance diodes CR1, CR2, decreases. In consequence, the VCO frequency increases until the phase difference between VCO and reference signals is nulled. Similar corrective action takes place if the divided VCO signal rise precedes the reference signal rise. Since the phase detector output assumes a high-impedance state (no changes in the control voltage) only when both its input signals rise simultaneously, the action described above locks the VCO frequency to a multiple of the 5-kHz reference frequency - the multiplication number being equal to the variable divider division ratio, K.
The output of Q1 is buffered by the gate U7A, and applied to the fixed divider (U4A, U5) and to the PLL programmable divider input (U1).

(4) Divider-by-50 (fig. 2-56). The operation of this circuit is similar to that of the divider-by-175 contained in module REF 1A3A6 (see para. 2-20). The divider consists of U4A, U5, U8A and U7B. The VCO output signal is applied to the input of U4A. D-flipflop U4A operates as a divide-by-2. Its output is applied to the 7-stage binary counter U5. Gate U8A decodes the state 11001 (binary equivalent of 25) and causes a low level to be applied via the R15, C12 delay network, to gate U7B. This causes a narrow positive pulse to appear at the U7B output for every 50 input pulses to U4A. The output pulses of U7B also resets U5. These pulses are inverted by U8B and applied to pin Q (LOF line). Fig. 2-56 shows typical waveforms.

(5) Programmable divider (fig. 2-54). This divider is programmed by the binary-coded decimal (BCD) information received from the front panel switches. The least significant bit of the 10-kHz digit presets a Johnson decimal counter, U3. The information from the 1-kHz and 100-Hz digits presets BCD down-counters U2 and U1, respectively. The division ratio varies between 300 to 499. The division cycle is initiated when the preset line, driven by U4B, returns to the low level. The counters U1, U2 then start counting down from the preset state.

(a) After $N_{100}+1$ (N_{100} is the 100-Hz digit) pulses (VCO cycles), output Q4 of U1 completes one cycle (U1 is then in the state 1001). The resulting pulse is fed to the clock input of U2. After the first pulse (whose appearance depends on the presetting of U1), the Q4 output of U1 completes one cycle for every 10 VCO cycles.

(b) After $N_{100}+1+10N_1$ clock pulses (VCO cycles) (N_1 is the 1-kHz digit), one output pulse is fed by Q4 of U2 to the clock input of U3. After that, one clock pulse appears for every 100 VCO cycles. Output Q5 of U3 will rise to the high level after 2 clock pulses, if X30 is low (even 10-kHz digit) or 3 clock pulses, if X30 is high (odd 10-kHz digit).

(c) The total number of clock pulses (VCO cycles), required to obtain a high level at output Q5 of U3 is:

$$N_{100}+1+10N_1+100(2 + X30)$$

When this happens, U1 and U2 are in state 1001 (the binary equivalent of 9).

(d) After 10 x 9 = 90 input clock pulses, U1 will return to 1001, while U2 will be in state 0000. Seven more pulses cause U1 to arrive to state 0010. The output of gate U8C will fall to the low level, and that of U7C will be high. Summarizing, this state is reached after:

$N_{100}+1+10N_1+100(2+X30)+10x9+7=$
$N_{100}+10N_1+100(3+X30)-2$ input pulses.

(e) The high output of U7C,

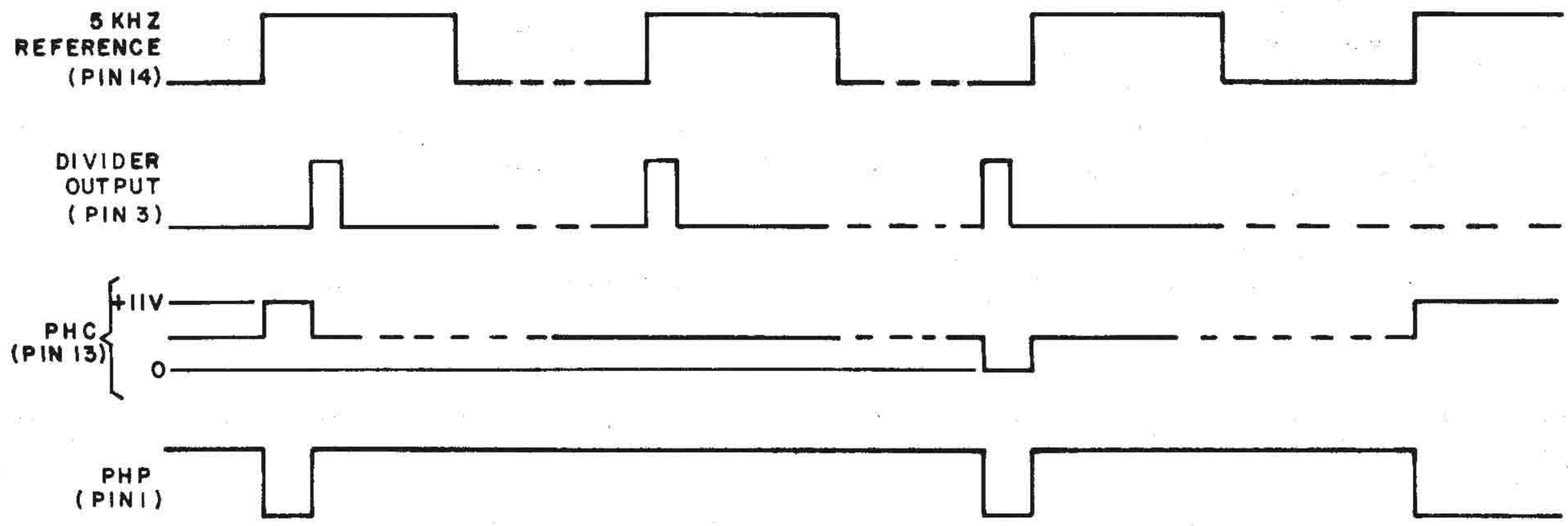


Fig. 2-55. Phase detector U6, typical waveforms

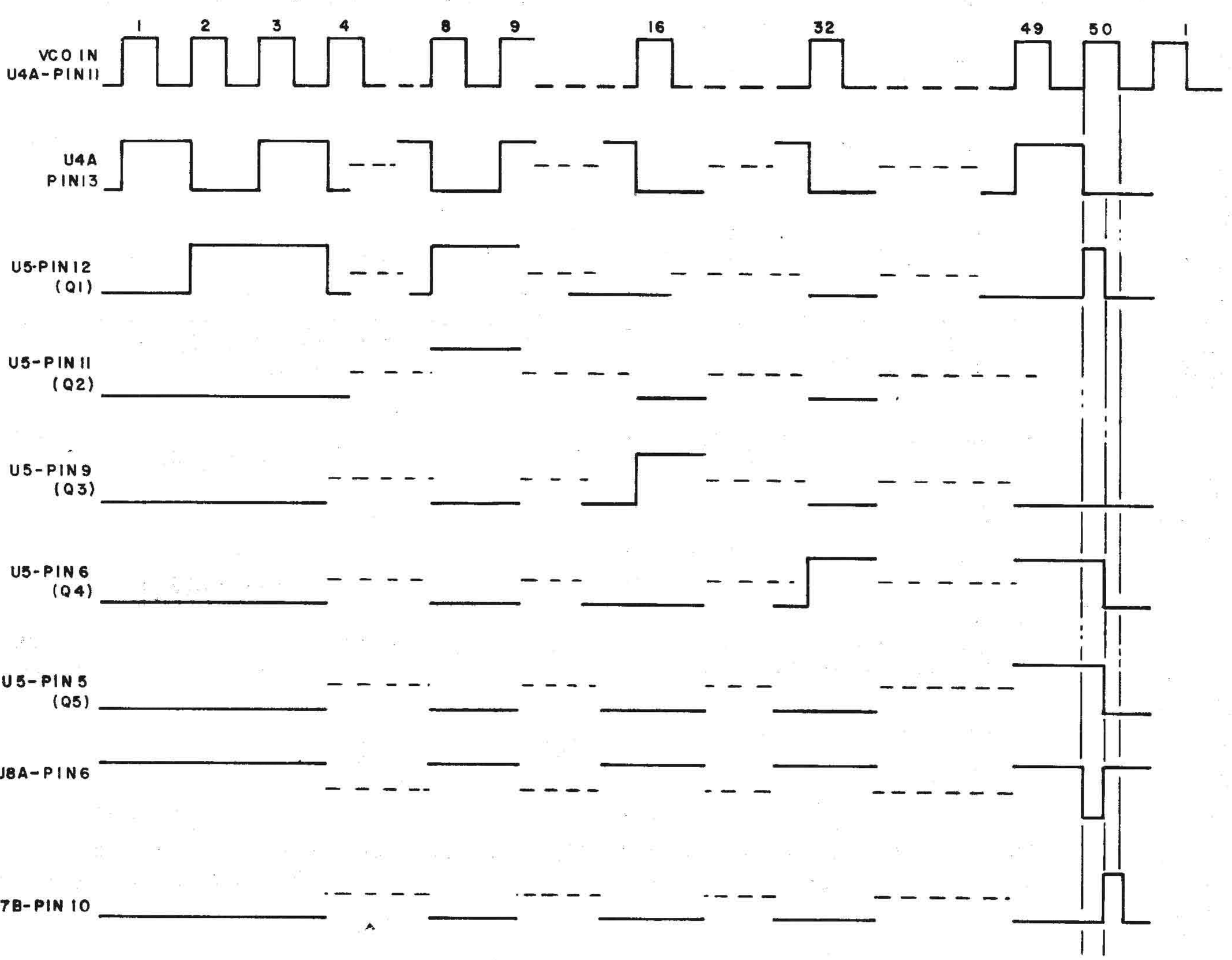


Fig. 2-56. Divider-by-50, typical waveforms

appearing at the $\overline{Q}$ output of U4B after one more clock pulse (VCO cycle), causes presetting of the counters. The low level at the Q output of U4B causes the output of U7C to return to a low level. The next input clock pulse (the last pulse of the division cycle) causes this level to be transferred to U4B Q output, thereby releasing the preset line. This permits the new division cycle to begin on the next VCO cycle.
The division ratio is:

$$K = N_{100} + 10N_1 + 100(3 + X30)$$

(6) Transistor Q4 supplies +11V to the digital circuits; its base drive is supplied from the +15V supply (filtered by C13 and C14) via R16 and R17.

2-19. Module USB 1A3A3 (fig. 2-57, 2-58)

Refer to para. 2-4 for an analysis of the synthesizer block diagram.

a. Block Diagram Analysis (fig. 2-57). Module USB 1A3A3 generates the F2 frequency and a 104.1-MHz frequency for module SUM 1A3A5 (see fig. 2-4). The module also contains a regulator which provides +17V for circuits in module VCP 1A3A1. The operation of the module is controlled by the USB line. When this line is grounded (USB mode selected at the front panel), the output of the +5V regulator appears on the +5V USB line, which powers the circuits in the USB section. Concomitently, +12V is connected to the 10.5-MHz line, thereby enabling the 10.5-MHz tripling in module REF 1A3A6. When the USB line is open-circuited (LSB mode selected at the front panel), the +5V is connected to the +5V LSB line, thereby energizing the LSB section, and the 10.5-MHz line is disconnected.

When operating in the LSB mode, the 104.1-MHz crystal oscillator is turned on, and its signal passes through a diode switch to the output amplifier, which drives the F2 line. The 104.1-MHz signal also passes to the LSB amplifier, which drives the 104.1-MHz line for module SUM 1A3A5.

When operating in the USB mode, the 114.6-MHz crystal oscillator is turned on, and its signal passes through a diode switch to the output amplifier which drives the F2 line. The 114.6-MHz signal is also applied to the USB amplifier. The amplified signal is mixed with the 10.5-MHz signal received from module REF 1A3A6, and the resulting difference signal at 104.1-MHz is sent via the 104.1-MHz line to module SUM 1A3A5.

b. USB Path Circuit Analysis (fig. 2-58).

(1) 114.6-MHz oscillator. The 114.6-MHz frequency is generated by a crystal oscillator built around Q1. The transistor operates as a common-base amplifier, with positive feedback applied from a tap of the collector tuned circuit, through the crystal, to its emitter. The bias to Q1 is supplied via R1, R2 and is temperature-compensated by CR3. C6, C7 are RF bypass capacitors. The DC voltage to the oscillator is supplied via Q9 and L2. Q9 saturates when the USB line (pin D) is low (in USB mode), thereby applying +5VDC on the 5V USB line to Q1. Current also flows from the +5V USB line through R25, CR1 and R24, causing conduction of RF switching diode CR1, while CR2 is reverse-biased. CR1 then connects the output signal of the 114.6-MHz oscillator to the F2 output amplifier, Q6.

(2) F2 amplifier. The F2 amplifier is built around Q6. The input signal is coupled through C35. R21 and R22 supply base bias. R23, bypassed at RF by C37, is the emitter bias resistor. The output signal develops across T13 and is coupled through C36 to connector P18. L14, C43 and C52 filter the +5V supply line of Q6.

(3) USB amplifier and mixer.

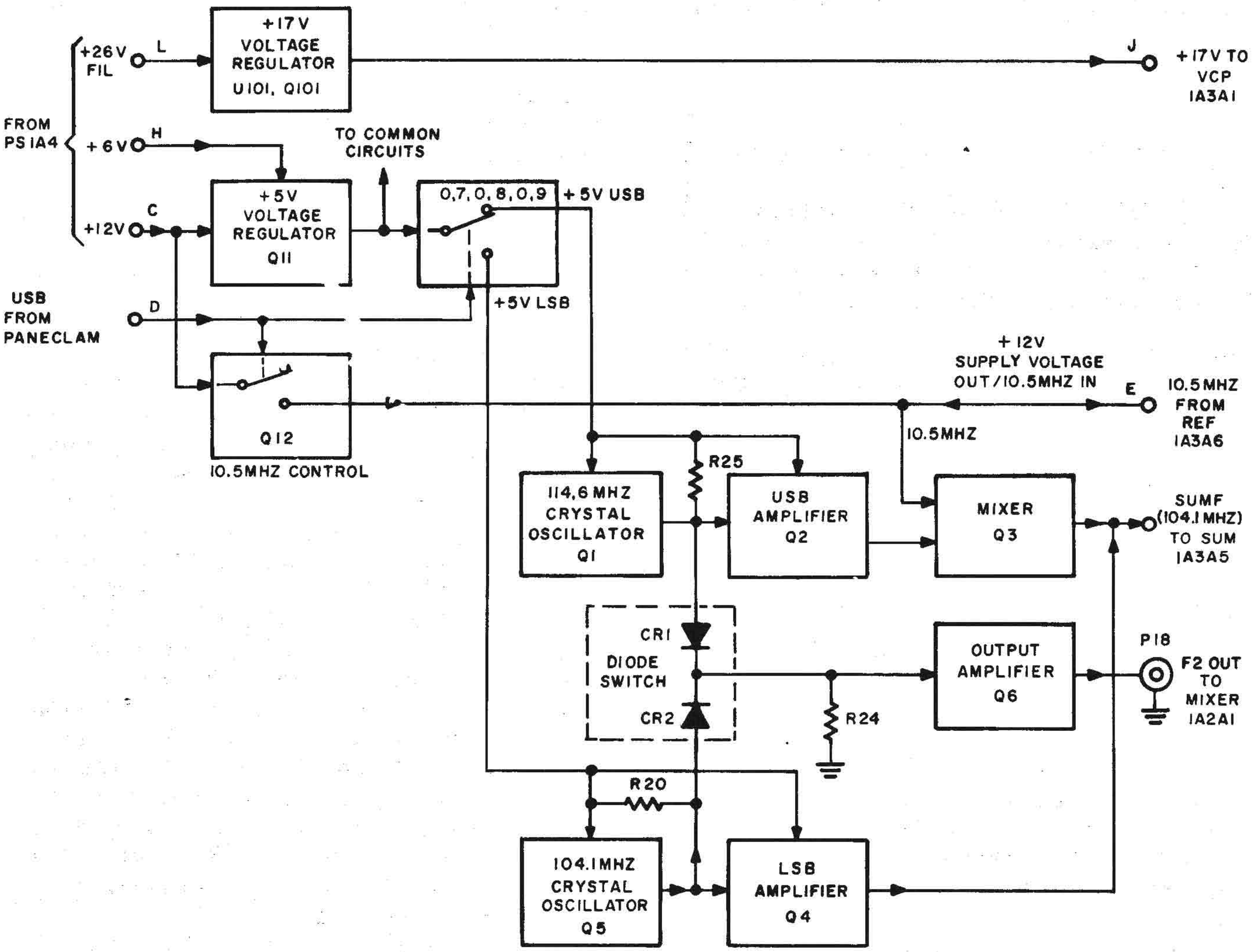
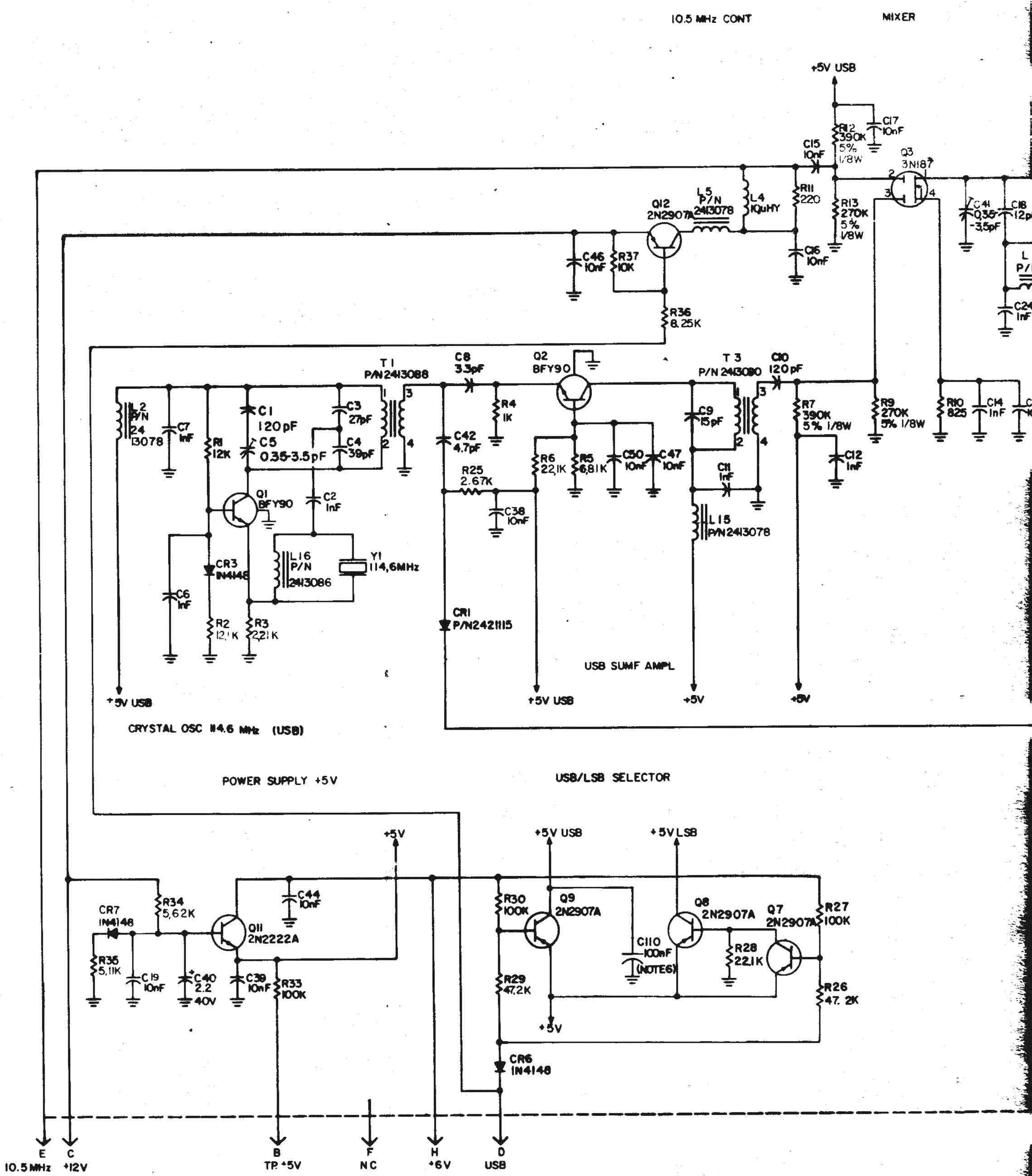


Fig. 2-57. Module USB 1A3A3, block diagram



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH 1A3-A3.
2. ALL RESISTORS ARE IN OHMS, 1/20W, 1% UNLESS OTHERWISE SPECIFIED.
3. R102 IS FACTORY SELECTED VALUES 34.8K & 36.5K.
4. R103 IS FACTORY SELECTED RESISTOR 3.92K & 4.02K.
5. C49, C50, C52 & C53 ARE CHIP CAPACITORS (24-12162)
6. C110 IS CHIP CAPACITOR (24-12163)
7. ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

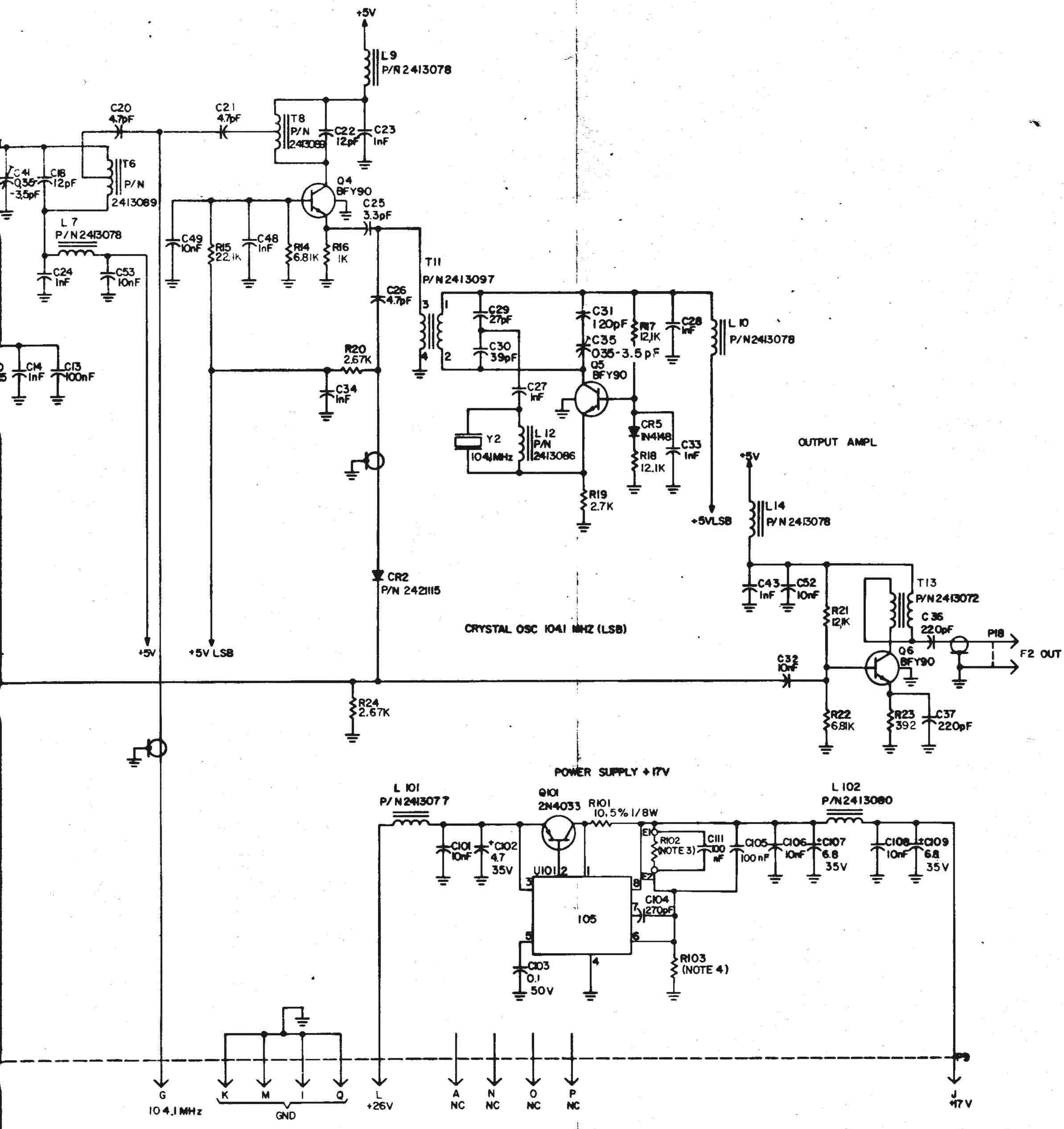


Fig. 2-58. Module USB 1A3A3, schematic circuit diagram

The output signal of Q1 is also coupled through C8 to the common-base amplifier Q2. The amplified signal is applied through the tuned transformer T3 to one of the gates of the MOSFET tetrode Q3. The second gate of Q3 receives the 10.5-MHz frequency from the tripler in module REF 1A3A6 (via pin E). The DC voltage to the tripler is supplied via Q12 (which saturates when the USB line is low), L5, L4, and R11. At the drain of Q3, a tuned circuit (C18, T6, C41) filters the 104.1-MHz difference frequency and passes it to pin G.

Note that when the USB is selected, transistor Q4 is not powered.

c. LSB Path Circuit Analysis (fig. 2-58). When LSB operation is selected, the USB control line rises to +12V and Q12 and Q9 cut off. Q7 also cuts off, and Q8 saturates due to base current flow via R28. The 104.1-MHz oscillator, designed around Q5 (identical to the 114.6-MHz oscillator) is activated, and its output signal is connected, via CR2 (forward-biased by the current flowing from the collector of Q8 through R20 and R24) to the base of the F2 amplifier, Q6. The 104.1-MHz signal is also connected to the common-base amplifier Q4. The Q4 amplifier output signal, taken from a tap of T8 in its collector circuit (T8, C22), is passed, via C21, to pin G.

d. +5V Regulator (fig. 2-58). The +5V supply voltage for the oscillator and amplifiers is supplied by Q11. The base drive for Q11 is supplied from the +12V supply (pin C), via the voltage divider comprised of R34, R35 and temperature-compensation diode CR7, and filtered by C40 and C41.

e. +17V Regulator (fig. 2-58). The +17V regulator consists of U101 and Q101. The integrated circuit regulator U101 controls booster transistor Q101, which reduces the higher battery voltage, applied to pin L, to the regulated +17V voltage. This voltage is filtered by C107, L102, C108, and C109 and connected to pin J. R101 is the current limiting sense resistor. The voltage divider comprised of R102 and R103 (both selected resistors), determines the output voltage.

2-20. Module SUM 1A3A5 (fig. 2-59, 2-60, 2-61)

Refer to paragraph 2-4 for an analysis of the synthesizer block diagram.

a. Block Diagram Analysis (fig. 2-59). Module SUM 1A3A5 contains a phase-lock loop, which adds the 30-to-49.9-kHz variable output frequency of module LOL 1A3A4 to the 104.1-MHz generated by the USB 1A3A3 module (refer to fig. 2-4 and to para. 2-22). The module also contains the digital part of the main phase detector; the other parts are contained in module VCP 1A3A1. The LOF signal received from module LOL 1A3A4 is applied to one of the phase frequency detector inputs, the other input is the difference between the SUMF and the 104.1-MHz signal received from module USB 1A3A3. The phase/frequency detector generates a control voltage. In normal operation (locked mode), the phase detector provides a control voltage proportional to the phase difference between its two aforementioned input signals. The control voltage is filtered by the loop filter and applied through a buffer to the control input of the voltage controlled crystal oscillator (VCXO). In case lock is lost, the phase detector provides a constant output level (high or low, according to the frequency difference between the input signals), which causes the VCO frequency sweep toward the desired frequency. After the VCXO frequency is sufficiently close to the desired frequency, the phase detector returns to the normal mode and the resulting control voltage locks the VCXO at the desired frequency.

The VCXO output signal, in the 20.826 to 20.82998 MHz frequency range, passes through a frequency quintupler to a tu-

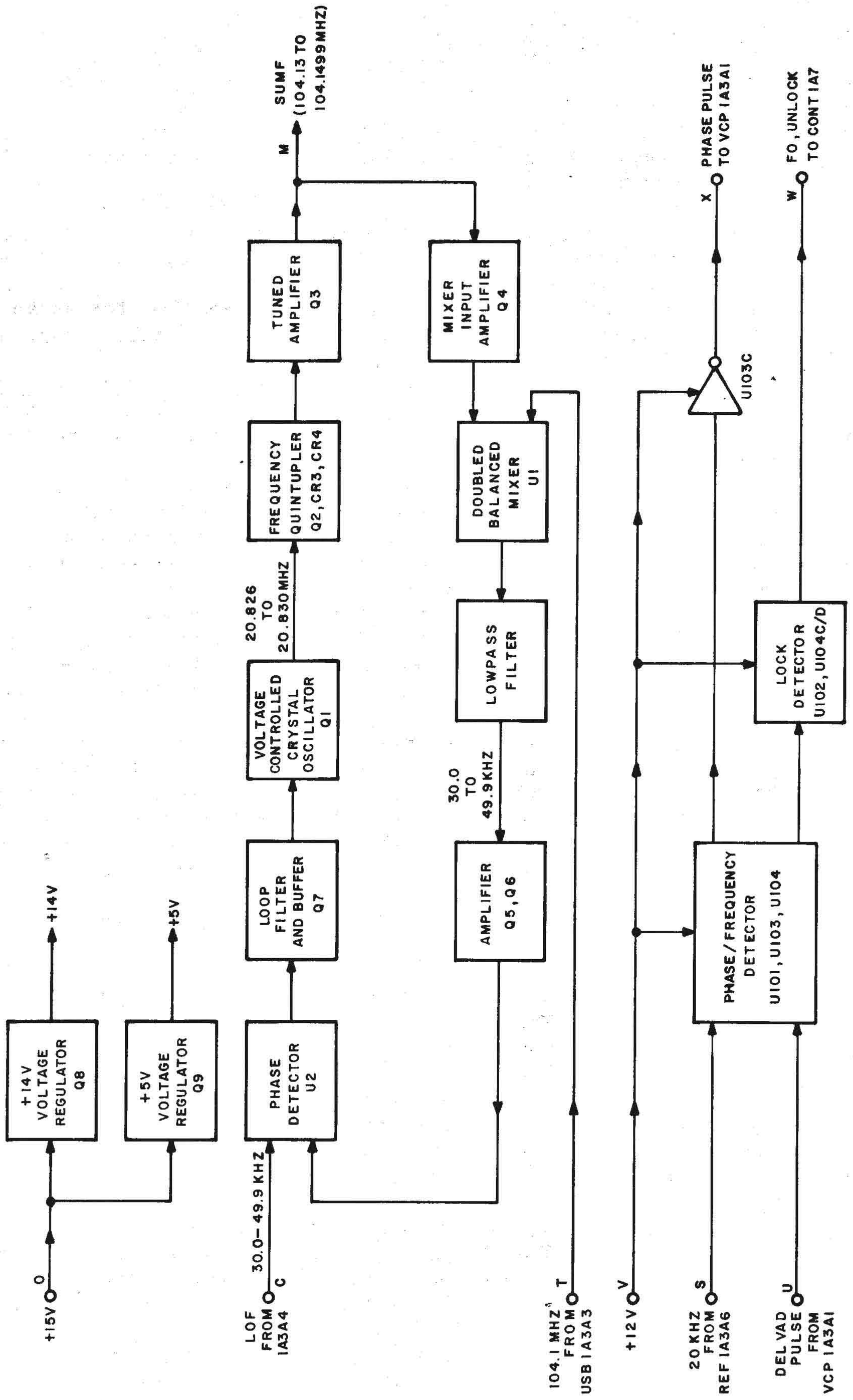


Fig. 2-59. Module SUM 1A3A5, block diagram

ned amplifier. The frequency of the signal, called SUMF, varies between 104.13 and 104.1499 MHz, according to the frequency of the LOF signal. The SUMF signal is sent to module VCP 1A3A1, and is also applied, through an amplifier, to a double-balanced mixer. In the mixer, the SUMF signal is mixed with the 104.1-MHz signal from module USB 1A3A3, and the resulting difference frequency is applied to the phase detector.

In addition to the circuits which generate the SUMF signal, module SUM 1A3A5 also contains the digital part of the main phase/frequency detector of the synthesizer PLL (the analog part being contained in module VCP 1A3A1). This detector receives the 20-kHz reference signal from module REF 1A3A6 and the DEL VAD signal from module VCP 1A3A1, and generates pulses (on the PHASE PULSE line) whose width is proportional to the difference between their rising edges; should the VCO in module VCP 1A3A1 lose lock, the operating mode of the detector changes and it provides a constant output level (high or low, according to the difference between the instantaneous VCO frequency and the desired lock frequency).

A digital lock detector monitors the phase/frequency detector output, and applies a high level on the FO UNLOCK line when loss-of-lock is detected.

The circuits contained in module SUM 1A3A5 are powered by two voltage regulators, which supply +14 and +5V.

b. <u>SUMF Generation, Circuit Analysis (fig. 2-60).</u>

(1) VCXO circuit. The SUMF output frequency is derived from the signal supplied by the VCXO built around Q1. Its frequency may be varied, in the 20.826 to 20.82998 MHz range, by the control voltage applied to the variable capacitance diode CR2. CR2 is part of the resonant circuit formed by the crystal X1, L1, and C2. The VCXO is a Colpitts oscillator with positive feedback determined by the ratio of C4 to (C5 + C3). R3, R4, CR7, and R6 form the bias circuit for Q1. The collector signal of Q1 develops across R5 and is coupled via the capacitive voltage divider C8, C9 to the base of Q2. Diode CR8 limits the reverse voltage across the base-emitter junction of Q1.

(2) Frequency quintupler. The VCXO signal is amplified by transistor Q2 and distorted by Schottky diodes CR3, CR4. The fifth harmonic of the resulting signal is filtered by the tuned coupled circuits T5, C12 and C13.

(3) Tuned amplifier. The filter output, in the range of 104.13 to 104.1499 MHz, is coupled through C14 to the base of Q3. The collector signal is coupled through the tuned transformer T8 to pin M (SUMF signal). C20 is used to adjust the SUMF signal level. Bias for Q3 is provided by R10 and R11. The supply voltage is filtered by L16 and C17.

(4) Mixer and associated amplifiers. A sample of the SUMF output signal is coupled from a separate winding of transformer T8, via C21, to the common-base amplifier stage built around Q4. The amplified signal appearing at the collector of Q4 is applied via transformer T9 and capacitor C27 to the carrier input of the double-balanced mixer U1. The second input to the mixer is the 104.1-MHz offsetting frequency signal arriving from module USB 1A3AB at pin I.

The 30 to 49.9-kHz difference frequency appearing at the mixer output (pin 6) is filtered by C34, L11, L12, and C35, and then amplified by Q5 and Q6.

(5) Phase/frequency detector, loop filter and buffer. The collector of Q6 is coupled to one of the inputs of the phase/frequency detector in U2. The 30.0 to 49.9-kHz reference frequency received from module LOL 1A3A4 (pin C) is applied to the other input.

Operation of the phase/frequency detector is similar to that of the LOL 1A3A4 detector (see para. 2-21.b(1)). The output signal of the phase detector, appearing at pin 13, is filtered by the loop filter, comprised of R36, R38, R49, C41, C43 and C42. The filtered control voltage is buffered by Q7 and applied to the variable capacitance diode CR2. The control voltage generated by the PLL is of such magnitude as to cause the VCXO to oscillate at a frequency which is exactly 1/5th of the sum of the LOF and 104.1-MHz signal frequencies.

(6) Voltage regulators. Transistors Q8 and Q9 supply filtered +14V and +5V voltages. Q8 is biased to saturation through R41. Q9 is biased through the voltage divider consisting of R42, CR1, and R43.

c. Main Phase/Frequency Detector and Lock Detector (fig. 2-61). The phase/frequency detector which controls the VCO in module VCP 1A3A1 consists of U101, U103 A/B and U104 A/B. The lock detector consists of U102, U103C and U104 C/D. Typical waveforms are shown in fig. 2-61.

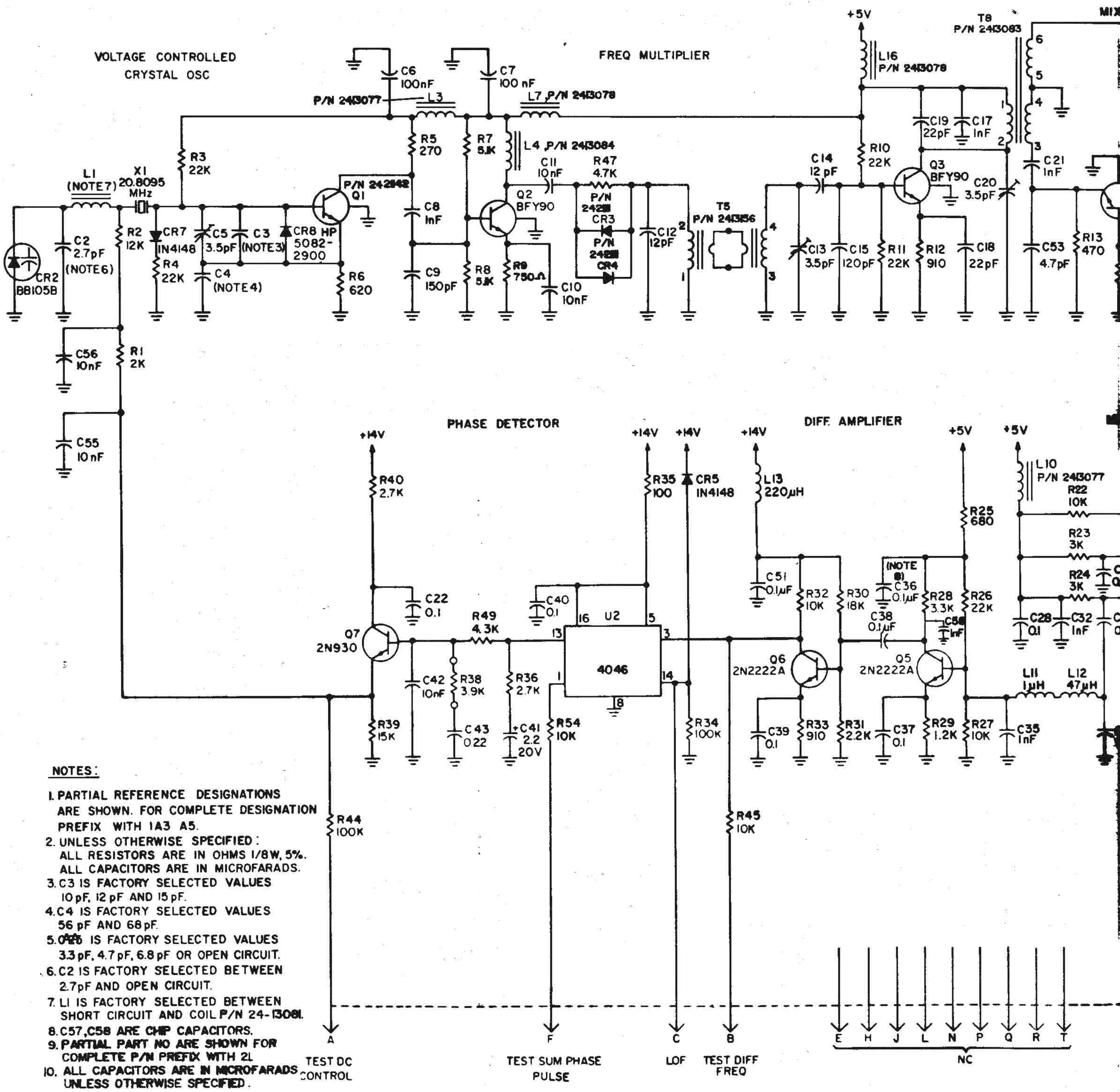
(1) Phase/frequency detector. The phase detector provides an output waveform (at pin X) whose duty cycle is proportional to the phase (time) difference between the rising edges of the 20-kHz reference and the DEL VAD pulse, which is received from variable divider VAD 1A3A2 through module VCP 1A3A1. The phase detector circuit consists of the input sampling flipflops U101A and U101B, the buffer flipflop, consisting of NOR gates U103A and U103B, and the output flipflop, consisting of NOR gates U104A and U104B.
U101A and U101B sample the positive transistions of the reference and variable inputs, respectively. This prevents dependence of the phase detector output waveform on the duty cycles of these signals.
The two NOR gates, U103A and U103B, form a set-reset flipflop. This flipflop registers which of the two input signals made a positive transition and triggers the output flipflop composed of U104A/B. Feedback from the gates U103A and U103B returns the Q-outputs of the flipflops U101A and U101B to a high level, after momentarily changing to low when a positive input transition occurs.
The NOR gates U104A and U104B form a set-reset flipflop, which registers and stores the momentary transitions of the U103A and U103B gates (the buffer flipflop):

(a) A positive transition at the output of U104A will occur only on a positive transition at the variable (DEL VAD) input which follows a positive transition at the reference input.

(b) A negative transition at the output of U104A will occur only on a positive transition at the reference input which follows a positive transition at the variable input.

(c) Conditions (a) and (b) imply that no change will occur following a transition at any input, if this transition was not preceded by a transition at the other input. This condition (two consecutive transitions at same input) may occur when a frequency difference exists between the two input signals. In this case, the output flipflop will remain in state "1" or "0" depending on which of the two input frequencies is higher.
When the input frequencies are equal, the low time of the U104A output equals the time (phase) difference between the positive transitions. The output of U104B is inverted by U103C and applied via pin X to the analog part of the phase/frequency detector which is contained in module VCP 1A3A1.

(2) Detailed circuit operation analysis. When the input frequencies are equal (e.g. pulses 1 through 4 in fig. 2-61), an alternating sequence of reference/DEL VAD pulse/reference/ etc., appears at the inputs. Let us assume that the last positive transi-



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A3 A5.
2. UNLESS OTHERWISE SPECIFIED: ALL RESISTORS ARE IN OHMS 1/8W, 5%. ALL CAPACITORS ARE IN MICROFARADS.
3. C3 IS FACTORY SELECTED VALUES 10 pF, 12 pF AND 15 pF.
4. C4 IS FACTORY SELECTED VALUES 56 pF AND 68 pF.
5. C25 IS FACTORY SELECTED VALUES 3.3 pF, 4.7 pF, 6.8 pF OR OPEN CIRCUIT.
6. C2 IS FACTORY SELECTED BETWEEN 2.7pF AND OPEN CIRCUIT.
7. L1 IS FACTORY SELECTED BETWEEN SHORT CIRCUIT AND COIL P/N 24-13081.
8. C57, C58 ARE CHIP CAPACITORS.
9. PARTIAL PART NO ARE SHOWN FOR COMPLETE P/N PREFIX WITH 2L
10. ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

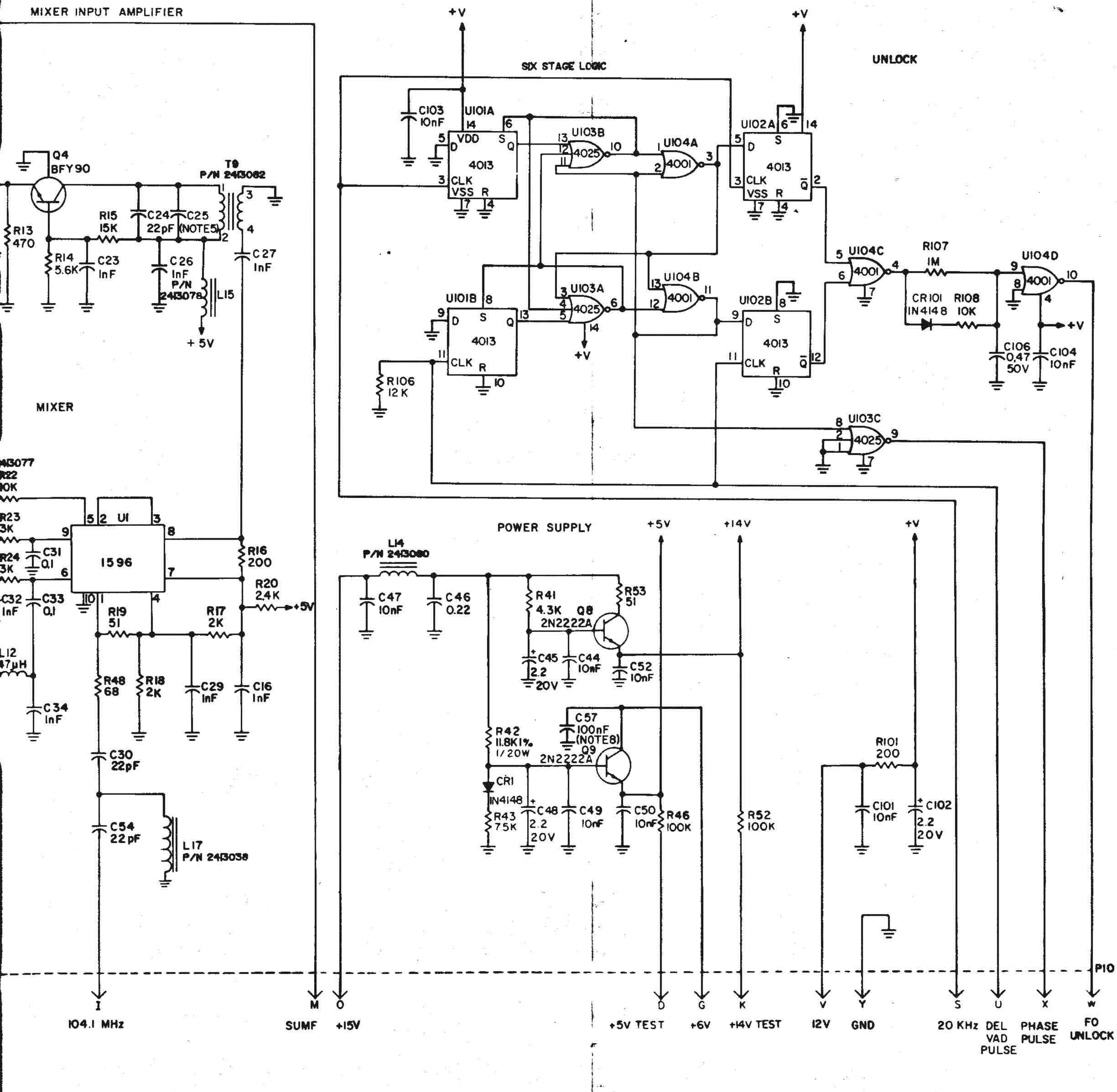


Fig. 2-60. Module SUM 1A3A5, schematic circuit diagram

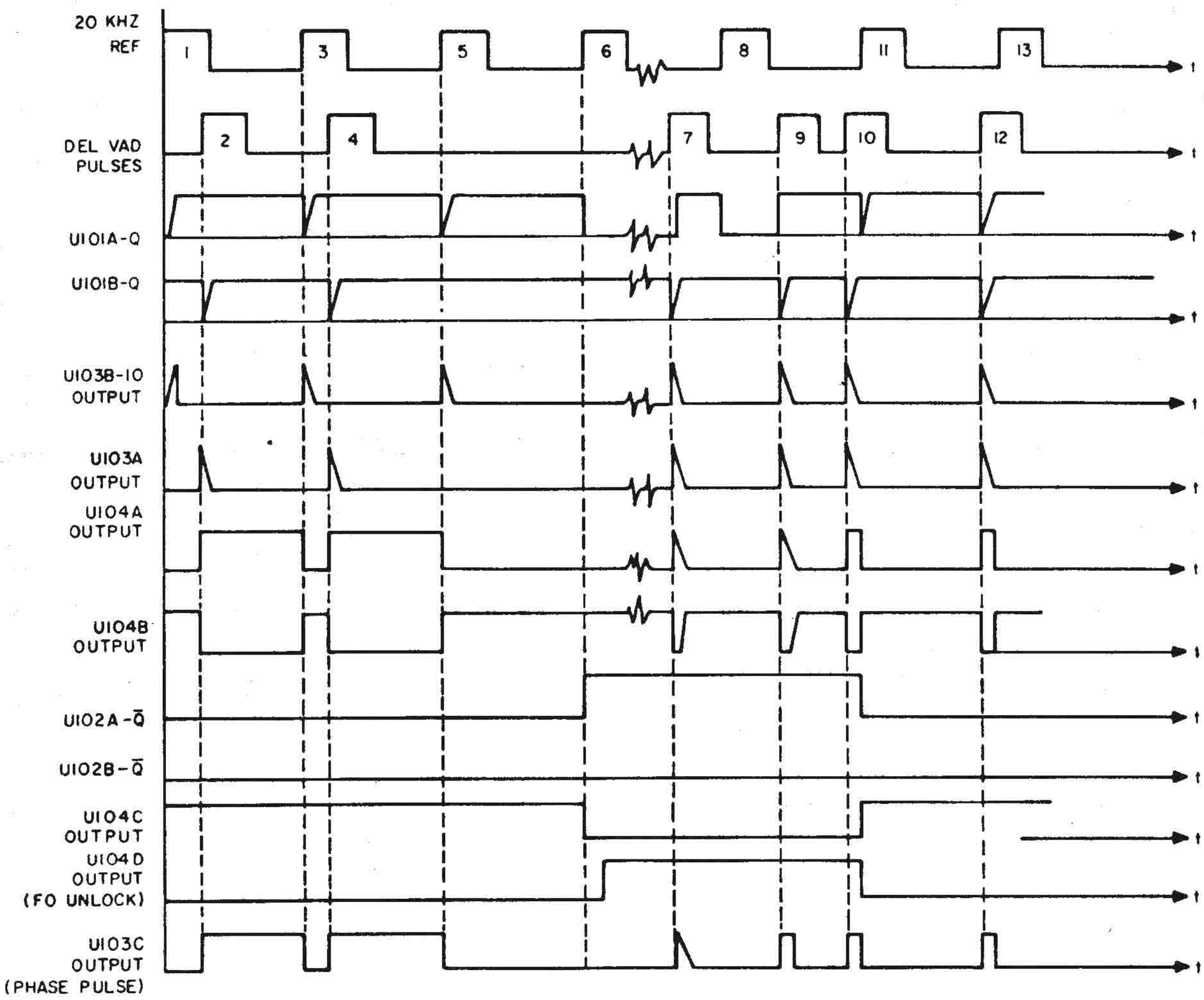


Fig. 2-61. Phase/frequency detector, typical waveforms

tion occurred in the 20-kHz reference and as a result, the output of U104A decreased to the low level (just after pulse No. 1 positive edge).

(a) At the moment the DEL VAD pulse (pulse No. 2) rises, the Q output of U101B falls to a low level. At this time, all three inputs to gate U103A are low and its output rises to the high level. Flipflop U101B is immediately set and a high level reappears at its Q output. Therefore, the output of U103A returns to the low level after a short high period.

(b) The short spike generated by gate U103A changes the state of the flipflop U104A/U104B.

(c) The arrival of pulse No. 3 causes the cycle described in (a) above to be repeated, this time by U101A and U103B. Arrival of pulse No. 4 initiates the following cycle (once again by U101B and U103A).

(d) If a frequency difference exists between the two input signals, then, at some instance, two pulses from the same source will intervene between the alternate pulses (e.g. pulses No. 5 and 6). When pulse No. 6 (a 20-kHz REF pulse) arrives, it

causes the output of U101A to decrease to the low level (gate U103B cannot set the U104A/U104B flipflop because a high level is now applied to its input by U104B). This indicates that an extraneous pulse has occurred at the reference input, (that is, the controlled oscillator runs too slow).
No change will occur in the output waveform as a result of pulse No. 6 or any additional pulses at the reference input.

(e) If a DEL VAD pulse (no. 7) appears now, it causes the regular spike at the output of U103A. However, except for a very short spike, the state of the output flipflop (U104A/U104B) does not change, because the momentary state is immediately reversed when U103B output changes to high, sets U101A and returns to the low level. At the end of the transient period, the output returns to its previous state.

(f) The phase detector returns to the state described in (d) above if the next pulse is again a reference pulse (see state after pulse No. 8).

(g) The phase detector returns to the normal sequence only when two consecutive pulses appear on the opposite line (e.g. pulses No 9,10). After the first pulse, the state described in (e) above is reached, then the second pulse reverses the state of the output flipflop, and if the correct input sequence is maintained, normal phase detector operation is resumed.

(3) Lock detector. The FO UNLOCK indication is generated by sampling the outputs of U104A and U104B with the rising edges of the input pulses; this is the function of the D-flipflops U102A and U102B. Normally, the outputs are sampled while at the high level, but when a frequency difference appears, one of the outputs remains low and causes the corresponding Q output to rise. The output of U104C goes low and after some delay (caused by R107 and C106), a high level is applied by U104D on the FO UNLOCK line. The delay prevents activation of the alarm line in case the lock is lost for only a short period. If lock is regained, capacitor C106 will quickly charge through CR101 and R108, causing the output of U104D to return to the low level.

2-21. Module VAD 1A3A2 (fig. 2-62, 2-63)

Refer to para. 2-4 for an analysis of the synthesizer block diagram.

a. Block Diagram Analysis (fig. 2-62). Module VAD 1A3A2 contains the programmable frequency divider, which divides the difference between the VCO output frequency in module VCP 1A3A1 (F1) (refer to para. 2-25) and the output frequency of module SUM 1A3A5. The division ratio is programmed by the digital frequency information. It changes from 361 to 1760 as the output frequency changes from 111.350 to 139.3499 MHz. When the phase-lock loop in module VCP 1A3A1 is locked, the divider output frequency is 20 kHz.

(1) Principle of operation. The technique by which the required division ratio is obtained is known as the "dual-modulus prescaler" technique.
In this technique, a frequency divider (called prescaler) whose modulus (division ratio) can be changed from P to P + 1 and vice versa by external commands, divides the frequency of the input signal. Two programmable counters, designated N and M, are connected in parallel to the prescaler output. The division cycle begins with the prescaler modulus set to P + 1. After M pulses (the division ratio of counter M) the modulus is changed to P and remains in this condition for the next N-M pulses (that is, until counter N times out). This signals the end of the division cycle and one output pulse is generated, while the N and M counters are again preset to the

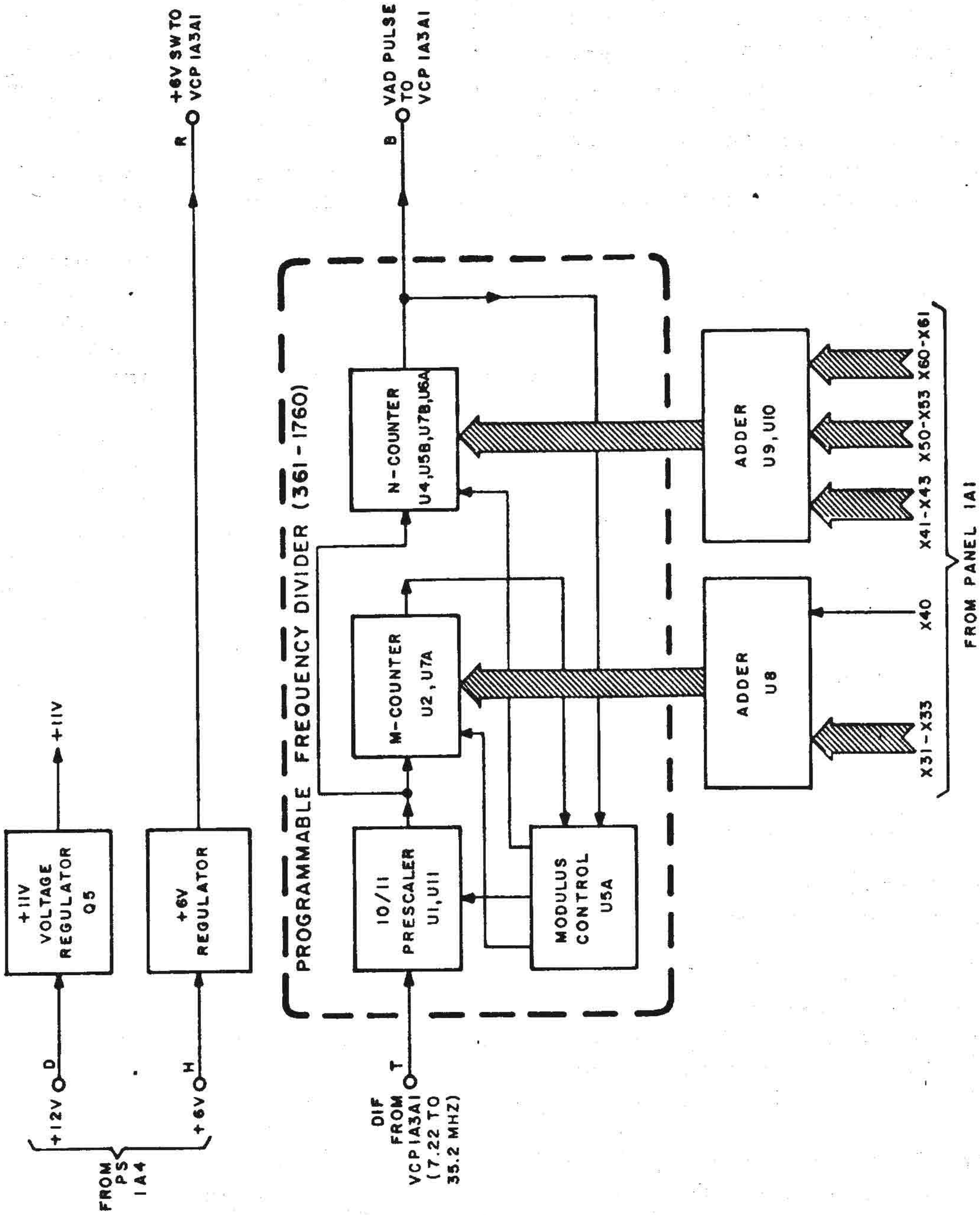


Fig. 2-62. Module VAD 1A3A2, block diagram

required division ratio.
In total, (P+1)M+(N-M)P input pulses are required before one output pulse is obtained. The total division ratio, K, is obtained by rearranging the expression above: K=PN+M. In this case, P=10, and K=10N+M.
The M-counter consists of U2, U7A and U5A; the N-counter consists of U3, U4, U5B, U6A and U7B.

(2) Calculation of the required division ratio. The division ratio required to obtain the required output frequency is determined by the frequency translation scheme. Referring to figs. 2-3 and 2-4, it is found that the nominal frequency, F_o, can be calculated by the following expression: $(MHz)F_o = SUMF + DIF - 109.35$, where:

(a) SUMF (generated by module SUM 1A3A5) may vary between 104.1300 and 104.1499 MHz, in 100-Hz increments.

(b) DIF is determined by the division ratio K:

$$(MHZ)DIF=0.02 \cdot K$$
or
$$(10\text{-kHz})DIF=2 \cdot K$$

This relationship holds only when module VCP 1A3A1 is locked.

(c) 109.35 MHz is the intermediate frequency used in module MIXER 1A2A1.

Among the 20-kHz steps generated by unity changes in the division ratio, the intermediate frequencies are supplied by the 100-Hz increments in SUMF. This leads to the following expression for DIF:

$$(MHz)DIF=F_o+109.35-SUMF=$$
$$=F_o+5.22$$

hence:

$$(10\ kHz)DIF=100F_o+522$$

From the last expression, the required division ratio, K, can be calculated for each output frequency:

$$K=(100F_o+522)/2$$

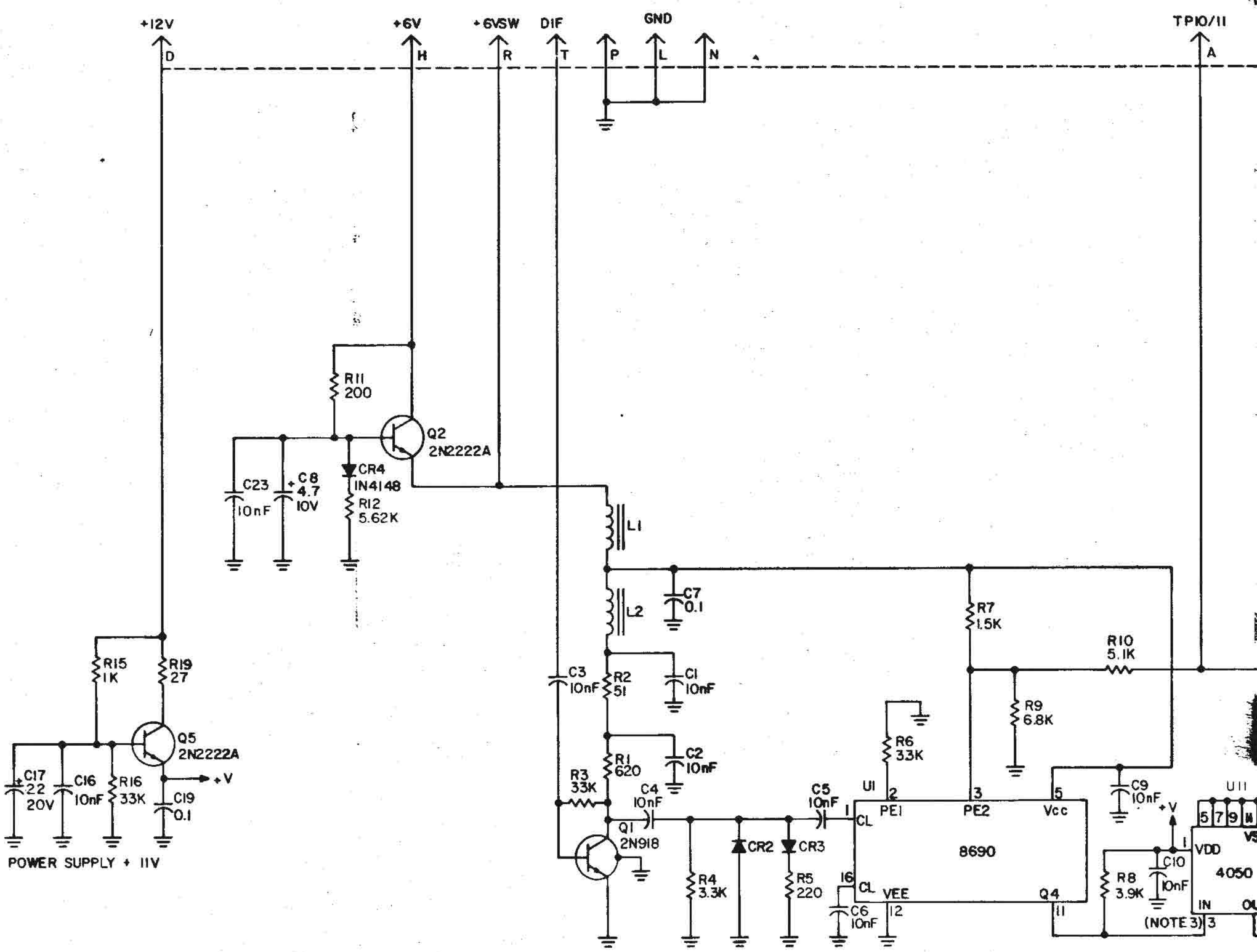
where all frequencies are expressed in multiples of 10 kHz.

The information for setting the value of K is supplied (in BCD form) from the front panel thumbwheel switches.

b. Functional Analysis of Divider Circuit (fig. 2-63).

(1) Referring to fig. 2-63, the prescaler is identified as the integrated circuit U1.
The input signal to the divider (at pin T) is amplified by Q1 and applied via a diode limiter (CR2, CR3 and R5) to the input of the prescaler U1. This prescaler is an ECL 10/11 divider. When the modulus control line (pin PE2) is high (4.1 to 4.5V), the division ratio is set to 10; when it is low (0 to 3.5V), the division ratio is 11. The output signal from the prescaler, appearing at pin 11, is coupled through the non-inverting buffer contained in U11 to the inputs of U2 and U3.

(2) M-counter. The M-counter referred to in para. a(1) above is U2. U2 is operated as a decimal down-counter. The presetting is done by applying a high level to pin PE; then the information present at the J1-J4 inputs is entered into the counter. The preset pulse also sets U5A, therefore a high level appears at its Q output, and the prescaler modulus is set at 10. However, if U2 is preset to a number other than zero, the output of gate U7A becomes low. On the next pulse, it changes the state of U5A and the prescaler modulus is set to 11. When the presetting ends, the counter steps down until it reaches state 0000. This state is decoded by U7A; a high level is then supplied by its output to the clock inhibit (CI) input of U2, which remains in this state until the end of the division cycle.
The next clock pulse (received from U1) causes the high level at the D-in-



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A3A2.
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, 1/8W, 5%.
   ALL CAPACITORS ARE IN MICROFARADS.
3. C10 IS A CHIP CAPACITOR 10 NANOFARADS.

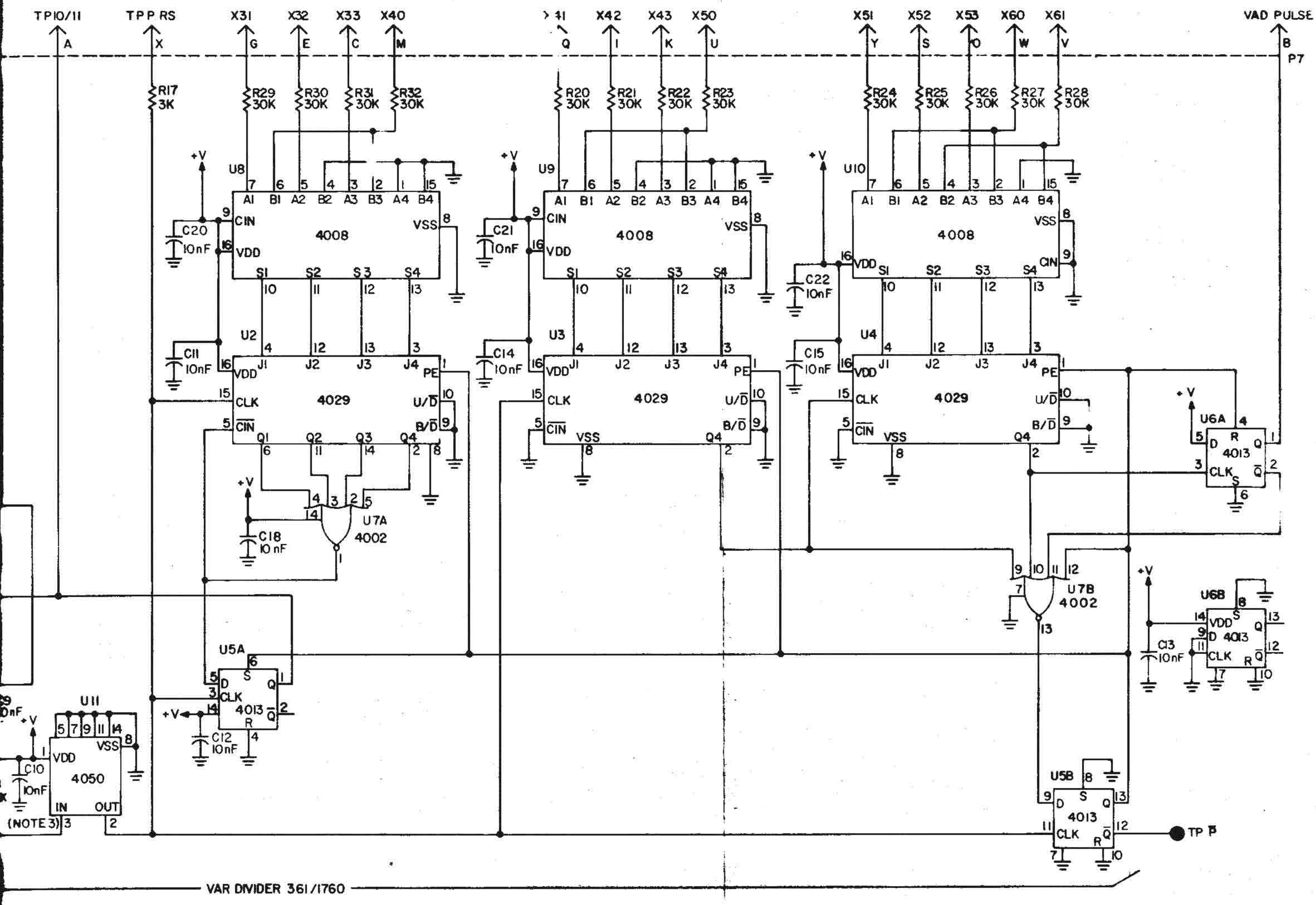


Fig. 2-63. Module VAD 1A3A2, schematic circuit diagram

put of U5A to appear at its Q output; this changes U1 modulus to 10, and this value is used until the division cycle ends.

(3) N-counter. The N-counter (see para. a(1) above) consists of U3, U4 (operating as decimal down-counters), and D-flipflop U6A. U3 and U4 are preset at the beginning of the division cycle and count down in parallel with U2 for the first M clock pulses received from U1.

After the modulus is changed, the counters continue to step down, until low levels are detected at the Q4-outputs of U3 and U4 and at the Q-output of U6A. The decoding of this condition is effected by U7B. This causes a high level to appear at the D-input of U5B. This level appears at its Q-output at the next clock pulse and presets the counters. The output of U7B will then return to the low level. The preset enable line (driven by its Q-output) remains high until the next clock pulse, then returns to the low level. This completes one division cycle. On its completion, one output pulse is supplied by U6A (VAD PULSE-pin B) to module VCP 1A3A1.

(4) Calculation of presetting information. The initial values preset into counters M and N determine the division ratio. These values are calculated by three 4-bit adders (U8, U9 and U10), using the BCD frequency information received from the front panel thumbwheel switches:

(a) The 10-kHz digit is carried by four lines: X33, X32, X31, X30 (X33 is the most significant). If frequency digit A is set on the thumbwheel switch, the code lines representing it are:

$$A = 2^3 \cdot X33 + 2^2 \cdot X32 + 2^1 \cdot X31 + 2^0 \cdot X30 =$$

$$= 8 \cdot X33 + 4 \cdot X32 + 2 \cdot X31 + X30$$

When line X is low, it represents bit value "0"; if it is high, it represents "1".

(b) The 100-kHz digit (B) is carried by X43 - X40; the 1-MHz digit (C) - by X53 - X50, and the 10-MHz digit (D) - by X61 and X60.

(c) The preset information must satisfy the following equation:

$$K=(100\ F_o + 522)/2 = 10N + M$$

This is achieved by using the BCD frequency information to determine the $100F_o/2$ part; the additional number, 522/2, is hardwired and added automatically.

(d) The number $100F_o/2$ is therefore the desired preset information. To obtain the numerical value

$$K=(1000D+100C+10B+A)/2=10N+M$$

a two-stage procedure is required:

1. Initially A/2 is used to determine the M-value; the rest of the digits are used to determine N:

$$N=(100D + 10C + B)/2$$

2. The division by 2 is easily implemented in binary numbers - by shifting one place to the right. However, for odd digits, a carry-over of decimal value 0.5 appears: this is dealt with by adding 5(0101) to the next lower digit, whenever X40, X50 or X60 is 1.

(e) The preset value (PV) information is given by the following expressions:

1. For U2:

$$PV2 = 2^2 \cdot X33 + 2^1 \cdot X32 + 2^0 \cdot X31 + X40 \cdot 5 + 1 =$$

$$= 4 \cdot X33 + 2 \cdot X32 + X31 + 5 \cdot X40 + 1$$

The addition of 1 is needed for the addition of 522/2.

E.g. for XX.07:
PV2 = 4·0+2·1+1+0·5+1 = 4

for XX.7:
PV2 = 4·0+2·1+1+1·5+1 = 9

2. For U3:

PV3 = 4·X43+2·X42+X41+5·X50+1

3. For U4:

PV4 = 4·X53+2·X52+X51+5·X60+10·X61

c. Detailed Analysis of Divider Circuit Operation (fig. 2-62). The general description of divider operation will now be integrated with the knowledge of preset information to carry out the analysis of divider operation for any input information (frequency).

(1) M-counter operation. Referring to para b.(2) above, the number of DIF input pulses required to time out the M-counter is calculated as follows:

(a) The first 10 DIF input pulses to U1 supply one input pulse to U2 and U5A. As a result, the value stored in U2 is now PV2-1, while U5A output becomes low and changes U1 modulus to 11.

(b) The next (PV2-1) pulses (from U1 output) bring U2 to state 0000. Immediately after the rise of the last pulse in this series, U7A output becomes high and locks U2 at the 0000 state. This is equivalent to 11 (PV2-1) DIF pulses.

(c) 11 additional pulses now pass before U5A receives one more clock pulse, changes to high and sets U1 modulus to 10.

(d) In total, 11 PV2 pulses pass: therefore, using the definition of para a(1) above, M=PV2.

(e) The first 10 input pulses are by the same definition equivalent to one decrement of the N-counter.

(2) N-counter operation (see para. b(3) above).

(a) The first PV3 input pulses bring U3 to state 0000 for the first time. Counter U4 still holds PV4.

(b) One additional input pulse to U3 moves it to state 1001. This applies one clock pulse to U4 and it decrements to PV4-1.

(c) 10 additional pulses to PV3 supply one more clock pulse to U4, so it decrements to PV4-2.

(d) From para (a)-(c) above, it is seen that U4 reaches state 0000 after PV3+1+10(PV4-1) input pulses.

(e) When U4 reaches state 0000, U3 is at 1001 and U6A - at 0. 10 more input pulses to U3 cause U4 to decrement to 1001. This applies a clock pulse to U6A and it changes state to 1 (therefore its Q*output is low).

(f) The division cycle ends when both Q4-outputs of U3 and U4 are low simultaneously (state "7" of U3 and U4); starting from the state described in para. (e) above, this requires 22 more clock pulses. When the 22nd pulse rises, U7B becomes high. One more clock pulse transfers this level to U5B output, which supplies the preset pulse to the whole divider, including U5A. The second clock pulse transfers the low level supplied by U7B to the U5B output, and the division cycle is now completed. The next pulse initiates another division cycle.

(g) The division ratio, N, is determined by calculating the number of input pulses required to obtain one output pulse:

N = PV3 + 1 + 10(PV4-1) + 10 + 22 + 2 =
= 10 PV4 + PV3 + 25.

(3) The division ratio, K, is

10N+M, therefore:

K=100PV4+10PV3+PV2+250.

(a) When the required frequency is 2.00 MHz, the BCD information is 00 0010 0000 0000. Then PV2=1, PV3=1, PV4=1, and:

K=100+10+1+250=361.

(b) When the required frequency is 29.99 MHz, the BCD information is 10 1001 1001 1001. Then PV2 = 10, PV3=10, PV4=14 and K=1400+100+10+250=1760. The same value holds for 29.98 MHz.

(c) For any other frequency use para (4)(e) to calculate PV2, PV3, PV4; use para (4)(c) to find K.

(2) The +12V supply voltage for U2-U7 is provided by Q5. The +5V required for the operation of U1 and also for several of the VCP 1A3A1 circuits is supplied by Q2, from the +6V line. The supply voltage to Q1 is filtered by C1, C2, R2, L2 and C7.

2-22. Module VCP 1A3A1, Mfg. Cat. No. 2124-91630-00
(fig. 2-4, 2-64, 2-65, 2-66, 2-67 and 2-68)

Refer to para. 2-4 for an analysis of the synthesizer block diagram.

a. Block Diagram Analysis (fig. 2-64). Module VCP 1A3A1 is part of the PLL circuit, which generates the F1 frequency, using the 20-kHz reference provided by module REF 1A3A6, and the 104.13 to 104.1499-MHz signal (SUMF) from module SUM 1A3A5. The PLL operates such that the VCO output frequency is higher than the SUMF frequency. The difference falls within the range of 7.22 to 35.2 MHz and is always an exact multiple of the 20-kHz reference.
The difference signal is generated by mixing the VCO output signal, F1, with the SUMF signal. The resulting signal is amplified and sent to the programmable divider in module VAD 1A3A2. The divider output signal, VAD PULSE, is processed by the sampling control circuit on module VCP 1A3A1. The resulting signal, called DEL VAD, is sent to the digital phase/ frequency detector contained in module SUM 1A3A5. The phase/frequency detector returns a pulse, called PHASE PULSE, whose width equals the phase difference between the 20-kHz reference and the DEL VAD pulse. The width is converted to a proportional voltage by the pulse-width-to-voltage converter circuit, which is the analog extension of the digital phase/ frequency detector. The conversion is made by starting a ramp when the PHASE PULSE starts and sampling the ramp voltage when the pulse ends. The ramp slope is made proportional to the frequency, by a circuit controlled by the 1-MHz and 10-MHz frequency lines. The sampled voltage is held until replaced by the next sample. The voltage appearing at the output of the sample-and-hold circuit is filtered by the loop filter and then applied to the control input of the VCO circuit, which generates the F1 signal. The F1 signal is amplified and sent to the MIXER 1A2A1. A sample of the output signal is applied to the mixer, for mixing with the SUMF signal.
The circuit contained in module VCP 1A3A1 receives two regulated voltages, derived from the +17V supplied by module USB 1A3A3, a +5V voltage, derived from the +15V and +6V, and -10V.

b. Circuit Analysis (fig. 2-65, 2-66, 2-67, 2-68).

(1) VCO circuit (fig. 2-65). The output signal of the module is generated by the voltage controlled oscillator built around FET Q101. The oscillation frequency depends on the values of L116 and L117 and the equivalent capacitance of variable capacitance diodes CR101 and CR102. The oscillator is a common-source Hartley oscillator. Its output signal is taken from Q101 source, via C105 and

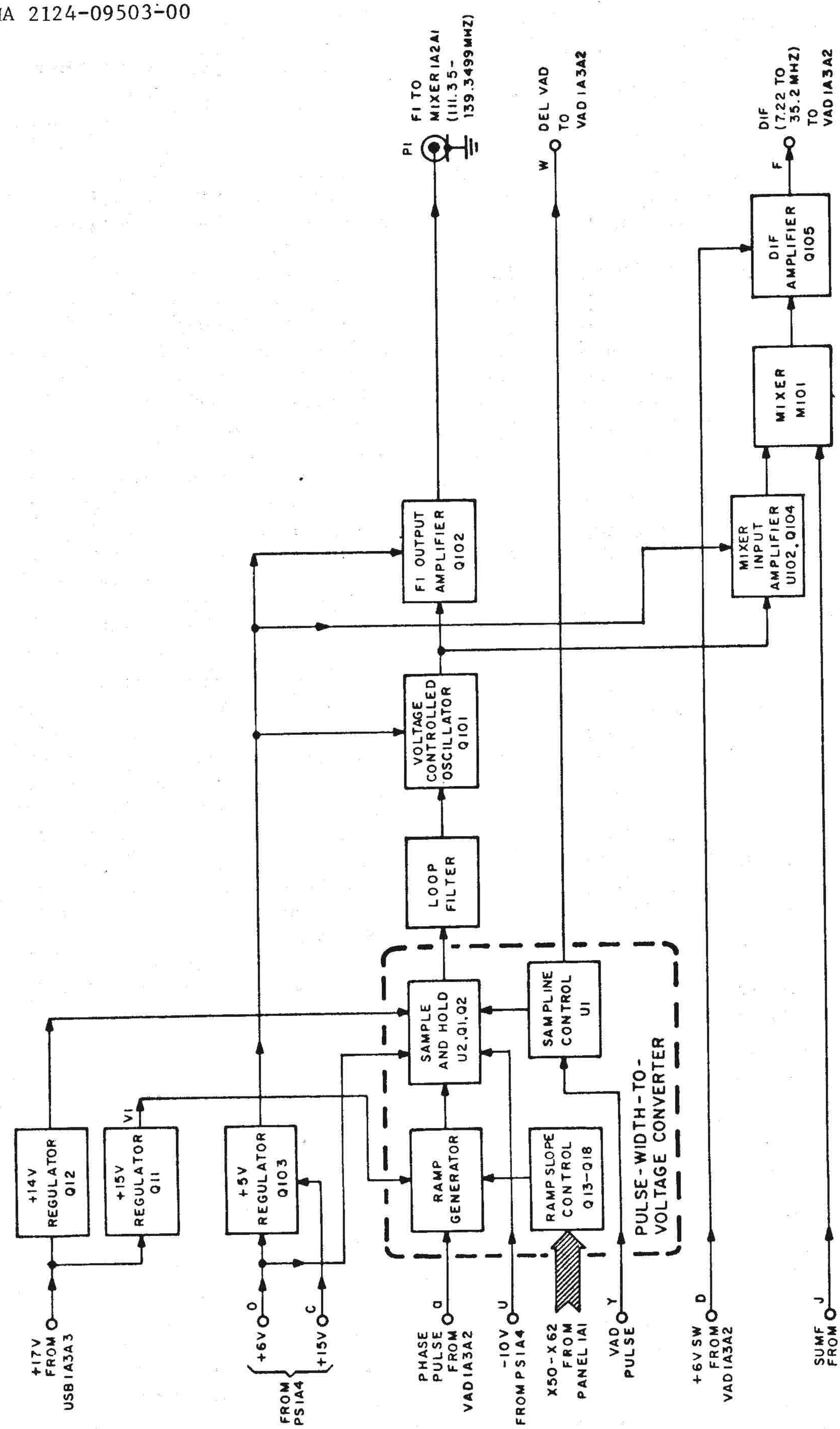
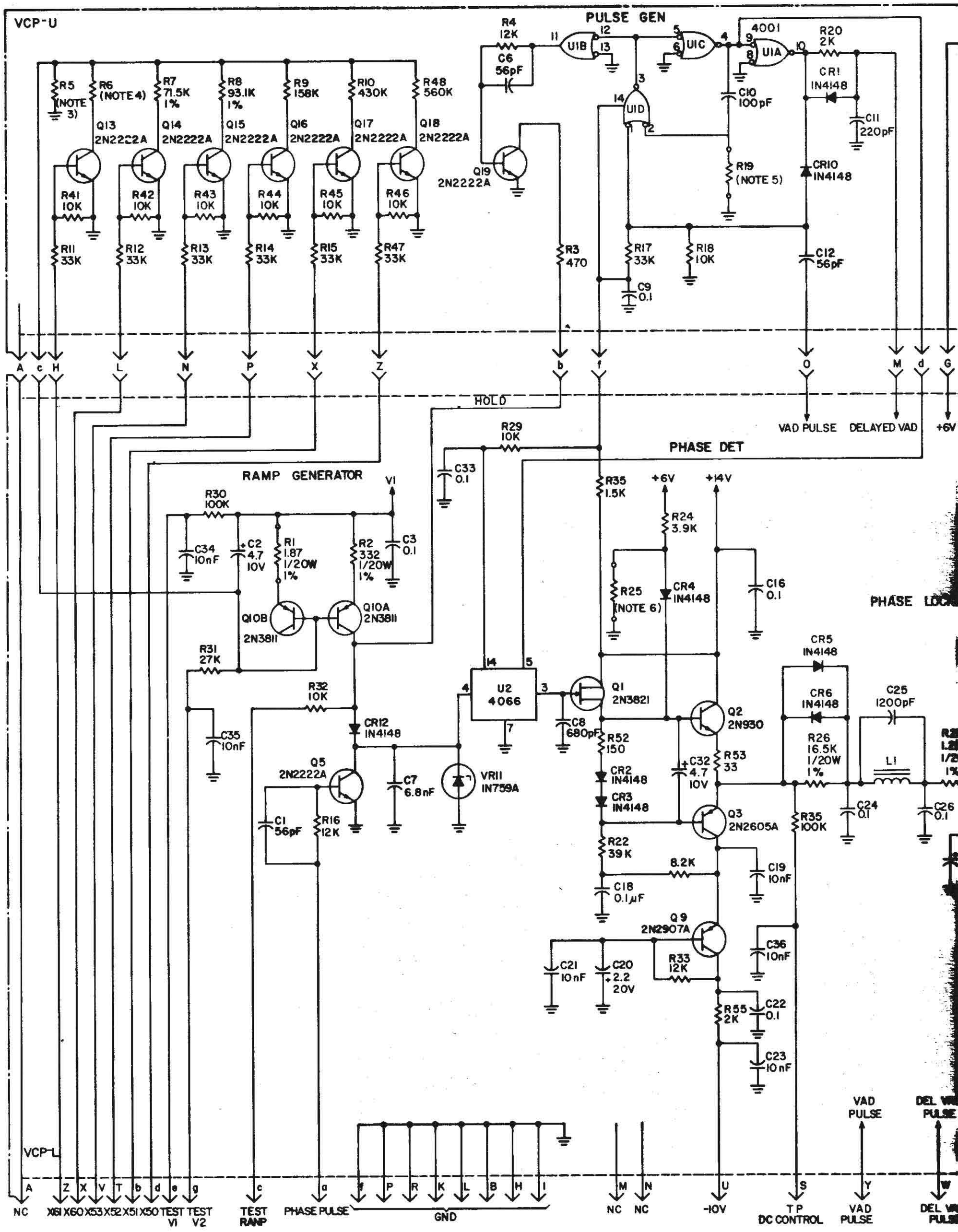


Fig. 2-64. Module VCP 1A3A1, block diagram



NOTES

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A3A1.
2. UNLESS OTHERWISE SPECIFIED :-
   ALL RESISTORS ARE IN OHMS, 1/8W, 5%
   ALL CAPACITORS ARE IN MICROFARADS.
3. R5 IS SELECTED, VALUES 93.1K 100K AND 110K.
4. R6 IS SELECTED, VALUES 16.2K AND 18.7K.
5. R19 IS SELECTED, VALUES 10K, 12K, 15K AND 16.2K.
6. R25 IS SELECTED, VALUES 3.9K, 4.7K AND 5.6K.
7. R116 IS SELECTED, VALUES 220, 270 AND 330.
8. R118 IS SELECTED, VALUES 68, 82.5 AND 100.
9. C145, C146 AND C147 ARE CHIP CAPACITORS.

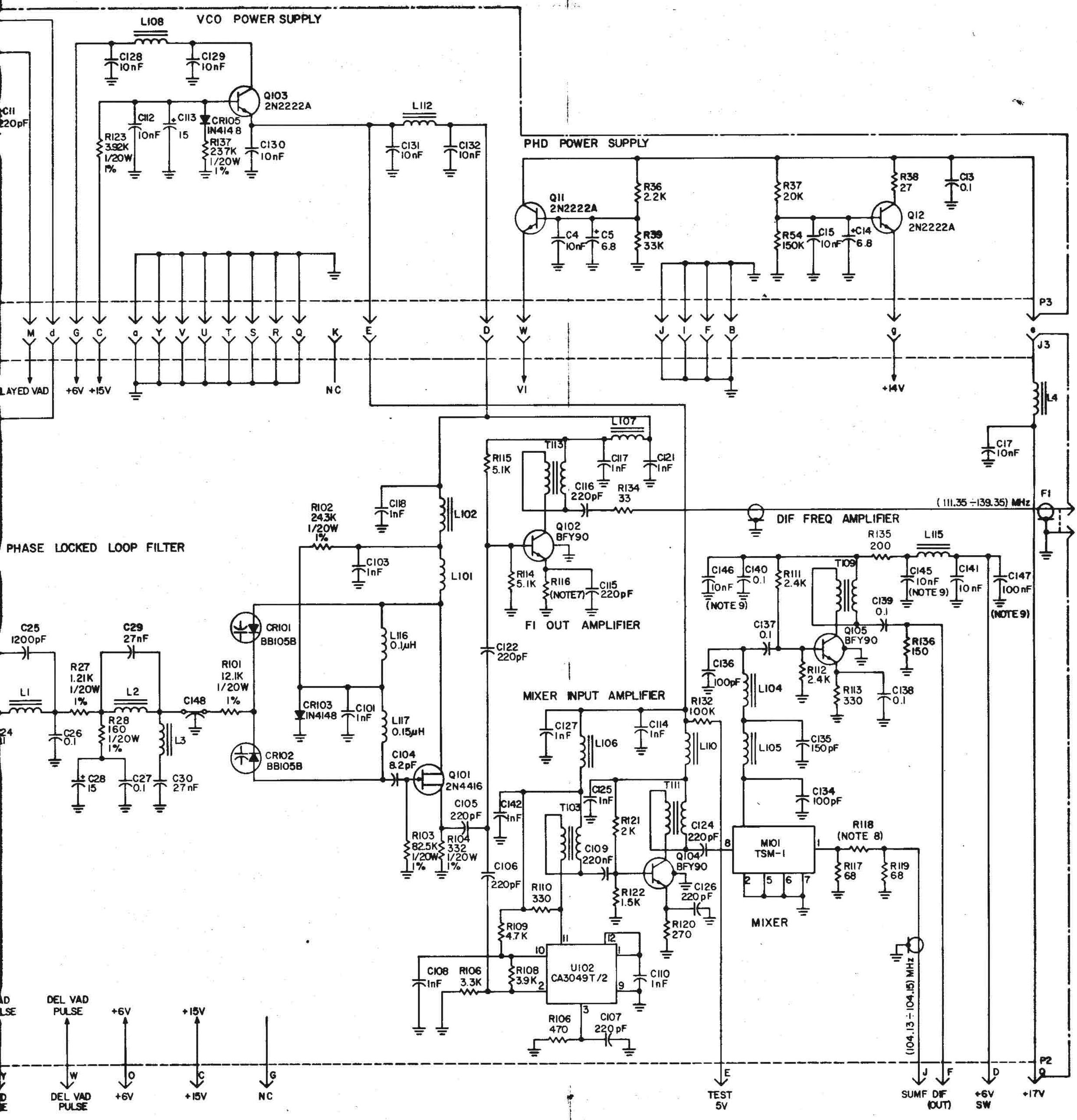


Fig. 2-65. Module VCP 1A3A1, schematic circuit diagram

C122, to the F1 amplifier.

(2) F1 amplifier (fig. 2-65). The F1 amplifier is built around Q102. R115 and R114 provide base bias. R116, bypassed at RF by C115, is selected to adjust the operating current. The output signal develops across transformer T113 and is sent through C116 and R134 to module MIXER 1A2A1.

(3) Mixer input amplifier (fig. 2-66). The VCO output signal is also coupled through C106 to the input of the integrated circuit U102, which contains a RF cascade amplifier. The output signal, appearing at pin 11, is coupled through transformer T103 to a second amplification stage built around Q104, which is identical to the F1 amplifier, Q102.

(4) Mixer (fig. 2-66). The output signal of Q104 drives one of the inputs to the passive double-balanced mixer M101. The other input of this mixer receives the SUMF signal (pin J) generated by module SUM 1A3A5. The SUMF signal is attenuated by R117, R118, and R119 before being applied to the mixer. The difference frequency, appearing at pin 3 of M101, is filtered by C134, L105, C135, L104, and C136.

(5) DIF amplifier (2-65). The filtered difference signal is coupled through C137, to the base of the Q105 amplifier. This amplifier is similar to the F1 amplifier, built around Q102. The amplified difference signal (between 7.22 and 35.20 MHz) passes through T109, C139 and pin F (DIF OUT) to the programmable divider in module VAD 1A3A2.

(6) Pulse-width-to-voltage converter (fig. 2-65, 2-67, 2-68). The VCO DC control voltage is generated by converting the output pulse of the digital phase/frequency detector contained in module SUM 1A3A5 to a DC voltage proportional to the pulse width. This is effected by a ramp generator designed around the matched pair of transistors, Q10A and Q10B. Transistor Q10B charges capacitor C7 with a constant current. The value of this current depends on the resistance connected from the base to ground. This resistance consists of a fixed resistor, R5, and one of the resistors R6 through R10 and R48. The appropriate resistors are switched in, according to the selected 10-MHz and 1-MHz digits, by the transistors Q13 through Q18. The value of the charging current is varied so as to keep the PLL gain constant at all frequencies. Capacitor C7 is discharged through Q5 when the PHASE PULSE line from the phase detector in module SUM 1A3A5 rises to a high level. When this line returns to a low level, the voltage across C7 begins to increase again. Diode CR11 prevents C7 voltage from increasing above +12V. Analog switch U2 samples the voltage on C7, when the output of U1C (see (8) below) rises to the high level. The voltage across C8 will then equal that across C7. The analog switch then turns off, and C8 holds the acquired voltage until the next sampling cycle. The C8 voltage is buffered by FET Q1, whose high input impedance prevents C8 from discharging. The signal appearing at the source of Q1 is buffered by Q2 and Q3, which provide a low output impedance to the filter network. A clamping network, comprised of R24, R25 and CR4, prevents Q1 source voltage from decreasing below the voltage at the junction of R24, R25 (because diode CR4 conducts in such a case and clamps the voltage). The value of R25 is selected so as to obtain a certain minimum VCO oscillation frequency (approximately 106 MHz). Transistor Q9 serves as an active filter for the negative supply voltage to the buffer stage.

(7) Loop filter (fig. 2-65). The loop filter consists of the following elements:

(a) Non-linear resistance,

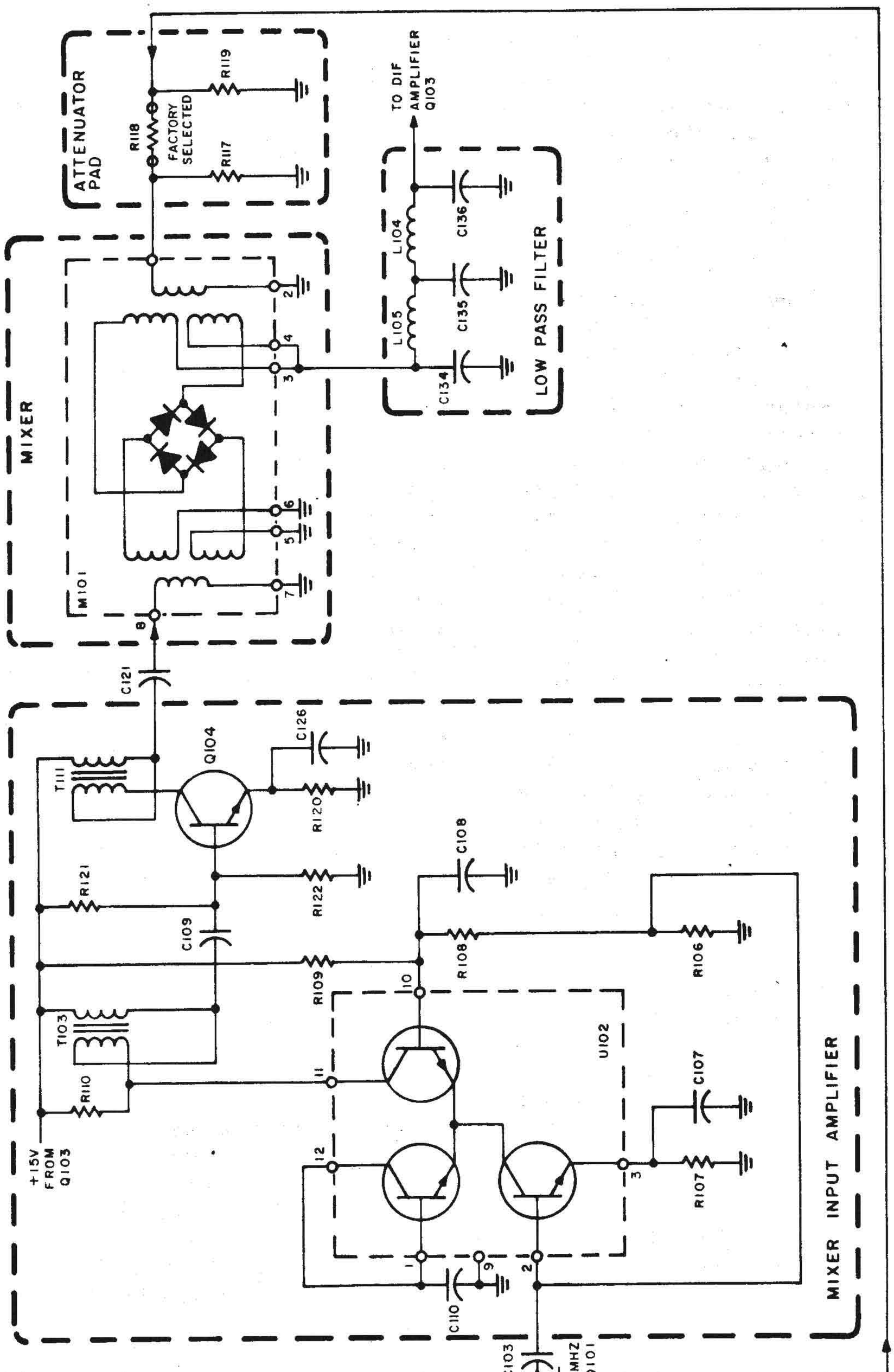


Fig. 2-66. Mixer and mixer input amplifier, simplified circuit diagram

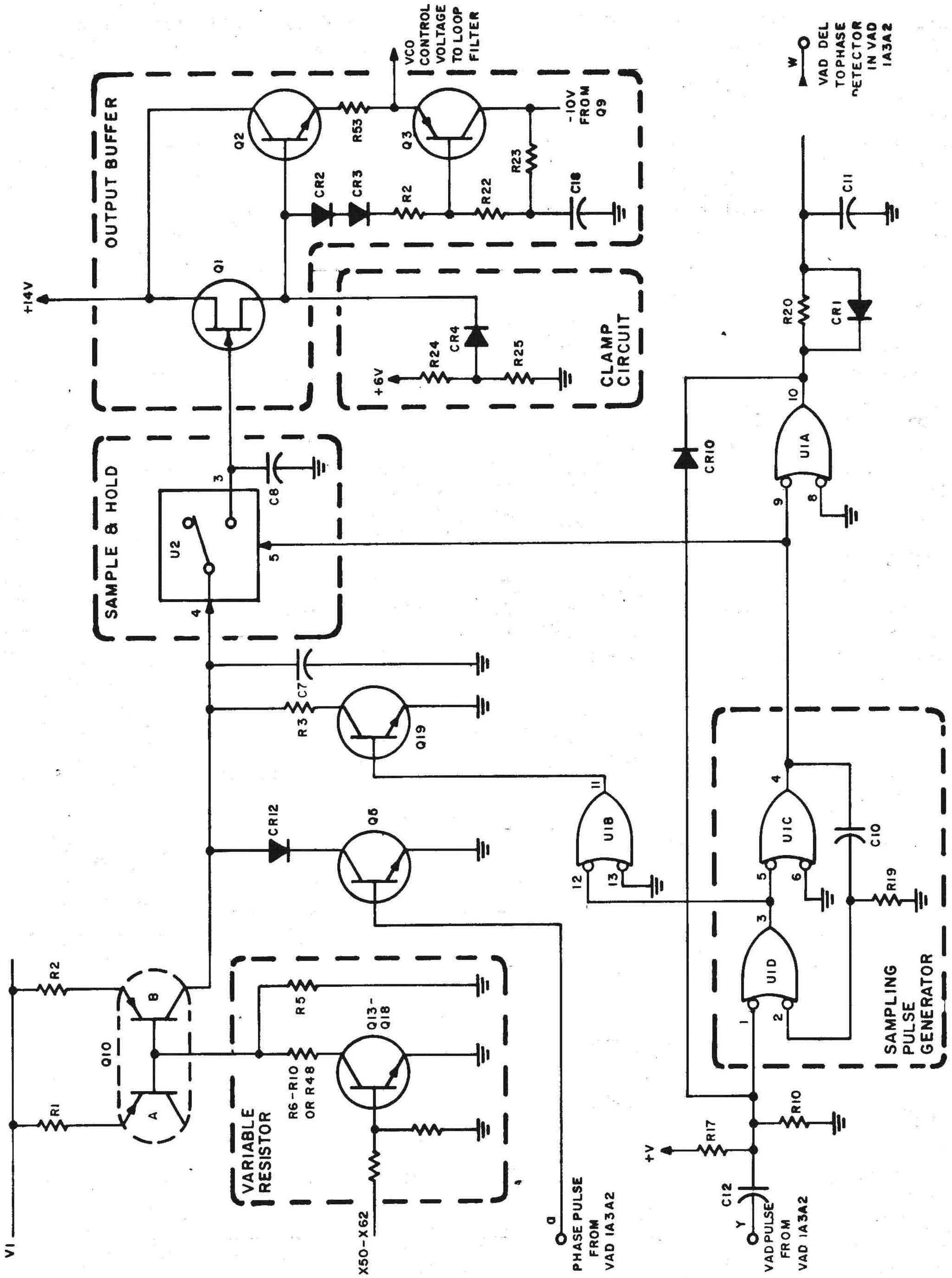


Fig. 2-67. Pulse-width-to-voltage converter, simplified circuit diagram

comprised of R26, CR5 and CR6, which improves the settling time.

(b) 40-kHz band stop filter, consisting of C25, L1, which attenuates the second harmonic of the sampling frequency.

(c) 20-kHz band stop filter, consisting of C29, L2 and L3, C30.

(d) C24, L1, C26 form a 5-kHz low pass filter.

(e) R26, R27, R28, C28, C27 form a pole/zero network.

The output voltage of the filter is connected via feedthrough capacitor C148 and resistor R101 to the variable capacitance diodes of the VCO, CR101 and CR102.

(8) Sampling pulse generator and associated circuits (fig. 2-67, 2-68). The sampling pulse generator consists of U1D and U1C, which form a monostable multivibrator. The monostable is triggered by the rise of the VAD PULSE (which is differentiated by C12, R17 and R18). The resulting positive pulse appearing at the output of U1C is applied to the analog switch U2. A similar pulse appears at the output of U1B and is used to bypass the charging current of C7 (through R3 and Q19) in order to prevent changes in C7 voltage during the sampling pulse. The sampling pulse is inverted by U1A and transferred to the digital phase/frequency detector in module SUM 1A3A5 as the DEL VAD pulse. The negative transition of this pulse occurs concurrently with the VAD PULSE rise, because capacitor C11 is discharged rapidly through CR1, whereas the positive transition is delayed by R20 and C11.

(9) Supply voltages. +15V is applied to the circuits in the VCP-L assembly from the regulator consisting of Q11 and bias network R36, R39. Transistor Q12 supplies filtered +14V to the VCP-L assembly.
Regulated +5V DC for the VCO is supplied by Q103.

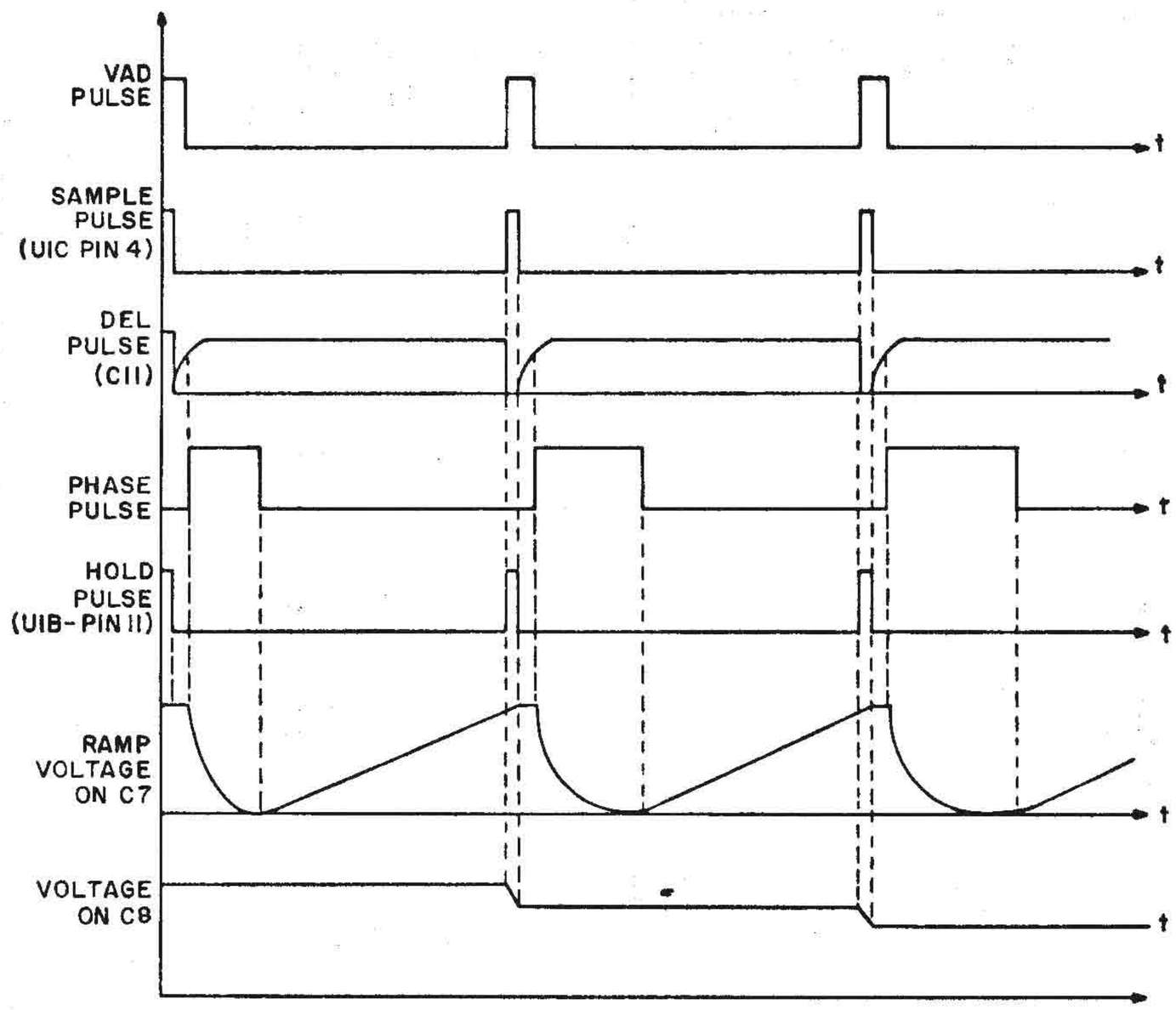


Fig. 2-68. Pulse-width-to-voltage converter, typical waveforms

2-22A. Module VCP 1A3A1, Mfg. Cat. No. 2124-91720-00 (fig. 2-4, 2-64A, 2-65A, 2-66A and 2-67A)

Refer to para. 2-4 for an analysis of the synthesizer block diagram.

a. Block Diagram Analysis (fig. 2-64A). Module VCP 1A3A1 is part of the PLL circuit, which generates the F1 frequency, using the 20-kHz reference provided by module REF 1A3A6, and the 104.13 to 104.1499-MHz signal (SUMF) from module SUM 1A3A5. The PLL operates such that the VCO output frequency is higher than the SUMF frequency. The difference falls within the range of 7.22 to 35.2 MHz and is always an exact multiple of the 20-kHz reference.

The difference signal is generated by mixing the VCO output signal, F1, with the SUMF signal. The resulting signal is amplified and sent to the programmable divider in module VAD 1A3A2. The divider output signal, VAD PULSE, passes through module VCP 1A3A1 and exits on the DEL VAD line. The DEL VAD signal is sent to the digital phase/frequency detector contained in module SUM 1A3A5. The phase/frequency detector returns a pulse, called PHASE PULSE, whose width equals the phase difference between the 20-kHz reference and the DEL VAD pulse. The width is converted to a proportional voltage by the pulse-width-to-voltage converter circuit, which is the analog extension of the digital phase/ frequency detector. The conversion is made by integrating the pulses and providing a DC voltage proportional to their width. The integration time constant is made proportional to the frequency, by a circuit controlled by the 1-MHz and 10-MHz frequency lines. The voltage appearing at the output of this circuit is filtered by the loop filter and then applied to the control input of the VCO circuit, which generates the F1 signal. The F1 signal is amplified and sent to the MIXER 1A2A1. A sample of the output signal is applied to the mixer, for mixing with the SUMF signal.

The circuit contained in module VCP 1A3A1 is powered from the +17V supplied by module USB 1A3A3, a +5V voltage, derived from the +15V and +6V supply lines, and -10V.

b. Circuit Analysis (fig. 2-65A, 2-66A, 2-67A).

(1) VCO circuit (fig. 2-65A). The output signal of the module is generated by the voltage controlled oscillator built around FET Q101. The oscillation frequency depends on the values of L116 and L117 and the equivalent capacitance of variable capacitance diodes CR101 and CR102. The oscillator is a common-source Hartley oscillator. Its output signal is taken from Q101 source, via C105 and C122, to the F1 amplifier.

(2) F1 amplifier (fig. 2-65A). The F1 amplifier is built around Q102. R115 and R114 provide base bias. R116, bypassed at RF by C115, is selected to adjust the operating current. The output signal develops across transformer T113 and is sent through C116 and R134 to module MIXER 1A2A1.

(3) Mixer input amplifier (fig. 2-66A). The VCO output signal is also coupled through C106 to the input of the integrated circuit U102, which contains a RF cascade amplifier. The output signal, appearing at pin 11, is coupled through transformer T103 to a second amplification stage built around Q104, which is identical to the F1 amplifier, Q102.

(4) Mixer (fig. 2-66A). The output signal of Q104 drives one of the inputs to the passive double-balanced mixer M101. The other input of this mixer receives the SUMF signal (pin J) generated by module SUM 1A3A5. The SUMF signal is attenuated by R117, R118, and R119 before being applied to the mixer. The difference frequency, appearing at pin 3 of M101, is filtered by C134, L105, C135, L104, and C136.

(5) DIF amplifier (2-65A). The filtered difference signal is coupled through C137, to the base of the Q105 amplifier. This amplifier is similar to the F1 amplifier, built around Q102.

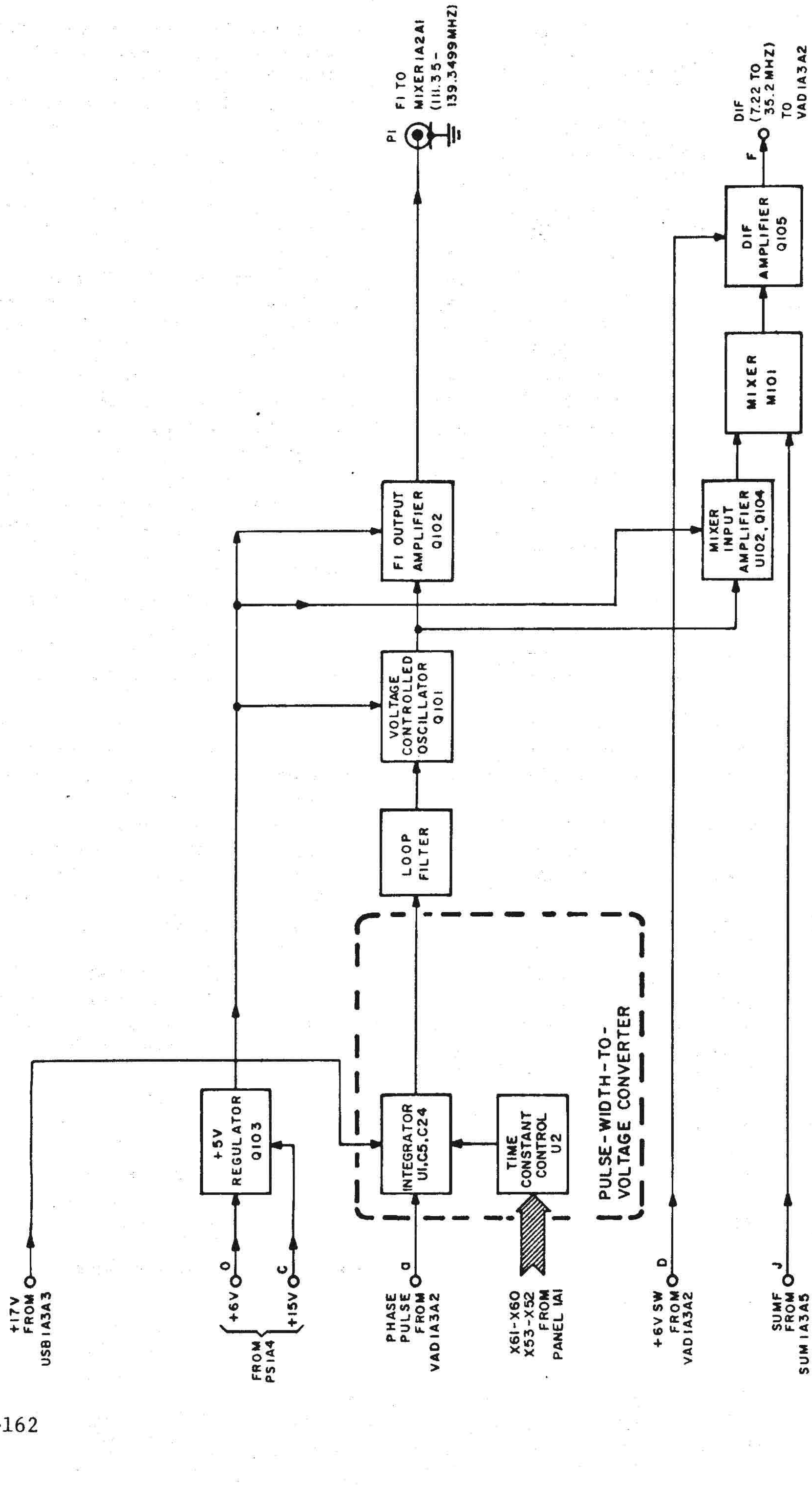
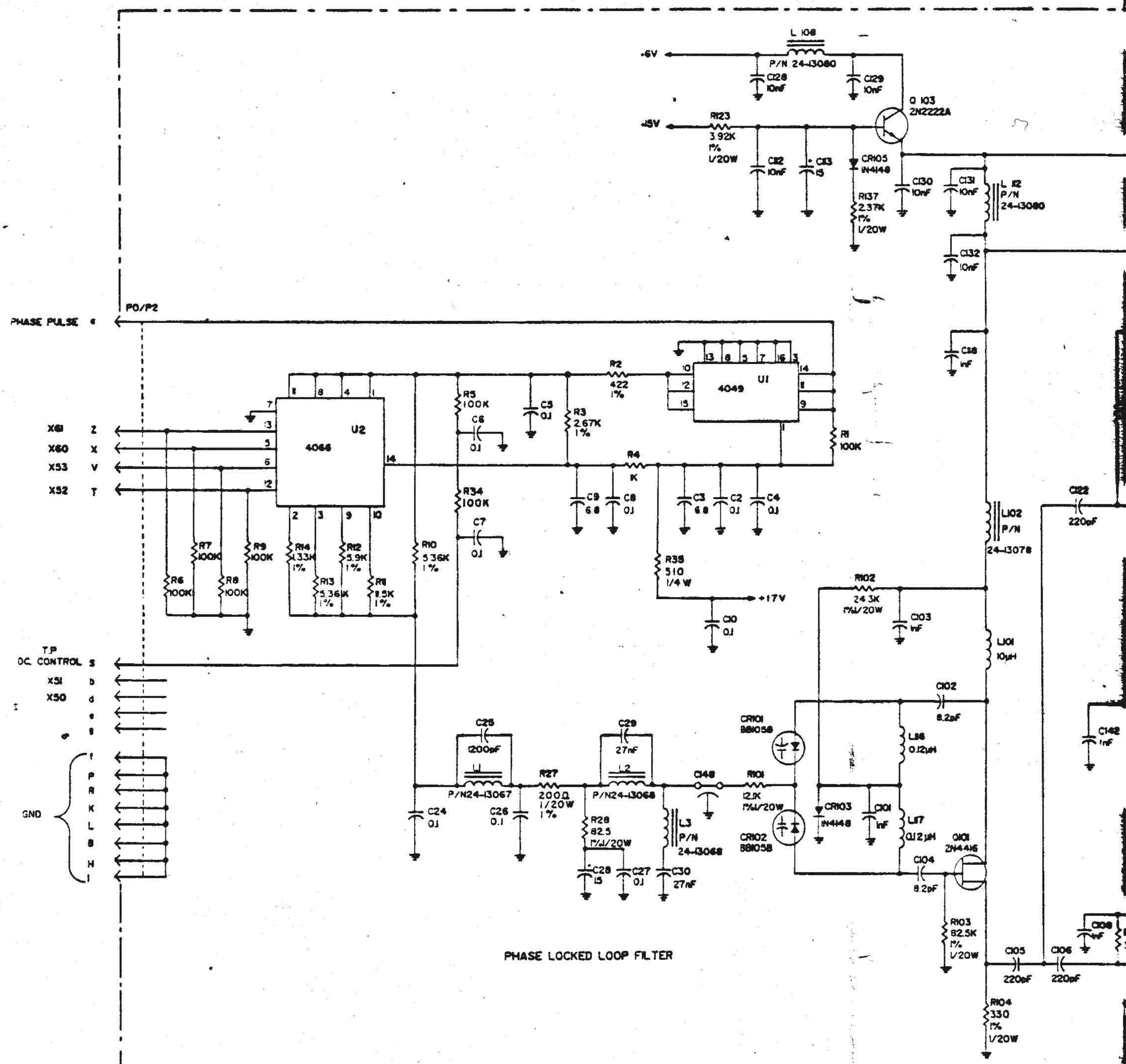


Fig. 2-64.A. Module VCP 1A3A1, Mfg. Cat. No. 2124-91720-00, block diagram



PHASE LOCKED LOOP FILTER

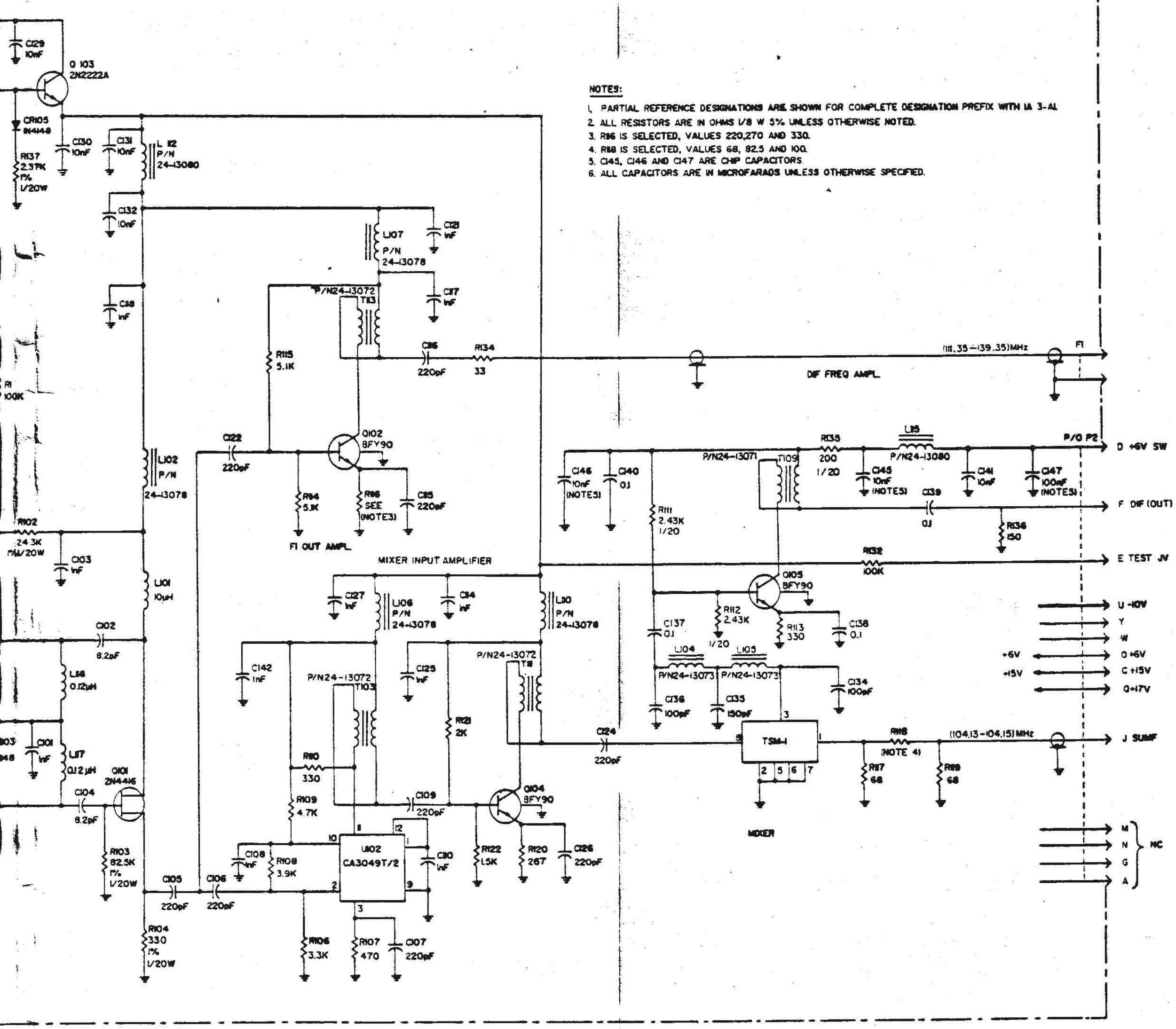


Fig. 2-65.A. Module VCP 1A3A1, Mfg. Cat. No. 2124-91720-00, Schematic Circuit Diagram

The amplified difference signal (between 7.22 and 35.20 MHz) passes through T109, C139 and pin F (DIF OUT) to the programmable divider in module VAD 1A3A2.

(6) Pulse-width-to-voltage converter (fig. 2-65A, 2-67A). The VCO DC control voltage is generated by converting the output pulse of the digital phase/frequency detector contained in module SUM 1A3A5 to a DC voltage proportional to the pulse width.
The conversion is performed by the resistors R2, R3 and capacitor C5, and the equivalent resistance of R10 thru R14 and C24.

(a) The PHASE PULSE is inverted by the buffers in U1 (three buffers connected in parallel to reduce the output resistance. The resulting low-level pulses affect the average charging current of capacitor C5, and thus its average voltage: the longer the PHASE PULSE, the lower the voltage.

(b) The voltage on capacitor C5 is filtered by an RC network, comprising resistors R10 thru R14 and C24. The analog switches in U2, controlled by the 10-MHz frequency lines (X61 and X60) and the most significant 1-MHz frequency lines (X53 and X52) connect one or more of the R11, R12, R13 or R14 resistors in parallel with R10 (a high level connects the corresponding resistor). This changes the time constant such as to compensate for the frequency-dependent gain of the VCO included in the PLL and ensure loop stability.
The polarity of control is such that an increasing phase difference decreases the duration of the positive part of the PHASE PULSE, and increases the average voltage across C5 and C24. This reduces the capacitance of the diodes CR101 and CR102, and increases the oscillation frequency.

(7) Loop filter (fig. 2-65.A). The loop filter consists of the following elements:

(a) 40-kHz band stop filter, consisting of C25, L1, which attenuates the second harmonic of the sampling frequency.

(b) 20-kHz band stop filter, consisting of C29, L2 and L3, C30.

(c) C24, L1, C26 form a 5-kHz low pass filter.

(d) R26, R27, R28, C28, C27 form a pole/zero network.
The output voltage of the filter is connected via feedthrough capacitor C148 and resistor R101 to the variable capacitance diodes of the VCO, CR101 and CR102.

(8) Supply voltages. The VCP 1A3A1 circuits are powered from the +6V SW and +17V lines. A regulator, Q103, converts, receives +15V and +6V and provides +5V for the VCO circuit and the mixer input amplifier.

2-23. Module CONT 1A7 (fig. 2-1, 2-69 through 2-79)

This module provides the visual and auditory indications for the radio set and serves as a switching and distribution center for the various PTT lines.

a. Block Diagram Analysis (fig. 2-69).

(1) PTT generation. The PTT generation is controlled by the state of the PTT HANG line from module PRE 1A2A4. When this line assumes a low level, the PTT LORD rises to a high level, unless one or more of the SF, RT or FO UNLOCK lines is also high.
The SF line is pulsed to a high level while the frequency selector switches change position. The R/T line assumes a high level when the receive-only mode is selected. The FO UNLOCK line assumes a high level when the lock detector in module VAD 1A3A2 detects loss of lock, or module LORD 1A5A2 detects that an out-of-range frequency had been selected.

(2) Supply voltage switching. The PTT generation circuit also controls the switching of supply voltages. The following voltages are switched on in the transmit mode: PTT 12V, PTT PRE +12V, PTT +6V, and the PTT +15V line is grounded. In the receive mode, the PTT +15V line is connected

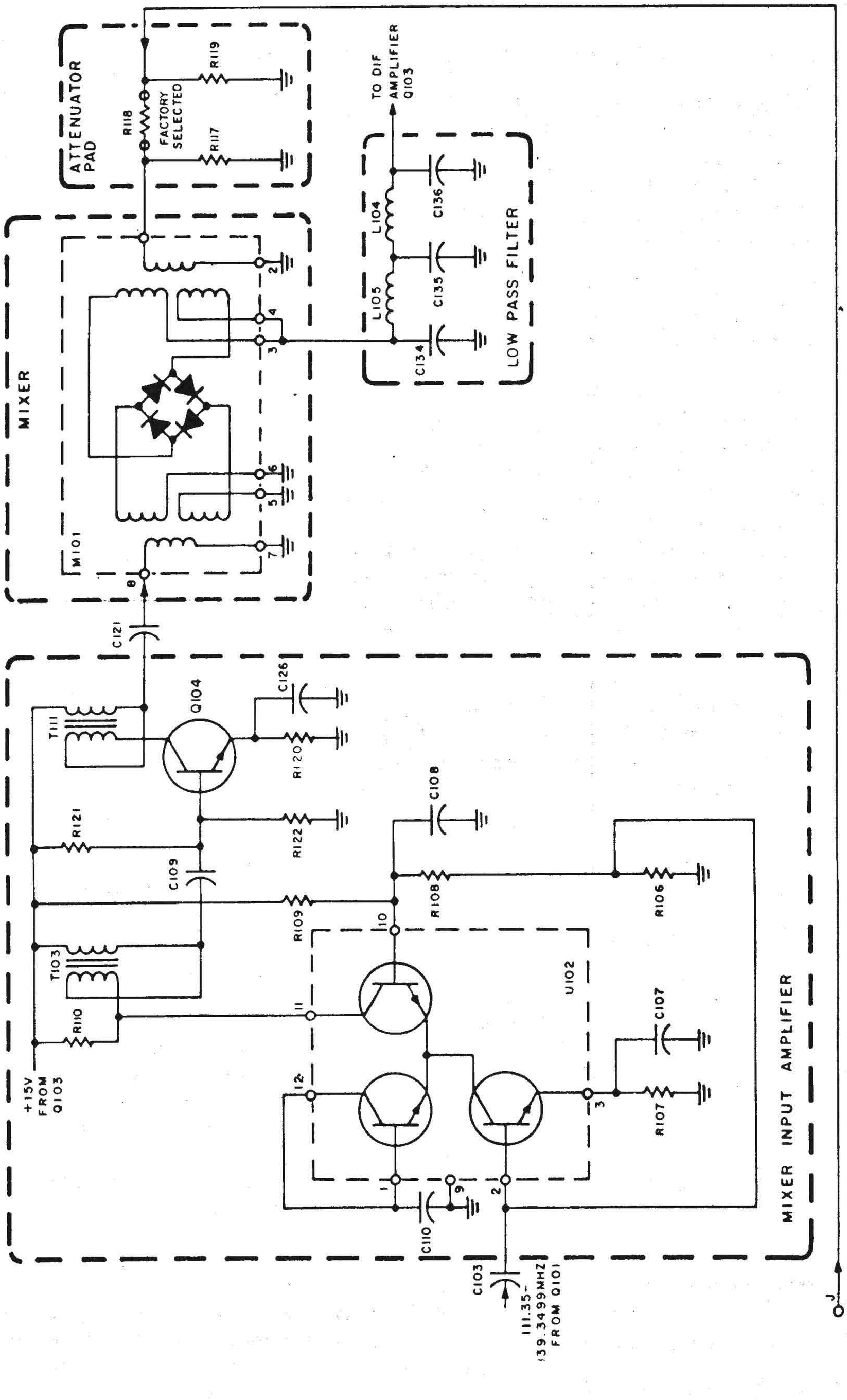


Fig. 2-66.A. Mixer and mixer input amplifier, simplified circuit diagram

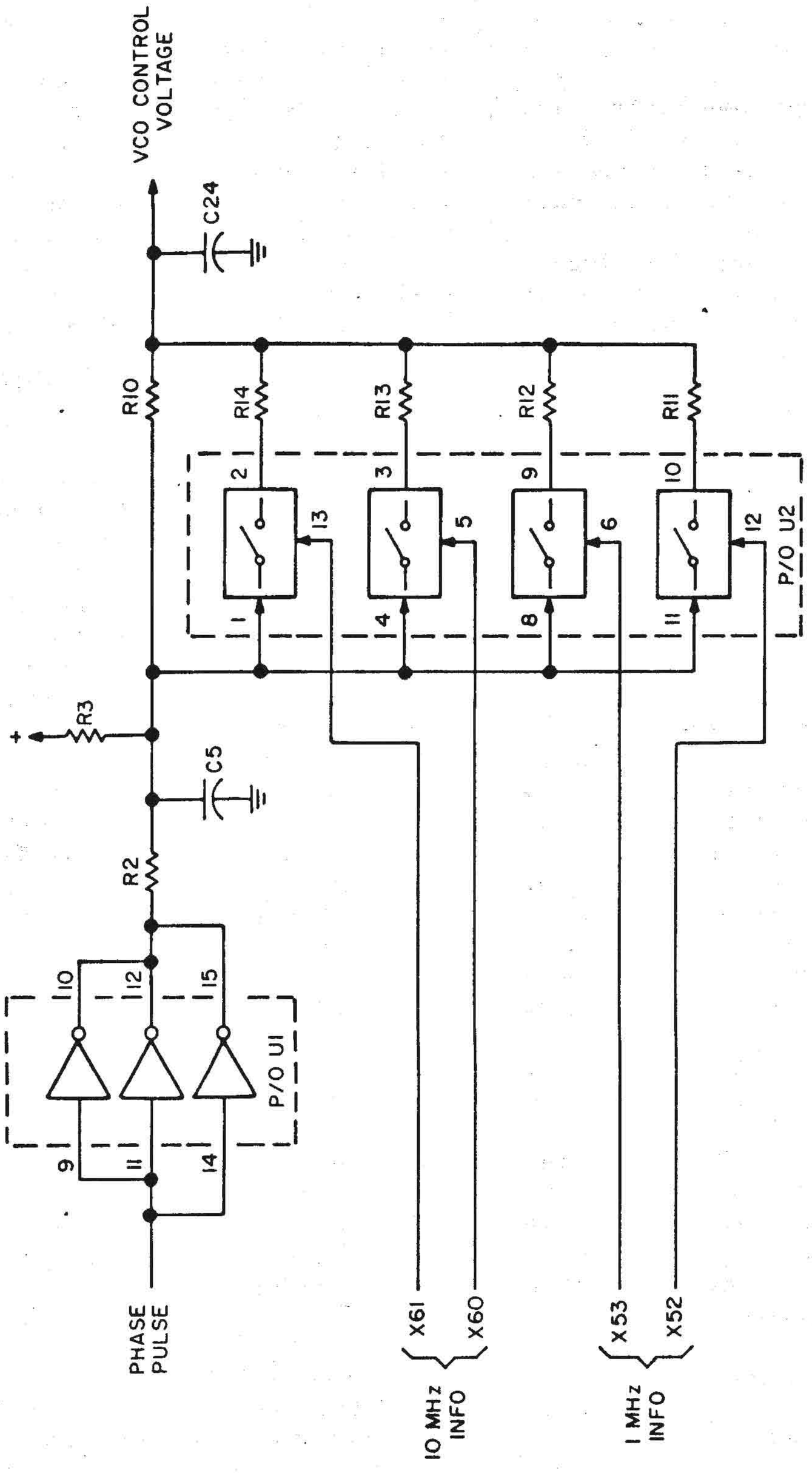


Fig. 2-67.A. Pulse-width-to-voltage converter simplified circuit diagram

to +15V, whereas the other lines are grounded, except PTT +12V, which is open-circuited.

(3) INH F3 control. The INH F3 line is normally at a high level, except in the AM receive mode - when it assumes a low level.

(4) Low-battery comparator. The primary DC voltage is monitored by a comparator. When the voltage becomes too low for proper operation, an auditory alarm is initiated.

(5) Indication priority logic. This logic circuit controls the operation of the indications and alarm circuits, and selects the indication and/or alarm to be activated according to its priority and the selected operation mode.

(6) Signaling generator. This circuit generates the various types of beeps heard in the earphone.

(7) Flashing driver. This circuit causes the display to flash during the low-battery no-match and loss-of-lock alarm conditions.

(8) Tune indication control. This circuit generates the "running lights" indication while tuning is in progress. The circuit is activated by turning on the 12.5-Hz oscillator, which serves as its clock source.

(9) Measurement sub-system. The measurement sub-system provides a bar-type display of the relative magnitude of the TX LEVEL (output power) voltage, S-METER (received signal strength) or primary DC voltage:

(a) In the BAT CHK mode, the primary voltage is continuously displayed.

(b) In the IND mode, the S-METER voltage is displayed in the receive mode, and the TX LEVEL - in the transmit mode.

The measurement is made by means of a modified successive-approximation analog-to-digital (A/D) converter. The converter output is decoded and used to drive the LEDs contained in the solid-state display.

b. Circuit Analysis (fig. 2-70 through 2-79).

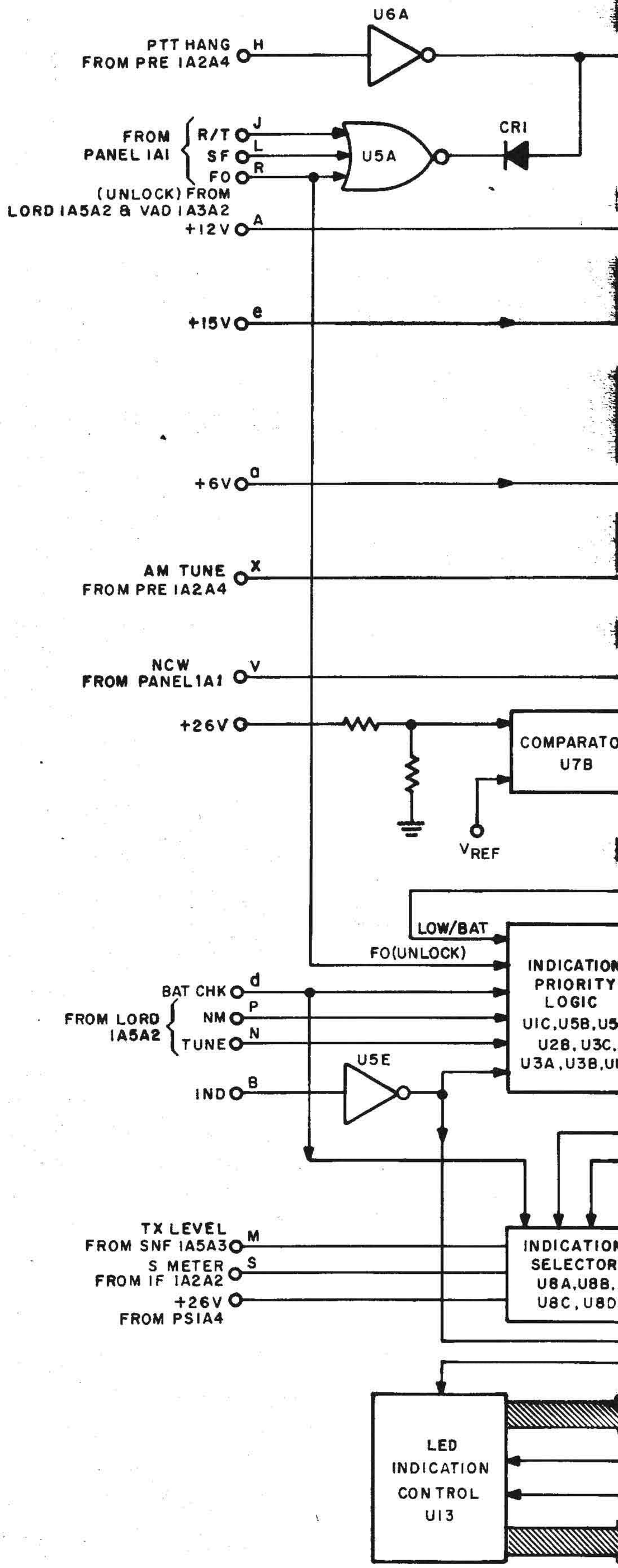
(1) PTT LORD and supply voltage control (fig. 2-70, 2-71). The PTT HANG line from module PRE 1A2A4 is applied, via R28, to U6A. R28, R29, and C8 form an anti-bounce circuit for the PTT line. When the PTT HANG line is at a low level, the output of U6A rises to a high level, which is applied to the Schmitt-trigger circuit formed by U6B, U6C, R30 and R33. This results in a high level on the PTT LORD line. Gate U5A inhibits transmission, by pulling the input of U6B to a low level through CR1, when a high level appears on either one of the SF, R/T or FO UNLOCK lines (see a.(1) above).

The output level of U6C is inverted by U6D and used to drive the supply voltage control circuit, comprised of transistors Q2, Q3 and relay K1.

In the receive mode (low level at the output of U6C), the high output of U6D does not allow bias current for Q3 to flow. As a result, Q3 and Q2 cut off, and relay K1 is unenergized. Contacts 6 and 8 pass the +15V to the PTT +15V line, whereas contacts 2 and 4 ground the PTT +6V line. In the transmit mode, a low level appears at the output of U6D causes saturation of Q3 and Q2. +12V appears on the PTT +12V and PTT PRE +12V lines. Relay K1 is energized and contacts 7 and 8 ground the PTT +15V line; contacts 2 and 3 pass the +6V to the PTT +6V line.

(2) INH F3 line (fig. 2-70). The INH F3 line is controlled by U2A, which receives the output of U6B (low in the transmit mode) and the AM TUNE line, arriving from module PRE 1A2A4 (high during tuning and in the AM mode). In the AM receive mode, the output of U2A assumes a low level, thereby interrupting the generation of the 5.25-MHz carrier in module REF 1A3A6.

(3) SSB CONT line (fig. 2-70). This line is controlled by U1A, which receives the NCW line from the front panel (high in the NCW mode) and the AM TUNE line. The SSB CONT line is at a high level in all SSB modes, except in the NCW mode.


U6A
PTT HANG
FROM PRE 1A2A4
H
FROM
PANEL 1A1
R/T
SF
FO
J
L
R
U5A
CR1
(UNLOCK) FROM
LORD 1A5A2 & VAD 1A3A2
+12V
A
+15V
e
+6V
a
AM TUNE
FROM PRE 1A2A4
X
NCW
FROM PANEL 1A1
V
+26V
COMPARATO
U7B
VREF
LOW/BAT
FO(UNLOCK)
INDICATION
PRIORITY
LOGIC
UIC,U5B,U5
U2B, U3C,
U3A, U3B,U
BAT CHK
d
FROM LORD
1A5A2
NM
P
TUNE
N
U5E
IND
B
TX LEVEL
FROM SNF 1A5A3
M
S METER
FROM IF 1A2A2
S
+26V
FROM PS1A4
INDICATION
SELECTOR
U8A,U8B,
U8C, U8D
LED
INDICATION
CONTROL
U13

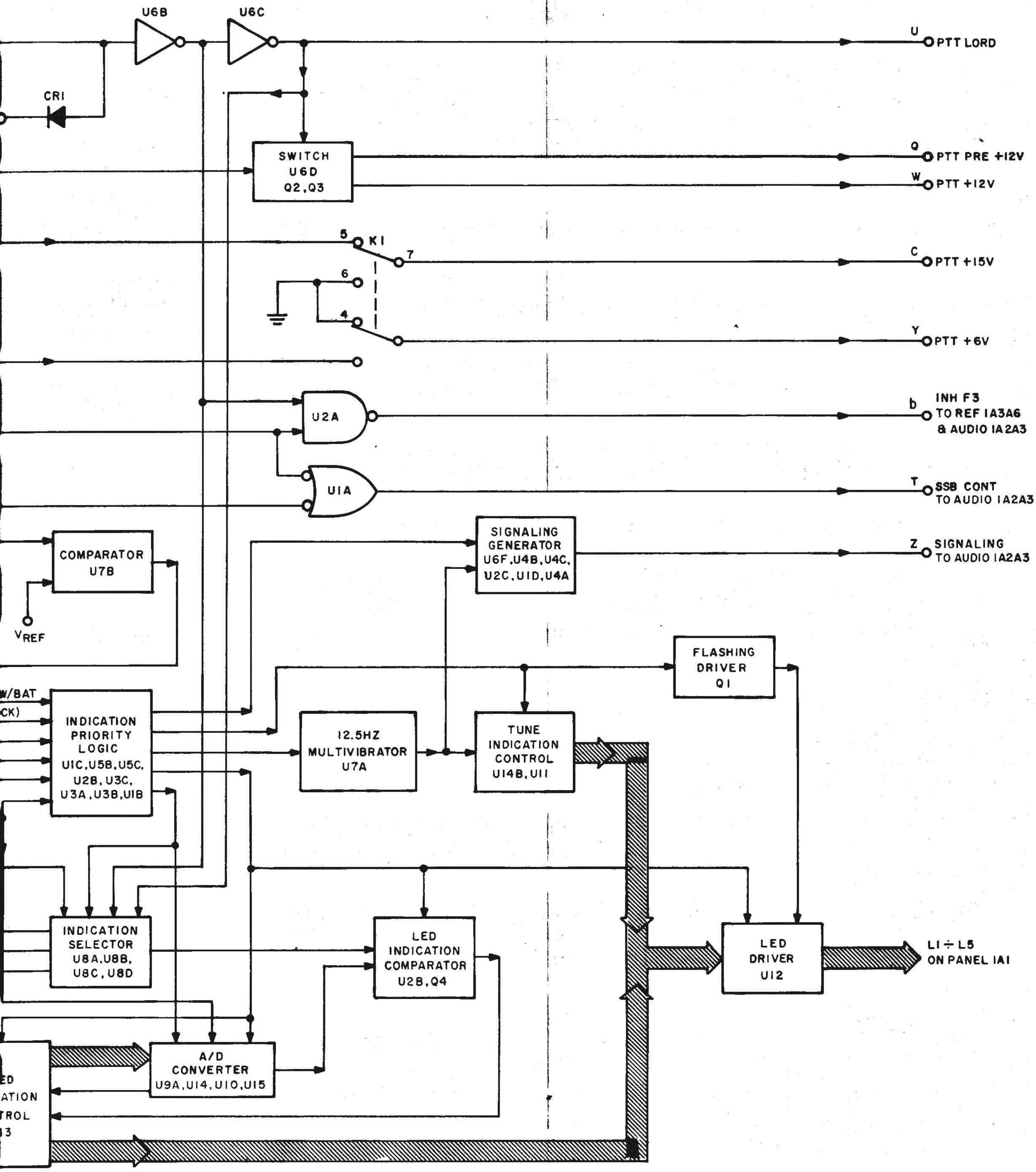
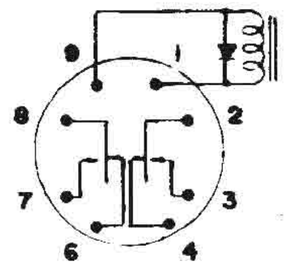
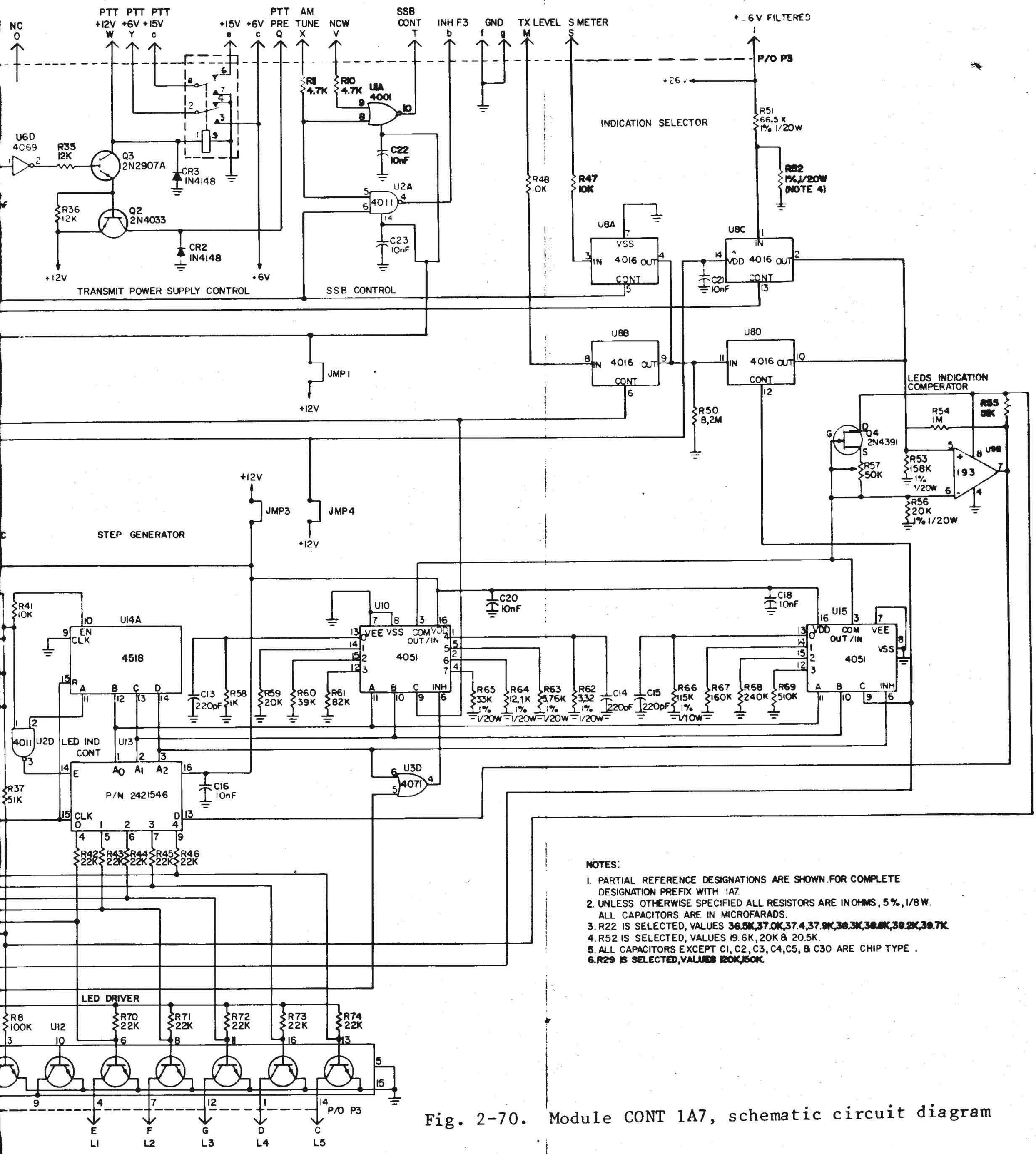


Fig. 2-69. Module CONT 1A7, block diagram



KI-SCHEMATIC DIAGRAM
(UN ENERGIZED POSITION
BOTTOM VIEW)

+12V A
R/T J
SF L
PTT HANG H
PTT LORD U
NC O
PTT LORD
R31 10K
R28 10K
U6A 4069
R30 10K
R33 30K
U6B 4069
U6C 4069
U6D 4069
R34 390K
R35 12K
C11 10nF
C4 2,2 20V
C8 10nF
C9 10nF
CR1 IN4148
U5A 4025
R29 (NOTE 7)
R32 150K
C10 10nF
+12V
TRANSMIT INH
LOW BATTERY CHECK
BLINK DRIVER
+26 V
R21 82,5K 1% 1/2W
R22 1% 1/2W
C7 10nF
(NOTE 3)
C27 10nF
U7B 193
C28 10nF
R23 5,1K
R6 825
12V
R24 390K
R25 10K
PRIORITY
+12V
C30 2,2 10V
Q1 2N2907A
R2 47K
R3 47K
SIGNALING GENERATOR
U4A 4023
U4B 4023
U2C 4011
U1D 4001
C6 10nF
R75 100K
U1C 4001
U4C 4023
U6F 4069
R4 47K
R5 47K
C5 10nF
CLOCK OSC
JMP
+12V
12,5Hz OSC
+6 V
R14 430K
U7A 193
R12 68K
C1 0,47
R13 680K
C29 1nF
TUNE CONTROL
C17 10nF
U14B 4518
CLK
EN
VDD
R
A B C D VSS
C26 10nF
U5B 4025
U2B 4011
U3C 4071
C24 10nF
R15 68K
U11 4028
Q0 Q1 Q2 Q3 Q4 Q5
C19 10nF
R16 22K
R17 22K
R18 22K
R19 22K
R20 22K
U3A 4071
U3B 4071
U1B 4001
U6E 4069
C25 10nF
R1 4,7K
R7 4,7K
R38 180K
U9A 193
R41 10K
C2 220pF
R40 390K
C3 15pF
R39 39K
+6V
+12V
R9 150K
R37 51K
U20 4011
R8 100K
U12
K TP LOW BAT
P NO MATCH
4 FO UNLOCK
TUNE
d BAT CHK
B IND
Z SIGNALING



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A7.
2. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE IN OHMS, 5%, 1/8 W. ALL CAPACITORS ARE IN MICROFARADS.
3. R22 IS SELECTED, VALUES 36.5K, 37.0K, 37.4, 37.9K, 38.3K, 38.8K, 39.2K, 39.7K.
4. R52 IS SELECTED, VALUES 19.6K, 20K & 20.5K.
5. ALL CAPACITORS EXCEPT C1, C2, C3, C4, C5, & C30 ARE CHIP TYPE.
6. R29 IS SELECTED, VALUES 120K, 150K.

Fig. 2-70. Module CONT 1A7, schematic circuit diagram

(4) Low-battery comparator (fig. 2-70). U7B compares the voltage obtained by dividing the primary DC voltage in the voltage divider R21, R22, with the regulated +6V voltage. When the primary DC voltage is too low for normal operation, the output of U7B rises to a high level.

(5) Indication priority control (fig. 2-70, 2-72, 2-75).

(a) Low battery indication. When the output of U7B rises to a high level, the outputs of U1C and U5C are forced to low levels, therefore the output of U4C is forced to a high level and does not influence the alarm indication. The alarm indication is then controlled by U4A. The output waveform of U4A is shown in fig. 2-75.B; from this figure, it can be seen that the output of U4A periodically assumes a low level, thereby causing the flashing control transistor Q1 to conduct and cause all LEDs to flash together. Moreover, the low level appearing at the output of U4A enables the signaling generator (see (7) below) which sends beeps to the AUDIO 1A2A3 module.

The low-battery alarm has the highest priority, therefore it masks all other alarms.

(b) No-match or loss-of-lock (FO UNLOCK) indication. This indication is controlled via U4C and is allowed to appear only when the battery is O.K (U7B output at low level) and the battery control is not set to BAT CHK: in either of these cases, the output of U4C is forced to a high level.

When either the NO MATCH (pin P) or FO UNLOCK (pin R) line rises to a high level, the output of U5C falls to a low level. This is inverted by U5B and the resulting high level lets the signaling waveform to pass via U4C. The resulting output waveform of U4C is shown in fig. 2-75.c. Q1 conducts while U4C output is at a low level, causing all LEDs to flash together, and the signaling generator sends beeps to the AUDIO 1A2A3 module. The NO-MATCH and FO UNLOCK alarm has priority over the tuning indication.

(c) 12.5-Hz oscillator control (fig. 2-72, 2-73). The 12.5-MHz oscillator provides the various waveforms necessary for differentiation between the alarms. The oscillator is turned on when a high level appears at the output of U3B. This happens when the TUNE line arriving from module LORD 1A5A2 rises to a high level (tuning in progress) and also when an alarm condition exists (U5B output at a high level).

(d) Tuning indication (fig. 2-72, 2-75). The tuning indication is controlled by U3C, in conjunction with U3B (see (c) above). When both the TUNE line and the output of U5C are at high levels (indicating that tuning is in progress and that there are no alarms), the output of U2B falls to a low level. Assuming that the LEDs are not being used for battery voltage display (BAT IND line at a low level), the output of U3C also assumes a low level and the tuning indication is enabled. An auditory indication is also provided, via U6F (see fig. 2-70 and 2-75.A).

(e) Solid-state display control. The solid-state display is used for indication of battery voltage when the BAT CHK line rises to a high level. This forces the output of U3A to a high level, thereby activating the A/D converter (see (8) below).
The A/D converter is also enabled, this time for measurement of the TX LEVEL and S-METER voltages, when the IND line rises to a high level. This forces the output of U3A to a high level, thereby activating the A/D converter (see (8) below).
The low level appearing at the output of U6E when the IND line assumes a high level adapts the measurement range of the A/D converter to that of the TX LEVEL or S-METER voltage (this

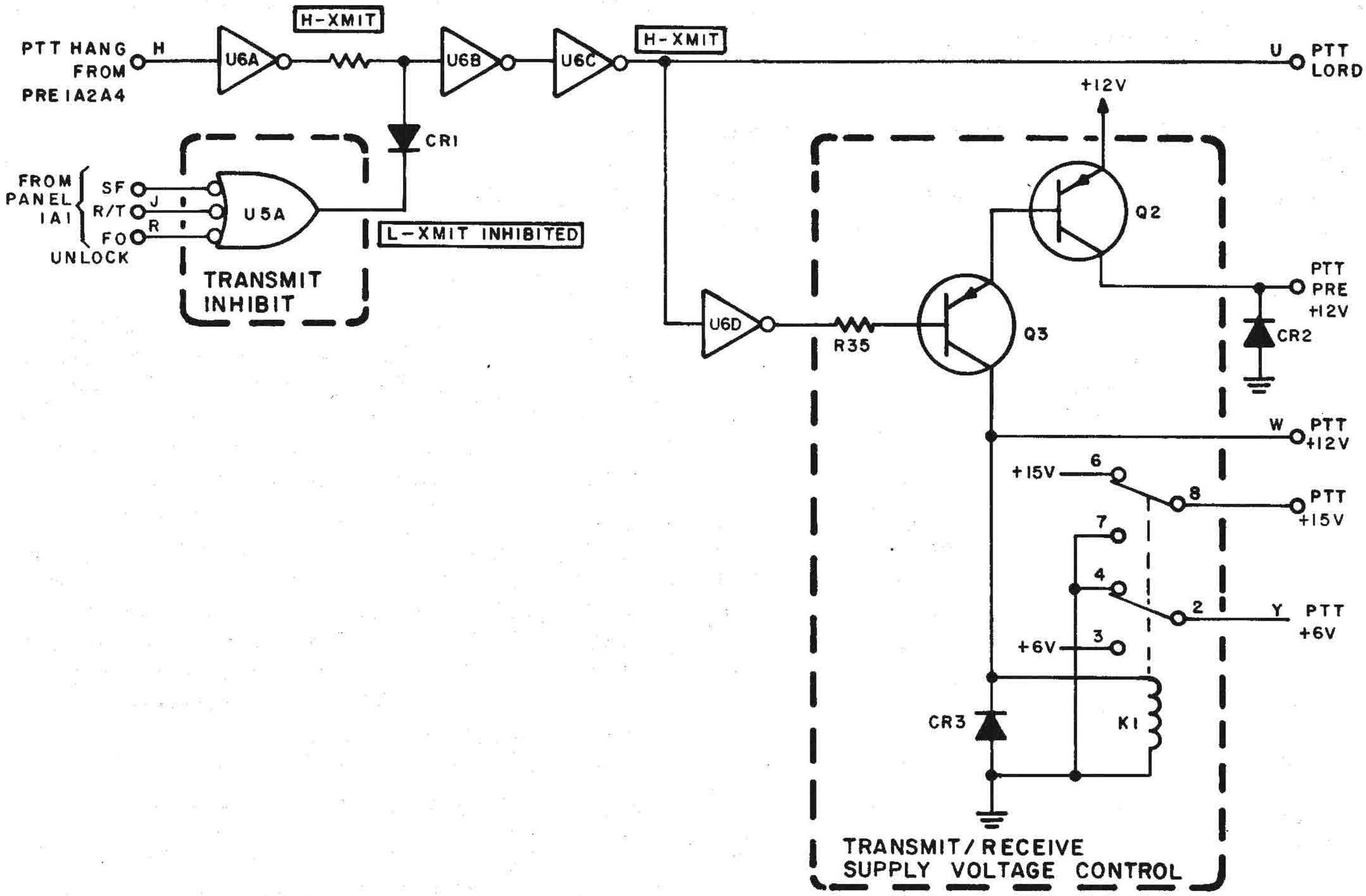


Fig. 2-71. PTT and supply voltage control, simplified circuit diagram

second selection is controlled by the state of the PTT LORD line).

When the output of U3B or U6E assumes a high level, the output of U1B assumes a low level, thereby adapting the measurement range of the A/D converter to the measurement of the battery voltage. The battery measurement has priority over TX LEVEL and S-METER measurement.

(6) Tuning indication control circuit (fig. 2-73, 2-74). The tuning

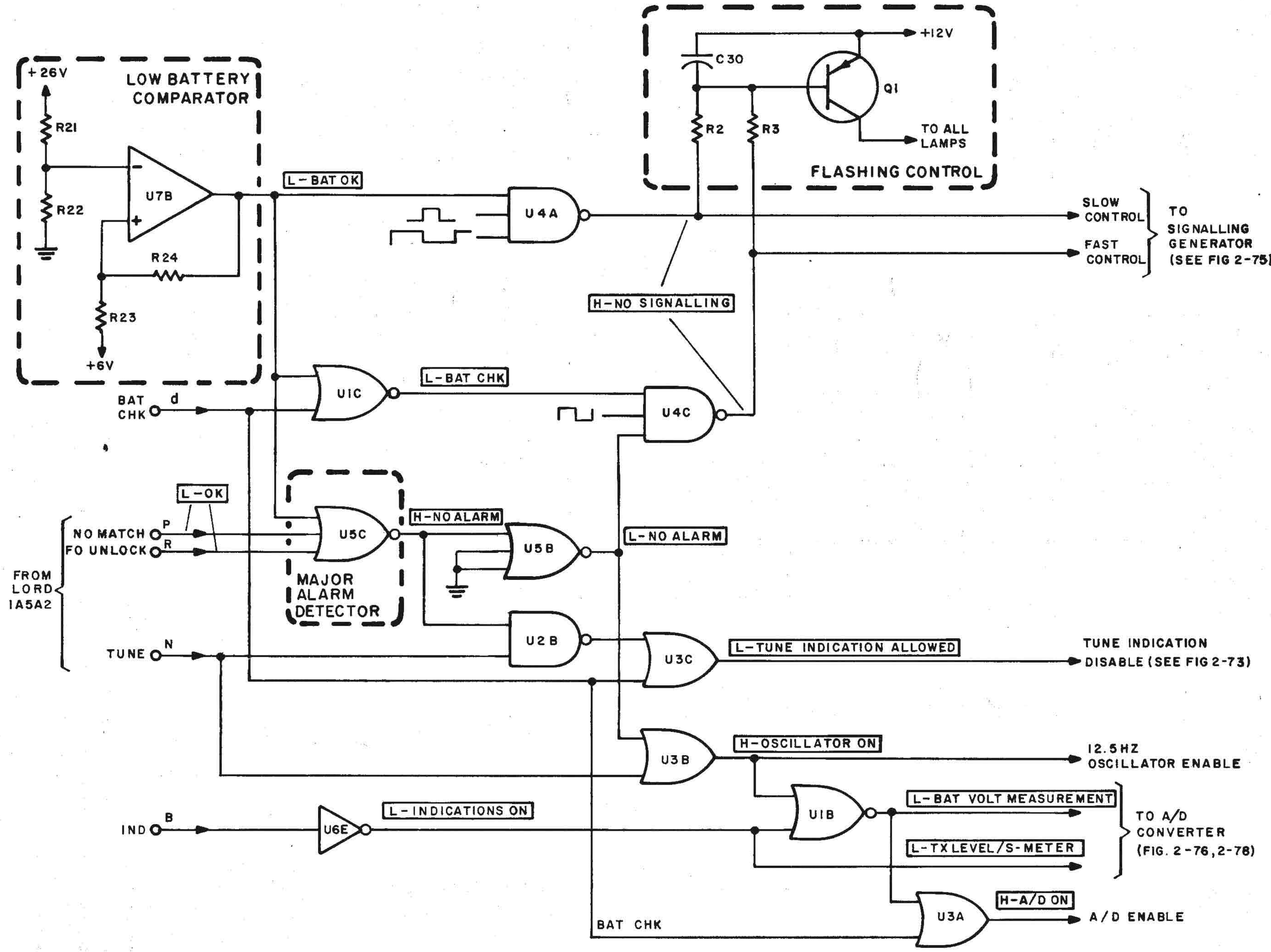


Fig. 2-72. Indication priority control, simplified circuit diagram

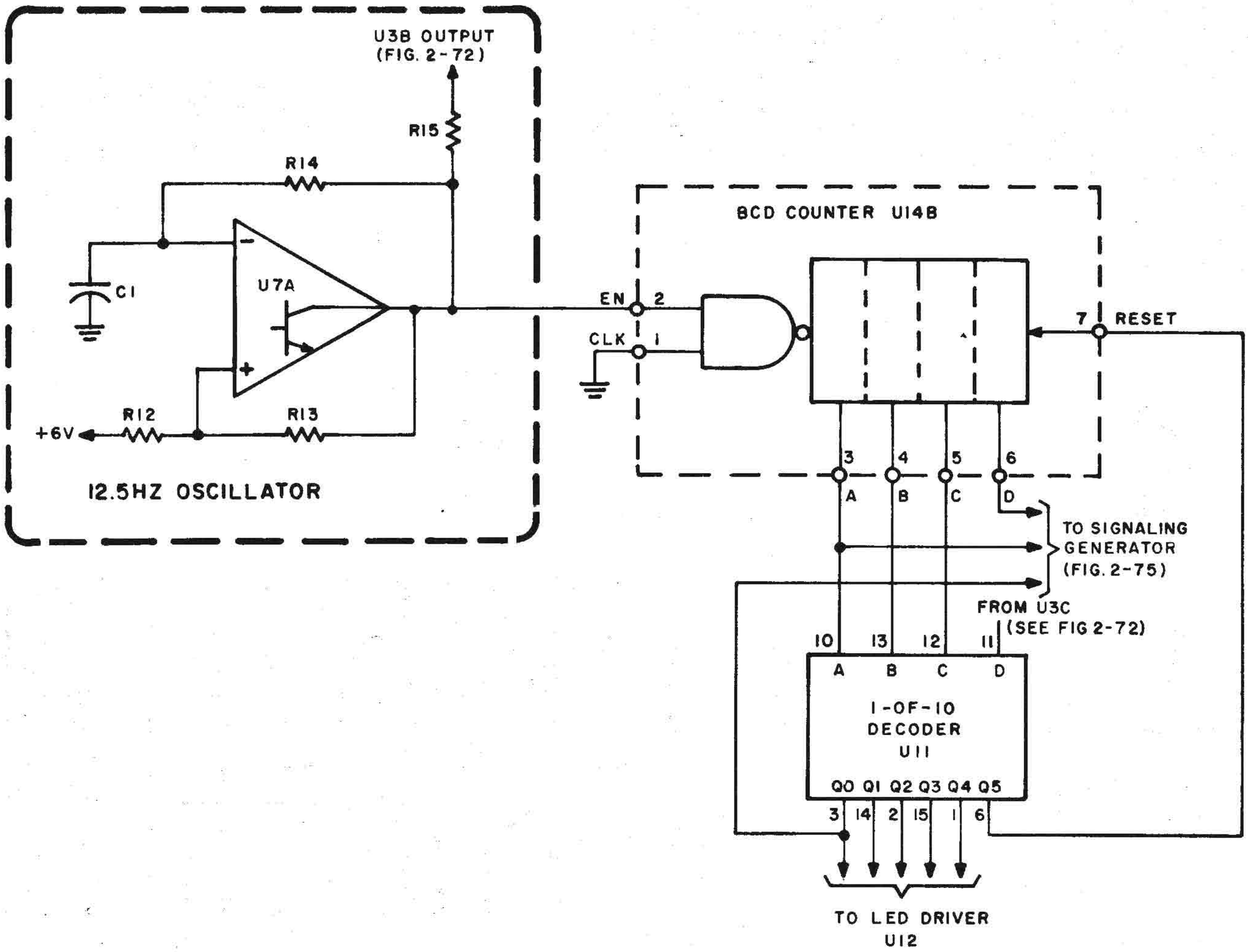


Fig. 2-73. Tuning indication control, simplified circuit diagram

indication is started when the output of U3B rises to a high level and the output of U3C is at a low level.

The 12.5-Hz oscillator is an astable multivibrator, built around U7A. The oscillation frequency depends on the values of the timing components R14 and C1, and on the value of the threshold voltage, determined by R12 and R13. U7A has an open-collector output, thereby internal signals may appear at the output only when an external voltage is applied to the collector resistor R15: this voltage is provided by U3B, when its output is at a high level.

The clock pulses provided by U7A are applied to a BCD counter, U14B. The BCD code appearing at its A, B and C outputs is used to drive the inputs of the 1-of-10 decoder, U11. The output of U3C is low during the tuning indication, therefore pulses appear cyclically at the Q0, Q1, Q2, Q3, Q4 and Q5 outputs, according to the binary value of the input word. When the Q5 output rises to a high level, it immediately resets U14B. This mode of operation is used for tuning indication purposes. Typical waveforms are shown in fig. 2-74.
When the output of U3C assumes a high level, the input address of U11 is modified and no pulses appear at the Q0 through Q5 outputs. This lets the BCD counter run freely through all its 10

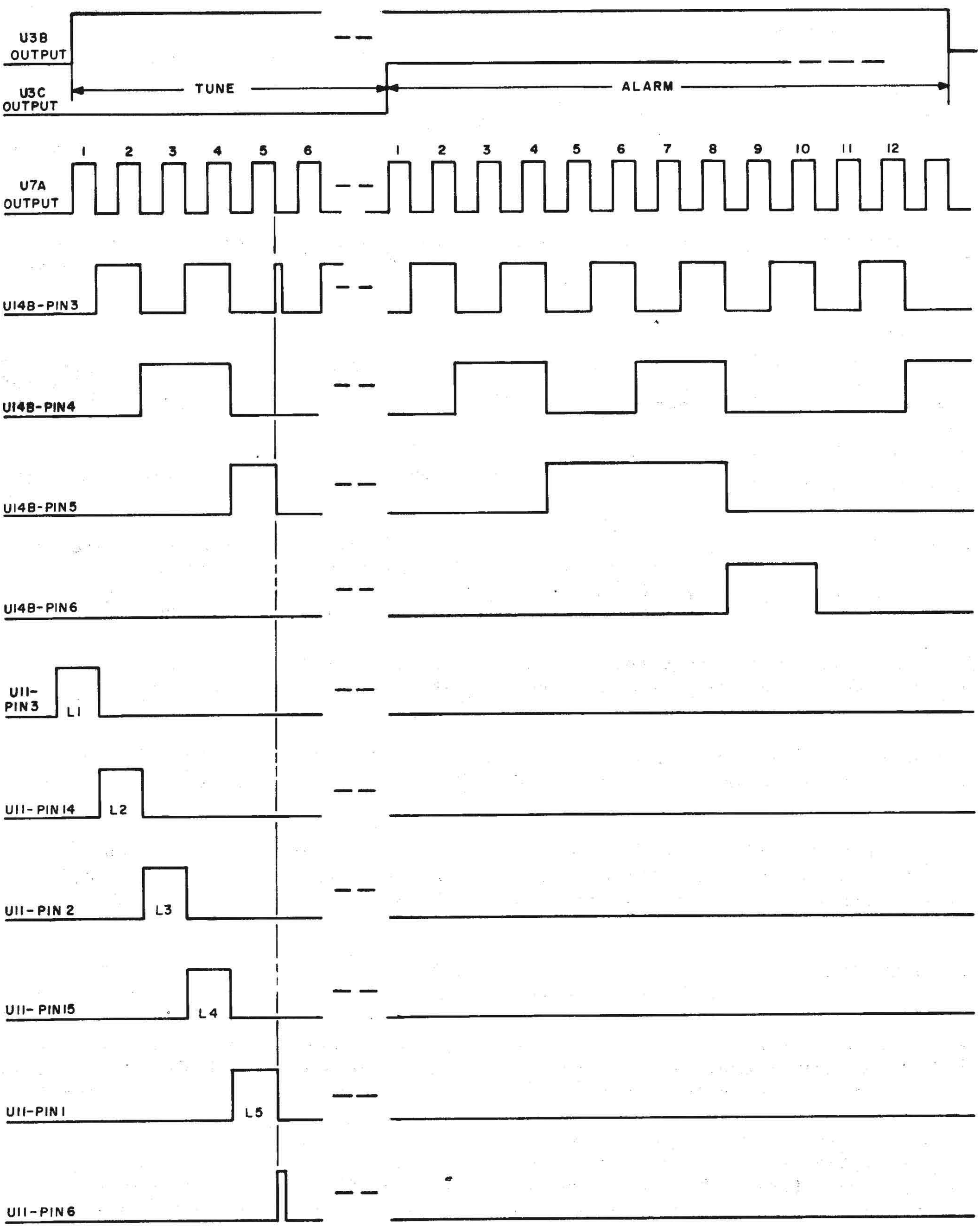


Fig. 2-74. Tuning indication control, typical waveforms

states. This mode of operation is used for the generation of auditory and visual indications when an alarm condition exists.

(7) Signaling generator operation (fig. 2-70, 2-75). The signaling generator consists of a gated 1-kHz oscillator, built of U2C and U1D. When the output of the control gate U4B rises to a high level, the oscillator is enabled, and it generates a square wave having a nominal frequency of 1 kHz. The oscillator frequency is determined by R4, R5 and C5.

Fig. 2-75 shows the gating signals applied to the oscillator and the resulting signaling waveforms.

The output signal of U10 is sent via C6, R75 and pin Z to the AUDIO 1A2A3 module.

(8) A/D converter (fig. 2-76 through 2-79).

(a) Input selector (fig. 2-76). The input selector receives the TX LEVEL, S-METER, and primary DC voltage and selects one of them for application to the A/D converter. The selection between TX LEVEL and S-METER is made by U8A and U8B according to the state of the PTT LORD line (the outputs of U6B and U6C). Another selector, comprised of U8C and U8D, selects between the primary DC voltage and the previously selected voltage, this time according to the state of the BAT CHK line.

(b) A/D converter block diagram (fig. 2-77). The A/D converter is essentially a modified successive-approximation converter, which compares the selected input signal with a staircase signal and determines the number of the stair on which the input signal value fits. The staircase is generated by decoding the outputs of a counter and varying accordingly the value of a resistance connected to a constant current source: the voltage developing across the resistance therefore changes in steps, which form the stairs of the staircase signal. The staircase signal serves as the reference voltage for the comparator. The output level of the comparator is loaded into sequential addresses of an addressable latch; one value is stored for each stair value. As long as the input voltage exceeds the instantaneous staircase reference, the comparator output remains at a high level. When the staircase exceeds the input signals, the comparator's output falls to a low level.

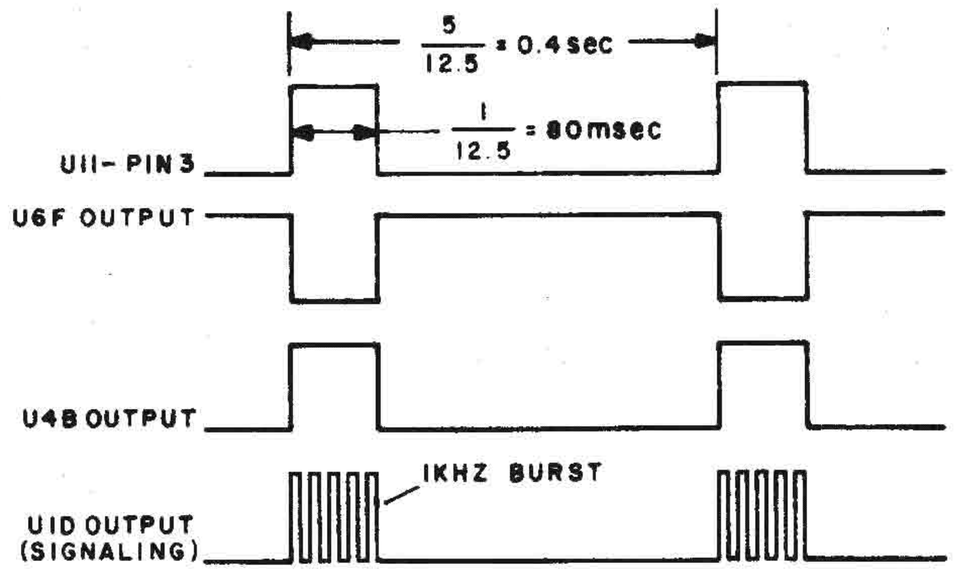
The outputs of the latch are applied to the lamp driver, which drives the LEDs of the solid-state display.

High latch output levels cause the corresponding LEDs to light, therefore the number of lit LEDs equals the number of stairs whose voltages are smaller than the input voltage.

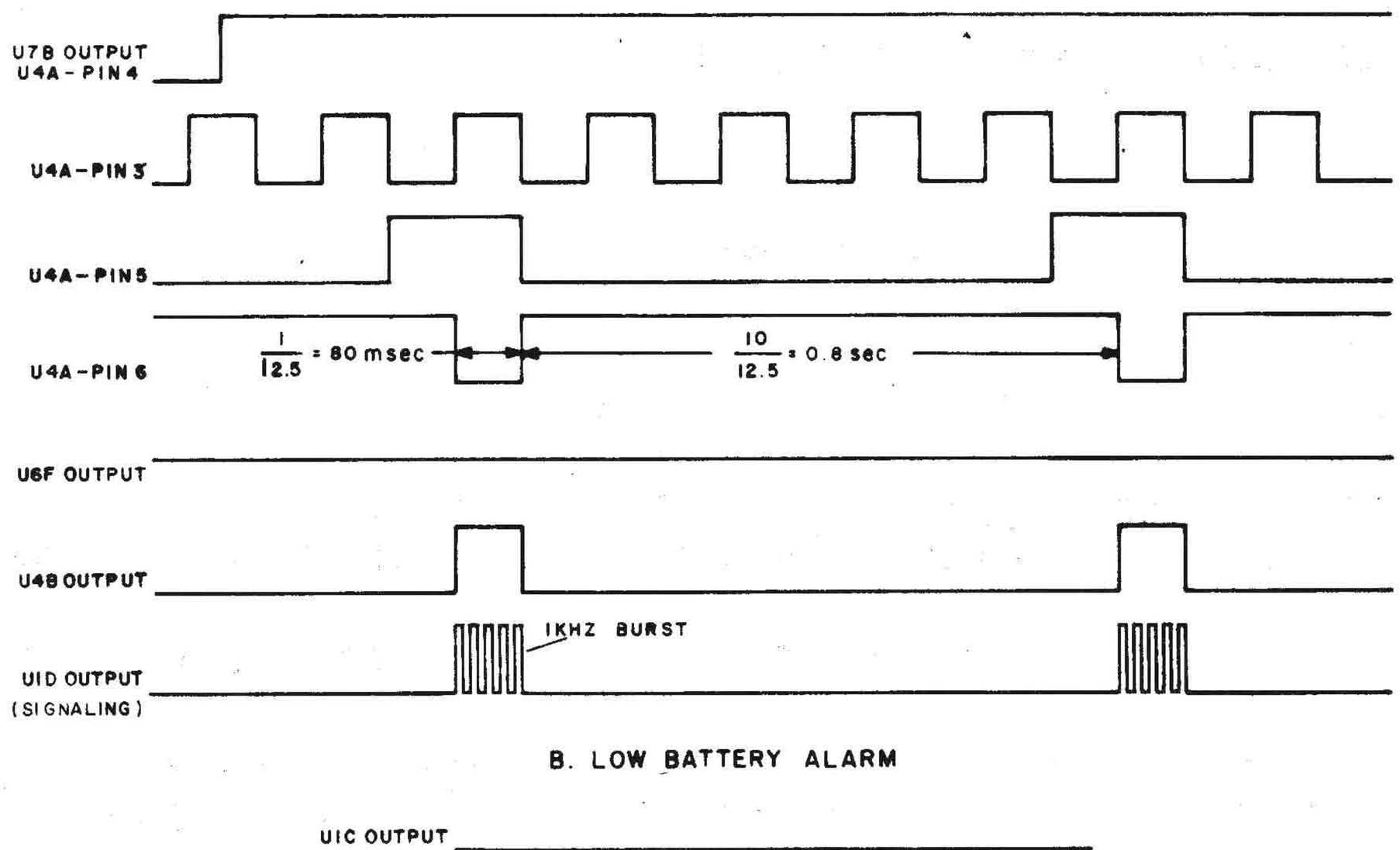
The operation of the A/D converter is started when the output of U3A rises to a high level. The appropriate staircase values are selected under control of U6E, U1B and the PTT LORD line.

(c) Circuit analysis (fig. 2-78, 2-79). The A/D converter starts when its clock oscillator is enabled. The clock oscillator is an astable multivibrator, built around U9A, which operates similarly to the 12.5-Hz oscillator (see (6) above). The oscillator is turned on when the output of U3A rises to a high level. The square wave signal generated by U9A is applied to the clock input of the BCD counter U14A. The counter (and also the addressable latch U13) is normally held in the reset state by the high level applied through R9. When the output of U3A rises to a high level, transistor U12A (one of the eight independent transistors contained in U12) saturates and applies a low level at the reset inputs of U14A and U13, and they may start operating.

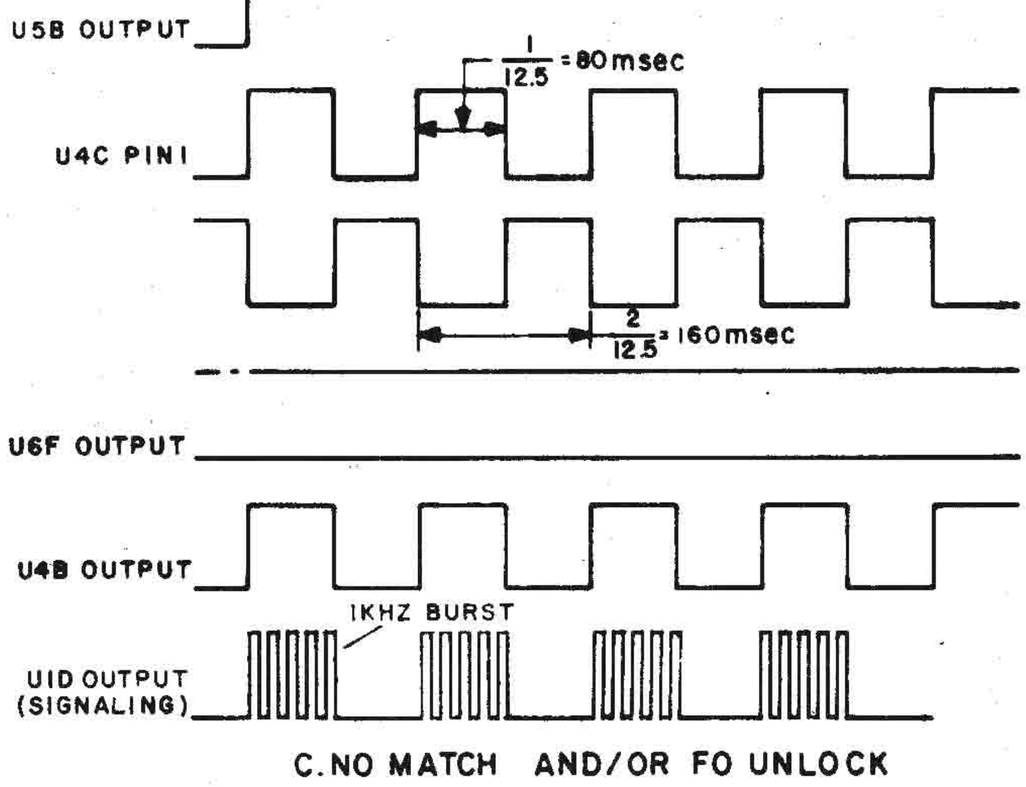
The bits appearing at the three most



A. TUNING INDICATION



B. LOW BATTERY ALARM



C. NO MATCH AND/OR FO UNLOCK

Fig. 2-75. Signaling generator, typical waveforms

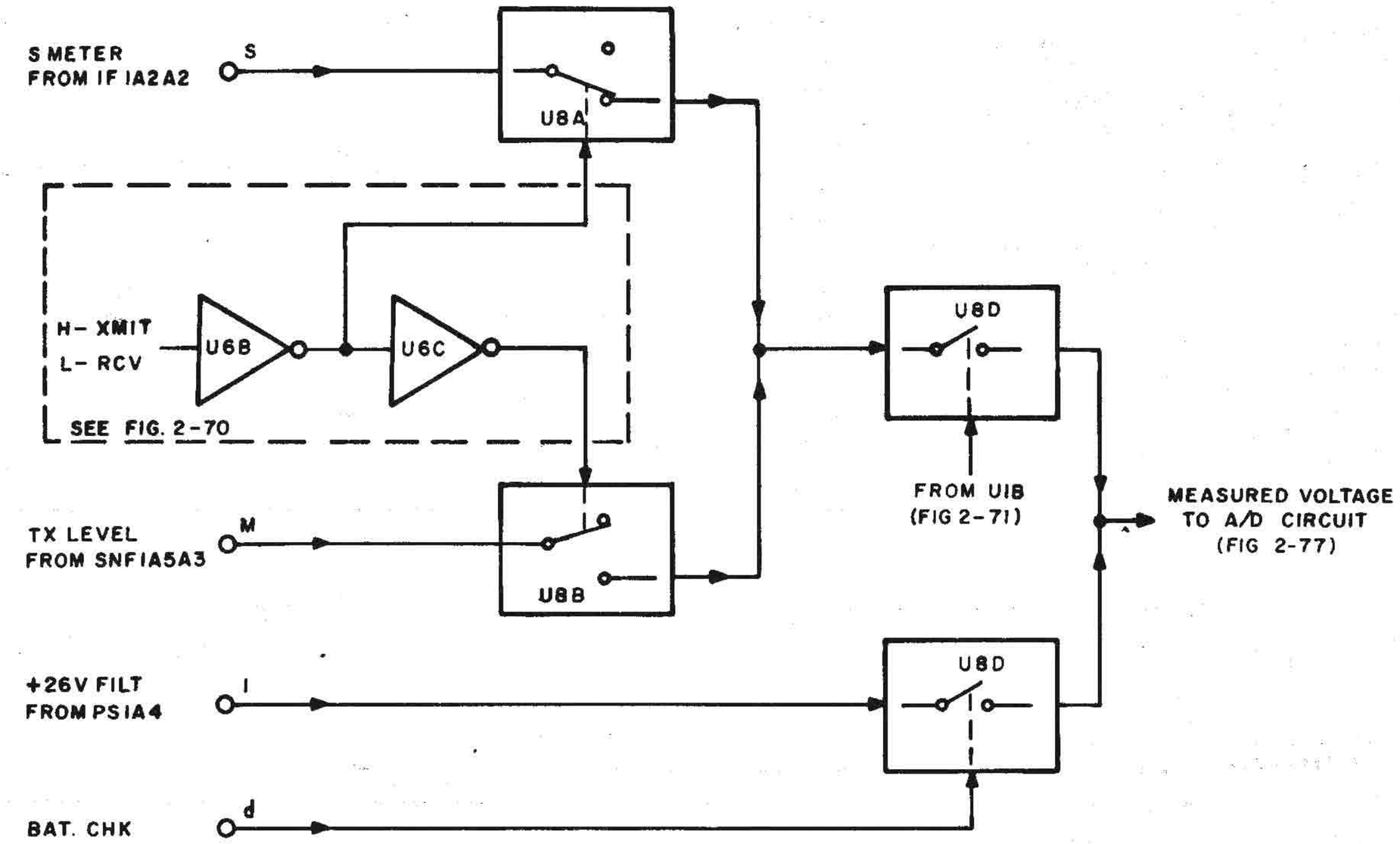


Fig. 2-76. A/D converter, input selector simplified circuit diagram

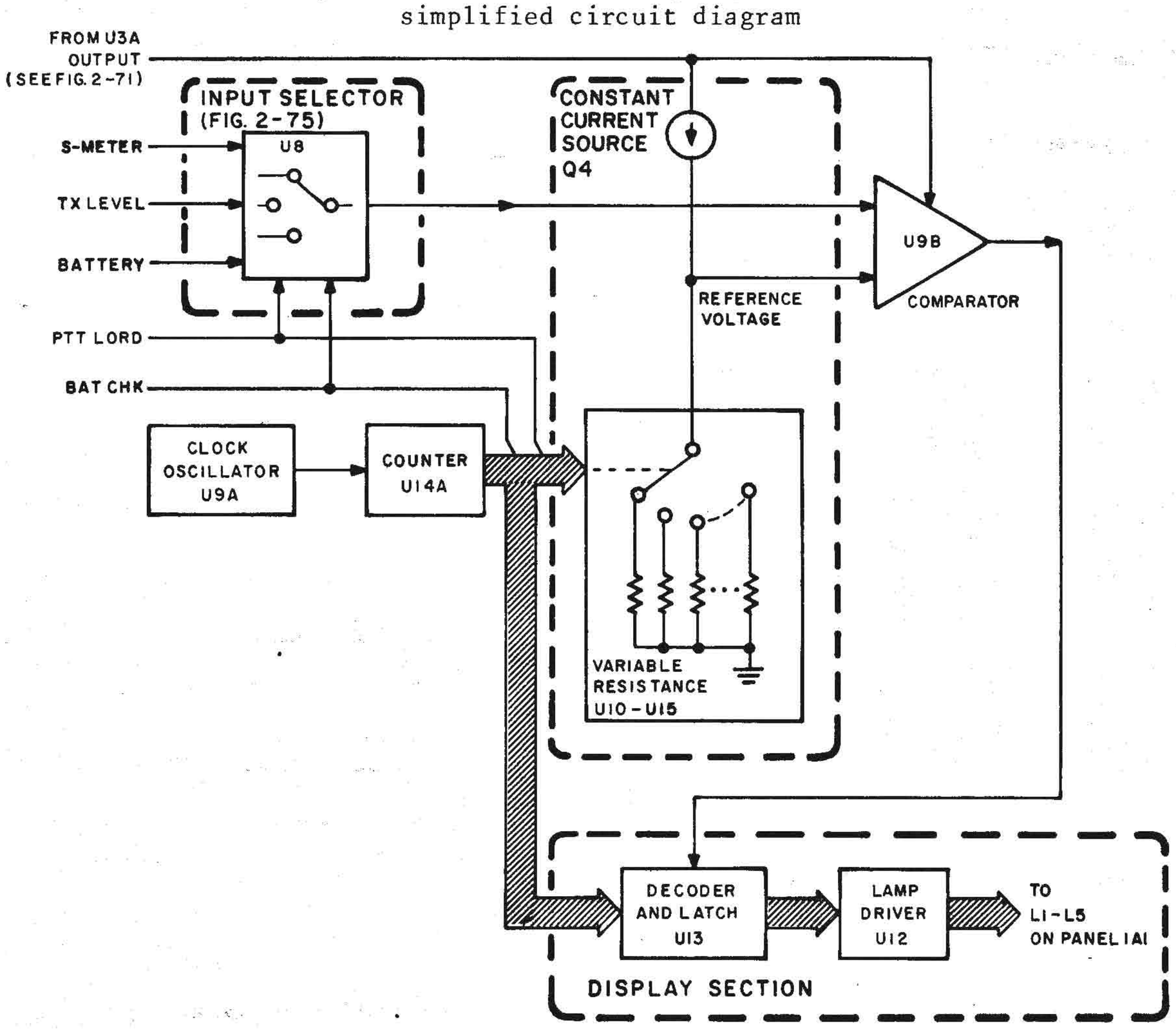


Fig. 2-77. A/D converter, block diagram

U3A
OUTPUT
(FIG 2-72)

CLOCK OSCILLATOR

R37

R8

R38

CR

U9A

+6V

R39

R40

10

EN

BCD
COUNTER
U14A

R

A B C D

11 12 13 14

U2D

REFERENCE VOLTAGE GENERA

U10
FUNCTIONAL
EQUIVALENT

PTT LORD

R58 R59 R60 R61

1 2 3

A0 A1 A2

U13

DECODER

+12V

R9

14 EN

RESET

LATCHES

D 13

R42 R43 R44 R45 R46

L1

L5

A E F G D C

U12

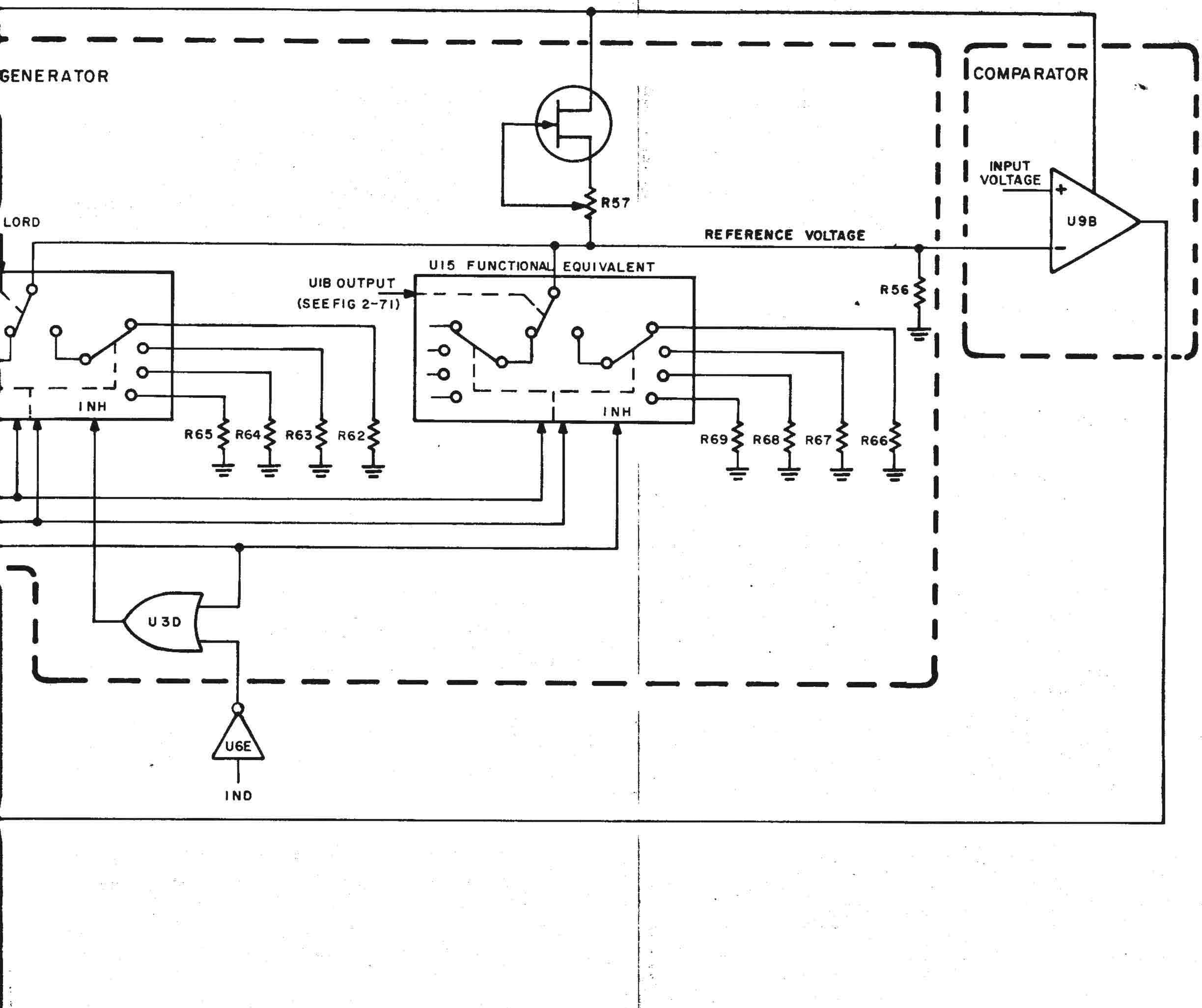
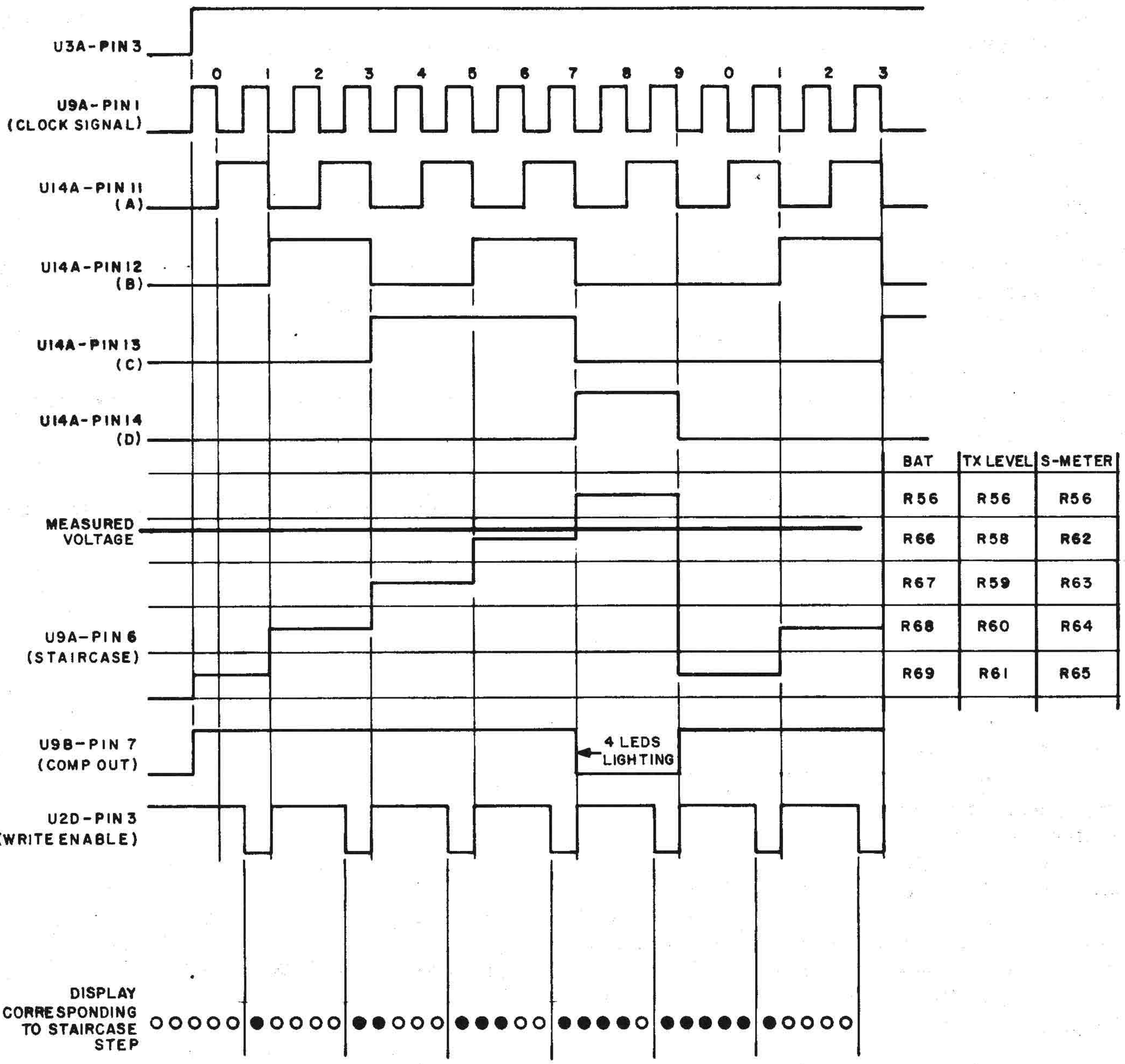


Fig. 2-78. A/D converter, simplified circuit diagram



BAT	TX LEVEL	S-METER
R56	R56	R56
R66	R58	R62
R67	R59	R63
R68	R60	R64
R69	R61	R65

Fig. 2-79. A/D converter, typical waveforms

significant outputs (B, C and D) of the counter are used as the address for the addressable latch U13 and also for the selectors U10 and U15, which selects the value of the reference resistance. Therefore, when the counter steps up resistors are connected in sequence to the current source consis- ting of FET Q4 and R57.

U15 is used to select the resistors for the measurement of the primary AC voltage. Only four resistor values are actually used, and these are addressed by means of the bits appearing on the A and B inputs (pin 11 and 10, respectively) while input C (pin 9) is at a low level. Input C is controlled by the output of U1B (see fig. 2-72) and is low when the primary DC voltage is measured. U15 has a fourth control input, INH (pin 6), which disables the outputs when raised to a high level. The INH input is controlled by the most significant output (D) of U14; this output is low during the conversion cycle, and rises to a high level between successive conversion cycles.

U10 operates similarly to U15, except that it provides two different sets of resistors: R58 through R61 for S-METER measurement, and R62 through R65 for TX LEVEL measurement.

The selection between the two sets is controlled by the PTT LORD line, connected to input C. The INH input of U10 is controlled by U3D, which generates a high level in two cases: when the D output of U14A rises to a high level and/or when the output of U6E is at a high level (battery control set to a position other than IND).

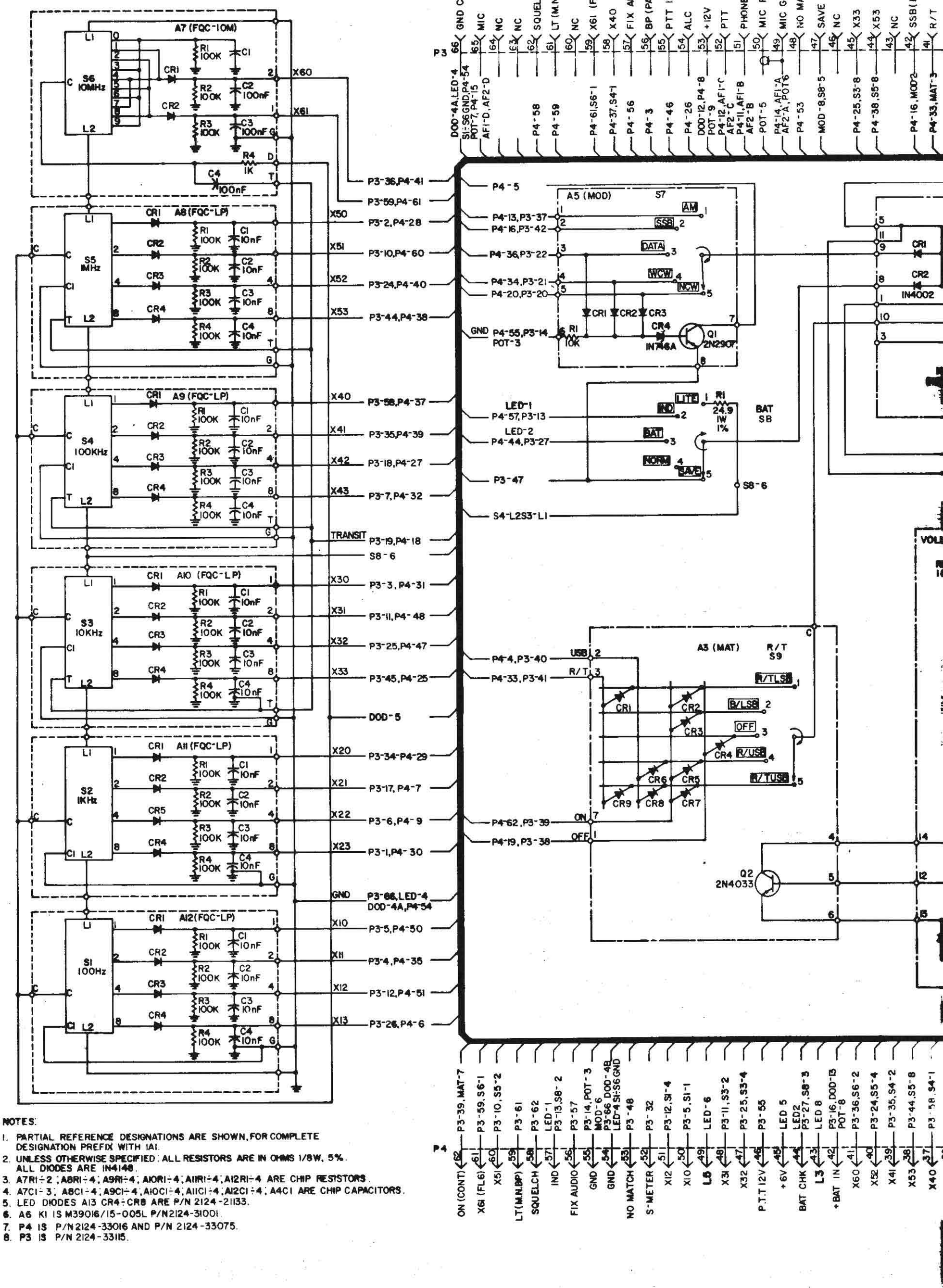
The voltage developing across the selected resistance, due to the current provided by Q4, is applied to the inverting input of U9B. U9B operates as a Schmitt trigger, which receives, at its non-inverting input, the selected input voltage. The output of U9B remains at a high level as long as the selected input voltage exceeds the voltage developing across the selected resistance. After each resistor change, the new output level of U9B is stored in the latch U13, at the address determined by the B, C and D outputs of the counter U14A. The latch outputs are connected to the transistors contained in U12. These transistors are used to connect the cathodes of the LEDs to ground. Therefore, the number of lighted LEDs equals the number of steps for which the output of U9B was at a high level.
Fig. 2-79 shows typical waveforms in the A/D counter circuit.

2-24. Panel Assembly 1A1 (fig. 2-80)

The front panel contains all operator controls, the solid state display, and the CONTR connector.

a. Remote Control Relay. The remote control relay, K1, connects, in its unenergized position, the +12V supply voltage for the front panel controls. This activates their output lines. When remote control is desired terminal 9 of the relay coil is grounded, via CR4 and pin 8 of the CONTR connector, at the remote control device. This energizes the relay; the +12V are then disconnected from the controls, and connected instead to the external device, via pin 23 of connector CONTR. Relay K1 also disconnects the ground line from the mode selector, S9.

b. Frequency Selectors. S1 through S6 are BCD-coded thumbwheel switches, which provide a BCD word whose decimal value equals the manually-selected position. The switches receive +12V at contact C and ground at contact C1. The output lines of the switches are connected in parallel with the external frequency control lines, available at connector CONTR (P3). Diodes prevent interference between the internal and external lines. At the T



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION PREFIX WITH 1A1.
2. UNLESS OTHERWISE SPECIFIED: ALL RESISTORS ARE IN OHMS 1/8W, 5%. ALL DIODES ARE IN4148.
3. A7R1÷2; A8R1÷4; A9R1÷4; A10R1÷4; A11R1÷4; A12R1÷4 ARE CHIP RESISTORS.
4. A7C1÷3; A8C1÷4; A9C1÷4; A10C1÷4; A11C1÷4; A12C1÷4; A4C1 ARE CHIP CAPACITORS.
5. LED DIODES A13 CR4÷CR8 ARE P/N 2124-21133.
6. A6 KI IS M39016/15-005L P/N2124-31001.
7. P4 IS P/N2124-33016 AND P/N 2124-33075.
8. P3 IS P/N 2124-33115.

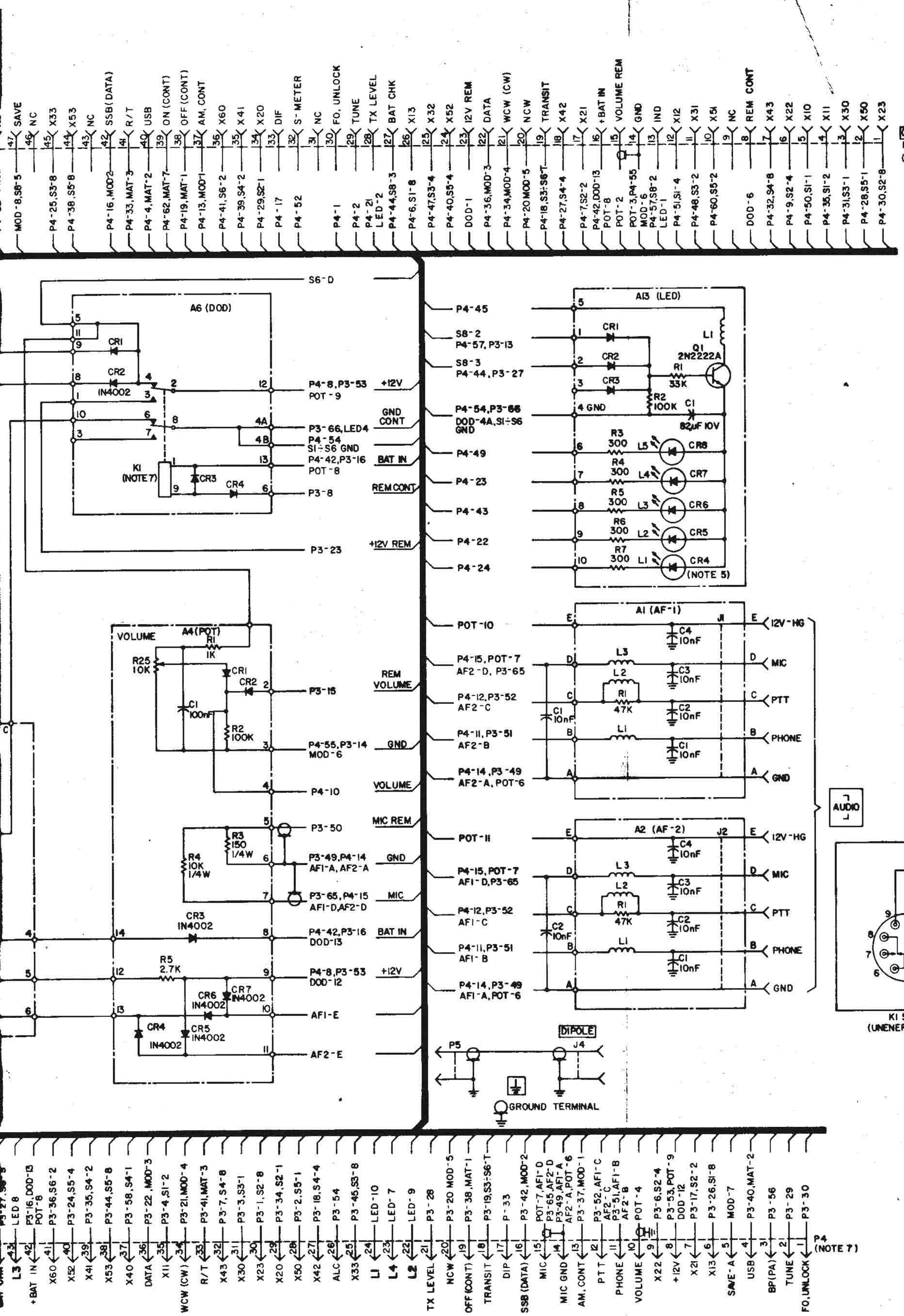


Fig. 2-80. Panel assembly 1A1, schematic circuit diagram

terminal of S3 through S6, a +12V pulse appears when the switch position is changed. This pulse passes through the TRANSIT line to the LORD 1A5A2, which generates in response to the SF pulse.

c. Function Selector S7 and Battery Control S8. The center contacts of these selectors receive +12V, and apply this voltage to the line corresponding to the selected position. In the LITE position of S8, current is supplied through R1 to the LEDs contained in switches S3 and S4.

In the SAVE position, the emitter of Q1 receives +12V. Current then flows from the base of Q1, through Zener diode CR4, and resistor R1 to ground, and the SAVE line rises to a high level. However, when the DATA, WCW or NCW mode is selected, the base of Q1 is pulled via CR1, CR2 or CR3 to +12V and the Q1 remains cut off. This disables the squelch circuits when operating in the DATA, WCW or NCW mode.

d. Mode Selector S9. The center contact of S9 is grounded, and grounds the corresponding line. A diode matrix is used to apply the ground on the ON CONT line, leading to the ON/OFF relay in the PS1A4 module, whenever the switch is set to a position other than OFF. Another group of diodes is used to ground the R/T line, leading to module CONT 1A7, when a receive/-transmit position is selected.

e. Volume Control and POT Assembly. The volume control, R25, provides a variable DC voltage for the electronic volume control circuit in module AUDIO 1A2A3. Diodes isolate the output of R25 from the remote volume control line.
The POT assembly also has an attenuator for the signal applied on the external high level microphone line, available at the CONTR connector. The attenuator presents a 150-ohm input resistance. An external battery charging input and an output for the +12V internal voltage is available at pins E of the AUDIO connectors, and at 53 of the CONTR connector. Current may flow from the internal +12V supply via diode CR5 or CR7 to an external load, or the internal battery may be charged via CR4 or CR6 and transistor Q1 on the MAT assembly when an appropriate source is connected.

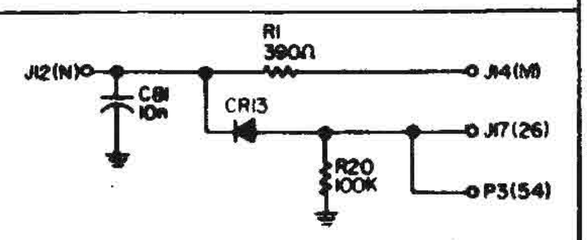
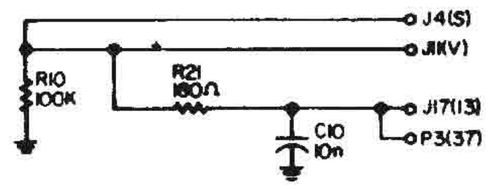
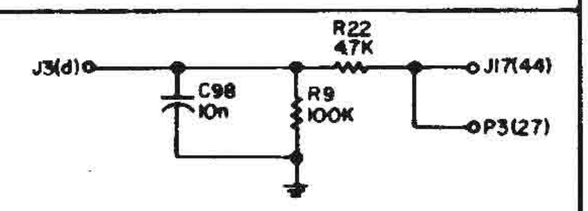
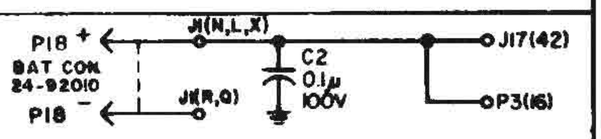
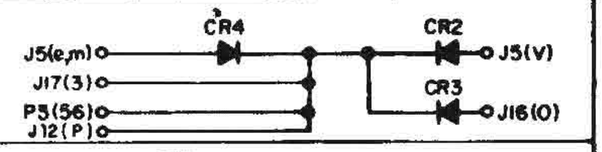
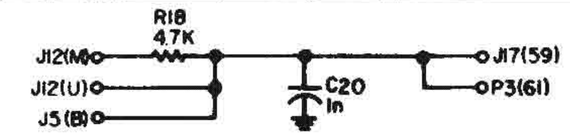
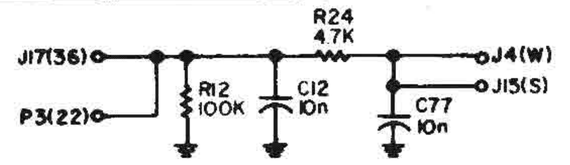
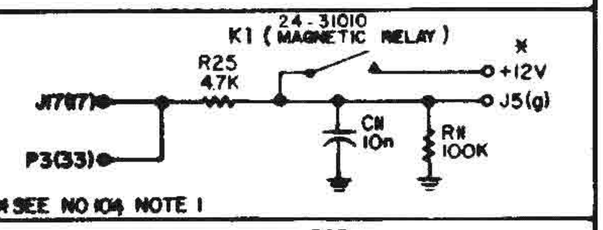
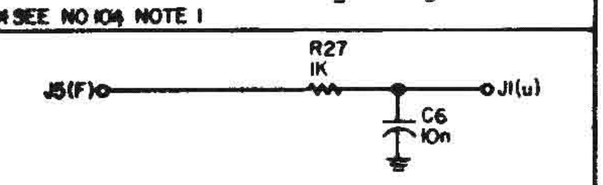
f. Solid State Display. The solid state display consists of five LEDs. The LED anodes receive +6V via transistor Q1 when either the IND or BAT CHK mode is selected. The cathodes are connected to the drivers in module CONT 1A7.

g. AUDIO Connectors. The AUDIO connectors contain RF filters.

h. CONTR Connector. The CONTR connector, P3, provides lines for a remote control device; most of them are connected in parallel with the corresponding lines coming from the front panel controls.

2-25. Chassis Wiring (fig. 2-81)

Fig. 2-81 provides a wiring table for the RT-936/PRC-174, arranged in alphabetic order according to the signal names.

NO	FUNCTION	PS J1	VCP J2	CONT J3	PRE J4	LORD J5	REF J6	VAD J7	LOL J8	USB J9	SUM J10	AUD J11	SNF J12	FIL J13	MIX J14	IF J15	PA J16	PANEL J17	REMOTE P3 NOTE 1	NOTES
1	AGC II														D,T	O,I				D&T, O&I ARE SHORTED INSIDE THE MODULES
2	A L C												N		M			26	54	
3	AM AUDIO											W				W				
4	AM, CONT				S							V						13	37	
5	AM TUNE			X	E									M						
6	AM TUNE,TX				J											B				
7	BAT CHK			d														44	27	
8	+BAT IN	N,L,X																42	16	
9	-BAT IN	R,Q																		
10	BP(PA)					V							P				O	3	56	
11	LT(M.N.BP)					B							U					59	61	
12	DATA				W											S		36	22	
13	DEL VAD PULSE		W								U									
14	DIF		F					T												
15	DIP					9												17	33	
16	EN CONT	M				F														

NOTES. 1. CONNECTION TO P3 (REMOTE CONNECTOR IN THE PANEL - 66 PIN CONNECTOR ONLY) IS FOR INFORMATION ONLY. IT IS NOT PART OF THIS MODULE.
2. ALL CAPACITORS EXCEPT C71, C2 AND C4 ARE CHIP CAPACITORS.
3. ALL DIODES ARE IN 4148.
4. W1, W2, W3 AND W5 ARE NOT PART OF 2124-91800-00 ASSY.

Fig. 2-81.A. Wiring of motherboard and chassis assembly (Sheet 1 of 8)

NO	FUNCTION	PS J1	VCP J2	CONT J3	PRE J4	LORD J5	REF J6	VAD J7	LOL J8	USB J9	SUM J10	AUD J11	SNF J12	FIL J13	MIX J14	IF J15	PA J16	PANEL J17	REMOTE P3	NOTES
17	FL1					R							H							
18	FL2					M							L							
19	FL3					j							C							
20	FL4					h							J							
21	FL5					f							G							
22	FIX AUDIO											A						56	57	J17(56) o—o J11(A) P3(57) o
23	H.T					D							S							J12(S) o—o J5(D) C7 10n
24	IF MOD DETEC													Q		U				
25	INH F3			b			G					X								J3(b) o—R28 4.7K—o J6(G) J11(X) o—C8 10n
26	IND			B														57	13	R15 100K, C89 10n J17(57), P3(13), J3(B)
27	LI			E														24		C9 10n J3(E), J17(24)
28	L2			F														22		C15 10n J3(F), J17(22)
29	L3			G														43		C16 10n J3(G), J17(43)
30	L4			D														23		C17 10n J3(D), J17(23)
31	L5			C														49		C18 10n J3(C), J17(49)
32	L.O.F								Q		C									
33	MIC				F.Y													15	65	
34	MIC GND				H													14	49	PIN 14 IS SHORTED TO CHASSIS GND
35	MOD IN													A	G					
36	MOD SIGN				C							T				F				
37	NO MATCH			P		S												53	48	J5(S) o—CR9—o J3(P) R4 100K, R56 4.7K J17(53), P3(48)
38	OFF (CONT)	Y																19	38	
39	ON (CONT)	P																62	39	
40	PH CONT					I							V							

Fig. 2-81.B. Wiring of motherboard and chassis assembly (Sheet 2 of 8)

NO	FUNCTION	PS J1	VCP J2	CONT J3	PRE J4	LORD J5	REF J6	VAD J7	LOL J8	USB J9	SUM J10	AUD J11	SNF J12	FIL J13	MIX J14	IF J15	PA J16	PANEL J17	REMOTE P3	NOTES
41	PHASE PULSE		a								X									
42	PHONE											R						11	51	
43	PTT				K													12	52	
44	PTT HANG			H	I															
45	PTT LORD			U		e,m														J17(3) — CR4 — R5 10K — J3(U); J5(e,m)
46	PTT PRE +12V			Q	T,V								M		A,C,Y	A				J4(T,V); J3(Q); J12(M); J14(A,Y,C); J15(A) — C101 100m; C86 100m — R60 22K — J15(Y)
47	PTT 6V			Y													K,M			
48	PTT 12V			W									A					46	55	
49	PTT 15V	O		c								O			B					J1(O) — L12 100µH — J11(O); J3(c) — C80 10n; C32 10n; C23 10n — J14(B)
50	PULSE															Y				
51	∅					C							Y							J12(Y) — C25 1n — J5(C)
52	R					G							W							J12(W) — C26 1n — J5(G)
53	RFS	J				H									I					J1(J) — CR10 — J5(H); J14(1) — R31 1K
54	RF IN												B							P20 — W4 — L22 2413171 — L23 2413172 — L21 2413170 — J12(B); C3 7-40P; C4 18P; FILTER 100
55	RF PRE				X												P			S.R.O; J16(P) — J4(X)
56	R/T			J														33	41	
57	SAVE					•						E						5	47	J17(5) — R59 270Ω — J11(E); C28 10n; P3(47)

Fig. 2-81.C. Wiring of motherboard and chassis assembly (Sheet 3 of 8)

NO	FUNCTION	PS J1	VCP J2	CONT J3	PRE J4	LORD J5	REF J6	VAD J7	LOL J8	USB J9	SUM J10	AUD J11	SNF J12	FIL J13	MIX J14	IF J15	PA J16	PANEL J17	REMOTE P3	NOTES
58	SF			L		K														
59	S' METER			S												G		52	32	* JMP2 IS NOT USED TO CONECT SF FUNCTION TO REMOTE CONECTOR P3. CONECT JMP2 AND DISCONECT JMP1.
60	SIGNALING			Z								U								J3(Z) – J11(U) – C14 10n
61	SSB AUDIO											Y				E				
62	SSB CONT			T										I						J3(T) – R17 1K – J13(I)
63	SSB (DATA)				B													16	42	J17(16) – L18 100µH – J4(B); P3(42) – C13 10n; R13 100K
64	SQUELCH											K						58	62	
65	SUMF		J								M									
66	TUNE			N	U	E							I					2	29	J5(E) – CR11 – J3(N); J12(I) – R6 100K; R57 1K – J4(U); J17(2); P3(29)
67	$\overline{\text{TUNE}}$	H				O														
68	TRANSIT					n												18	19	J5(n) – CR12 – +12V *; R7 10K; L19 100µH – J17(18); P3(19); * CONNECTED TO +12V ON FUNC. NO. 104
69	TX LEVEL			M								N	K					21	28	J17(21); P3(28); J12(K) – CR8; R3 100K; C19 10n – J11(N); J3(M)
70	TX				R										K					
71	FQ, UNLOCK			R		o					W							1	30	J17(1) – R33 4.7K; J5(o) – CR5; J10(W) – CR6; R2 100K; C29 10n – P3(30); J3(R)
72	USB									D								4	40	J9(D) – C30 10n – J17(4); P3(40)
73	VAD PULSE		Y					B												

Fig. 2-81.D. Wiring of motherboard and chassis assembly (Sheet 4 of 8)

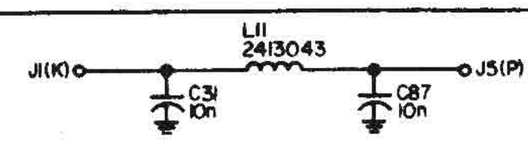
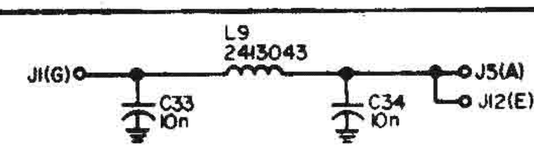
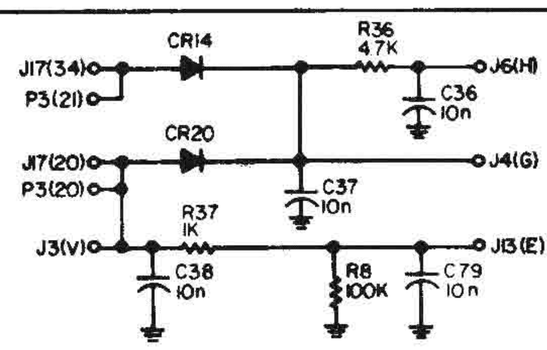
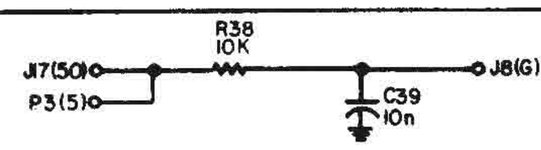
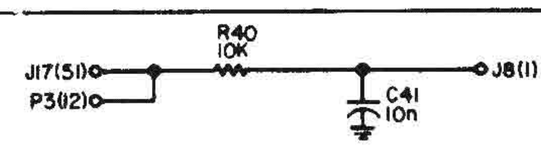
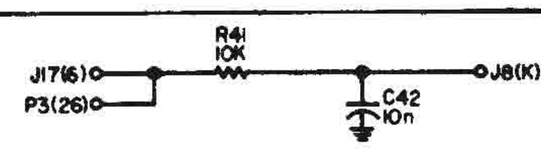
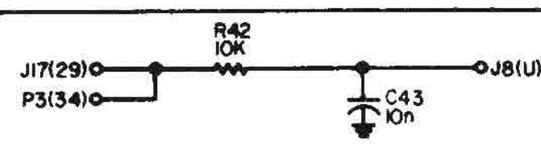
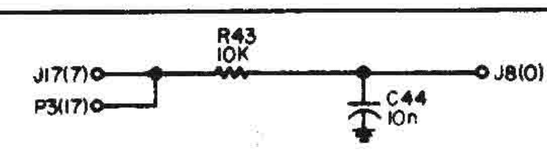
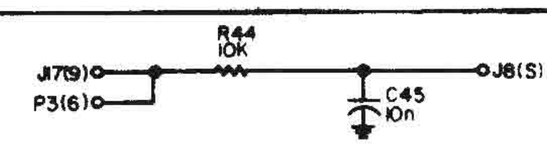
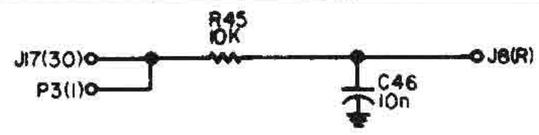
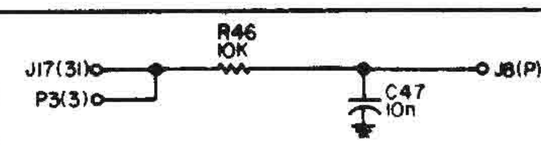
NO	FUNCTION	PS J1	VCP J2	CONT J3	PRE J4	LORD J5	REF J6	VAD J7	LOL J8	USB J9	SUM J10	AUD J11	SNF J12	FIL J13	MIX J14	IF J15	PA J16	PANEL J17	REMOTE P3	NOTES
74	VEN1	K				P														
75	VEN 2	G				A							E							
76	VOLUME											P						10		
77	WCW(CW)				G		H											34	21	
78	NCW			V										E				20	20	
79	X10								G									50	5	
80	X11								E									35	4	
81	X12								I									51	12	
82	X13								K									6	26	
83	X20								U									29	34	
84	X21								O									7	17	
85	X22								S									9	6	
86	X23								R									30	1	
87	X30								P									31	3	

Fig. 2-81.E. Wiring of motherboard and chassis assembly (Sheet 5 of 8)

NO	FUNCTION	PS J1	VCP J2	CONT J3	PRE J4	LORD J5	REF J6	VAD J7	LOL J8	USB J9	SUM J10	AUD J11	SNF J12	FIL J13	MIX J14	IF J15	PA J16	PANEL J17	REMOTE P3	NOTES
88	X31							G										48	11	J17(48) P3(11) J7(G) C48 10n
89	X32							E										47	25	J17(47) P3(25) J7(E) C49 10n
90	X33							C										25	45	J17(25) P3(45) J7(C) C50 10n
91	X40							M										37	58	J17(37) P3(58) J7(M) C51 10n
92	X41							Q										39	35	J17(39) P3(38) J7(Q) C52 10n
93	X42					Y		I										27	18	J17(27) P3(38) R47 2.2K J7(I) J5(Q) C53 10n
94	X43					Z		K										32	7	J17(32) P3(7) R48 2.2K J7(K) J5(Z) C54 10n
95	X50		d			X		U										28	2	J17(28) P3(2) R49 2.2K J7(U) J5(X) J2(d) C55 10n
96	X51		b			J		Y										60	10	J17(60) P3(10) R50 2.2K J7(Y) J5(J) J2(b) C56 10n
97	X52		T			i		S										40	24	J17(40) P3(24) R51 2.2K J7(S) J5(i) J2(T) C57 10n
98	X53		V			Q		O										38	44	J17(38) P3(44) R52 2.2K J7(O) J5(Q) J2(V) C58 10n
99	X60		X			b		W										41	36	J17(41) P3(36) R53 2.2K J7(W) J5(b) J2(X) C59 10n
100	X61(FL6)		Z			d		V					F,Q					61	59	J17(61) P3(59) R55 2.2K J7(V) J5(d) J2(Z) C61 10n R54 22K J12(F,Q) C60 100n
101	+6V	C	O	o				H		H	G				S	Q		45		L5 2413043 J1(C) L20 100µH C62 10n C1 33µ C68 10n J2(O) J3(a) J7(H) J9(H) J10(G) J14(S) J17(45) J15(Q)

Fig. 2-81.F. Wiring of motherboard and chassis assembly (Sheet 6 of 8)

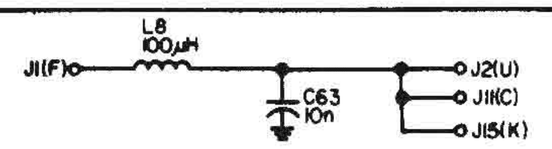
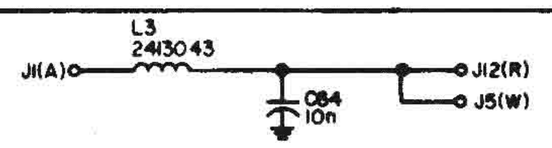
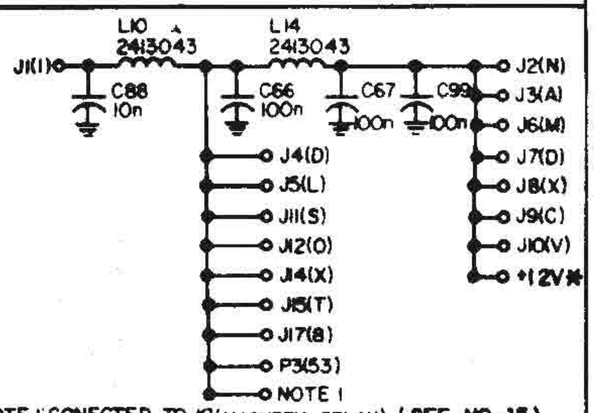
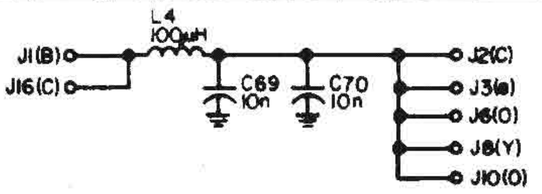
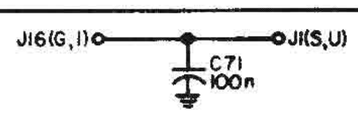
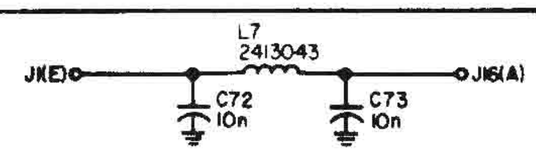
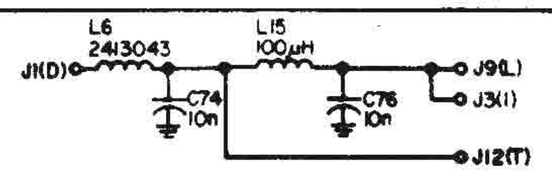
NO	FUNCTION	PS J1	VCP J2	CONT J3	PRE J4	LORD J5	REF J6	VAD J7	LOL J8	USB J9	SUM J10	AUD J11	SNF J12	FIL J13	MIX J14	IF J15	PA J16	PANEL J17	REMOTE P3	NOTES
102	-10V	F	U									C				K				
103	-10V EN	A				W							R							
104	+12V	I	N	A	D	L	M	D	X	C	V	S	O		X	T		B	53	 NOTE 1 CONECTED TO K1(MAGNETIC RELAY) (SEE NO-15). * CONNECTED TO +12V* ON FUNC. NO. 68
105	+15V	B	C	e			O		Y		O						C			
106	+17V		Q							J										
107	+34V	S,U															G,I			
108	+26V UNFILTERED	E															A			
109	+26V FILTERED	D		I						L			T							
110	1041 MHZ									G	I									
111	20 KHZ						F				S									
112	10.5 MHZ						I			E										
113	5KHZ						A		A											
114	+6V SW		D					R												
115	10KHZ				A		D													
116	5.25 MHZ						E									C				
117	GND	T,V,W	B,G H,I K,L P,R f	f,g	O,Q L,M N	k	K,L J	L,N J,P	L,M N	K,F M,D P,Q	H,J L,E N,P R,T Y	H,J, L,M	X,D	B,C D,F G,H J,K L,N Q,P	P,Q F,R U,W H,J L,N	H,J L,N P,R	B,D F,H Q,J L,N	54 55	66 14	
118	SPARE												P				E			

Fig. 2-81.G. Wiring of motherboard and chassis assembly (Sheet 7 of 8)

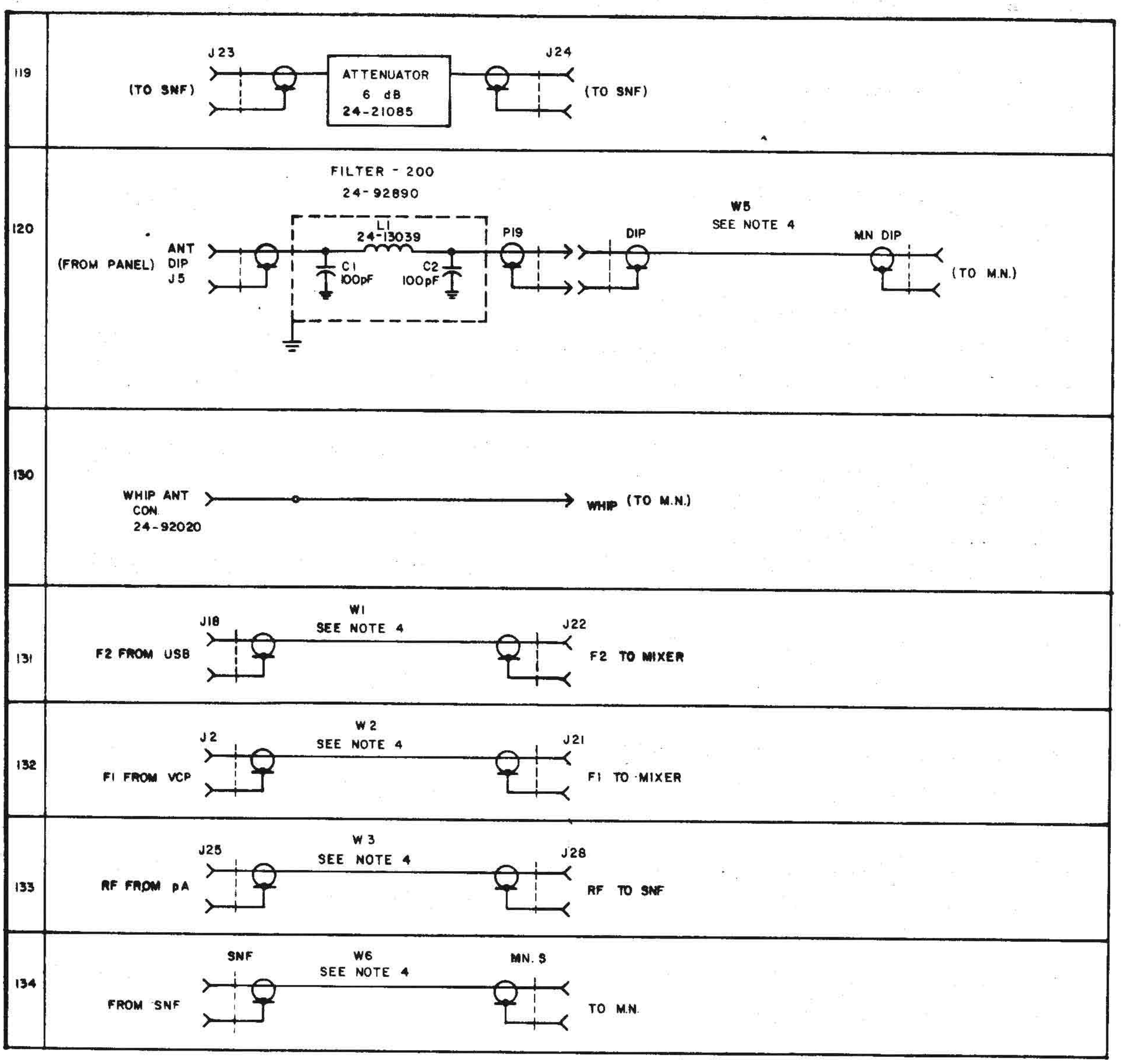


Fig. 2-81.H. Wiring of motherboard and chassis assembly (Sheet 8 of 8)

CHAPTER 3

DIRECT SUPPORT MAINTENANCE

Section I. GENERAL

3-1. Scope

a. The maintenance procedures in this chapter supplement the operator's checks, maintenance, and troubleshooting procedures detailed in publication OM 107-10: "Radio Set PRC-174 Operator's Manual", Chapter 3.

b. Section II presents systematic testing and troubleshooting techniques using the Automatic Test Set, TS-1748.

c. Sections III and IV present testing and troubleshooting procedures carried out using general purpose test equipment.

d. Section V contains instructions for direct-support repairs.

e. Section VI contains instructions for alignment following direct support repair.

3-2. Organization of Troubleshooting Procedures

a. General. The first step in troubleshooting a defective RT-936/-PRC-174 is to sectionalize the fault to a major area such as function switches, circuits, wiring, power supply, etc. The second step is to localize the fault to a defective module, assembly or area. The third step is to locate the defective module or faulty component part.

b. Sectionalization. The following tests are arranged to reduce unnecessary work and to expedite troubleshooting a defective RT-936/PRC-174:

(1) Visual inspection. Visual inspection may locate faults without tests or measurements. Check for front panel fault indications physical damage to the case, front panel controls, and connectors, broken or damaged internal wiring and connections, loose module or component connections.

(2) Operational tests. Operational tests frequently indicate the general location of a trouble. Perform the operational checks specified in OM 107-10, Chapter 3, before commencing troubleshooting procedures.

(3) Intermittent trouble. The possibility of intermittent trouble should not be overloooked. If present this type of trouble may often be made to appear by tapping or jarring the RT-936/PRC-174.
To locate such trouble, check wiring, connections, plugs, and jacks of the various modules.

Section II. TEST AND TROUBLESHOOTING PROCEDURES USING TEST SET TS-1748

3-3. Tools and Test Equipment

Table 3-1 lists the test equipment required for troubleshooting Radio Set PRC-174 using Test Set TS-1748.

3-4. Test Set TS-1748 (fig. 3-1)

a. General. The Automatic Test Set TS-1748 is a portable instrument capable of testing radio set PRC-174 without any additional equipment. The TS-1748 determines whether the radio set under test meets the required operational standards. If the radio set fails to meet the standards, the TS-1748 localizes the problem and indicates which section is defective. The Test Set TS-1748 contains signal and noise generators which produce the required RF and audio signals for stimulation of the radio set. A data acquisition system checks the radio set circuits and measures its significant parameters. A digital command unit, including a microprocessor, memory and logic circuits, controls the sequence of tests and computes the results. This command unit automatically controls all functions of the radio set including the operating mode and frequency. The operator makes no settings whatsoever during the test procedure. An alphanumeric display on the front panel of the automatic test gives a visual read-out of the defective function and frequency.

b. Modes of Operation. The automatic test set has two modes of operation:

(1) Fault detection mode. The TS-1748 automatically measures the parameters at 22 preselected test frequencies. Testing proceeds until the full range of frequencies and parameters have been checked. If during a particular testing sequence, the radio set fails to meet requirements, the test set will halt the testing cycle and display the fault parameter and frequency. If no fault occurs, a "PASS" lamp lights.

(2) Fault isolation mode. The TS-1748 measures the sequence of parameters and, at the end of this sequence, indicates the suspected modules or group of modules.

c. Tested Parameters. The following are amongst the parameters tested by the TS-1748:

(1) RF output power level (at whip and dipole antennas).

(2) Frequency accuracy.

(3) Noise figure (sensitivity).

(4) Audio output level.

(5) Audio distortion.

(6) Power consumption (during receive and transmit modes of operation).

(7) Battery voltage.

(8) Those remote control functions which assist in fault location.

Table 3-1. Test Equipment and Accessories Required for Testing and Troubleshooting with TS-1748.

Item	Equipment	Cat. No.
1	Test Set, Automatic, TS-1748	2409007
2	Simulator, Whip, for TS-1748/RT-936/PRC-174	2409416

Table 3-1. Test Equipment and Accessories Required for Testing and Troubleshooting with TS-1748 (Cont'd.)

Item	Equipment	Cat. No.
3	Handset, H-189/GR	2509029
4	Cable Assembly, Audio, CX-2424	2009050
5	Cable Assembly, Power, Radio Set Cable, CX-1792	2409247
6	Cable Assembly, Power, CX-1788 (Note)	2409246
7	Cable Assembly, RF, CG-409 (two)	2009046
8	Cable Assembly, Control, CX-1787	2409220
9	Battery, Rechargeable, TNC-660, for TS-1748 (NOTE)	2409465

NOTE:
TS-1748 may be powered from rechargeable battery TNC-660, or from an external 28VDC power source, using cable CX-1788. If necessary, it is also possible to connect the rechargeable battery, type TNC-1770 (used with the PRC-174), via cable CX-1748.

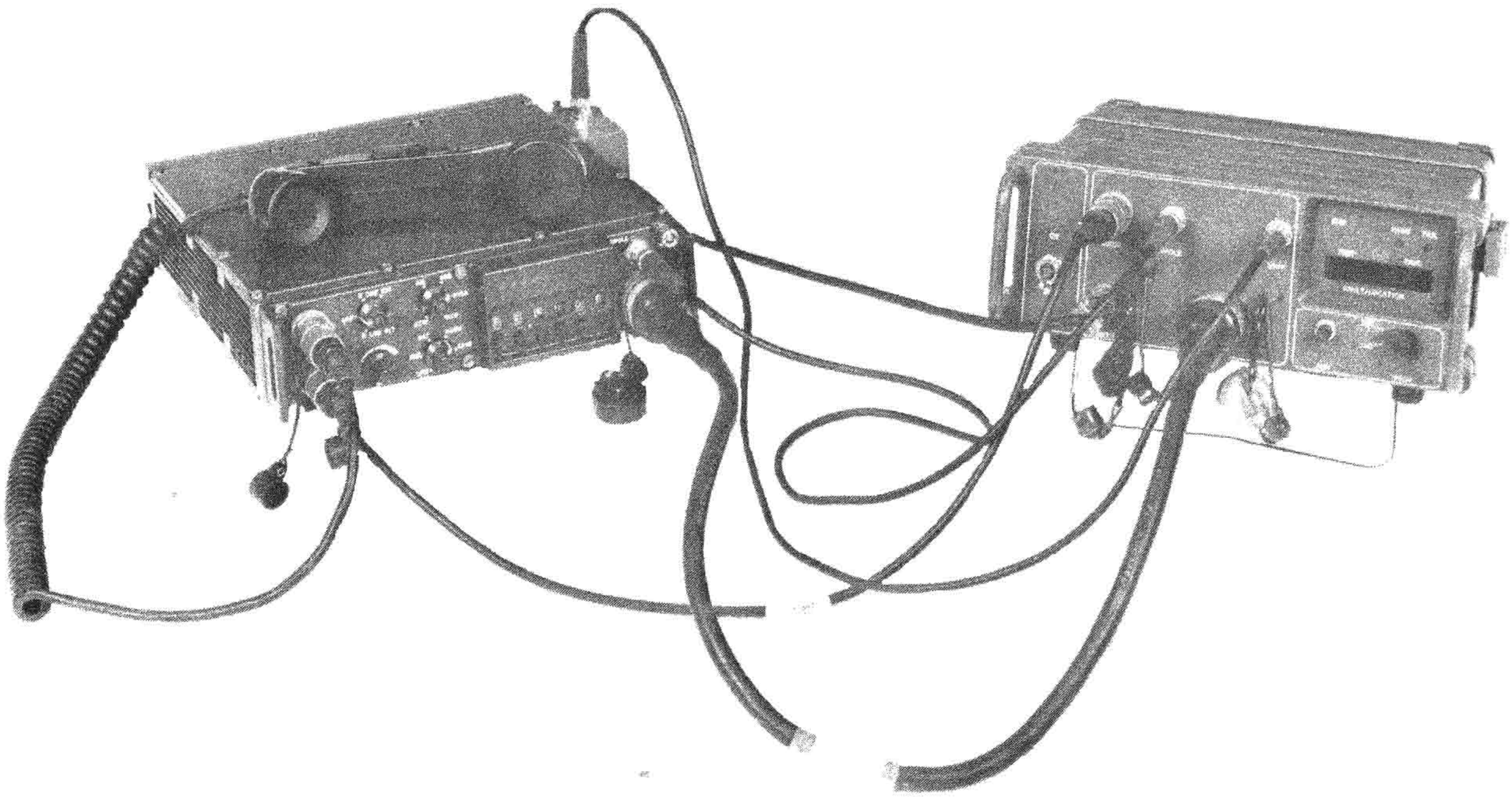


Figure 3-1. Test Set TS-1748 with Radio Set PRC-174

3-5. Test Set TS-1748 - Controls, Indicators and Connectors (fig. 3-2)

Table 3-2 describes the controls, indicators and connectors of the TS-1748 and defines their functions.

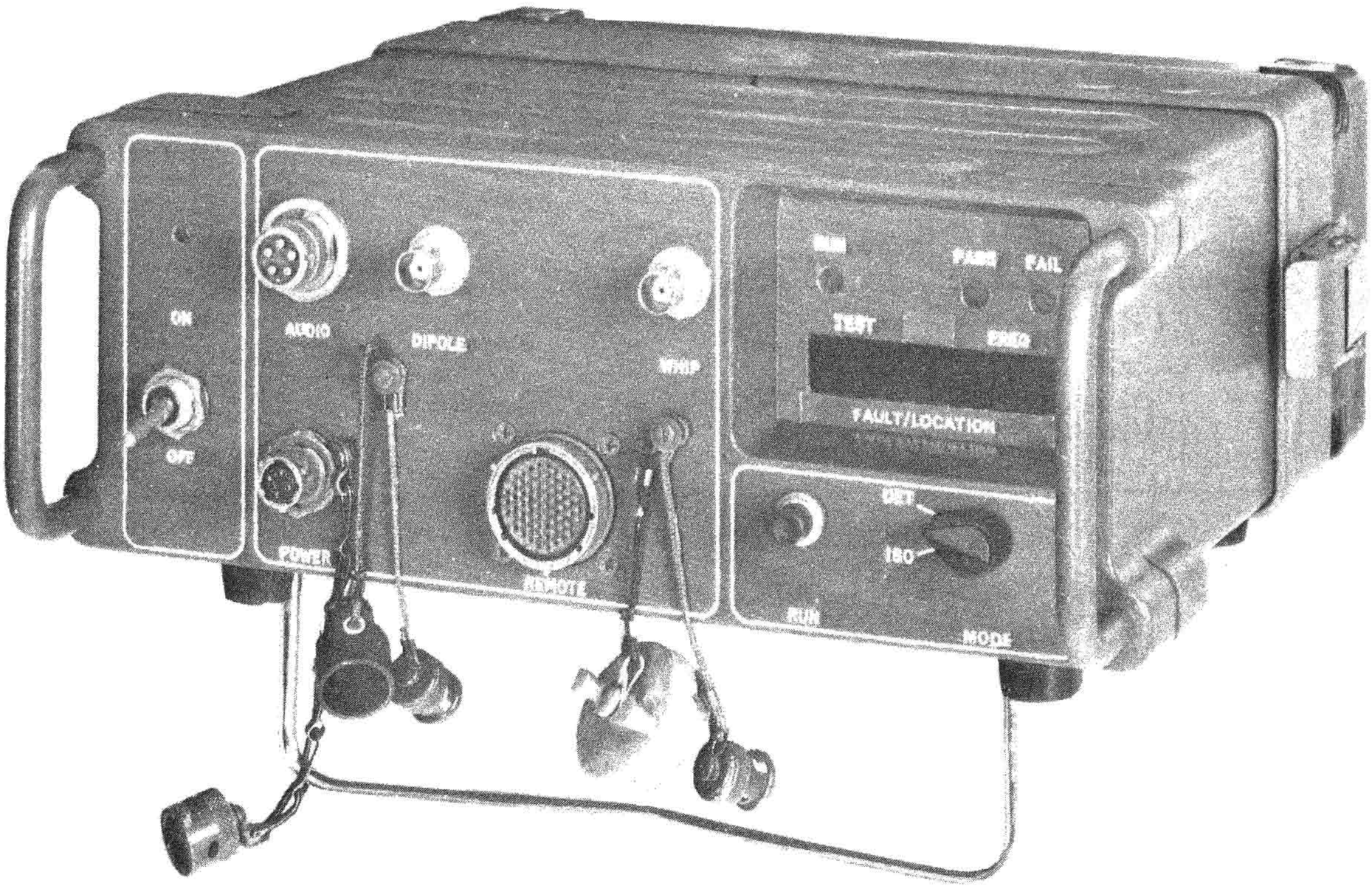


Figure 3-2. Test Set TS-1748 controls, indicators and connectors

Table 3-2. TS-1748, Controls, Indicators and Connectors

No	Control, Indicator or Connector	Function
1	Power ON/OFF Switch	Turns power on or off. Trips on overload.
2	Power Indicator	Lights when power is on.
3	RUN Indicator	Lights when test program is running.
4	PASS Indicator	Lights upon completion of a successful test run.
5	FAIL Indicator	Lights upon detecting a fault during a test run.

Table 3-2. TS-1748, Controls, Indicators and Connectors (Cont'd.)

No	Control, Indicator or Connector	Function
6	Alphanumeric Display	Shows test in progress or failure mode.
7	MODE DET/ISO Switch	Selects fault detection (DET) or fault isolation (ISO) mode.
8	RUN Switch	Starts operation, or restarts it after halting and/or displaying a prompt.
9	DIPOLE Connector	Connection for RF signals to the receiver/transmitter DIPOLE connector.
10	WHIP Connector	Connection for RF signals to the whip simulator.
11	AUDIO Connector	Connection for AF and control signals to the receiver/ transmitter AUDIO connector.
12	REMOTE Connector	Connection for control and status signals to the receiver/transmitter CONTR connector.
13	POWER Connector	Connection for power supply to the receiver/transmitter.
14	Battery Connector (28V) (mounted on rear panel)	Connection for test set battery or external power supply.

3-6. Preparation for Testing (fig. 3-3)

a. Test Set-up (fig. 3-3).

CAUTION

Check that both the TS-1748 and the UUT are switchd OFF before starting assembly.

(1) Attach the whip simulator to the whip connector of the UUT. Tighten the two screws by hand.

(2) Attach the power cable to the UUT. Ensure pin alignment, then tightly screw cable sleeve.

(3) Adjust the TS-1748 viewing angle using the fold-out leg.

(4) Place UUT beside TS-1748 and remove protective caps from all connectors. Store caps in a bag.

(5) Attach the extension sleeve end of the control cable to the UUT CONTR connector.

(6) Connect the free end of the control cable to the TS-1748 REMOTE connector.

(7) Connect the free end of the power cable to the TS-1748 POWER connector.

(8) Connect the RF cable between the simulator and the TS-1748 WHIP connector.

(9) Connect the second RF cable between the DIPOLE connectors of the UUT and TS-1748.

(10)Connect the audio cable between the AUDIO connectors of the UTT and TS-1748.

(11)Connect Handset H-189/GR to the second AUDIO connector of the UUT (optional).

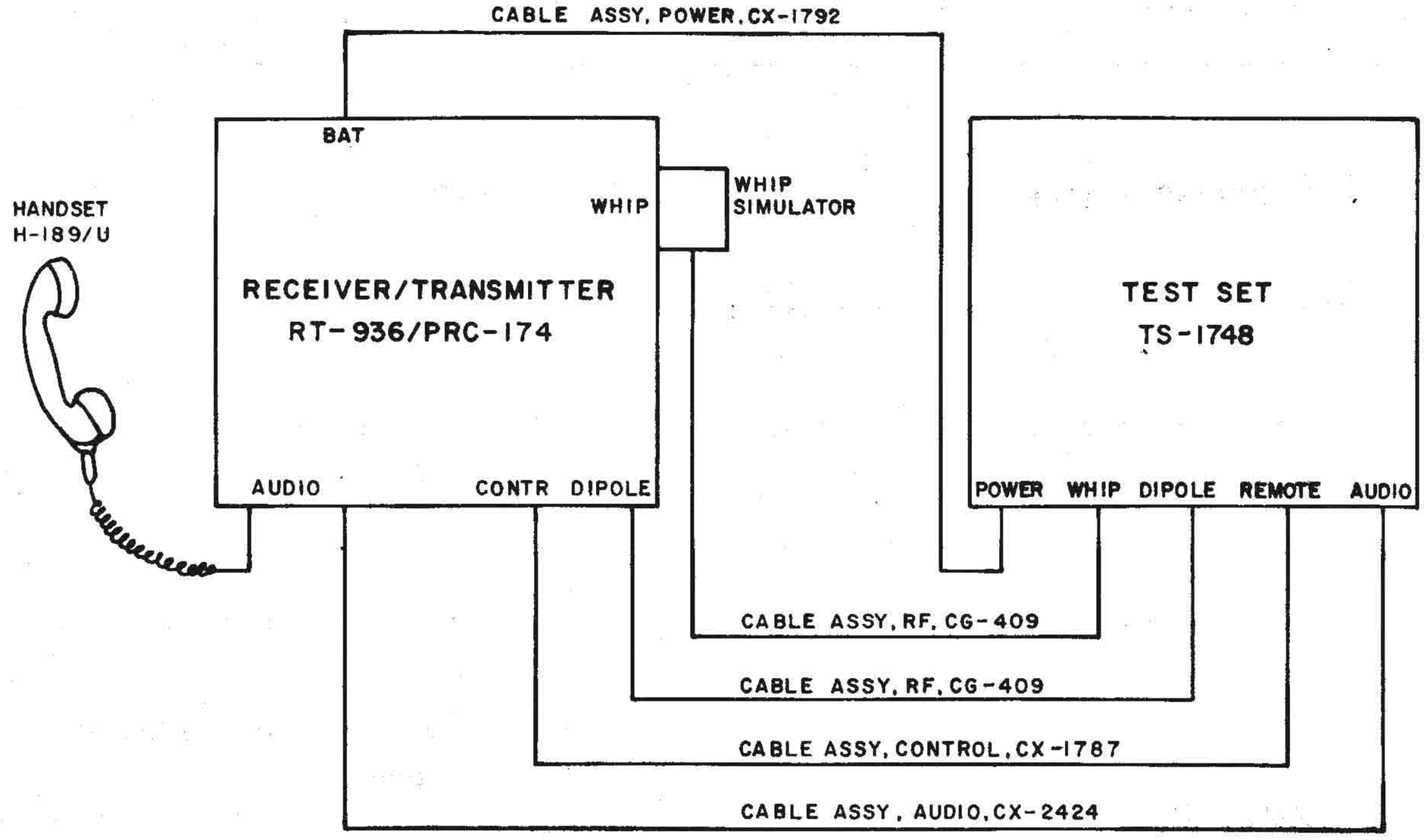


Figure 3-3. Test set-up for RT-936/PRC-174 using TS-1748

b. Power Source Connection. If an appropriate 28VDC source is available, connect cable CX-1788 between the rear connector of the TS-1748 and the power source. Otherwise, install rechargeable battery TNC-660 in the rear battery compartment of the TS-1748. If it is desired to use battery type TNC-1770, connect it to the TS-1748 using cable CX-1748.

3-7. Testing and Troubleshooting Procedure

NOTE

High power RF fields may disrupt the measurement process and lead to unreliable results. Do not operate the test system close to an active radio transmitter or a transmitting antenna.

a. Fault Detection Mode.

(1) Starting sequence.
   (a) Set MODE switch to DET.
   (b) Set POWER switch to ON.
   (c) Wait until display shows "START".

WARNING

Dangerous voltages are present at the antenna connections and at several internal points of the radio set. Do not touch! Observe safety precautions!

NOTE

Do not depress the RUN switch for more than 1.5 seconds at a time, unless specifically instructed otherwise.

(2) Normal test sequence.

(a) If no faults are present the display state sequence appears as shown below:

Step	Display State
1	START
2	END 02
3	END 03
4	END 04
5	END 05
6	END 06
7	END 07
8	END 08
9	END 09
10	END 10
11	END 11
12	END 12
13	END 13
14	END 14
15	END 16
16	END 18
17	END 19
18	END 20
19	END 22
20	END 24
21	END 26
22	END 28
23	END 29
24	END AD
25	PRC OK

(b) Test program halts at step 25.

1. To end testing, set POWER switch to OFF.

2. To repeat test, press RUN switch and wait until display shows "START".

(3) Skipping test frequencies. Testing at any of the standard test frequencies, except 2 MHz, may be skipped if desired.

(a) To enter skip mode, press the RUN switch for at least 2 seconds after prompt "END WW" ("WW" is the last test frequency) disappears.

(b) Release the RUN switch before the next prompt "END XX" ("XX" is the next test frequency) disappears.

(c) The TS-1748 skips through the standard test frequencies without performing the tests until skip mode is exited or the 5-MHz receiver tests are reached. For each frequency "YY", the display shows "END YY" after skipping.

(d) To exit skip mode at any frequency, depress again the RUN switch for at least 2 seconds after prompt "END YY" disappears.

(e) Release the RUN switch before the next prompt "END ZZ" ("ZZ" is the next frequency to be tested) disappears.

(4) Fault detection. When a fault is detected, its presence is displayed at the end of the current test. The test program halts and the FAIL indicator lights.

(a) To continue testing, press RUN switch.

(b) Repeat (a) as required.

(c) At the end of the test sequence, the display shows "FAULT" instead of "PRC OK" (step 25).

NOTE

TS-1748 stores test results for use by the fault isolation program. The test results will be lost if the TS-1748 is switched OFF.

1. To end testing, set the POWER switch to OFF.

2. To repeat the test, press RUN switch and wait until display shows "START".

3. To isolate the detected fault, set the MODE switch to ISO and press RUN switch. For further information, see b. below.

(d) Fault codes are listed in Table 3-3.

Table 3-3. Fault Codes

Fault Code	Fault Description
System fault codes	
FLTBT.....	Test set fault.
FLTTS.....	Test set fault.
SN 04.....	Minor fault in the UUT receiver. The accuracy of subsequent receiver sensitivity measurements will be reduced, but normal testing can proceed.
5-character codes	
FLTOF.....	UUT does not switch off.
NL-01.....	"Unlock" absent when out-of-range frequency is selected.
RECCR.....	Excessive current drain during receive mode.
REMBT.....	Low voltage at BAT IN.
12VAD.....	12V absent in AUDIO connector.
12VRM.....	12V absent in REMOTE connector.
3-character codes (last two characters are "05", to indicate that test frequency is 5.001 MHz)	
ADA.....	Noise level not reduced in presence of AM carrier.
ADD.....	Low phone output power (Dipole, DATA).
ADN.....	Low phone output power (Dipole, NCW).
ADU.....	Low phone output power (Dipole, SSB/USB).
AWU.....	Low phone output power (Whip, SSB/USB).
DAU.....	High audio distortion in receive mode.
FIX.....	Low output power at FIX LEVEL output.
RMH.....	Low output power at remote phone.
SDN.....	Poor SINAD in receive mode (Dipole, NCW).
SDU.....	Poor SINAD in receive mode (Dipole, SSB/USB).
SMT.....	Incorrect S-METER output.
SQL.....	Squelch fault.
SWU.....	Poor SINAD in receive mode (Whip, SSB/USB).
3-character codes (last two characters indicate the MHz digits of a standard test frequency)	
ALC.....	High RF output power with ALC line at high level.
BPH.....	High RF output power during PA bypass.
BPL.....	Low RF output power during PA bypass.
BTD.....	Low supply voltage in transmit mode.
FRD.....	Frequency deviation fault.
MOD.....	Low envelope power in AM transmit mode.
NAU.....	Low receiver background noise level.
NLF.....	"Unlock" when setting frequency.
NMD.....	"No match" on transmit to dipole antenna.

Table 3-3. Fault Codes (Cont'd.)

Fault Code	Fault Description
NMW.....	"No match" on transmit to whip antenna.
NTD.....	TUNE pulse absent on transmit to dipole antenna.
NTF.....	TUNE pulse absent after TRANSIT pulse.
NTW.....	TUNE pulse absent on transmit to whip.
PDA.....	Low RF output power (Dipole, AM).
PDD.....	Low RF output power (Dipole, DATA).
PDL.....	Low RF output power (Dipole, SSB/LSB).
PDN.....	Low RF output power (Dipole, NCW).
PDU.....	Low RF output power (Dipole, SSB/USB).
PDW.....	Low RF output power (Dipole, WCW).
PID.....	Excessive DC input power in transmit mode with dipole antenna.
PIW.....	Excessive DC input power in transmit mode with whip antenna.
PTT.....	Transmission without PTT activation.
PWD.....	Low RF output power at whip output.
RMM.....	Low RF output power with remote microphone.
RMP.....	Low RF output power with remote PTT.
RT.....	Transmit while in the receive state
SNU.....	Poor SINAD in receive mode (Dipole, SSB/USB).
12P.....	PTT 12V absent when PTT line is activated.

b. Fault Isolation Mode.

(1) Starting sequence. The TS--1748 may be set to the fault isolation mode at any time, whether operating or not.

(a) Set MODE switch to ISO.

(b) If TS-1748 is switched off, set power switch to ON and press RUN switch.

(c) If TS-1748 is operating but has halted and shows a prompt, press the RUN switch.

(d) If TS-1748 is operating and running a test, no further action is required.

(e) TS-1748 repeats entire fault detection program unless all test results are stored in its memory from a prior test. Any faults detected are displayed as they occur, but program does not halt.

(f) Program halts with display showing the generic fault description code (see Table 3-4).

(2) Fault display. The generic fault description codes are listed in Table 3-4.

(a) To display the primary suspected module or component, press the RUN switch. Suspected modules are identified by codes; these codes are given in Table 3-5.

(b) To display the next suspected module/component code, if any, press again the RUN switch. Each time another suspected module/component code is displayed. After the last code, display shows "END IS" to indicate that isolation program has ended.

(c) To end test, set PO- WER switch to OFF.

(d) To repeat test, press the RUN switch and wait until the display shows "START".

Table 3-4. General Fault Codes

Code	Fault Description
AUDIO	Receiver audio output
D-PWR	RF power during transmission to dipole
FONL	Unlock - outside operating frequency range
FREQ	Frequency deviation
HI-CR	High DC input power
NLFLT	Unlock - inside frequency range
OFFLT	Cannot switch off
PINS	Remote control line(s)
R-FLT	Transmit in receive mode
RTFLT	Transmit without PTT
TNFLT	TUNE pulse
W-PWR	RF power during transmission to whip

Table 3-5. Identification Codes

Code	Suspected Module/Component	Mfg. No.
ATT-6	6dB Attenuator	2124-91085-00
AUD--	Module AUDIO 1A2A3	2124-91230-00
BAT--	Battery	2124-09461-00
COAX-	Coaxial wiring on motherboard	---
CONT-	Module CONTROL 1A7	2124-91700-00
FIL--	Module FILTER 1A2A5	2124-91250-00
FL200	Filter 200	2124-92890-00
IF--	Module IF 1A2A2	2124-91220-00
LOL--	Module LOL 1A3A4	2124-91340-00
LORD-	Module LORD 1A5A2	2124-91520-00
MIX--	Module MIXER 1A2A1	2124-91210-00
MN---	Module MN	2124-91510-00
PA---	Module PA 1A6	2124-91600-00
PANEL	Panel Assembly 1A1	2124-96370-00
PRE--	Module PRE 1A2A4	2124-91240-00
PS---	Module PS 1A4	2124-91400-00
R-REL	Magnetic Switch 1A8K1	2124-31010-00
REF--	Module REF DIVIDER 1A3A6	2124-91360-00
SIM	Whip Simulator	2124-09416-00
SNF	Module SNF 1A5A3	2124-91530-00
SUM--	Module SUM 1A3A5	2124-91350-00
SYN--	Synthesizer System 1A3	---
USB--	Module USB 1A3A3	2124-91330-00
VAD--	Module VAD 1A3A2	2124-91320-00
VCP--	Module VCP 1A3A1	2124-91630-00
WPC--	WHIP Connector 1A8J20	2124-92020-00

c. Troubleshooting the UUT.

(1) General.

(a) The troubleshooting procedure is carried out by substituting approved modules and components for the suspected module/component indicated by the TS-1748.

(b) Due to the strong interaction among the various modules required to fulfil a given function, TS-1748 provides a list of suspected modules, arranged in the order of decreasing probability. Several modules may have to be replaced before the fault is corrected.

(2) Unsuccessful troubleshooting. In a few exceptional cases, faults may occur in the motherboard and repair can not be carried out by module replacement. In such cases, the radio set shall be sent for higher echelon maintenance.

WARNING

Troubleshooting is performed with the radio set protective covers removed. Dangerous RF voltage are present at the antenna connections and at several internal points. Do not touch while live! Observe safety precautions!

(3) Preparation for troubleshooting.

(a) Remove the radio set protective covers.

(b) Put radio set on a flat, clean surface covered with a soft, isolating material.

(c) Assemble the test set-up as shown in fig. 3-3.

(4) Troubleshooting procedure.

(a) Perform fault isolation (b above). Note the list of suspected modules/components.

(b) Set the TS-1748 power switch to OFF and replace the first suspected module/components with an approved spare part.

(c) Repeat (a). If fault returns, re-install the original module/component, then replace the next listed module/component.

(d) Repeat (c) until fault is corrected.

NOTES

1. When replacing modules PA1A6, PRE 1A2A4, SNF 1A5A3 or MIXER 1A2A1, it may be necessary to adjust the ALC circuits. A suitable load (50-W, 20 dB attenuator, Bird model 8321 or equivalent) and RF voltmeter (HP-410C) are required. Potentiometer RV-3 on module SNF 1A5A3 shall be adjusted to obtain an RF output voltage of 28.5V when transmitting in the WCW mode.

2. When replacing modules MIXER 1A2A1 or IF 1A2A2, AGC adjustment may be needed. RF signal generator (HP-8640B) and multimeter (FLUKE 8000A) are required. Potentiometer RV-3 on module IF 1A2A2 shall be adjusted to obtain a DC voltage of 0.5 volts at pin I of module IF 1A2A2, when a 10 microvolt RF signal (at the nominal channel frequency + 1 KHz) of is applied to the DIPOLE connector.

(4) Ending the troubleshooting. Turn off the test set and disassemble the setup.

Section III. DIRECT SUPPORT TEST PROCEDURES

3-8. Test Equipment and Additional Equipment Required (fig. 3-4)

The following chart lists the equipment required to carry out direct support testing and troubleshooting of RT-936/PRC-174. If the specific equipment models are not available, other test equipment having similar characteristics may be used.

a. Test Equipment.

Test Equipment	Manufacturer	Model
RF Generator	Hewlett Packard	8640B, opt 001
Distortion Analyzer	Hewlett Packard	333A
AF Oscillator	Hewlett Packard	204D
Frequency Counter	Hewlett Packard	5328A opt. 010
T-Connector	Hewlett Packard	11042
Voltmeter, AC (including AC Probe HP 11036)	Hewlett Packard	410C
Oscillator	Tektronix	466
Multimeter	Fluke	8000A
Attenuator, 50W, 30dB	Bird	8321
Attenuator, Variable, 0-120dB	Telonic	8143

b. Additional Equipment Required.

Equipment	Mfg. No./Description
Whip Simulator for PRC-174	08-24-138
Cable, Coaxial, 1.5m	RG-58 with BNC connectors
Cable, Shielded, Audio, 1.5m	Banana jacks at both ends
Cable, Coaxial, 1.5m	RG-58 with BNC male connector and banana jacks
Adaptor, Coaxial, N-male-to-BNC female	-
T-Adapter, BNC Connectors (two required)	-
Junction Box	Fig. 3-4

3-9. Visual Inspection and Mechanical Tests

Inspect each part as directed in the chart below. Repair and/or replace defective components which are within the scope of direct support repairs (see Section).

Table 3-6. Visual Inspection and Mechanical Tests

Sequence	Item to be Inspected	Procedure
1	Protective case	Inspect for damage, loose or missing parts or screws. Remove dust and dirt.
2	Connectors	Check that connectors are securely mounted. Inspect shell and contacts for damage and corrosion. Clean and remove all foreign material.

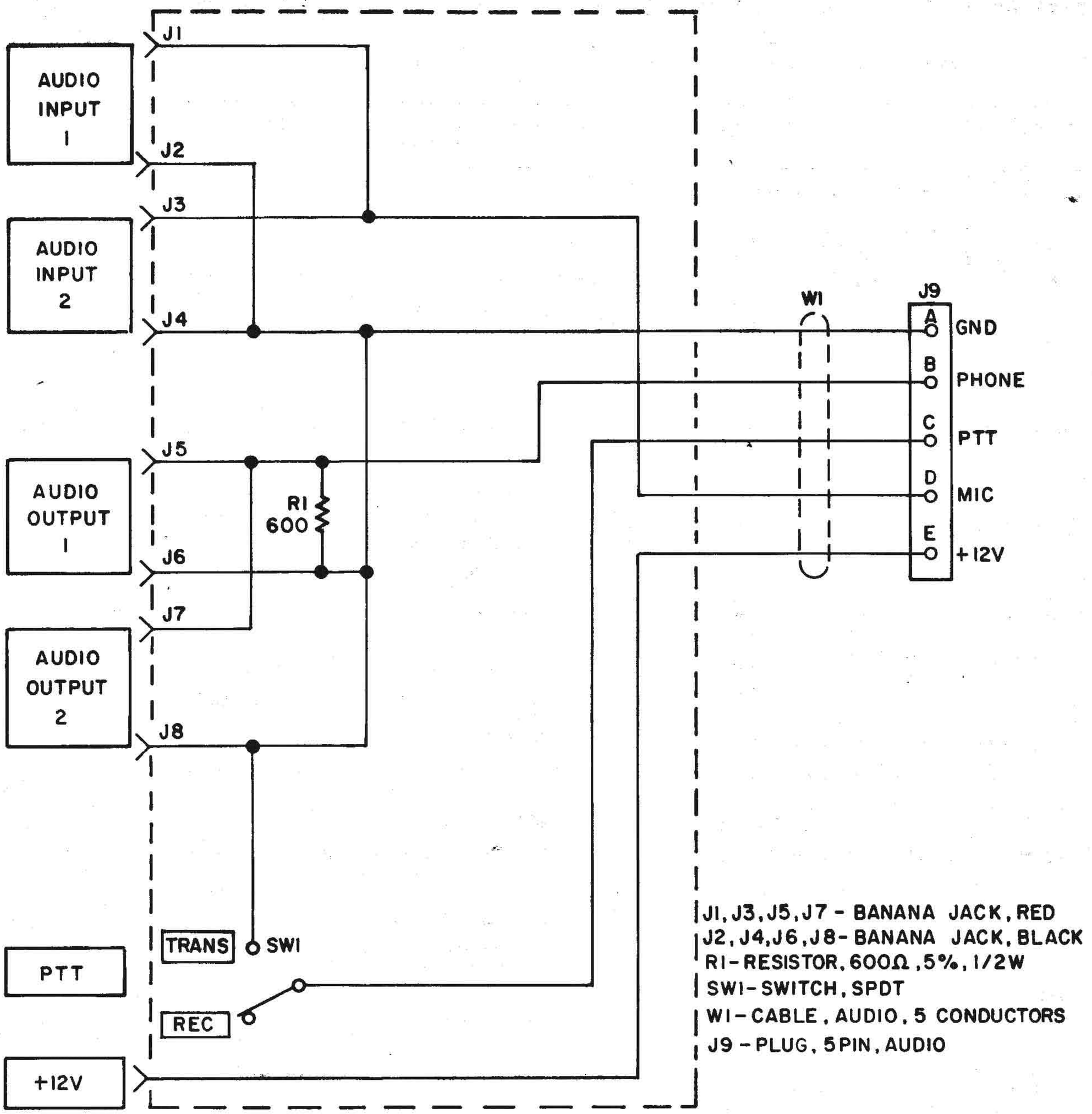


Fig. 3-4. Junction box, for connection to RT-936/PRC-174 AUDIO connectors

Table 3-6. Visual Inspection and Mechanical Tests (cont'd.)

Sequence	Item to be Inspected	Procedure
3	Controls	Check all controls for looseness and damage. Turn controls through each of their positions and check that they operate properly without binding or excessive looseness. Tighten knobs.
4	Display	Inspect for damage and cracks.

Table 3-6. Visual Inspection and Mechanical Tests (cont'd.)

Sequence	Item to be Inspected	Procedure
5	Battery compartment	Check for damage of cover and cover clamps. Check for damage and corrosion of battery compartments.
6	Gaskets	Check for breaks, cuts, or twists. Replace gasket if in doubt.
7	External finish	Check condition of painted metal surfaces and panel lettering. Paint bare metal surfaces. NOTE Touch-up painting is recommended in lieu of refinishing wherever practicable. Screw heads, connectors, and plastic parts should not be painted or polished with abrasives.

3-10. Test Procedure
(fig. 3-5)

It is recommended that the tests described below should be performed in the specified order. Allow 15 minutes warm up prior to performing any test.

NOTE

Insert a fresh battery in the unit under test or use an appropriate external power supply.

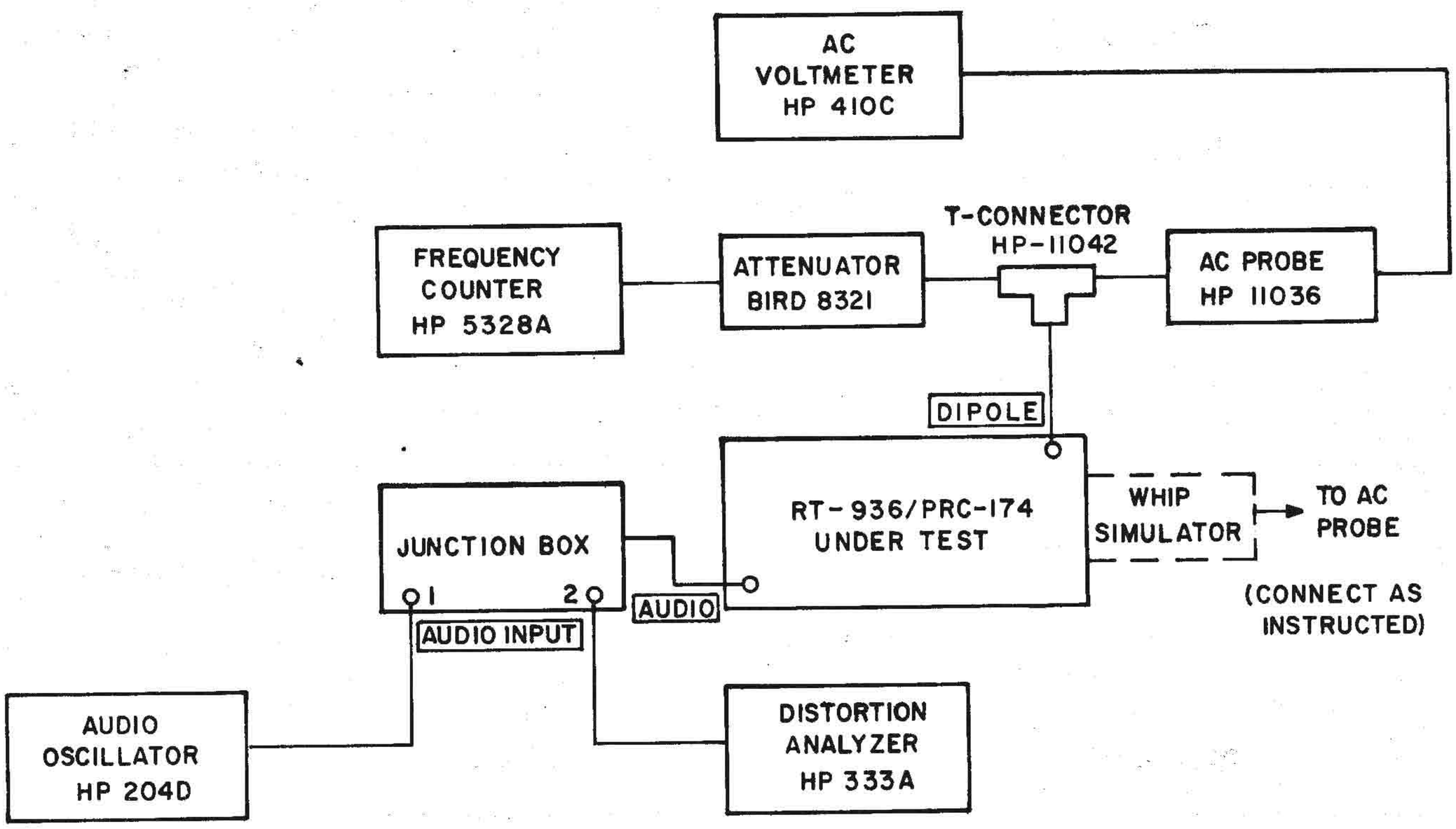


Fig. 3-5. Test setup for transmitter output power and frequency accuracy

Table 3-7. Transmitter Output Power and Frequency Accuracy

Step No.	Test equipment control settings	Equipment-under-test control settings	Test procedure	Performance standard
1	AC Voltmeter HP 410C Operation Switch: ON FUNCTION Selector: 50V AC ZERO Potentiometer: Adjust meter deflection to zero. Frequency Counter HP 5328A Power Switch: ON FUNCTION Selector: FREQ.A FREQ. RESOLUTION: 0.1 Hz SAMPLE RATE: Rotate fully counter-clockwise LEVEL A: PRESET ATTEN: x10 AC-DC Coupling Selector: AC SEP-COM Selector: SEP. Audio Oscillator HP 204D RANGE Selector: X1K. AMPLITUDE, ATTEN: As required. Output Impedance Selector: Set to 600 ohms. Distortion Analyzer HP 333A Operation Switch ON FUNCTION Selector: Voltmeter. RANGE Selector: 1V.	Function Selector: USB R/T Mode Selector: AM. Battery Control: IND Frequency: 2.0000 MHz	a. On the junction box, set PTT switch to TRANS.	a. Solid state display (SSD) indicates output power (three to four lamps illuminate).
		b. Disconnect the audio oscillator HP 204D, then measure transmitter frequency.	b. Within 2 Hz of nominal frequency.
		c. Reconnect the audio oscillator, then adjust its output to 5mV at 1 kHz.	c. None.
		d. Measure the RF output voltage indicated by HP 410C.	d. 28 to 40V.
		e. On the junction box, set PTT switch to REC, then turn mode selector on the unit under test to SSB.	e. None.
		f. On the junction box, set PTT switch to TRANS and measure the RF output voltage as indicated by HP 410C.	f. 28 to 40V.
		g. On the junction box, set PTT switch to REC, then turn function selector on UUT to LSB R/T.	g. None
		h. On the junction box, set PTT switch to TRANS and measure the RF output vol-	h. 28 to 40V.

Table 3-7. Transmitter Output Power and Frequency Accuracy (Cont'd.)

Step No.	Test equipment control settings	Equipment-under-test control settings	Test procedure	Performance standard
	Junction Box PTT Switch: REC.		tage as indicated by HP 410C.	
			i. On the junction box, set PTT switch to REC, then turn function selector on UUT to USB R/T and the mode selector to DATA.	i. None
			j. Adjust HP 204D output to 0.78V at 1 kHz.	j. None.
			k. On the junction box, set PTT switch to TRANS and measure RF output voltage as indicated by HP 410C.	k. 28 to 40V.
			1. Disconnect HP204D.	1. None.
			m. On the junction box, set PTT switch to REC, then turn mode selector on UUT to WCW.	m. None.
			n. On the junction box, set PTT switch to TRANS and measure the RF output voltage as indicated by HP 410C.	n. 28 to 40V.
			o. On the junction box, set PTT switch to REC, then turn mode selector on UUT to NCW.	o. None.
			p. On the junction box, set PTT switch to TRANS and measure the RF output voltage as indicated by HP 410C.	p. 28 to 40V.

Table 3-7. Transmitter Output Power and Frequency Accuracy (Cont'd.)

Step No.	Test equipment control settings	Equipment-under-test control settings	Test procedure	Performance standard
1	Cont'd.		q. On the junction box, set PTT switch to REC, then turn mode selector on UUT to AM.	q. None.
2	Same as step 1 above.	Same as step 1 above.	a. Repeat step 1 above at the following frequencies (MHz): 2.4000 13.2222 3.1111 14.3222 3.9999 16.4400 4.2222 18.5550 5.3333 19.6660 6.4444 20.7000 7.5555 22.8800 8.6666 24.9990 9.7777 26.1000 10.8888 28.2600 11.9999 29.9999 12.1111	a. Same performance standards except the frequency accuracy (para. b) shall be as follows: Freq. (MHZ) / Tolerance (Hz) 2.0000 2.0 2.4000 2.4 3.1111 3.1 3.9999 4.0 4.2222 4.2 5.3333 5.3 6.4444 6.4 7.5555 7.5 8.6666 8.7 9.7777 9.8 10.8888 10.9 11.9999 12.0 12.1111 12.1 13.2222 13.2 14.3222 14.3 16.4400 16.4 18.5550 18.5 19.6660 19.7 20.7000 20.8 22.8800 22.9 24.9990 25.0 26.1000 26.1 28.2600 28.3 29.9999 30.0
3	Same as step 1 above.	Same as step 1 above.	a. Set UUT controls as follows: (1) Function Selector: USB R. (2) Mode Selector: WCW.	a. None.

Table 3-7. Transmitter Output Power and Frequency Accuracy (Cont'd.)

<table>
<tr><th>Step No.</th><th>Test equipment control settings</th><th>Equipment-under-test control settings</th><th>Test procedure</th><th>Performance standard</th></tr>
<tr><td>3</td><td>Cont'd.</td><td></td><td>b. On the junction box, set PTT switch to TRANS and observe HP 410C indication.</td><td>b. No output.</td></tr>
<tr><td></td><td></td><td></td><td>c. Repeat step b with the function selector at LSB R.</td><td>c. No output.</td></tr>
<tr><td>4</td><td>Same as step 1 above.</td><td>Same as step 1 above.</td><td>a. Connect the whip simulator to the UUT, to measure the output power at the whip connector.</td><td>a. None.</td></tr>
<tr><td></td><td></td><td></td><td>b. Connect the test leads of AC Probe HP 11036 to the whip simulator.</td><td>b. None.</td></tr>
<tr><td></td><td></td><td></td><td>c. Set UUT controls as follows:
(1) Function Selector: USB R/T.
(2) Mode Selector: WCW.</td><td>c. None.</td></tr>
<tr><td></td><td></td><td></td><td>d. On the junction box, set the PTT switch to TRANS and observe HP 410C indication.</td><td>d. Min 13.9V.</td></tr>
<tr><td></td><td></td><td></td><td>e. Return the PTT switch to REC.</td><td>e. No output.</td></tr>
<tr><td></td><td></td><td></td><td>f. Repeat steps d,e above at the following frequencies (MHz):
2.4000, 3.5000
8.0000, 11.0000
17.0000, 25.0000
29.9000.</td><td>f. The RF voltage measured by HP 410C shall conform to the following chart:
<table>
<tr><th>Freq (MHz)</th><th>Min RF Output (V)</th></tr>
<tr><td>2.4</td><td>13.9</td></tr>
<tr><td>3.5</td><td>13.9</td></tr>
<tr><td>8.0</td><td>15.6</td></tr>
<tr><td>11.0</td><td>15.6</td></tr>
<tr><td>17.0</td><td>15.6</td></tr>
<tr><td>25.0</td><td>13.9</td></tr>
<tr><td>29.9</td><td>13.9</td></tr>
</table></td></tr>
</table>

Table 3-8. SSB Output Power, Matching and Incorrect Frequency Indications

Use set-up shown in fig. 3-5.

Step No.	Test equipment control settings	Equipment-under-test control settings	Test procedure	Performance standard
1	AC Voltmeter HP 410C Operation Switch: ON FUNCTION Selector: 50V AC ZERO Potentiometer: Adjust meter deflection to zero. Audio Oscillator HP 204D RANGE Selector: X1K. AMPLITUDE, ATTEN: As required. Output Impedance Selector: Set to 600 ohms. Distortion Analyzer HP 333A Operation Switch: ON FUNCTION Selector: Voltmeter. RANGE Selector: 1V. Junction Box PTT Switch: REC.	Function Selector: USB R/T Mode Selector: DATA Battery Control: IND Frequency: 16.0000 MHz	a. Adjust HP 204D frequency to 1 kHz and reduce its output to minimum. b. On the junction box, set the PTT switch to TRANS. c. Slowly increase the audio input to the UUT and observe the RF voltage (as indicated by HP410C) at which each lamp turns on. NOTE: Do not apply more than 2V at the AUDIO input. d. Return the PTT switch to REC and reduce audio input to zero.	a. None. b. None. c. The turn-on voltages shall conform to the following chart: Lamp No. / Turn-on RF Voltage (V) 1 (leftmost) / 4.35-6.9 2 / 6.15-9.75 3 / 7.9 -15.4 4 / 13.7-21.8 5 / 19.5-30.8 d. None.
2	Same as 1 above	Same as 1 above	a. Adjust the HP-204D to 5mV at 1 1 kHz. b. Connect the distortion analyzer to to the receiver AUDIO OUTPUT (instead of MIC IN).	a. None. b. None.

Table 3-8. SSB Output Power, Matching and Incorrect Frequency Indications (Cont'd.)

Step No.	Test equipment control settings	Equipment-under-test control settings	Test procedure	Performance standard
2	Cont'd.		c. Set the PTT switch to transmit and note the voltage indicated by the distortion analyzer.	c. 0.2 to 0.65V.
			d. Rotate the VOLUME control from end to end and observe distortion analyzer reading.	d. No change as the control is rotated.
			e. Set the PTT switch to receive.	e. None
3	Same as 1 above	Same as 1 above and : VOLUME : Midrange	a. Connect the whip simulator to the UUT.	a. None
			b. Set PTT switch to transmit.	While matching is carried out, lamps light sequentially from left to right and beeps are heard in the headphone. After a few seconds, indications stop as matching is achieved.
			c. Set PTT switch to receive.	c. None
			d. Disconnect the whip simulator, leaving both antenna connections open-circuited.	d. None

Table 3-8. SSB Output Power, Matching and Incorrect Frequency Indications (Cont'd)

Step No.	Test equipment control settings	Equipment-under-test control settings	Test procedure	Performance standard
3	Cont'd.		e. Set PTT switch to transmit.	e. Matching indications appear for 15±5 seconds, then are replaced by the "no-match" indications: the lamps flash together 6±2 times per second and beeps are heard in the headphone.
			f. Return the PTT switch to receive.	f. Indications stop.
			g. Connect the whip simulator.	g. None.
			h. Change the frequency to 0.0000MHz.	h. Lamps flash together and beeps are heard in the headphone.
			i. Change the frequency to several other frequencies under 2.0000MHz.	i. Same indications.
			j. Set the frequency to 2.0000MHz.	j. Indications stop.

Table 3-9. Receiver Sensitivity and Audio Output

Use set-up shown in fig. 3-6

Step No.	Test equipment control settings	Equipment-under-test control settings	Test procedure	Performance standard
1	RF Generator HP 8640B LINE: ON RF: ON OUTPUT LEVEL: -100 dBm AM: OFF MODULATION	Function Selector: USB-R. Mode Selector: SSB. Battery Control: NORM Frequency: 2.0000 MHz	a. Adjust RF generator to 2.001000 MHz (= test frequency +1000 Hz), using x10 EXPAND function; then lock the output signal to the in-	a. None.

Table 3-9. Receiver Sensitivity and Audio Output (Cont'd.)

Step No.	Test equipment control settings	Equipment-under-test control settings	Test procedure	Performance standard
1	Cont'd. FREQUENCY: FIXED FREQUENCY 1 KHz FM: OFF TIME BASE VERNIER: CAL (fully clock-wise). COUNTER MODE: Press INT, re-lease all other pushbuttons. RANGE: 2-4 MHz		ternal time base by pressing LOCK pushbutton. b. Adjust HP 8640B output level to -110 dBm (0.7uV). c. Adjust the volume control, until an audio output of 2.45V is indicated by the distortion analyzer.	 b. None. c. None.

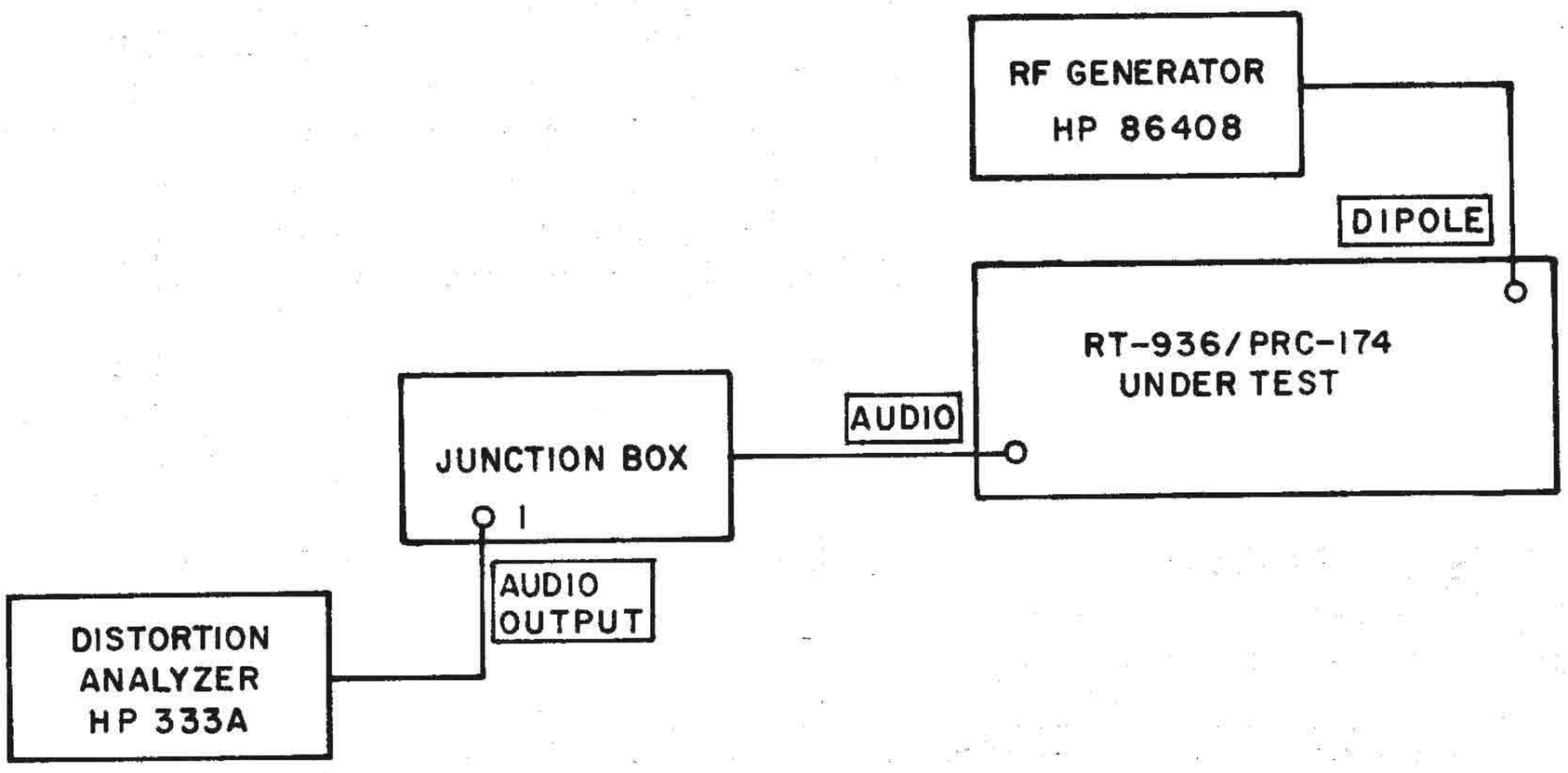


Fig. 3-6. Receiver sensitivity and audio output level, test set-up

Table 3-9. Receiver Sensitivity and Audio Output (Cont'd.)

Step No.	Test equipment control settings	Equipment-under-test control settings	Test procedure	Performance standard
1	Cont'd. Distortion Analyzer HP 333A Operation Switch: ON FUNCTION Selector: Voltmeter. FREQUENCY RANGE: x100 FREQUENCY Dial: 10.0. HIGH PASS FILTER: OUT. MODE: MANUAL.		d. Adjust HP 333A controls as follows: (1) FUNCTION: SET LEVEL. (2) METER RANGE: 0.3V. (3) SENSITIVITY: Adjust to obtain a meter indication of 0dB. e. Turn FUNCTION selector on HP 333A to DISTORTION, then adjust FREQUENCY and BALANCE control to obtain a minimum indication on the meter and record it.	d. None e. Noise + distortion less than -10dB.
2	Same as step 1 above.	Same as step 1 above.	a. Repeat step 1 above at the following frequencies (MHz): 2.4000 13.2222 3.1111 14.3222 3.9999 16.4400 4.2222 18.5550 5.3333 19.6660 6.4444 20.7000 7.5555 22.8800 8.6666 24.9990 9.7777 26.1000 10.8888 28.2600 11.9999 29.9999 12.1111	a. Same performance standards.

Table 3-10. AGC Operation Test (fig. 3-6)

Step No.	Test equipment control settings	Equipment-under-test control settings	Test procedure	Performance standard
1	RF Generator HP 8640B LINE: ON RF: ON OUTPUT LEVEL: -100 dBm AM: OFF MODULATION FREQUENCY: FIXED FREQUENCY 1 KHz FM: OFF TIME BASE VERNIER: CAL (fully clock-wise). COUNTER MODE: Press INT, release all other pushbuttons. RANGE:16-32 MHz FREQUENCY TUNE Controls: Adjust to 16.0010 MHz. Distortion Analyzer HP 333A Operation Switch: ON FUNCTION Selector: Voltmeter. METER RANGE: 3V. FREQUENCY RANGE: x100 FREQUENCY Dial: 10.0. HIGH PASS FILTER: OUT. MODE: MANUAL.	Function Selector: USB-R. Mode Selector: SSB. Battery Control: NORM Frequency:16.0000 MHz	a. Adjust output level of HP 8640B to -110dBm (0.7uV). b. Adjust the volume control, until an audio output of 2.45V is indicated by the distortion analyzer. c. Increase HP 8640B output level to -97 dBm (10uV) and observe the change in the audio level indicated by HP 333A. d. Increase HP 8640B output level to +7 dBm (0.5V) and observe the audio output.	a. None. b. None. c. Audio output shall change by less than 6dB, relative to that set in step b. above. d. Audio output shall change by less than +6dB, relative to that set in step b. above.

Table 3-11. Distortion and Audio Output Level (fig. 3-6)

Step No.	Test equipment control settings	Equipment-under-test control settings	Test procedure	Performance standard
1	RF Generator HP 8640B LINE: ON RF: ON OUTPUT LEVEL: -100 dBm AM: OFF MODULATION FREQUENCY: FIXED FREQUENCY 1 KHz FM: OFF TIME BASE VERNIER: CAL (fully clock-wise). COUNTER MODE: Press INT, re-lease all other pushbuttons. RANGE:16-32 MHz FREQUENCY TUNE Controls: Adjust to 16.0010 MHz. Distortion Analyzer HP 333A Operation Switch: ON FUNCTION Selector: Voltmeter. METER RANGE: 3V. FREQUENCY RANGE: x100 FREQUENCY Dial: 10.0. HIGH PASS FILTER: OUT. MODE: MANUAL.	Function Selector: USB-R. Mode Selector: SSB. Battery Control: NORM Frequency:16.0000 MHz	a. Adjust output level of HP 8640B to -110dBm (0.7uV). b. Rotate the volume control fully clock-wise and record the output level in-dicated by HP 333A. c. Rotate the volume control fully coun-ter clockwise and observe the output level. d. Increase HP 8640B output level to -7 dBm (100mV). e. Adjust the volume control, to obtain an indication of 2.45V on HP 333A. f. Measure the dis-tortion at the audio output.	a. None. b. At least 2.45V. c. Less than 77mV. d. None. e. None. f. Less than 5%.
2	Same as 1 above	Same as 1 above.	a. Adjust the HP 8640B for -110 dBm (0.7uV) at 16.00035 MHz.	a. None.

Table 3-11. Distortion and Audio Output Level (Cont'd.)

Step No.	Test equipment control settings	Equipment-under-test control settings	Test procedure	Performance standard
2	Cont'd.		b. Rotate the volume control fully clockwise and record the output level indicated by HP 333A.	b. At least 2.45V.
			c. Adjust the HP 8640B for -110 dBm (0.7uV) at 16.00033 MHz.	c. None.
			d. Rotate the volume control fully clockwise and record the output level indicated by HP 333A.	d. At least 2.45V.
3	Same as 1 above.	Same as 1 above.	a. Adjust HP 8640B frequency to 16.0000 MHz, then set AM switch to ON and obtain an output of -96 dBm (3.5uV), modulated 30% by 1 kHz.	a. None.
			b. Turn mode selector on the UUT to AM.	b. None.
			c. Repeat steps 1.b through 1.f above.	c. Same performance standards as in 1.b,c,d,e, and f above.

Table 3-12. Receiver Signal Indication (fig. 3-6)

<table>
<tr><th>Step No.</th><th>Test equipment control settings</th><th>Equipment-under-test control settings</th><th>Test procedure</th><th>Performance standard</th></tr>
<tr><td>1</td><td><u>RF Generator HP 8640B</u>
LINE: ON
RF: ON
OUTPUT LEVEL: -100 dBm
AM: OFF
MODULATION FREQUENCY: FIXED FREQUENCY 1 KHz
FM: OFF
TIME BASE VERNIER: CAL (fully clockwise).
COUNTER MODE: Press INT, release all other pushbuttons.
RANGE:16-32 MHz
FREQUENCY TUNE Controls: Adjust to 16.0010 MHz.

<u>Distortion Analyzer HP 333A</u>
Operation Switch: ON
FUNCTION Selector: Voltmeter.
METER RANGE: 3V.
FREQUENCY RANGE: x100
FREQUENCY Dial: 10.0.
HIGH PASS FILTER: OUT.
MODE: MANUAL.</td><td>Function Selector: USB-R.
Mode Selector: SSB.
Battery Control: IND
Frequency:16.0000 MHz</td><td>a. Reduce HP 8640B output level to -107 dBm (1 uV), then slowly increase the level and record the power at which each indicator lamp turns on.

NOTE: Do not increase the input power to more than -47dBm (1mV).</td><td>a. Turn-on thresholds shall conform with the following chart:
<table><tr><th>Lamp No.</th><th>Turn-on Input Level(uV)</th></tr><tr><td>1 (left-most)</td><td>3 to 10</td></tr><tr><td>2</td><td>10 to 30</td></tr><tr><td>3</td><td>30 to 100</td></tr><tr><td>4</td><td>100 to 300</td></tr><tr><td>5</td><td>300 to 1000</td></tr></table></td></tr>
</table>

Table 3-13. Squelch Test (fig. 3-6)

Step No.	Test equipment control settings	Equipment-under-test control settings	Test procedure	Performance standard
1	RF Generator HP 8640B LINE: ON RF: ON OUTPUT LEVEL: -100 dBm (0.7uV) AM: OFF FM: OFF TIME BASE VERNIER: CAL (fully clock-wise). COUNTER MODE: Press INT, re-lease all other pushbuttons. RANGE:16-32 MHz FREQUENCY TUNE Controls: Adjust to 16.0005 MHz. Distortion Analyzer HP 333A Operation Switch: ON FUNCTION Selector: Voltmeter. METER RANGE: 3V. HIGH PASS FILTER: OUT Audio Oscillator HP 204D RANGE Selector: X5. ATTENUATOR: +10 AMPLITUDE Rotate fully counter-clockwise. Output Impedance Selector: 600 ohms. Junction Box PTT Switch: REC.	Function Selector: USB-R. Mode Selector: SSB. Battery Control: NORM Frequency:16.0000 MHz	a. Adjust the volume control for an audio output of 2.45V (+10 dBm) as indicated by the distortion analyzer. b. Adjust oscillo-scope controls for a stable display (500 Hz). c. Adjust HP 204D to +3 dBm (1.1 V) at a frequency of 5 Hz. d. Set HP 8640B AM control to DC and the MODULATION con-trol for a modu-lation index of 55%. e. Rapidly rotate the AM control of the HP 8640B until modulation is re-duced to 8%, and measure the time required for squelch activation.	a. None. b. None. c. None. d. None. e. 2 to 4 seconds.

Table 3-14. Battery Voltage Indication

Step No.	Test equipment control settings	Equipment-under-test control settings	Test procedure	Performance standard
1	Power Supply Adjust to 26 V	Function Selector: USB-R Mode Selector: SSB Frequency: 16.0000MHz Battery Control: BAT	a. Slowly reduce the supply voltage until all lamps start flashing together approx. once per second, and beeps are heard in the headphone.	a. Supply Voltage Range: 20.0 ÷ 21.0 V
			b. Slowly increase the supply voltage until alarm stops. CAUTION Do not exceed 32V	b. All lamps extinguish.
			c. Slowly increase the supply voltage up to 32 V and note the voltage at which each lamp turns on.	No. of Lighted Lamps / Supply Voltage Range 0 — 20.5-22.5V 1 — 21.5-23.5V 2 — 22.5-24.5V 3 — 23.5-25.5V 4 — 24.5-26.5V 5 — 26.5V and higher
			d. Reduce supply voltage to 26 V.	d. None

a. Operational Test. This test is carried out by communicating with an approved PRC-174 radio set.

(1) Turn on the UUT, connect its whip antenna, and tune to 2.0000 MHz.

(2) Turn the battery control to LITE, and check that the frequency selector is illuminated.

(3) Turn battery control to BAT and observe the solid state display (SSD); three or more indicator lamps should light.

NOTE

A smaller number of lamps may indicate that the battery is discharged.

(4) On the frequency selector, set frequencies between 0.2 MHz to 1.9 MHz. The "incorrect frequency" alarm should appear: fast beeps (approx. 6/sec) and concomitant flashing of the SSD.

(5) Adjust the controls on the UUT and on the approved unit as follows:

(a) Function selector: USB R/T.
(b) Mode selector: SSB.
(c) Frequency: 2.0000 MHz.
(d) Battery control: IND.

(6) Listen to the UUT handset while the approved unit transmits. Adjust the UUT volume control and check

for clear reception. Observe the SSD - several lamps will light, in proportion to the received signal amplitude.

(7) Press the PTT switch on the UUT handset and check whether the tuning indication appears (slow beeping and "running" lamps on the SSD). The indication should stop after several seconds. If the "no match" indication appears, press again and wait for the transmitter to tune.

(8) Press the PTT switch and talk to the approved radio set. Check existence of sidetone and make sure the sidetone level is not influenced by the setting of the volume control. The SSD should indicate the emitted power.

(9) Turn function selector to USB-R and make sure transmission is impossible.

(10) Return the function selector to USB-R/T.

(11) Set the UUT battery control to SAVE: the receiver noise should stop.

(12) On the approved radio set, set the mode selector to WCW and press the PTT. Check that the UUT remains in squelch.

(13) Return the mode selector of the approved set to SSB and talk into the handset: the UUT should unsquelch and the speech should be clearly heard.

(14) Return the battery control to IND.

(15) Repeat the communication test at LSB-R/T and AM.

(16) Check WCW and NCW operation: when the radio set is keyed, a 1-kHz tone shall be heard.

(17) Repeat above tests at the following frequencies:

2.4000	8.6666	16.4400
3.1111	9.7777	18.5500
3.9999	10.8888	19.6660
4.2222	11.9999	20.7000
5.3333	12.1111	22.8800
6.4444	13.2222	24.9990
7.5555	14.3000	26.1000
		29.9999

(18) After the test is completed, turn off the radio sets.

Section IV. TROUBLESHOOTING THE RT-936/PRC-174

3-11. General

a. The troubleshooting procedures presented below enable a direct support repairman to correct malfunctions and troubles found during the tests of Section III.

b. The tests of Section III are arranged in a manner which allows fast and efficient determination of the UUT operational status and provides unambiguous data for troubleshooting. It is therefore recommended:

(1) To perform the tests in the given order.

(2) To troubleshoot in the same order: e.g. if the UUT fails both the frequency accuracy and receiver sensitivity tests, correct the frequency accuracy problem first; this may also solve the sensitivity problem.

c. Troubleshooting is performed by systematically substituting approved modules for those suspected. If several modules were replaced before locating the defective module, it is recommended that the former modules be reinstalled in the radio set. However, after each replacement, check that the trouble does not reappear. The UUB should be in the OFF position when replacing modules.

d. See Section I for further troubleshooting hints.

3-12. Troubleshooting Chart

a. Instructions for Use.

(1) Arrange the troubles in the order of pertinence to Section III tests and proceed in that order.

(2) Identify the closest fitting description of the observed symptoms appearing in the troubleshooting chart and follow the related troubleshooting procedure.

NOTES

1. When replacing modules PA1A6, PRE 1A2A4, SNF 1A5A3 or MIXER 1A2A1, it may be necessary to adjust the ALC circuits. A suitable load (50-W, 20-dB attenuator, Bird model 8321 or equivalent) and RF voltmeter (HP-410C) are required. Potentiometer RV-3 on module SNF 1A5A3 shall be adjusted to obtain an RF output voltage of 28.5V when transmitting in the WCW mode.

2. When replacing modules MIXER 1A2A1 or IF 1A2A2, AGC adjustment may be needed. RF signal generator (HP-8640B) and multimeter (FLUKE 8000A) are required. Potentiometer RV-3 on module IF 1A2A2 shall be adjusted to obtain a DC voltage of 0.5 volts at pin I of module IF 1A2A2, when a 10 microvolt RF signal (at the nominal channel frequency + 1 KHz) of is applied to the DIPOLE connector.

Table 3-15. Troubleshooting Chart

Step No.	Trouble Symptoms	Corrective Measures
1	Equipment does not operate when turned on.	Replace the listed modules until the trouble is corrected: (1) PS 1A4. (2) Panel 1A1.
2	"Low battery" alarm.	a. Replace the battery with a fresh one. b. If the alarm reappears, replace the modules listed below until the trouble is corrected: (1) PS 1A4 (2) CONT 1A7 (3) Panel 1A1
3	"No match" alarm	Replace the listed modules, until the trouble is corrected: (1) LORD 1A5A2 (2) MN 1A5A1 (3) SNF 1A5A3 (4) CONT 1A7
4	"No lock" indication	Replace the listed modules until the trouble is corrected: (1) VCP 1A3A1 (2) SUM 1A3A5 (3) PS 1A4 (4) USB 1A3A3 (5) VAD 1A3A2 (6) REF 1A3A6 (7) LORD 1A5A2 (8) Panel 1A1.
5	Low output power only at the dipole or only at the whip connector	Replace the listed modules, until the trouble is corrected: (1) MN 1A5A1 (2) SNF 1A5A3 (3) LORD 1A5A2.

Table 3-15. Troubleshooting Chart (Cont'd.)

Step No.	Trouble Symptoms	Corrective Measures
6	Low output power at some frequencies	Replace the listed modules, until the trouble is corrected: (1) PA 1A6 (2) MN 1A5A1 (3) SNF 1A5A3 (4) LORD 1A5A2 (5) PRE 1A2A4 (6) MIX 1A2A1
7	Low output power in SSB or NCW or AM mode	Replace the listed modules, until the trouble is corrected: (1) FILTER 1A2A5 (2) Panel 1A1.
8	Low output power in DATA or WCW/ NCW mode	Replace the listed modules, until the trouble is corrected: (1) PRE 1A2A4 (2) For WCW/NCW only - REF 1A3A6 (3) Panel 1A1.
9	Low output at all frequencies	Replace the listed modules until the trouble is corrected: (1) PA 1A6 (2) PS 1A4 (3) REF 1A3A6 (4) PRE 1A2A4 (5) MIX 1A2A1 (6) IF 1A2A2 (7) SNF 1A5A3 (8) LORD 1A5A2 (9) FILTER 1A2A5
10	Frequency tolerance exceeded at all frequencies	Replace module REF 1A3A6.
11	Frequency error - for 0.1/1/10 KHz steps only.	Replace the listed modules until the trouble is corrected: (1) LOL 1A3A4 (2) SUM 1A3A5 (3) REF 1A3A6 (4) Panel 1A1
12	Frequency does not respond to 20 KHz steps	Replace the listed modules until the trouble is corrected: (1) VAD 1A3A2 (2) Panel 1A1.

Table 3-15. Troubleshooting Chart (Cont'd.)

Step No.	Trouble Symptoms	Corrective Measures
13	Frequency error - for some digits	Replace the listed modules until the trouble is corrected: (1) VAD 1A3A2 (2) Panel 1A1.
14	Unstable frequency reading	Replace the listed modules until the trouble is corrected: (1) VCP 1A3A1 (2) PS 1A4 (3) SUM 1A3A5 (4) VAD 1A3A2 (5) LOL 1A3A4
15	Incorrect frequency - at all frequencies	Replace the listed modules until the trouble is corrected: (1) VCP 1A3A1 (2) REF 1A3A6 (3) SUM 1A3A5 (4) VAD 1A3A2 (5) USB 1A3A3 (6) Panel 1A1
16	Incorrect output power indication	Replace the listed modules until the trouble is corrected: (1) CONT 1A7 (2) SNF 1A5A3 (3) Panel 1A1.
17	Sidetone level too low (output power within tolerance)	Replace the listed modules until the trouble is corrected: (1) AUDIO 1A2A3 (2) PRE 1A2A4 (3) SNF 1A5A3.
18	Failure in AM communication test	Replace the listed modules until the trouble is corrected: (1) IF 1A2A2 (2) REF 1A3A6
19	No receiving noise	Replace the listed modules until the trouble is corrected: (1) AUDIO 1A2A3 (2) Panel 1A1 (3) IF 1A2A2 (4) MIX 1A2A1 (5) FILTER 1A2A5 (6) PS 1A4.

Table 3-15. Troubleshooting Chart (Cont'd.)

Step No.	Trouble Symptoms	Corrective Measures
20	Low receiver sensitivity - at dipole only or whip only connector	Replace module MN 1A5A1.
21	Low receiver sensitivity at some frequencies	Replace the listed modules until the trouble is corrected: (1) MIXER 1A2A1 (2) VCP 1A3A1 (3) SNF 1A5A3 (4) MN 1A5A1 (5) LORD 1A5A2.
22	Low receiver sensitivity at all frequencies	Replace the listed modules until the trouble is corrected: (1) MIXER 1A2A1 (2) USB 1A3A3 (3) VCP 1A3A1.
23	Low audio output	Replace the listed modules until the trouble is corrected: (1) AUDIO 1A2A3 (2) IF 1A2A2 (3) MIXER 1A2A1 (4) FILTER 1A2A5 (5) Panel 1A1
24	Distorted audio output	Replace the listed modules until the trouble is corrected: (1) AUDIO 1A2A3 (2) IF 1A2A2.
25	Incorrect received signal level indication.	Replace the listed modules until the trouble is corrected: (1) CONT 1A7 (2) IF 1A2A2 (3) Panel 1A1.
26	Faulty SAVE (squelch) operation	Replace the listed modules until the trouble is corrected: (1) CONT 1A7 (2) IF 1A2A2 (3) Panel 1A1.

Table 3-15. Troubleshooting Chart (Cont'd.)

Step No.	Trouble Symptoms	Corrective Measures
27	Frequency display is not illuminated when battery control is set to LITE.	Replace the panel 1A1.
28	Solid state display inoperative.	Replace the listed modules until the trouble is corrected: (1) Panel 1A1 (2) CONT 1A7.

Section V. DIRECT MAINTENANCE REPAIRS

3-13. Scope of Direct-Support Repairs

The repair operations allowed at the direct-support maintenance category are:

a. Removal and replacement of protective covers and gaskets.

b. Replacement of modules.

c. Removal and replacement of front panel assembly.

d. Replacement of knobs and screws.

3-14. Protective Covers, Removal and Replacement

a. Remove battery case and disconnect all cables connected to the radio set.

b. Loosen the screws fastening the cover to the case frame, then lift cover.

c. Before replacement, visually inspect the condition of the gasket cover recess. If necessary, clean inside areas with a clean, lintfree cloth.

NOTE

Replace the gasket if there are any breaks or twists. The gasket recess must be free of dirt.

d. To replace the gasket, proceed as follows:

(1) Use tweezers or a small screwdriver to remove the gasket. Take care not to burr or chip the gasket recess edges.

(2) Remove remaining adhesives then spread a thin layer of RTV silicone adhesive over the bottom of the recess.

(3) Prepare gasket for insertion in the recess with the narrow side up. Insert gasket and press it into place. Wait for adhesive to dry before replacing covers.

e. Before replacing, make sure cover is not bent, sheared, or otherwise damaged. Put cover in place, then fasten the screws holding it in place.

3-15. Module Replacement

a. Remove both protective covers (see para. 3-15).

b. Put radio set on a flat, clean surface, with motherboard side up.

c. Loosen the two screws holding the module in place and remove them.

d. Turn radio set over, so that the modules face upwards, and screw two module extractors into the holes provided on the module frame. To remove module, pull evenly on both extractors.

CAUTION

The module shall be handled only with the extractors or held by its frame. Do not grasp it by hand - the components may be damaged.

e. To replace a module, proceed as follows:

(1) Check condition of module and motherboard connectors. Do not try to insert a module if any connector appears damaged (bent, loose, or broken contacts, broken or cracked plastic body).

(2) Screw the module extractors into the module.

(3) Position the module, so that its name will be readable from the front of the radio set. Do not apply pressure until it is seated, then press evenly on both ends until its connector engages the mating motherboard connector.

(4) Remove the module extractors and turn radio set over so its motherboard faces up.

(5) Place lock washers on the module holding screws, insert the screws into position, and fasten them.

3-16. Front Panel Replacement

a. Loosen the five captive screws and the grounding screw holding the front panel in place, then using both handles, pull it forward.

b. Before replacing panel, check gasket condition and replace it if necessary (see para. 3-15). Also inspect the connector.

c. To replace the front panel, place it in front of the radio set, so that its connector will be exactly opposite the radio set connector, then push it into place, exerting equal forces on both handles. Fasten the five screws and the grounding screw.

3-17. Knob Replacement

NOTE

Before removing a knob, note the switch position.

a. Remove the screw holding the knob, then pull knob straight out.

b. To replace, mount the knob so that its white stripe shall point in the same direction as when the knob was removed.

c. Place a lockwasher on the screw and fasten it to hold the knob in position.

3-18. Alignment and Final Testing

Before returning the radio set to the using organization, the radio set shall be aligned, whenever necessary, according to the instructions given in Section VI, and then be subjected to the tests of Section II or III, as appropriate.

Section VI. DIRECT SUPPORT ALIGNMENT PROCEDURES FOR RT-936/PRC-174

3-19. Scope

a. The direct support alignment procedures are performed after module replacement, and also whenever necessary, in order to improve performance and reduce tolerances.

b. The direct-support alignment procedures consist of the following:

(1) Transmitter output power adjustment.

(2) Battery condition indication adjustment.

(3) AGC adjustment.

(4) Squelch adjustment.

(5) IF rejection alignment.

(6) Modulation index adjustment.

(7) Receiver gain alignment.

3-20. Test Equipment and Additional Equipment Required (fig. 3-4)

The following chart lists the equipment required to carry out direct alignment procedures of RT-936/PRC-174. If the specific equipment models are not available, other test equipment having similar characteristics may be used.

a. Test Equipment.

Test Equipment	Manufacturer	Model
RF Generator	Hewlett Packard	8640B, opt 001
Distortion Analyzer	Hewlett Packard	333A
AF Oscillator	Hewlett Packard	204D
Counter, Frequency	Hewlett Packard	5328A opt. 010
T-Connector	Hewlett Packard	11042
Voltmeter, AC (including AC Probe HP 11036)	Hewlett Packard	410C
Oscillator	Tektronix	466
Multimeter	Fluke	8000A
Attenuator, 50W, 30dB	Bird	8321
Attenuator, Variable, 0-120dB	Telonic	8143

b. Additional Equipment Required.

Equipment	Mfg. No./Description
Whip Simulator for PRC-174	08-24-138
Cable, Coaxial, 1.5m	RG-58 with BNC connectors
Cable, Shielded, Audio, 1.5m	Banana jacks at both ends
Cable, Coaxial, 1.5m	RG-58 with BNC male connector and banana jacks
Adaptor, Coaxial, N-male-to-BNC female	-
T-Adapter, BNC Connectors (two required)	-
Junction Box	Fig. 3-4

3-21. Preparation for Alignment (fig. 3-5, 3-6)

a. Remove both protective covers (see para. 3-15).

b. Put radio set on a flat, clean surface, with motherboard side up.

c. Assemble the test setup shown in fig. 3-5 (for transmitter section alignments) or fig. 3-6 (for receiver section alignments).

3-22. Alignment of Output Power (fig. 3-5)

a. Adjust the supply voltage to 26±1V.

b. Set UUT controls as follows:

Control	Position
Function	USB-R/T
Mode	WCW
Battery	IND
Frequency	22.0000 MHz.

c. Set UUT to transmission.

d. Adjust potentiometer RV3 on module SNF 1A5A3 to obtain an output voltage of 31V.

e. Return UUT to reception.

f. Check the output voltage at each frequency given in Table 3-16. If at any frequency the output voltage is lower than 28.5V, raise it to the required level. Be sure to set the UUT to receive before changing frequencies.

g. Set the UUT to receive.

h. Connect the whip simulator to the whip receptacle, and connect the AC voltmeter to the simulator.

i. Repeat the output power measurements at each frequency listed in Table 3-17. If the measured output voltage at any particular frequency is less than the value given in Table 3-17, readjust potentiometer RV3 on module SNF 1A5A3 until the voltage reading required by Table 3-17 is obtained.

Table 3-16. Frequencies for Power Output Measurement at "Dipole" Connector.

Frequency (MHz)	Required Voltage
2.0000 MHz	12.1111 MHz
2.4000 MHz	13.2222 MHz
3.1111 MHz	14.3220 MHz
3.9999 MHz	16.4400 MHz
4.2222 MHz	18.5500 MHz
5.3333 MHz	19.6660 MHz
6.4444 MHz	20.7000 MHz
7.5555 MHz	22.8800 MHz
8.6666 MHz	24.9990 MHz
9.7777 MHz	26.1000 MHz
10.8888 MHz	28.2600 MHz
11.9999 MHz	29.9999 MHz

Table 3-17. Frequencies for Power Output Measurement via Whip Simulator

Frequency (MHz)	Required Voltage
2.0000	13.9
2.4000	13.9
3.5000	13.9
5.5000	13.9
8.0000	15.6
11.0000	15.6
17.0000	15.6
25.0000	13.9
29.0000	13.9

3-23. Battery Condition Indicator Alignment (fig. 3-5)

a. Use the test setup of fig. 3-5.

b. Set UUT controls as follows:

Control	Position
Function	USB R/T
Mode	SSB
Battery	BAT
Frequency	16.000 MHz

c. Slowly reduce the power supply voltage to 20 VDC. Audio beeps shall be heard in the earphones and the solid state meter lights shall blink at a pulse rate of approx. 1.2 Hz. If required response does not occurwithin the 20 ± 0.5 V range, select another value for resistor R22 in module CONT 1A7 (see specified values in fig. 2-70).

d. Slowly increase the power supply voltage up to 27 VDC and check that the solid state LEDs light according to Table 3-18. If necessary, adjust potentiometer R57 in module CONT 1A7 to meet the requirements of Table 3-18.

Table 3-18. Battery Indication

Power Supply Voltage Range	Lighted LEDs
21.5V to 23.5V	L1
22.5V to 24.5V	L1+L2
23.5V to 25.5V	L1+L2+L3
24.5V to 26.5V	L1+L2+L3+L4
Over 26.5V	L1+L2+L3+L4+L5

3-24. AGC Alignment
(fig. 3-6)

a. Use the test setup shown in fig. 3-6.

b. Adjust power supply voltage to 26 ± 1V.

c. Adjust the RF signal generator to obtain a 3 microvolt CW signal at 16.001 MHz.

d. Set UUT controls as follows:

Control	Position
Function	USB-R
Mode	WCW
Battery	IND
Frequency	16.00000 MHz.

e. Slowly change the RF signal generator output from 3 microvolts to 1000 microvolts and check that the solid state lamps light according to Table 3-19. If necessary, adjust potentiometer RV3 on module IF 1A2A2 so that each indicator lamp on the UUT will light within its respective signal range, according to Table 3-19 (from left to right).

Table 3-19. Indicator Light Ranges as a Function of Input Signal

RF Level (microvolt)	Lamp Lighting Sequence
3 - 10	First
10 - 30	Second
30 - 100	Third
100 - 300	Fourth
300 - 1000	Fifth

f. Set the signal generator to 10 microvolts and check that the voltage at pin I of module IF 1A2A2 is 0.3 to 0.7V.

3-25. Squelch Alignment
(fig. 3-6)

a. Use the test setup shown in fig. 3-6.

b. Adjust the power supply voltage to 26 ± 0.5V.

c. Adjust the signal generator to obtain a 16.0005 MHz, 3 microvolt signal. Select the EXT AM mode.

d. Set audio generator to 100 Hz. Adjust its level to produce 17.5% AM modulation of the signal generator (as indicated by the modulation meter on the signal generator).

e. Change the frequency of the audio generator to 5 Hz, without changing its level.

f. Set UUT controls as follows:

Control	Position
Function	USB-R
Mode	SSB
Battery	SAVE
Frequency	16.0000 MHz

g. Slowly adjust potentiometer RV1 on module AUDIO 1A2A3, until audio output is squelched.

h. Slowly readjust potentiometer RV1 until a modulated tone is heard in the headphone.

i. Decrease audio generator output level to obtain 8% modulation, as indicated by the signal generator's meter. The tone in the headphone should be squelched off (silenced) after two to four seconds.

j. If necessary, readjust potentiometer RV1 on module AUDIO 1A2A3 until the requirements of both para. h and i are met.

3-26. IF Rejection Alignment (fig. 3-6)

a. Use the test setup shown in fig. 3-6.

b. Set power supply voltage to 26 ± 0.5V.

c. Set UUT controls as follows:

Control	Position
Function	USB-R
Mode	SSB
Battery	NORM
Frequency	29.0000 MHz

d. Tune the signal generator to 29.001 MHz (CW output), and adjust its output level to obtain 10 dB signal-to-noise ratio (SINAD) at the audio output, with the VOLUME control set for an audio output of 2.45V.

e. Tune the signal generator to 109.349 MHz (CW) and increase the output level by 80 dB, relative to d. above. Slowly vary the frequency within ± 1000 Hz of the nominal frequency to find the maximum audio signal at the output of the UUT. Hold that frequency.

f. Adjust trimmer capacitor CV1 of the FL100 (located on the motherboard) to obtain minimum output from the UUT; then measure the SINAD. Make sure that it is lower than 10 dB.

g. Secure the trimmer with a drop of "Q-Dope" glue or equivalent.

3-27. Alignment of Modulation Index (fig. 3-5)

a. Use the test setup shown in fig. 3-5.

b. Adjust power supply voltage to 26 ± 0.5 V.

c. Adjust the audio generator for 5mV at 1KHz.

d. Set UUT controls as follows:

Control	Position
Function	USB-R/T
Mode	AM
Battery	NORM
Frequency	2.0000

e. Set the UUT to transmission.

f. Using the oscilloscope, measure the modulation index of the RF output: it should be 70% to 95%.

g. If modulation index is outside the 70 to 95% range, change the value of resistor R86 in module IF 1A2A2 to one of the other values specified in fig. 2-16.

NOTES:

1. To increase the modulation, increase the value of R86, and vice versa.
2. Modulation index, m, is given by:

$$(\%)\ m = \frac{Vmax - Vmin}{Vmax + Vmin} \times 100$$

where Vmax - is the peak-to-peak amplitude at a modulation crest.

Vmin - is the peak-to-peak amplitude at a modulation through.

h. Repeat g, if necessary, until the requirements are met.

3-28. Receiver Gain Alignment (fig. 3-6)

NOTE

The following procedure shall be performed only if the UUT fails the sensitivity test.

a. Use the test setup as shown in fig. 3-6.

b. Adjust the power supply voltage to 26 ± 1V.

c. Adjust the signal generator to obtain a 0.7 microvolt CW signal at 2.001 MHz.

d. Set UUT controls as follows:

Control	Position
Function	USB-R
Battery	NORM
Frequency	2.0000 MHz

e. Adjust the volume control to obtain 2.45V at the headphone output.

f. Trim coil L19 in module MIXER 1A2A1, to obtain a SINAD of at least 10 dB.

CHAPTER 4

GENERAL SUPPORT AND DEPOT MAINTENANCE

Section I. GENERAL SUPPORT TESTING OF RT-936/PRC-174

4-1. Scope of General Support and Depot Maintenance

The maintenance procedures given in this chapter supplement the direct support maintenance procedures detailed in Chapter 3.

a. Section I presents test procedures for Receiver-Transmitter RT-936/-PRC-174 and sets forth performance standards that a receiver-transmitter must meet before being returned to the using organization.

b. Section II provides information on signals available at module connectors and test points, which allow signal tracing and troubleshooting of the RT-936/PRC-174 down to the module level, using extenders and general-purpose test equipment.

4-2. Test Equipment and Additional Equipment Required for General Support Testing of RT-936/PRC-174 (fig. 4-1, 4-2, 4-3)

a. General-purpose test equipment for the RT-936/PRC-174 is listed in Table 4-1. If the specific test equipment models are not available, other test equipment having similar characteristics may be used.

Table 4-1. General-Purpose Test Equipment for General Support Testing of the RT-936/PRC-174

Item	Description	Manufacturer	Model
1	Frequency Counter	Hewlett-Packard	5328A, opt 010
2	RF Signal Generator	Hewlett-Packard	8640B
3	RF Voltmeter (incl. AC probe)	Hewlett-Packard	410C
4	AC Probe Adapter	Hewlett-Packard	11042A
5	Distortion Analyzer	Hewlett-Packard	333A
6	Spectrum Analyzer, Mainframe	Hewlett-Packard	141T
7	Spectrum Analyzer, IF Plug-In Unit	Hewlett-Packard	8552B
8	Spectrum Analyzer, RF Plug-In Unit	Hewlett-Packard	8553B
9	Multimeter	Fluke	8010A
10	Audio Oscillator	Hewlett-Packard	204D
11	Attenuator, 50 W, 30 dB	Bird	8321
12	Attenuator, Variable	Telonic	8143
13	Oscilloscope	Tektronix	465B
14	DC Power Supply	Hewlett-Packard	6274B
15	Spectrum Analyzer, RF Plug-In Unit	Hewlett-Packard	8554B

b. Additional equipment required for testing the RT-936/PRC-174 is listed in Table 4-2.

Table 4-2. Additional Equipment for General Support Testing of the RT-936/PRC-174

Item	Description	Manufacturer Cat.
1	Final Test Fixture for RT-936/PRC-174	210824284
2	Whip Simulator	210824344
3	Control Cable	212409230
4	Audio Cable	210824265
5	DC Power Cable	2124009201
6	Coaxial Cable, BNC/BNC	-
7	Cable, BNC-to-Banana Plugs	-
8	Cable, Banana Plugs	-
9	Adapter, N-BNC	UG-201A/U

(1) Final test fixture for RT-936/PRC-174 (fig. 4-1, 4-2). This test fixture provides for connection of test equipment to the RT-936/PRC-174 under test, controls the unit-under-test (UUT) and generates several test signals.

Table 4-3. Final Test Fixture for RT-936/PRC-174, Controls, Indicators and Connectors

Item	Control, Indicator or Connector	Function
1	ON/OFF Switch	Turns on DC power to the test fixture and the unit-under-test.
2	ON Indicator	Lights when the test fixture receives DC power.
3	BAT Jacks	Two jacks for connection of DC power (positive lead to upper jack) to the RT-936/PRC-174 under-test.
4	CURRENT Meter	Measures the DC current drawn by the RT-936/-PRC-174 under-test.
5	REMOTE 1 Connector	Connection to the CONTROL connector of the RT-936/PRC-174 under-test.
6	PA/CBP Switch	Toggle switch having two positions:

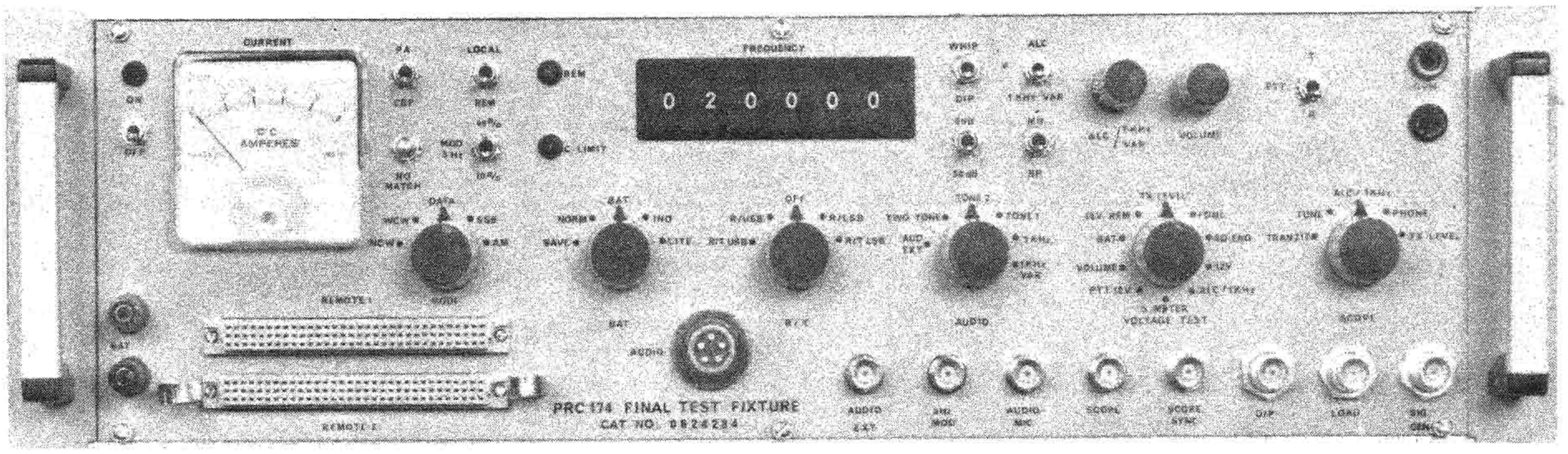


Fig. 4-1. Final Test Fixture, View of the Front Control Panel

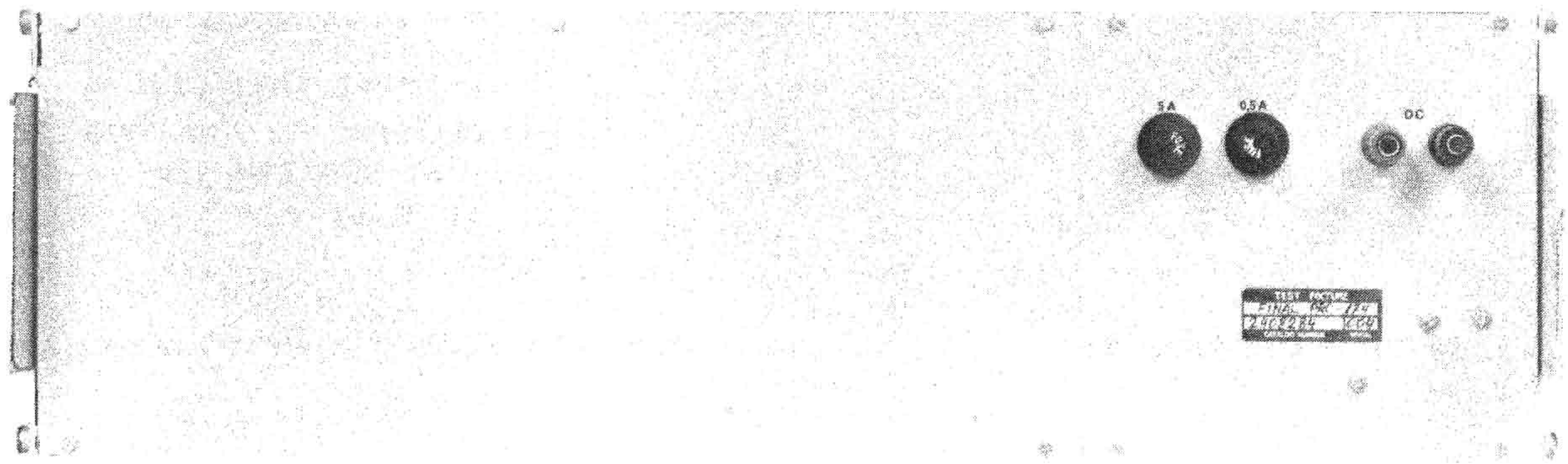


Fig. 4-2. Final Test Fixture, View of the Rear Panel

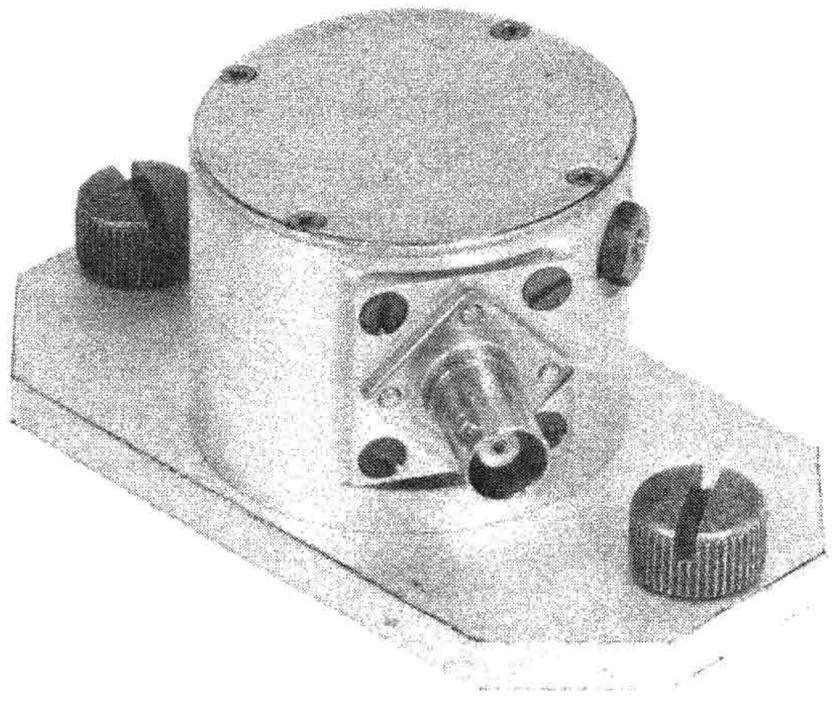


Fig. 4-3. Whip Simulator for the RT-936/PRC-174

Table 4-3. Final Test Fixture for RT-936/PRC-174, Controls, Indicators and Connectors (Cont'd.)

Item	Control, Indicator or Connector	Function
6	Cont'd.	Position — Function PA — The power amplifier of the RT-936/PRC-174 is operative. CBP — The power amplifier is by-passed.
7	LOCAL/REM(ote) Switch	Selects the control mode of the RT-936/PRC-174 under-test. Position — Function LOCAL — The RT-936/PRC-174 is controlled from its own front panel. REM — The RT-936/PRC-174 is controlled from the test fixture panel.
8	REM(ote) Indicator	Lights when the remote control mode is selected.
9	C LIMIT Indicator	Lights when the RT-936/PRC-174 draws excessive current.
10	NO MATCH Pushbutton	When pressed, simulates the existence of the no-match alarm.
11	5 Hz MOD(ulation) Switch	Selects the modulation factor of the RF signal generator used to test the squelch function.
12	MODE Selector	Controls the operating mode of the RT-936/-PRC-174 under-test, when it is under remote control. Position — Function NCW — Narrow-band CW mode. WCW — Wideband cw mode. DATA — Data mode. SSB — Single-sideband voice mode.
13	BAT Control	Controls the operation of the squelch circuit and solid-state display of the RT-936/-PRC-174 under-test, when it is under remote control.

Table 4-3. Final Test Fixture for RT-936/PRC-174, Controls, Indicators and Connectors (Cont'd.)

Item	Control, Indicator or Connector	Function
13	Cont'd.	**Position** — **Function** SAVE — Squelch circuit enabled. NORM — Squelch circuit disabled. BAT — Solid state display indicates the relative value of the DC supply voltage. IND — Similar to the NORM mode, except that the solid state display is operative. LITE — Frequency selectors of the RT-936/PRC-174 are illuminated.
14	AUDIO Connector	Connection to the AUDIO receptacles of the RT-936/PRC-174 under-test.
15	FREQUENCY Selectors	Digital thumbwheel switches which select the operating frequency of the RT-936/PRC-174 under-test, when it is under remote control.
16	R/T Selector	Controls the operation of the RT-936/PRC-174 under-test, when it is under remote control. **Position** — **Function** OFF — Receiver-transmitter turned off. R/USB — Receiver-transmitter turned on; receive-only operation in USB or AM modes. R/T USB — Receiver-transmitter turned on; receive and transmit operation in USB and AM modes. R/LSB — Same as R/USB, except that the operation modes are LSB and AM. R/T LSB — Same as R/T USB, except that the operation modes are LSB and AM.
17	REMOTE 2 Connector	Wired in parallel with REMOTE 1; intended for connection to other test fixtures (not required when testing the RT-936/PRC-174).
18	WHIP/DIP Switch	Selects the operative RF port of the receiver-transmitter.

Table 4-3. Final Test Fixture for RT-936/PRC-174, Controls, Indicators and Connectors (Cont'd.)

Item	Control, Indicator or Connector	Function
19	ALC/1 kHz VAR Switch	a. Connects, for test purposes, the DC voltage supplied via the ALC potentiometer (no. 20) to the ALC line. b. Selects the variable to be controlled by the ALC/1 kHz VAR control (20).
20	ALC/1 kHz VAR Control	Varies the DC voltage to be applied to the ALC line or the amplitude of the 1 kHz VAR signal, as selected by (19).
21	220 mV/5 mV	Selects the level of the audio modulation signal supplied by the test fixture.
22	MN/BP Switch	When set at BP, the matching network contained in module MN 1A5A1 is by-passed.
23	AUDIO Selector	Controls the operation of the internal audio generator, whose signal is available at the AUDIO and AUDIO MIC connectors. Position — Function 1 kHz VAR — 1000 Hz, variable amplitude 1 kHz — 1000 Hz TONE 1 — 1500 Hz TONE 2 — 2500 Hz TWO TONE — 1500 Hz + 2500 Hz EXT AUDIO — Supplied by external source
24	5-Hz MOD Connector	BNC output connector for the modulation signal supplied to the RF signal generator in order to test the squelch function.
25	AUDIO MIC Connector	BNC connector, connected in parallel with the microphone line in the AUDIO connector.
26	VOLTAGE TEST Selector	Connects the DVM connector (no. 32) to the listed measurement points (available at the CONTROL connector of the RT-936/PRC-174). Position — Function S METER — Analog indication of received signal level. PTT 12V — PTT 12-V line in the CONTROL connector. VOLUME — DC voltage supplied by the VOLUME control (no. 29).

Table 4-3. Final Test Fixture for RT-936/PRC-174, Controls, Indicators and Connectors (Cont'd.)

Item	Control, Indicator or Connector	Function
26	Cont'd.	**Position** — **Function** BAT — Battery voltage. 12V REM — 12-V REM line. TX LEVEL — Analog indication of output power. FONL — Loss-of-lock indication. SQ ENG — "Squelch energized" line in the CONTROL connector. 12V — 12V line in the CONTROL connector. ALC — ALC voltage supplied by the ALC control (no. 20).
27	SCOPE Connector	BNC connector for the oscilloscope; used in conjunction with the SCOPE selector (no. 33).
28	SCOPE SYNC Connector	BNC connector, supplies a trigger pulse for oscilloscope synchronization when squelch is enabled.
29	VOLUME Control	Supplies a variable DC voltage which controls the audio output of the RT-936/PRC-174 under-test, when it is under remote control.
30	PTT Switch	Controls transmission of the RT-936/PRC-174 under-test.
31	EXT AUDIO Connector	BNC connector for connection of an external audio signal generator.
32	DVM Connector	Banana jacks for connection of an external DVM; used in conjunction with the VOLTAGE TEST selector (no. 26).
33	SCOPE Selector	Connects the SCOPE connector (no. 27) to the listed measurement points (available at the CONTROL connector of the RT-936/PRC-174). **Position** — **Function** TRANSIT — TRANSIT pulse following a frequency change. TUNE — TUNE line. ALC — ALC line. PHONE — Receiver audio output. FX LEVEL — Fixed level audio output.

Table 4-3. Final Test Fixture for RT-936/PRC-174, Controls, Indicators and Connectors (Cont'd.)

Item	Control, Indicator or Connector	Function
34	DIP Connector	BNC connector, for connection to the DIPOLE connector of the RT-936/PRC-174 under-test.
35	LOAD Connector	BNC connector, for connection of 50-ohm load to the transmitter output.
36	SIG GEN Connector	BNC connector for the RF signal generator.
37	CONTROL Connector (rear panel)	Connection to other test fixtures (not required for testing the RT-936/PRC-174).
38	5 A Fuse (rear panel)	Protects the DC supply line for the RT-936/PRC-174 under-test.
39	0.5 A Fuse (rear panel)	Protects the DC supply line for the test fixture.
40	VIN Connector (rear panel)	Connection to the DC power supply.

(2) Whip simulator (fig. 4-3). The whip simulator contains a reactive network loaded by a resistor, which possesses an input impedance closely simulating the typical input impedance of whip antenna AT-1741. The whip simulator connects to the whip receptacle of the RT-936/PRC-174. A test point is provided, at which the RF voltage developing across the internal resistance can be measured.

4-3. Test and Alignment Procedures for Receiver/Transmitter RT-936/PRC-174 (fig. 4-4 through 4-10)

a. Applicability. This paragraph presents the test procedures to be carried out at the general support maintenance category:

(1) After repair of equipment.

(2) Periodically, at intervals determined by the maintenance authority. The test procedures include alignment instructions, which permit to adjust certain parameters and bring them within narrower tolerances. All necessary adjustment components can be reached after removing the covers of the RT-936/PRC-174; no further disassembly is required.

b. Preparation for Test (fig. 4-4).

(1) Check that the function switch of the RT-936/PRC-174 and the ON/OFF switch of the test fixture are set to OFF.

(2) Remove the top and bottom covers of the RT-936/PRC-174 under-test; then lay the RT-936/PRC-174 on a clean, flat working surface covered by an insulating material.

CAUTION

Do not turn on equipment used in the test setup.

(3) Assemble the test setup shown in fig. 4-4.

(4) Turn on the DC power supply and adjust its output voltage to 26V.

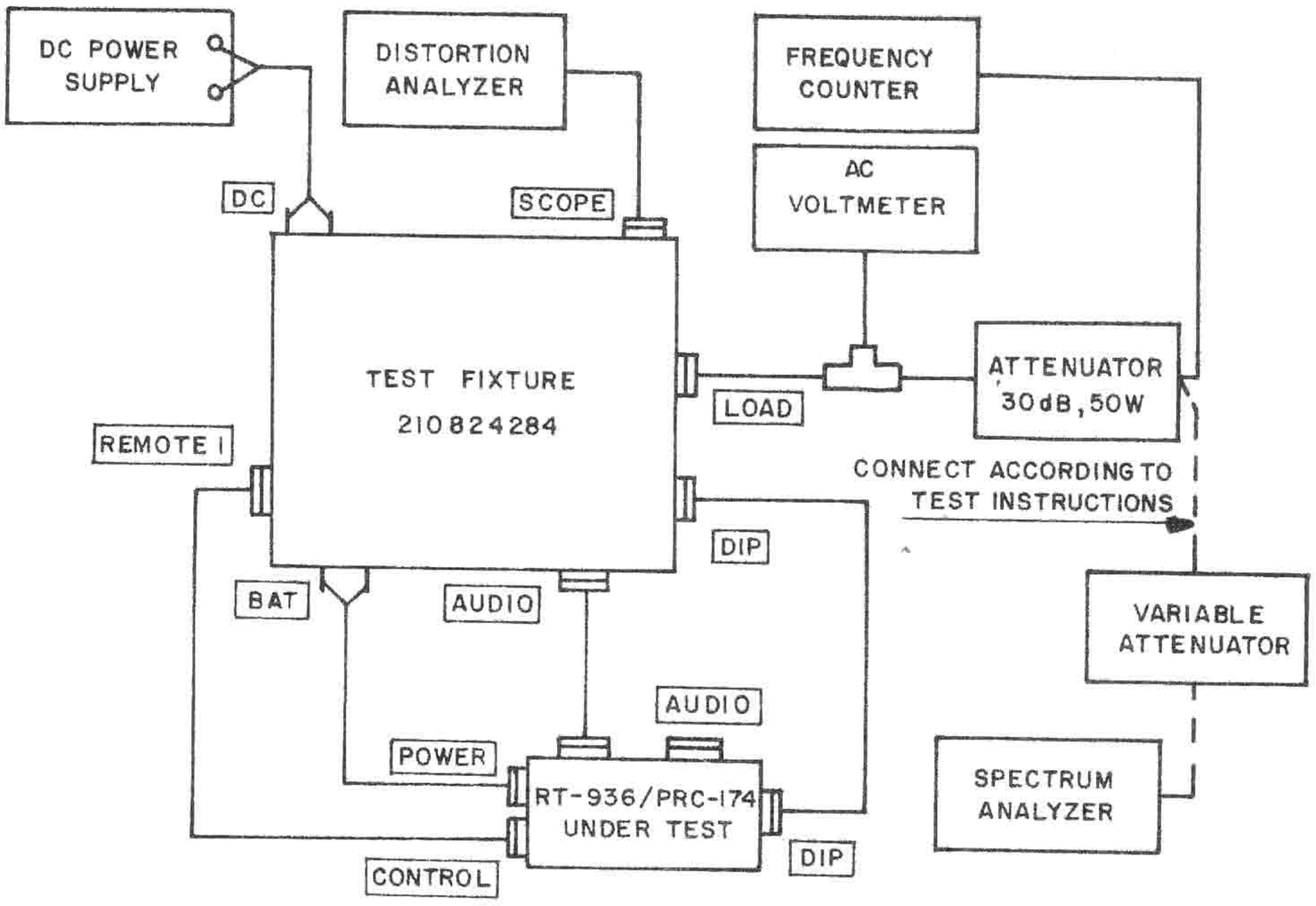


Fig. 4-4. Test Set-up for Transmitter Tests

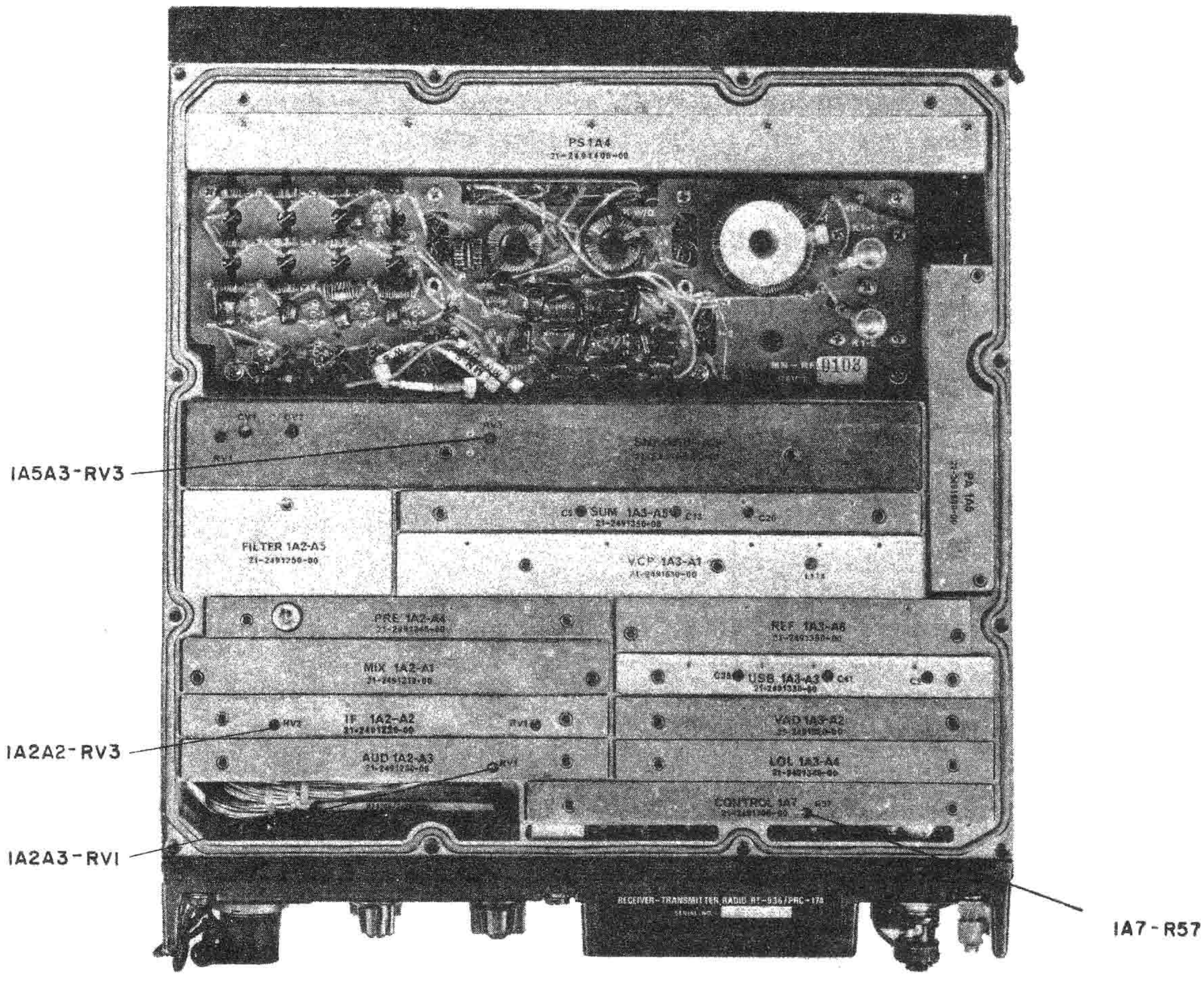


Fig. 4-5. RT-936/PRC-174, Identification of Alignment Points

c. Test and Alignment Procedures. Carry out the test and alignment instructions given in Table 4-4 (transmitter), Table 4-5 (receiver), Table 4-6 (solid state display and indications), and the operational checks given in Chapter 3, para. 3-11. If a malfunction is found which could cause damage to the equipment, stop the tests and correct the trouble before continuing.

NOTE

1. For most tests, the RT-936/PRC-174 is controlled by test fixture controls. The controls on the front panel of the unit-under-test need not be touched, unless specifically instructed to do so.
2. Unless otherwise stated, the R/T selector on the front panel of the unit-under-test should be in the OFF position. The setting of all other controls of the unit-under-test is irrelevant.

Table 4-4. Test and Alignment Procedures for the Transmitter Section of the RT-936/PRC-174

Item	Test	Test Fixture Control Settings	Procedure	Performance Standard
1	Frequency Accuracy	ON/OFF : ON MODE : AM MN/BP : MN BAT : IND CAL/REM : REM R/T : R/T USB PA/CBP : PA FREQUENCY 2.000 WHIP/DIP : DIP ALC/1 kHz VAR : 1 kHz VAR PTT : R	(1) Use the test setup shown in fig. 4-4. (2) Set the PTT switch to T. Read the frequency indicated on the frequency counter, and calculate the frequency error. (3) Repeat the PTT switch to R. (4) Repeat steps (2), (3) above at each of the following frequencies: 2.4000 3.1111 3.9999 4.2222 5.3333 6.4444 7.5555 8.6666 9.7777 10.8888 11.9999 12.1111 13.2222 14.3222 16.4400 18.5500 19.6660 20.7000	N/A Less than 2 Hz N/A Tolerance (Hz) 2.4 3.1 4.0 4.2 5.3 6.4 7.6 8.7 9.8 10.9 12.0 12.1 13.2 14.3 16.4 18.6 19.7 20.7

Table 4-4. Test and Alignment Procedures for the Transmitter Section of the RT-936/PRC-174 (Cont'd)

Item	Test	Test Fixture Control Settings	Procedure	Performance Standard
1	Cont'd.		22.8800 24.9990 26.1000 28.2600 29.9999 (5) Set the PTT switch to R.	22.0 25.0 26.1 28.3 30.0
2	Output Power (dipole)	ON/OFF : ON MODE : AM BAT : IND LOCAL/REM: REM R/T : R/T USB PA/CBP : PA FREQUENCY: 2.0000 WHIP/DIP : DIP ALC/1 kHz VAR : 1 kHz VAR PTT : R MN/BP : MN AUDIO : 1 kHz 220mV/5mV: 5 mV		N/A
	a. Measurement - AM		(1) Set the PTT switch to T and measure the RF output voltage indicated by the AC voltmeter.	28 to 40 V
			(2) Return the PTT switch to R.	N/A
	- SSB/LSB		(3) Repeat steps (1), (2) above with the MODE switch at SSB.	28 to 40 V
	- SSB/USB		(4) Repeat steps (1), (2) above with the MODE switch at SSB and the R/T switch at R/T USB.	28 to 40 V
	- DATA/USB		(5) Repeat steps (1), (2) above with the MODE switch at DATA and the 220 mV/5 mV switch at 220 mV.	28 to 40 V

Table 4-4. Test and Alignment Procedures for the Transmitter Section of the RT-936/PRC-174 (Cont'd)

Item	Test	Test Fixture Control Settings	Procedure	Performance Standard
	- WCW/USB		(6) Repeat steps (1), (2) above with the MODE switch at WCW.	28 to 40 V
	- NCW/USB		(7) Repeat steps (1), (2) above with the MODE switch at NCW.	28 to 40 V
			(8) Repeat steps (1) through (6) above at each of the following frequencies:	28 to 40 V
			2.4000 8.6666 18.5500	28 to 40 V
			3.1111 9.7777 19.6660	28 to 40 V
			3.9999 10.8888 20.7000	28 to 40 V
			4.2222 11.9999 22.8800	28 to 40 V
			5.3333 12.1111 24.9990	28 to 40 V
			6.4444 13.2222 26.1000	28 to 40 V
			14.3222 28.2600	28 to 40 V
			16.4400 29.9999	28 to 40 V
			(9) Set the PTT switch to R.	
	b. Adjustment of ALC circuits	Same as for a. above, except: 220mV/5mV: 220 mV MODE : DATA	(1) Set the test fixture controls to the required positions.	N/A
			(2) Identify potentiometer RV3 on module SNF 1A5A3 (fig. 4-5).	N/A
			(3)Refer to the test results obtained above (or those obtained in item 3 on the whip, as appropriate) and locate the frequency at which the output power is at minimum.	N/A
			(4) Set the frequency of the minimum output power on the FREQUENCY selectors, then set the PTT switch to T.	N/A
			(5) Adjust potentiometer RN3 to obtain an indication of 28.5 V on the AC voltmeter.	N/A
			(6) Repeat the output power test at all test frequencies and readjust the potentiometer if necessary.	28 to 40 V
			(7) Set the PTT switch to R.	
3	Whip Antenna Output Power	ON/OFF : ON MODE : WCW BAT : IND LOCAL/REM: REM R/T : R/T USB	(1) Assemble the test setup shown in fig. 4-6.	N/A
			(2) Set the PTT switch at T and observe the RF voltage indicated by the AC voltmeter.	Min 13.9 V

NOTE

To be carried out:

1. If the RT-936/PRC-174 failed the output power test (either on the dipole or whip).
2. After replacement or repair of module PA 1A6, PRE 1A2A4, SNF 1A5A3, MIX 2A2A1.

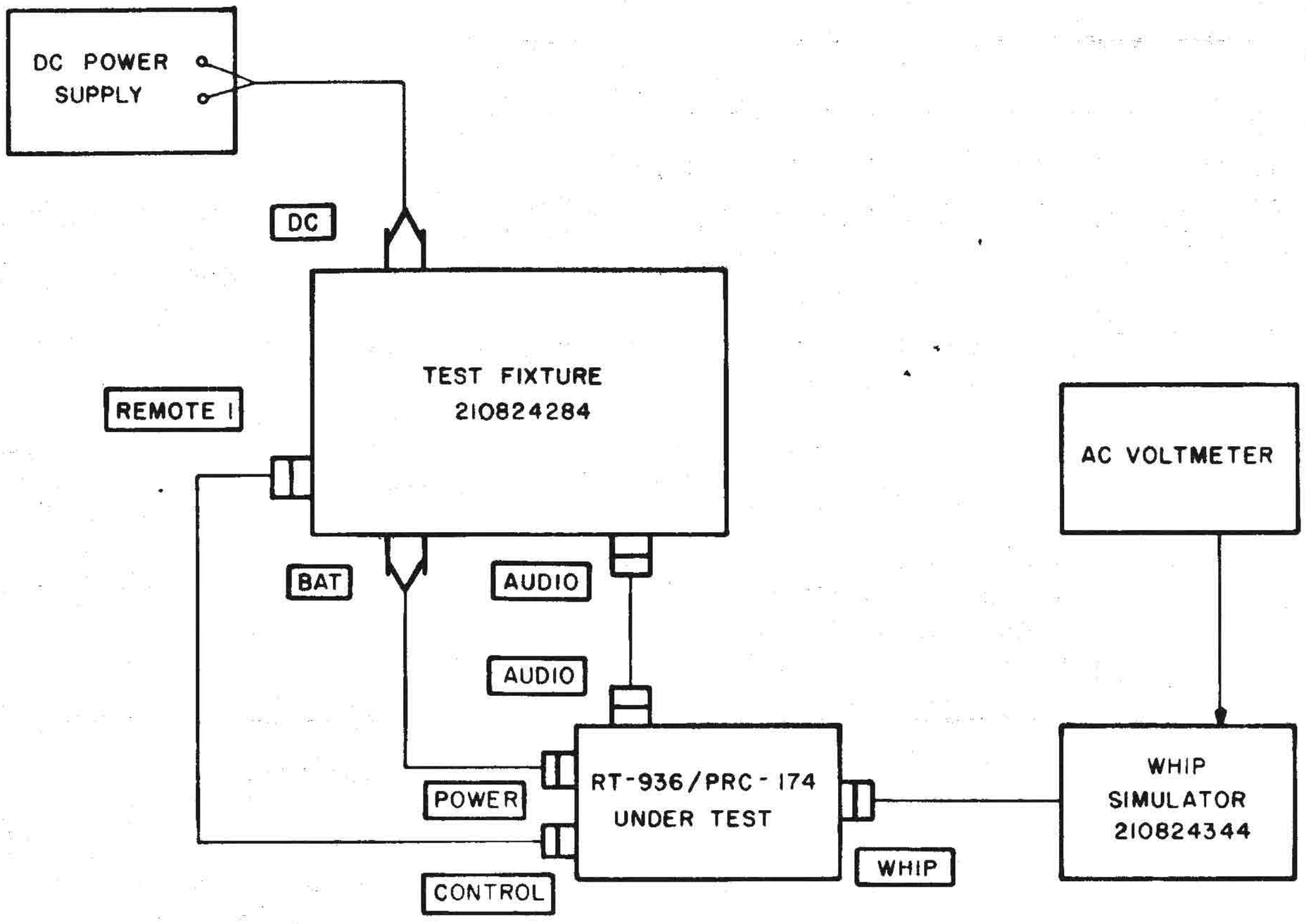


Fig. 4-6. Whip Antenna Output Power, Test Setup

Table 4-4. Test and Alignment Procedures for the Transmitter Section of the RT-936/PRC-174 (Cont'd)

Item	Test	Test Fixture Control Settings	Procedure	Performance Standard
3	Cont'd	PA/CBP : PA FREQUENCY: 2.0000 WHIP/DIP : WHIP ALC/1kHz VAR: 1 kHz VAR PTT : R MN/BP ; MN	(3) Return the PTT switch to R. (4) Repeat steps (2), (3) above at each of the following frequencies: 2.4000 8.0000 25.0000 3.5000 11.0000 29.9000 17.0000 NOTE: Adjust the ALC circuits (item 2.b above) if performance standards are not met.	N/A Freq. (MHz) / Min RF Output (V) 2.4000 / 13.9 3.5000 / 13.9 8.0000 / 15.6 11.0000 / 15.6 17.0000 / 15.6 25.0000 / 13.9 29.9000 / 13.9

Table 4-4. Test and Alignment Procedures for the Transmitter Section of the RT-936/PRC-174 (Cont'd)

Item	Test	Test Fixture Control Settings	Procedure	Performance Standard
4	Transmitter Sidetone	ON/OFF : ON MODE : SSB BAT : IND LOCAL/REM: REM R/T : R/T UBS PA/CBP : PA FREQUENCY: 16.0000 WHIP/DIP : DIP ALC/1 kHz VAR : 1 kHz VAR PTT : R MN/BP : MN AUDIO : 1 kHz 220mV/5mV: 5 mV SCOPE : PHONE	(1) Use the test setup shown in fig. 4-4. (2) Set the PTT switch to T. (3) Observe the RF signal indicated on the AC voltmeter. (4) Measure the sidetone level, using the distortion analyzer as a voltmeter. (5) Rotate the VOLUME control of the test fixture over its full range and observe the indication of the distortion analyzer. (6)Return the PTT switch to R.	N/A 1N/A 28 to 40 V 200 to 650 mV No change N/A
5	AM Modulation Index	ON/OFF : ON MODE : AM BAT : IND LOCAL/REM: REM R/T : R/T USB PA/CBP : PA FREQUENCY: 2.0000 WHIP/DIP : DIP ALC/1 kHz VAR : 1 kHz VAR PTT : R MN/BP : BP 220mV/5mV:	(1) Use the test setup shown in fig. 4-7. (2) Set the PTT switch to T. (3) Evaluate the modulation index, m, uising the oscilloscope. Use the following formula: $(\%)\ m = \frac{Vmax - Vmin}{Vmax + Vmin} \times 100\%$ where (see fig. 4-8): Vmax - peak voltage of modulated signal at a modulation crest. Vmin - peak voltage of modulated signal at a modulation through. (4) Set the PTT switch to R. (5) If modulation index is out side the 70 to 95% range, change the value of resistor R86 in module IF1A2A2 to one of the other values specified in fig. 2-16.	N/A 70 to 95% N/A

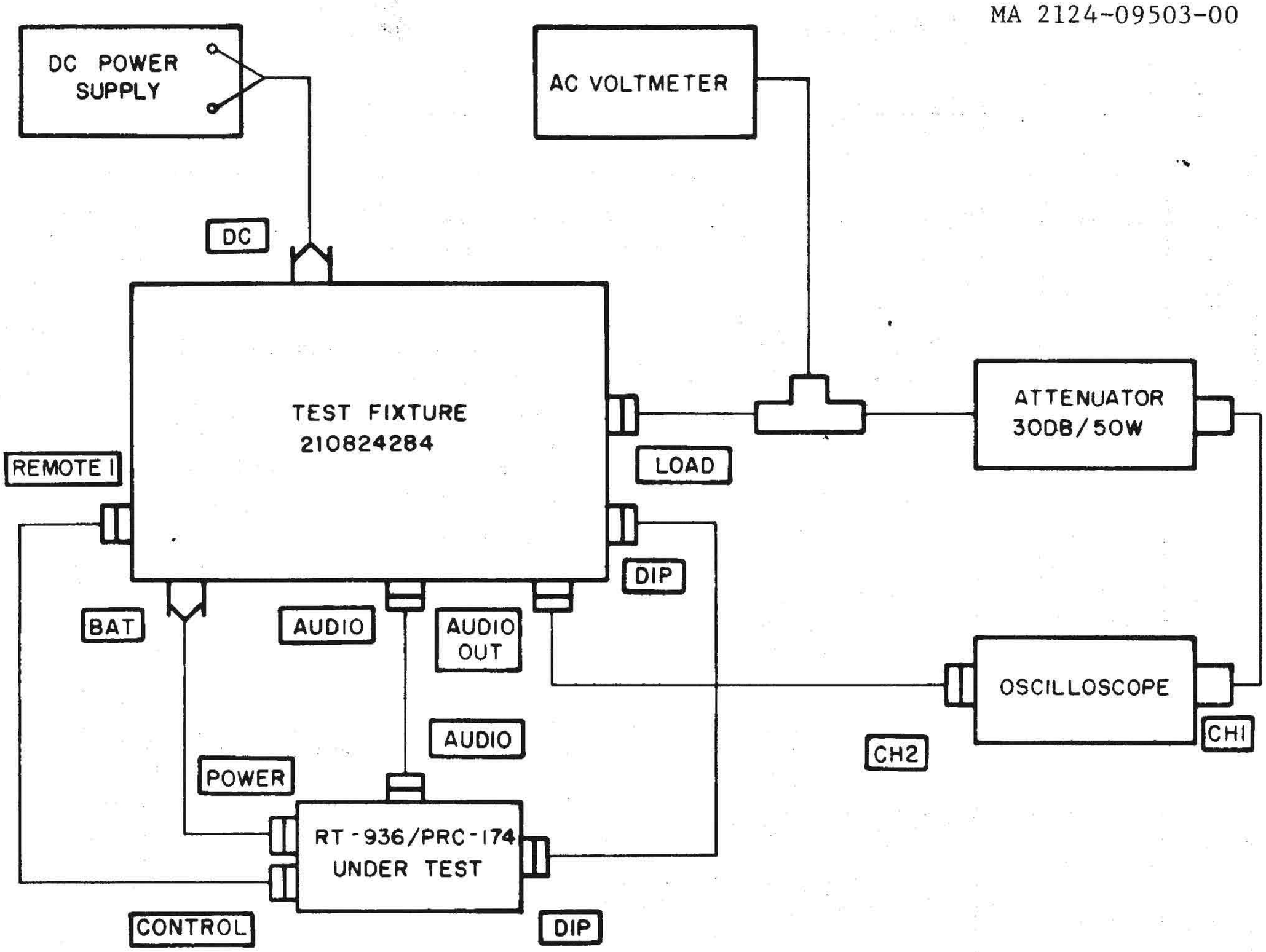
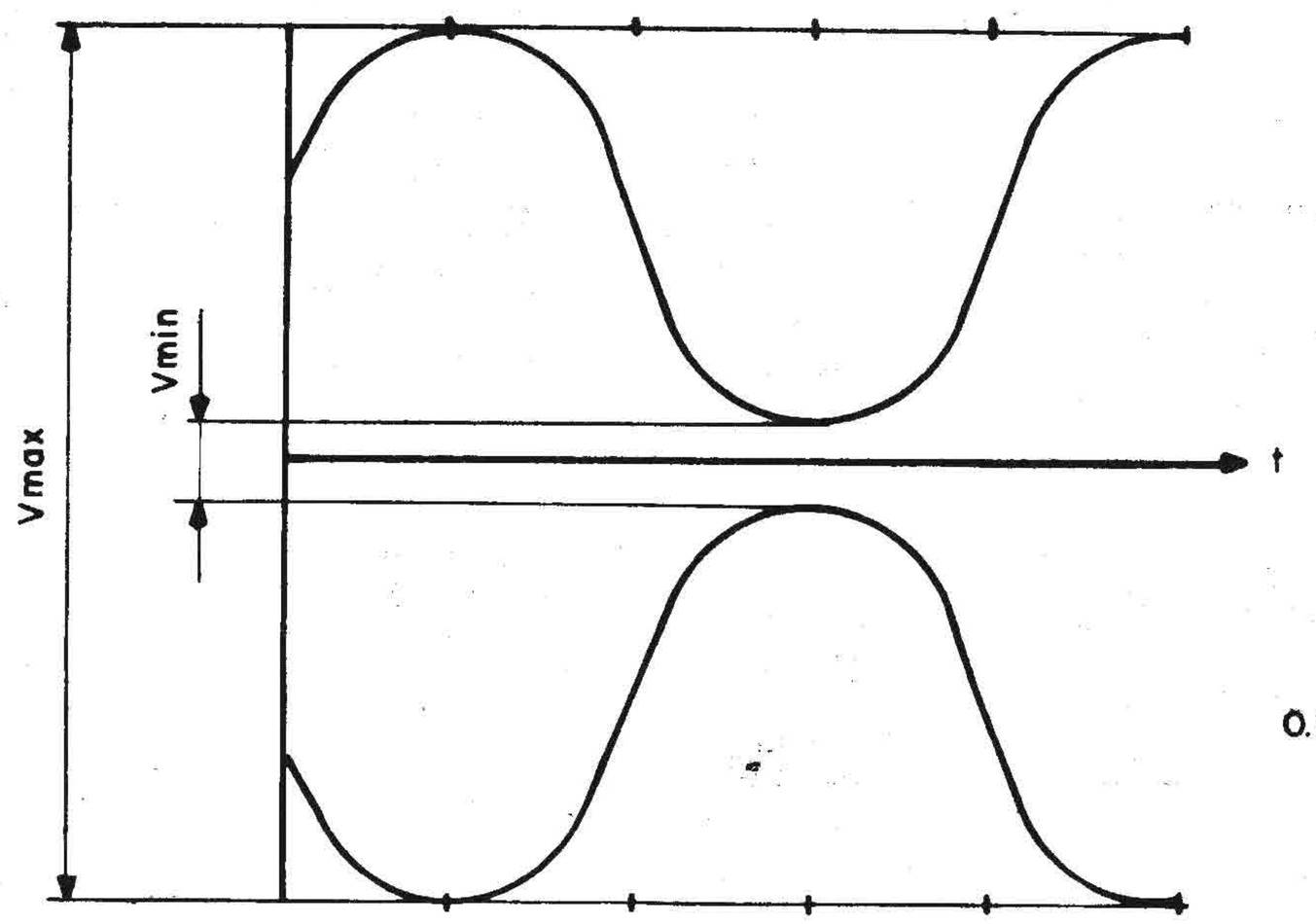


Fig. 4-7. AM Modulation, Test and Adjustment Setup



$$0.95 > \frac{V_{max} - V_{min}}{V_{max} + V_{min}} \geq 0.7$$

Figure 4-8. Evaluation of Modulation Index from Oscilloscope Display

Table 4-5. Test and Alignment Procedures for the Receiver Section of the RT-936/PRC-174

Item	Test	Test Fixture Control Settings	Procedure	Performance Standard
1	Receiver	Operation Switch : ON MODE : SSB R/T : R USB BAT : IND LOCAL/REM: REM PTT : R PA/CBP : PA MN/BP : MN ALC/1kHz VAR : 1 kHz VAR WHIP/DIP : DIP FREQUENCY : 2.0000 SCOPE : PHONE	(1) Assemble the test setup shown in fig. 4-9. (2) Tune the RF signal generator to the (test frequency +1 kHz), and adjust it to obtain a CW test signal of 0.7 microvolts. (3) Set the MODE selector on the test fixture to SSB. (4) Adjust the VOLUME control, located on the front panel of the test fixture, until the distortion analyzer indicates an audio output of 0.775V. (5) Use the distortion analyzer to measure the ratio of (signal + noise + distortion) to (noise + distortion). (6) Repeat steps (2) through (5) above at each of the following test frequencies: 2.4000 8.6666 18.5500 3.1111 9.7777 19.6660 3.9999 10.8888 20.7000 4.2222 11.9999 22.8800 5.3333 12.1111 24.9990 6.4444 13.2222 26.1000 7.5555 14.3222 28.2600 16.4400 29.9999	N/A N/A N/A At least 10 dB
2	Receiver Gain Alignment NOTE This alignment shall be carried out only if sensitivity requirements are not met.	Same as 1 above, except: FREQUENCY:2.0000 MHz	(1) Use the test setup shown in fig. 4-9. (2) Tune the RF signal generator to 2.001 MHz and adjust its output to 0.7 microvolts. (3) Adjust the VOLUME control to obtain 0.775V on the distortion analyzer. (4) Trim coil L19 in module MIXER 1A2A1 (fig. 4-14) to obtain a SINAD of at least 10 dB.	N/A N/A N/A N/A

Table 4-5. Test and Alignment Procedures for the Receiver Section of the RT-936/PRC-174

Item	Test	Test Fixture Control Settings	Procedure	Performance Standard
3	Audio Output Power	ON/OFF : ON MODE : SSB R/T : R/USB BAT : IND LOCAL/REM: REM PTT : R PA/CBP : PA MN/BP : MN ALC/1kHz VAR : 1 kHz VAR WHIP/DIP : DIP FREQUENCY: 16.0000 SCOPE : PHONE	(1) Use the test setup shown in fig. 4-9. (2) Tune the RF signal generator to 16.0010 MHz and adjust it to obtain a CW test signal of 1.0 microvolts. (3) Turn the VOLUME control located on the front panèl of the test fixture fully clockwise and measure the audio output level, using the distortion analyzer as a voltmeter. (4) Turn the VOLUME control on the test fixture fully counter-clockwise and measure the audio output level. (5) Return the VOLUME control to the fully clockwise position.	N/A N/A At least 2.45V Less than 77mV N/A

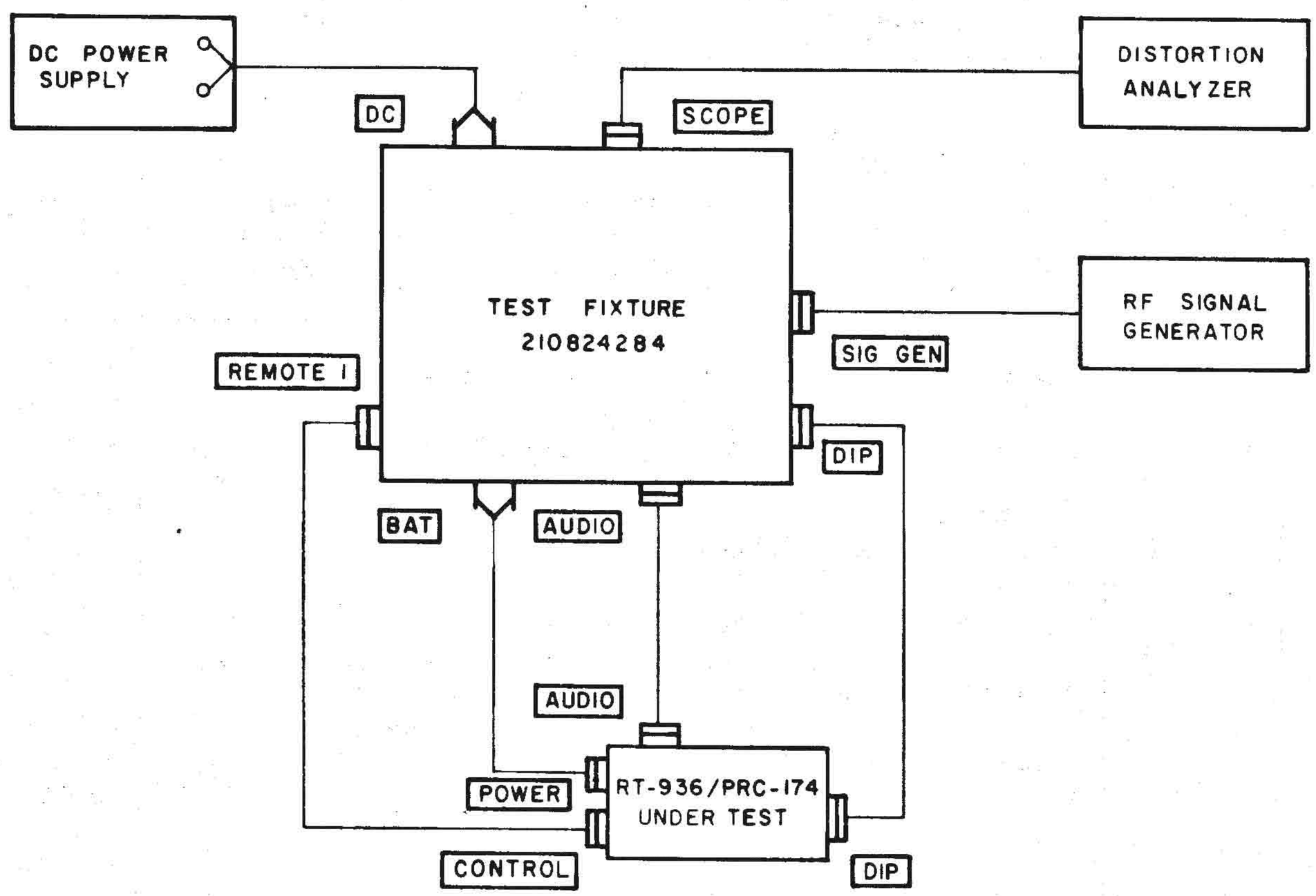


Fig. 4-9. Receiver section, test setup

Table 4-5. Test and Alignment Procedures for the Receiver Section of the RT-936/PRC-174

Item	Test	Test Fixture Control Settings	Procedure	Performance Standard
3	Cont'd.		(6) Change the frequency of the RF test signal to 16.00035, then to 16.00240 MHz and record the audio output level obtained at each frequency. (7) Set the MODE selector to AM. (8) Tune the RF signal generator to 16.0000 MHz and adjust it to obtain a 5 microvolt test signal, modulated 30% by a 1-kHz tone. (9) Record the audio output level.	The output level remains at least 2.45V N/A N/A At least 2.45V
4	Audio Distortion	ON/OFF : ON MODE : SSB R/T : R/USB BAT : IND LOCAL/REM: REM PTT : R PA/CBP : PA MN/BP : MN ALC/1kHz VAR : 1 kHz VAR WHIP/DIP : DIP FREQUENCY: 16.0000 SCOPE : PHONE	(1) Use the test setup shown in fig. 4-9. (2) Tune the RF signal generator to 16.0010 MHz and adjust it to obtain a 100 mV CW test signal. (3) Turn the VOLUME potentiometer located on the front panel of the test fixture, until the distortion analyzer indicates an audio output of 2.45V. (4) Measure the distortion of the audio output. (5) Repeat steps (2) through (4) above with RF signals of 16.000350 and 16.002400 MHz.	N/A N/A N/A Less than 5%
5	Squelch a. Measurement	ON/OFF : ON MODE : SSB R/T : R/USB BAT : IND LOCAL/REM: REM PA/CBP : PA MN/BP : MN ALC/1kHz VAR : 1 kHz VAR WHIP/DIP : DIP FREQUENCY: 16.0000 SCOPE : PHONE MOD : 60%	(1) Use the test setup shown in fig. 4-10. (2) Tune the signal generator to 16.00050 MHz and adjust it to obtain a 0.7 microvolt test signal, modulated 55% by the external modulation signal provided by the test fixture. Use DC coupling at the external AM input. (3) Listen to the handset.	N/A N/A A 500-Hz tone, modulated in amplitude by a 5-Hz tone should be heard.

Table 4-5. Test and Alignment Procedures for the Receiver Section of the RT-936/PRC-174 (Cont'd.)

Item	Test	Test Fixture Control Settings	Procedure	Performance Standard
5	Cont'd.		(4) Set the MOD selector, located on the front panel of the test fixture, to 10%. Adjust the modulation index of the RF signal generator to 8% if necessary.	The receiver output is squelched after 2 to 4 seconds following reduction of modulation index to 8%.
	b. Adjustment of squelch circuit	Same as for a. above.	(1) Tune the RF signal generator to 16.00050 MHz and adjust it to obtain a 3 microvolt test signal modulated 17.5% by the external modulation signal provided by the test fixture. Use DC coupling at the external AM input. (2) Identify potentiometer RV1 on module AUDIO 1A2A5 (fig.4-5).	N/A.

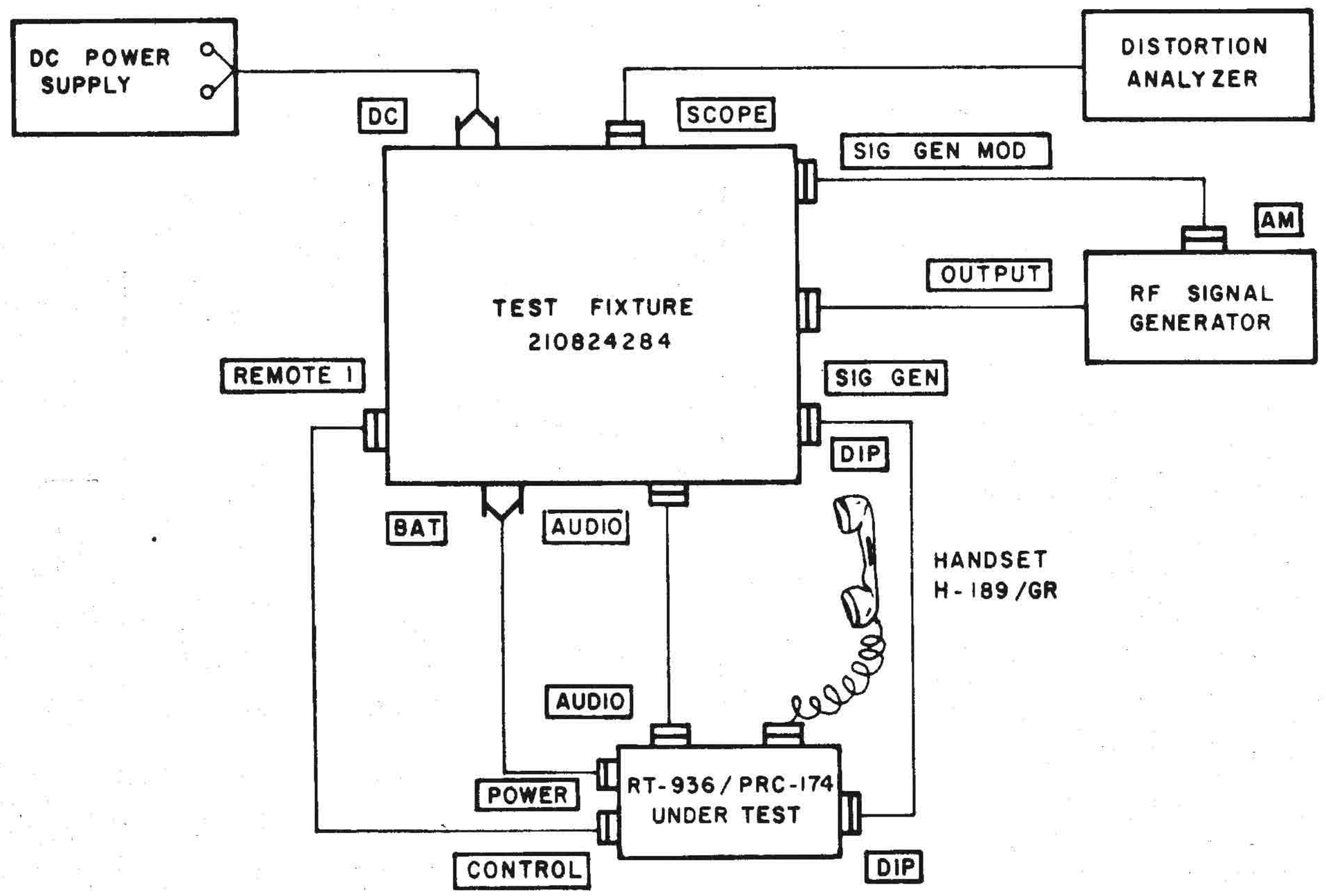


Fig. 4-10. Squelch Test and Adjustment Setup

Table 4-5. Test and Alignment Procedures for the Receiver Section of the RT-936/PRC-174

Item	Test	Test Fixture Control Settings	Procedure	Performance Standard
5	NOTE Perform if: 1. If the RT-936/ PRC-174 failed the squelch test. 2. After repair or replace-ment of module AUDIO 1A2A3.		(3) Listen to the handset; if the receiver output is squelched slowly adjust potentiometer RV1 until the squelch is disabled. (4) Reduce the modulation index to 8% and check that after 2 to 4 seconds the receiver is squel-ched. If necessary, readjust potentiometer RV1 until the re-quirements of steps (3) and (4) are both met.	N/A. N/A.

Table 4-6. Test and Alignment of Solid State Display, Alarms and indications of the RT-936/PRC-174

Item	Test	Test Fixture Control Settings	Procedure	Performance Standard
1	Received Signal Level Meter	ON/OFF : ON MODE : SSB R/T : R/USB BAT : IND LOCAL/REM: REM PTT : R PA/CBP : PA MN/BP : MN ALC/1kHz VAR : 1 kHz VAR WHIP/DIP : DIP FREQUENCY: 16.0000 SCOPE : PHONE	(1) Use the test setup shown in fig. 4-9. (2) Tune the RF signal genera-tor to 16.001 MHz and adjust it to obtain a 0.7 microvolt CW test signal. (3) Vary the amplitude of the RF test signal from 3 to 1000 microvolt and record the RF voltage at which each of the solid state display lamps turns on. L1 designates the leftmost lamp, and L5 desig-nates the rightmost lamp. (4) If the required perfor-mance is not attained, refer to Table 4-5, Item 2 for ad-justment instructions.	N/A N/A Lamp / Turn-on Thres-hold (uV) L1 3- 10 L2 10- 30 L3 30- 100 L4 100- 300 L5 300-1000 N/A.

Table 4-6. Test and Alignment of Solid State Display, Alarms and indications of the RT-936/PRC-174

<table>
<tr><th>Item</th><th>Test</th><th>Test Fixture Control Settings</th><th>Procedure</th><th>Performance Standard</th></tr>
<tr><td>2</td><td>Battery Voltage Indication and Alarm

a. Measurement</td><td>ON/OFF : ON
MODE : SSB
R/T : R/USB
BAT : IND
LOCAL/REM: REM
PTT : R
PA/CBP : PA
MN/BP : MN
ALC/1kHz VAR :
1 kHz VAR
WHIP/DIP : DIP
FREQUENCY: 16.0000
SCOPE : PHONE</td><td>(1) Use the test setup shown in fig. 4-9.
(2) Connect Handset, H-189/GR, to the free AUDIO connector of the RT-936/PRC-174.
(3) Reduce the supply voltage to 20 VDC.

(4) Set BAT selector on the test fixture to BAT.
(5) Slowly increase the supply voltage to 21 VDC.

CAUTION
Do not increase supply voltage above 32 V.

(6) Continue to increase slowly the supply voltage up to 27VDC and record the turn-on voltage for each lamp. L1 designates the leftmost lamp; L5 designates the rightmost.</td><td>N/A

N/A

All solid state display (SSB) lamps should flash together, and beeps should be heard in the earphone at a rate of approx. 1.2Hz.

The alarm indications should stop.

<table>
<tr><th>Illuminated Lamps</th><th>Turn-on Threshold (V)</th></tr>
<tr><td>L1</td><td>21.5 - 23.5</td></tr>
<tr><td>L1+L2</td><td>22.5 - 24.5</td></tr>
<tr><td>L1+L2+ L3</td><td>23.5 - 25.5</td></tr>
<tr><td>L1+L2+ L3+L4</td><td>24.5 - 26.5</td></tr>
<tr><td>L1+L2+ L3+L4+ L5</td><td>More than 26.5V</td></tr>
</table></td></tr>
<tr><td></td><td>b. Alignment</td><td>Same as a. above.</td><td>(1) If the required performance is not attained, adjust potentiometer R57 in module CONT 1A7.</td><td></td></tr>
</table>

Table 4-6. Test and Alignment of Solid State Display, Alarms and indications of the RT-936/PRC-174

Item	Test	Test Fixture Control Settings	Procedure	Performance Standard
3	Matching System Operation	ON/OFF : ON MODE : SSB BAT : IND LOCAL/REM: REM R/T : R/T USB PA/CBP : PA FREQUENCY: 2.0000 WHIP/DIP : WHIP ALC/1kHz VAR : 1 kHz VAR PTT : R MN/BP : MN	(1) Use the test setup shown in fig. 4-9. (2) Connect Handset, H-189/GR, to the free AUDIO connector of the RT-936/PRC-174. (3) Set the PTT switch on the test fixture to T.	N/A N/A SSD lamps should light sequentially from left to right and audio beeps should be heard in the earphone at a rate of approximately 1.2 Hz. The indications should stop after matching has been achieved.
		WARNING Do not touch the exposed contacts of the antenna connector of the unit-under-test. Dangerous RF voltages are present at these points.	(4) Return the PTT switch to R, then disconnect the whip simulator. (5) Set the PTT switch on the test fixture to T.	N/A After 15 ± 5 seconds, the matching indication should be replaced by the "no match" alarm: all SSD lamps flash together, and audio beeps are heard, at a rate of approximately 6 times per second.
			(6) Return the PTT switch to R, then disconnect the whip simulator.	The alarm indications should stop.

Table 4-6. Test and Alignment of Solid State Display, Alarms and indications of the RT-936/PRC-174

Item	Test	Test Fixture Control Settings	Procedure	Performance Standard
3	Cont'd.		(7) Press the NO MATCH push-button located on the front panel of the test fixture.	The "no-match" alarm indications should be displayed for the time the pushbutton is kept pressed.
4	Faulty Frequency Indication	ON/OFF : ON MODE : SSB BAT : IND LOCAL/REM: REM R/T : R/T USB PA/CBP : PA WHIP/DIP : WHIP ALC/1kHz VAR : 1 kHz VAR PTT : R MN/BP : MN	(1) Set the FREQUENCY selectors to 0.0 MHz. (2) Repeat the check at several other frequencies below 2.0 MHz. (3) Set the FREQUENCY selectors to 2.0000 MHz.	All SSD lamps flash together and audio beeps are heard, at a rate of approximately six times per second. Same results The alarm indications stop.
5	Transmitter Output Power Indication	ON/OFF : ON MODE : SSB BAT : IND LOCAL/REM: REM R/T : R/T USB PA/CBP : PA FREQUENCY: 16.0000 WHIP/DIP : WHIP ALC/1kHz VAR : 1 kHz VAR PTT : R MN/BP : MN AUDIO : 1kHzVAR ALC/AUDIO VAR: Fully counter-clockwise.	(1) Use the test setup shown in fig. 4-4. CAUTION At no stage of this test should the RF voltage indicated by the AC voltmeter be allowed to exceed 40V. (2) Set the PTT switch to T. (3) Slowly turn the ALC/1kHz VAR control clockwise and record the RF voltage (indicated on the AC voltmeter) at which each lamp of the solid state meter turns on. L1 designates the leftmost lamp; L5 designates the rightmost lamp. (4) Return the PTT switch to R. (5) Set the R/T selector on the test fixture to OFF.	N/A N/A Lamp / Turn-on Threshold(V) L1 4.35-6.9 L2 6.15-9.75 L3 7.9 -15.4 L4 13.7 -21.8 L5 19.5 -30.8 N/A N/A

d. Operational Check. After the test and alignment procedures detailed in Tables 4-4, 4-5 and 4-6 have been successfully carried out, perform an operational check of the RT-936/PRC-174 using the instructions given in Chapter 3, para. 3-10.a.

Section II. SIGNAL TRACING AND TROUBLESHOOTING TECHNIQUES FOR THE RT-936/PRC-174

4-4. General (fig. 4-11)

a. Scope. The scope of general-support signal tracing and troubleshooting of the RT-936/PRC-174 is to locate defective modules or sub-assemblies which cause malfunctions and failure to meet the performance standards listed in Table 4-4, 4-5, and 4-6.

b. Method. The test setups used for signal tracing in the RT-936/PRC-174 are shown in fig. 4-11.a (transmit mode) and fig. 4-11.b (receive mode). Upon detection of a failure, signal tracing is initiated, using the symptoms gathered during testing as a starting point. Before starting, the general troubleshooting procedures presented in para. 3-2 should be reviewed. The information gathered during the signal tracing procedure is then analyzed using the theory of operation presented in Chapter 2, and used to isolate the fault to a specific component.

c. Test Point Information. Para. 4-5 through 4-22 below provide typical values for DC voltages and AC signal levels and frequencies at the contacts of the module connectors and other critical points at a frequency of 16 MHz. These contacts are accessible, after removal of the bottom cover, at the rear side of the motherboard printed circuit.

CAUTION

Use extreme care when making test point measurements, to avoid shorts which could be caused by exposed test equipment probes. Tape or sleeve test probes and clips if necessary, to leave as little exposed surface as needed to make contact to the test point.

In order to gain safe access to module connectors, it is recommended to use extenders. The extenders must plug into the motherboard connector and physically raise the module-under-test above the other modules. Suitable extenders, which include easily accessible test points wired in parallel with each connector contact, can be obtained from the manufacturer.

d. Test Equipment. The test equipment used for signal tracing and troubleshooting is listed in Table 4-7.

Table 4-7. General Purpose Test Equipment for Signal Tracing and Troubleshooting

Item	Description	Manufacturer	Model
1	Frequency Counter	Hewlett-Packard	5328A, opt 010
2	RF Signal Generator	Hewlett-Packard	8640B
3	RF Voltmeter (incl. AC probe)	Hewlett-Packard	410C
4	AC Probe Adapter	Hewlett-Packard	11042A
5	Distortion Analyzer	Hewlett-Packard	333A
6	Spectrum Analyzer, Mainframe	Hewlett-Packard	141T
7	Spectrum Analyzer, IF Plug-In Unit	Hewlett-Packard	8552B
8	Spectrum Analyzer, RF Plug-In Unit	Hewlett-Packard	8553B

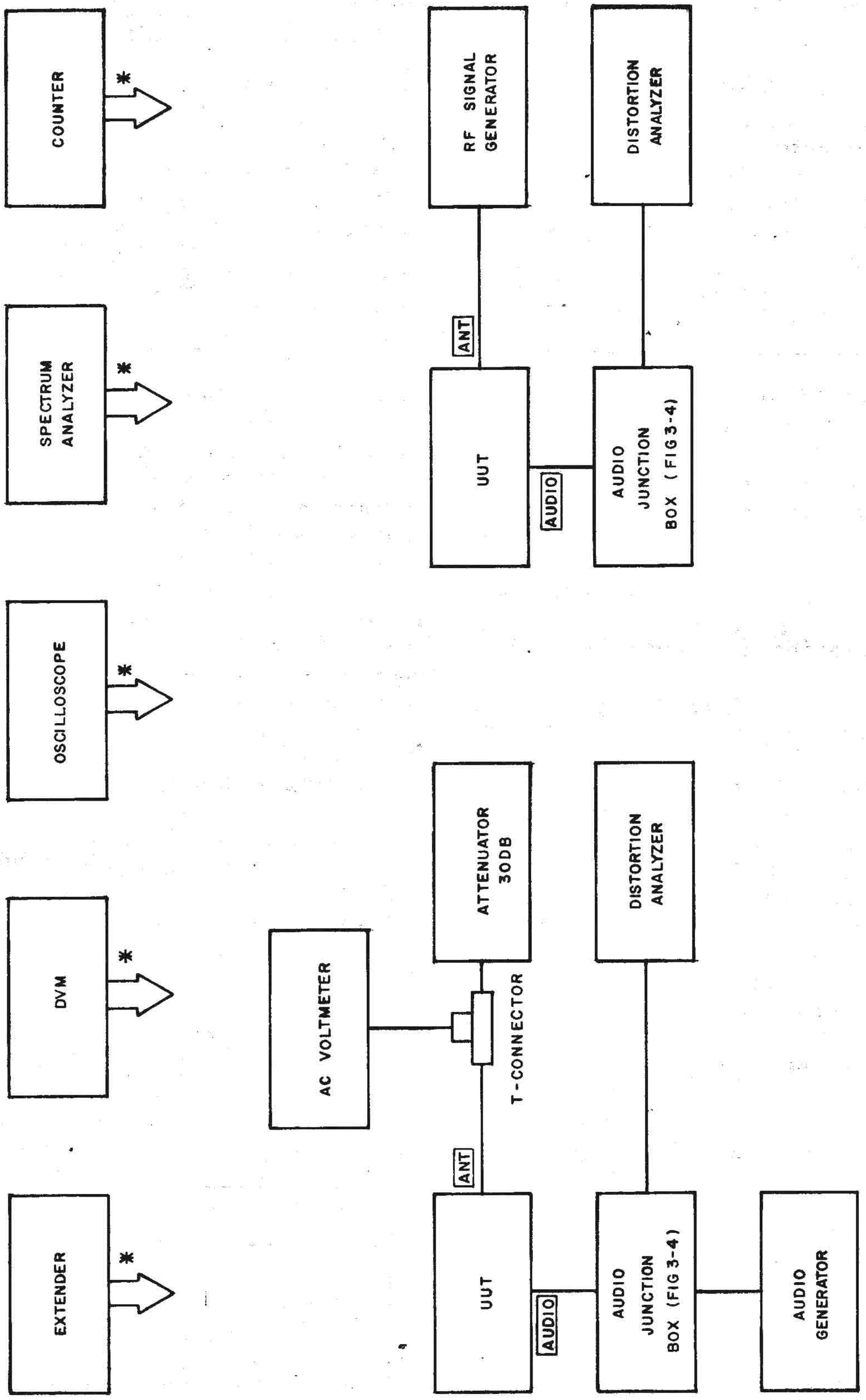


Fig. 4-11. Signal tracing and troubleshooting set-ups

Table 4-7. General Purpose Test Equipment for Signal Tracing and Troubleshooting (Cont'd.)

Item	Description	Manufacturer	Model
9	Multimeter	Fluke	8010A
10	Audio Oscillator	Hewlett-Packard	204D
11	Attenuator, 50 W, 30 dB	Bird	8321
12	Attenuator, Variable	Telonic	8143
13	Oscilloscope	Tektronix	465B
14	DC Power Supply	Hewlett-Packard	6274B
15	Spectrum Analyzer, RF Plug-In Unit	Hewlett-Packard	8554B

e. Standard Test Conditions. The following applies, unless otherwise specified:

(1) Assemble set-up and adjust the DC supply voltage to 26 VDC.

(2) Set the function selector to USB R/T.

(3) Set the battery control to IND.

(4) Operating frequency is 2.0000 MHz.

f. Standard Audio Inputs (used in the transmit mode).

(1) Mode selector at SSB and AM: connect audio generator to the AUDIO INPUT of the audio junction box, and adjust the signal to 5 mV, at 1 kHz.

(2) Mode selector at DATA: as para. (1) above, but change the input signal amplitude to 0.778 V.

(3) Mode selector at WCW/NCW: no input signal required.

g. Standard Operating Modes

(1) Transmit mode: set R/T switch on the audio junction box to TRANS.

(2) Receive mode: set R/T switch on the audio junction box to REC.

(3) Tune mode: disconnect the antenna and set the R/T switch on the audio junction box to TRANS (to achieve continuous tuning).

(4) NO-MATCH: after tuning at 2.0 MHz (as in (3) above).

(5) FONL: the state of the UUT, when the selected frequency is lower than 2.000 MHz.

4-5. Module PS 1A4

a. Test Conditions.

(1) Input voltage - 26 VDC.

(2) Equipment in receive mode, unless otherwise specified.

(3) Attenuator connected to DI-POLE connector.

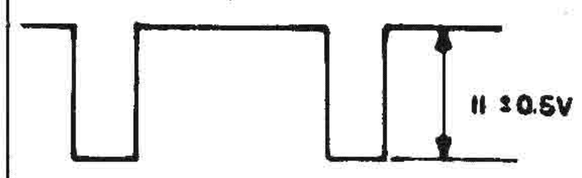
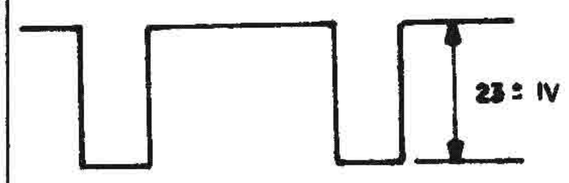
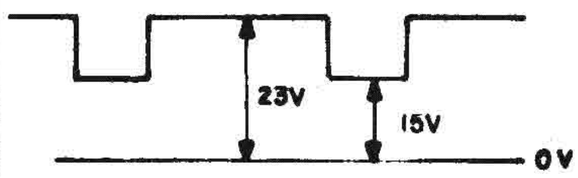
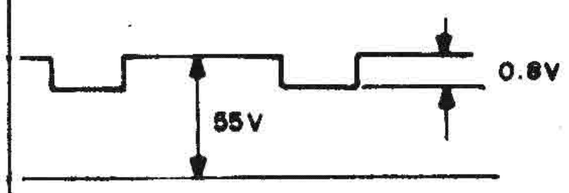
b. Recommended Test Equipment.

(1) Multimeter, Fluke model 8010A.

(2) Attenuator, Bird model 8321.

Test Point	Function	Measurement Method	Result
Q,R,T V,W (GND)	Ground	Use DVM	0 VDC
X,N,L (BAT IN)	26 VDC input voltage	Use DVM	26.0 VDC

Test Point	Function	Measurement Method	Result
Y (OFF CONT)	26 VDC	Use DVM	Equipment off: 0 VDC Equipment on: 26.0 VDC
P (ON CONT)	26 VDC	Use DVM	Equipment on: 0.3 VDC Equipment off: 26.0 VDC
E (+26V Un-filtered)	26 VDC	Use DVM	26.0 VDC
D (+26V Filtered)	Filtered 26 VDC to CONT 1A7, SNF 1A5A3 and USB 1A3A3	Use DVM	26.0 VDC
B (+15V)	15VDC to CONT 1A7 and VCP 1A3A1	Use DVM	15.0 ± 0.5 VDC
I (+12V)	12 VDC to 1A7, 1A2A2, 1A3A1, 1A3A2 1A3A3, 1A3A4, 1A3A1 1A3A2, 1A3A3, 1A3A5, 1A3A6, 1A5A2, 1A5A3	Use DVM	12.0 ± 0.5 VDC
C (+6V)	6 VDC to 1A2A1, 1A2A2, 1A3A1, 1A3A2, 1A3A3, 1A3A5	Use DVM	6 ± 0.2 VDC
F (-10V)	-10 VDC to 1A2A2, 1A2A3, 1A3A1	Use DVM	-10.0 ± 0.5 VDC
0 (PTT+15V)	15 VDC from CONT 1A7 in receive mode	Use DVM	Receive: 15 ± 0.5 VDC Transmit: 0 VDC
S,U (+ 34V)	34 VDC to PA 1A6 in transmit mode	Use DVM	Transmit: 34.5 ± 0.6 VDC Receive: 25.5 ± 0.5 VDC
H (TUNE)	Low level from LORD 1A5A2 during tuning	Use DVM	Tune: 0 VDC Other modes: 12 ± 0.5 VDC
J (RFS)	Control signal to MIX 1A2A1	AM transmit mode. Use DVM.	Less than 3 VDC.

Test Point	Function	Measurement Method	Result
A (EN-10V)	-10 VDC to 1A5A2	Use DVM	Transmit and tune: -10 ± 0.5 VDC Other modes: +3 to + 11 VDC
M (EN-CONT)	Control signal from LORD 1A5A2 during tuning	Use oscilloscope	Tune: Pulsed waveform with amplitude 11 ± 0.5 Vp-p Other modes: 0 VDC 
K (VEN 1)	Supply voltage to LORD 1A5A2 during tuning	Use oscilloscope	Tune: Pulsed waveform, amplitude 23 ± 1 Vp-p Other modes: 0.6 ± 0.2 VDC 
G (VEN 2)	26VDC to LORD 1A5A2 and SNF 1A5A3 during tuning	Use oscilloscope	Tune: Pulsed waveform, switching between 15 ± 0.5 V and 23 ± 1 V Other modes: 14.5 ± 0.7 VDC 
U5, pin 3	ERROR AMPLIFIER NON-INVERTING INPUT	Measure the level and waveform in transmit mode. Use oscilloscope in DC mode.	5.5 ± 0.5 V Pulse amplitude: approx. 0.8 V at 35 ± 7 kHz 
U5, pin 2	ERROR AMPLIFIER INVERTING INPUT	Measure the level and waveform in transmit mode Use oscilloscope in DC mode.	Same as for U5, pin 3
U5, pin 7	ERROR AMPLIFIER OUTPUT	Measure the level in transmit mode. Use DVM.	15.0 ± 1 VDC

4-6. Module PRE 1A2A4

a. Test Conditions.

(1) 5 mV at 1 kHz applied to the microphone input.

(2) RT-936/PRC-174 in transmit mode, unless otherwise specified.

(3) Attenuator connected to DI-POLE connector.

b. Recommended Test Equipment

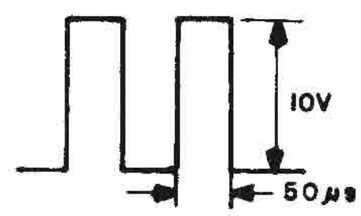
(1) Multimeter, Fluke model 8010A.

(2) Attenuator, Bird model 8321.

(3) Distortion analyzer, Hewlett-Packard model 333A.

(4) Oscilloscope, Tektronix model 465B.

Test Point	Function	Measurement Method	Result
L,M,N Q, H (GND)	Ground	Use DVM	Q VDC
D (+12V FIX)	12 VDC from PS 1A4	Use DVM	12±0.5 VDC
T,V (PTT PRE)	12 VDC from CONT 1A7 in transmit mode	Use DVM	Transmit: 12±0.5V Tune: 12±5V Receive: 0.7 V
I (PTT HANG)	Internal PTT line to CONT 1A7	Set mode selector to each of its positions. Use DVM.	Transmit: 0.7 V Tune: 0.7V Receive: 11.8 ± 0.5 V NCW, WCW: Time delay of 1.2±0.25 sec between rise of PTT line and rise of PTT HANG line.
K (PTT)	0 VDC from AUDIO connector in transmit mode	Use DVM	Transmit: 0.7 VDC Receive: 12 ± 0.5 VDC
U (TUNE)	Control signal from LORD 1A5A2	Use DVM	Transmit: 0.7 VDC Tune: 12 ± 0.5 VDC Receive: 0 VDC
S (AM CONT)	Control signal from the mode selector	Use DVM. Set mode selector to each of its positions.	AM mode: 10.5 ± 0.5 VDC Other modes: 0.7 VDC
E (AM TUNE)	AM and tune control signal to CONT 1A7 and FILTER 1A2A5	Set mode selector to each of its positions. Use DVM.	AM mode: 9.8 ± 0.5 VDC Tune: 10.5 ± 0.5 VDC Other modes: 0.7 VDC
J (AM TUNE TX)	AM and tune control signal to IF 1A2A2	Set mode selector to each of its positions. Use DVM.	Tune and AM mode: 12 ± 0.5 VDC Other modes: 0.7 VDC

Test Point	Function	Measurement Method	Result
B (12 V SSB)	SSB control signal from the mode selector	Set mode selector to each of its positions. Use DVM.	SSB mode: 11.8 ± 0.5 VDC Other modes: 0.7 VDC
G (CW)	WCW/NCW control signal from the mode selector	Set mode selector to each of its positions. Use DVM.	WCW/NCW: 10.7 ± 0.5 VDC Other modes: 0 VDC
W (DATA)	DATA control signal from mode selector	Set mode selector to each of its positions. Use DVM.	DATA mode: 11.2 VDC ± 0.5 Other modes: 0.7 VDC
F (MIC)	Audio input signal from PANEL 1A1	Use DVM.	5 mVAC
A (10 kHz)	10 kHz, square wave from REF 1A3A6	Use oscilloscope	WCW, NCW modes: Pulse width: 0.05 ms Pulse amplitude: approx. 10 V Other modes: No signal 
Y (DATA-IN)	Data input signal from AUDIO connector on front panel	Same as for point F	Same as for point F
C (MOD SIG)	Audio output signal to IF 1A2A2 and AUDIO 1A2A3	Set SSB transmit mode. Use oscilloscope and DVM.	Sinewave, 230-300 mVRMS
R (TX IN)	RF input signal from module MIXER 1A2A1	Transmit mode. Use oscilloscope.	AM : 70 ± 20 mVp-p SSB : 70 ± 20 mVp-p
X (RF PRE)	RF output signal to PA 1A6	Transmit AM mode, audio generator disconnected. Use oscilloscope.	3.5 ± 1.5 Vp-p
U2A, pin 11	Input of MOD SIGN transmission gate	Transmit mode. Use oscilloscope.	Sinewave, 0.8 ± 0.2 Vp-p

4-7. Module AUDIO 1A2A3

a. Test Conditions.

(1) SSB receive modes: RF signal of 100 mV at (test frequency +1 kHz) applied to DIPOLE connector.

(2) AM receive mode: RF signal of 100 mV at test frequency, modulated 30% by 1 kHz tone, applied to DIPOLE connector (3 V before attenuator).

(3) Transmit mode: 5 mV at 1 kHz applied to the microphone input.

(4) Attenuator permanently connected to DIPOLE connector.

b. Recommended Test Equipment.

(1) Multimeter, Fluke model 8010A.

(2) Attenuator, Bird model 8321.

(3) Distortion analyzer, Hewlett-Packard model 333A.

(4) Oscilloscope, Tektronix model 465B.

(5) RF signal generator, Hewlett-Packard model 8640B.

Test Point	Function	Measurement Method	Result
H, I, J L (GND)	Ground	Use DVM	0 VDC
S (+12V)	12 VDC from PS 1A4	Use DVM	12 ± 0.5 VDC
C (-10 V)	-10 VDC from PS 1A4	Use DVM	-10 ± 0.5 VDC
O (PTT +15V)	15 VDC from CONT 1A7 in receive mode	Use DVM	Receive: 15 ± 0.5 VDC Transmit: 0.7 VDC
E (SAVE)	12 VDC from battery control, to disable squelch circuits	Set battery control at each of its positions. Use DVM	SAVE mode: 12 ± 0.5 VDC Other modes: 0.7 VDC
V (AM CONT)	12 VDC from mode selector in AM mode	Set mode selector at each of its positions. Use DVM.	AM mode: 10.5 ± 0.5 VDC Other modes: 0.7 VDC
X (INH F3)	12 VDC from CONT 1A7	Set mode selector at each of its positions. Use DVM.	AM mode: 0 VDC Other modes: 12 ± 0.5 VDC
W (AM AUDIO)	AM audio input from IF 1A2A2	Select AM receive mode. Use oscilloscope to observe waveform. Use distortion analyzer to measure distortion.	350 ± 100 mVp-p, 1-kHz sinewave. Distortion: 5% max.
Y (SSB AUDIO)	SSB AUDIO input from IF 1A2A2	Select SSB receive mode. Use osciloscope and distortion analyzer.	SSB: 700 ± 100 mVp-p sinewave at 1 kHz. Distortion: 2% max.
P (VOLUME)	DC control voltage from the front panel VOLUME control	Use DVM	Volume control fully clockwise more than 10 VDC. Volume fully counterclockwise: less than 0.7 VDC.

Test Point	Function	Measurement Method	Result
R (PHONE)	Audio output signal to earphone	Receive mode. Use oscilloscope to observe waveform. Use distortion analyzer to measure level.	Volume control fully clockwise: 2.45 VAC or more at 1 kHz. Volume control fully counterclockwise: less than 100 mVAC.
A (FIX AUDIO)	Audio output signal to CONTROL connector	Use oscilloscope to observe waveform. Use distortion analyzer to measure level.	350 to 450 mVRMS sinewave at 1 kHz
U (SIGNALING)	Audio signal from module CONT 1A7 during tuning	Use oscilloscope	Bursts of 1 kHz during tuning
T (MOD SIGN)	Audio input signal from PRE 1A2A4 in transmit mode	Select SSB transmit mode. Use oscilloscope and DVM.	250 to 300 mVRMS at 1 kHz.
N (TX LEVEL)	Test point for checking control signal to transmission gate U5C	Use DVM	Transmit mode: 0 to 10 VDC, proportional to transmitter output power.
K or Q5/C (SQUELCH TP)	Test point for checking control signal to transmission gate U5C	Use SSB receive mode. Set RF generator for 3.0 uV at 16.0005 MHz. Tune the UUT to 16.0000 MHz. Adjust the volume control for +10dBm (2.45V) on the distortion analyzer. Set the audio generator to 5 Hz. Connect audio generator to EXT MOD input of RF generator. Set the AUDIO OUTPUT LEVEL to obtain 55% modulation. Connect DVM to collector of Q5 in the module and measure the output level. Change the modulation to 8% and measure again the output level with the DVM.	55% modulation: VCQ5 = 12V ± 0.5. 8% modulation: VCQ5 = OV
D (TP SIG)	Test point for checking level of rectified speech envelope	See test point K"	55% modulation: VD = 3.0 ± 1 VDC. 8% modulation VD = 0.7 ± 0.2 VDC.

Test Point	Function	Measurement Method	Result
B (TP NOISE)	Test point for checking level of rectified signal at the output of the noise path	See test point K	55% modulation: VB = 1.6 ± 0.3 V 8% modulation: VB = 1.45 ± 0.3 V
U5A/3		Use oscilloscope	0.7 ± 0.1 Vp-p CYCLE TIME: 1 ms
U5C/2		Use oscilloscope	2.5 ± 0.2 Vp-p CYCLE TIME: 1 ms
U2A/4		Set the battery control to SAVE and measure the voltage with the DVM.	+6.5 ± 0.5 VDC .
U2A/11		See U2A/4	-6.5 ± 0.5 VDC .

4-8. Module IF 1A2A2

a. Test Conditions.

(1) SSB receive modes: RF signal of 100 uV at (test frequency +1 kHz) applied to DIPOLE connector (3 mV before attenuator).

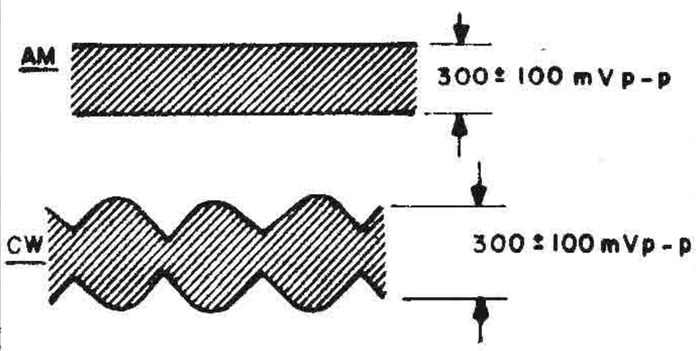
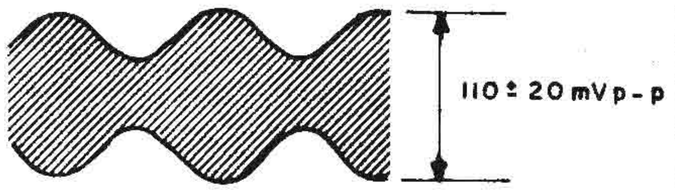
(2) AM receive modes: RF signal of 100 uV modulated 30% by 1 kHz tone applied to DIPOLE connector (3 mV before attenuator).

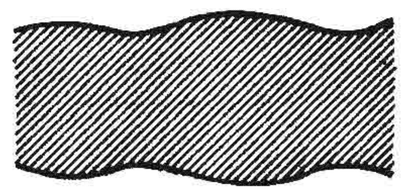
(3) Transmit mode: 5mV at 1 kHz applied to the microphone input.

b. Recommended Test Equipment.

(1) Multimeter, Fluke model 8000A.
(2) Attenuator, Bird model 8321.
(3) Distortion analyzer, Hewlett-Packard Model 333A.
(4) Oscilloscope, Tektronix model 465B.
(5) RF signal generator, Hewlett-Packard model 8640B.
(6) Frequency counter, Hewlett-Packard model 5328A, opt 010.

Test Point	Function	Measurement Method	Result
P, N, L, J, H, D, R (GND)	Ground	Use DVM	0 VDC
T (+12V FIX)	12 VDC from PS 1A4	Use DVM	12 ± 0.5 VDC
Q (+6V)	6 VDC from PS 1A4	Use DVM	6 ± 0.2 VDC

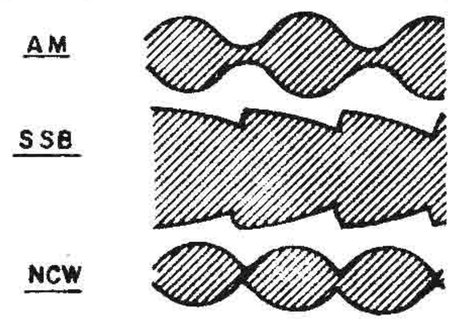
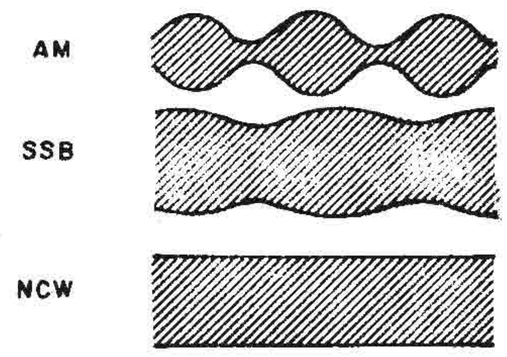
Test Point	Function	Measurement Method	Result
M,K (-10V)	-10 VDC from PS 1A4	Use DVM	-10 ± 0.5 VDC
A (PTT PRE)	12 VDC from CONT 1A7 in transmit mode	Use DVM	Transmit: 12 ±0.5 VDC Tune: 12 ±0.5 VDC Receive: 0.7 VDC
B (AM TUNE TX)	AM/tune control signal from PRE 1A2A4	Transmit mode. Use DVM.	Tune and AM modes: 12 ± 0.5 VDC Other modes: 0.7 VDC
F (MOD SIGN)	Audio input signal from PRE 1A2A4	AM transmit mode. Use oscilloscope and DVM.	230 to 300 mVRMS sinewave at 1 kHz
C (5.25 MHz)	5.25 MHz from REF 1A3A6, serving as the IF carrier frequency	Select SSB receive mode. Use oscilloscope with low capacitance probe to observe waveform and measure its level, and counter to check frequency.	250-300 mVp-p sinewave at 5.25 MHz
U (IF MOD DETEC)	IF output signal to FILTER 1A2A5	Set transmit mode. Disconnect aud. generator. Use oscilloscope with low capacitance probe to observe waveforms and measure levels	AM and CW modes: 200 to 400 mVp-p at 5.25 MHz. 
T1, pin 4	IF amplifier	AM receive: 100 mV RF signal, 30% modulation at 1 kHz. Use oscilloscope.	Sinewave modulated by 1 kHz. Amplitude: 110 ± 20 mVp-p 
Q7, pin C	Supply line to IF amplifier	Use DVM to measure voltage in receive mode.	5.6 ± 0.2 VDC

Test Point	Function	Measurement Method	Result
U5C, pin b(13)	AGC detector input	SSB receive mode. Use oscilloscope to measure the level.	130 ± 20 mVp-p sinewave at 5.25 MHz 
U4, pin 8	Balanced demodulator input	SSB receive mode. Use oscilloscope.	220±20 mVp-p sinewave at 5.25 MHz
U3, pin 7	Balanced modulator input	Transmit mode. Use oscilloscope.	250-300 mVp-p sinewave at 5.25 MHz in SSB mode.
Y (PULSE)	12 VDC from CONT 1A7 to discharge C48	Use DVM	Receive: 0.35 ± 0.15VDC Transmit: 7.5 ± 0.5 VDC
S DATA	Data control signal from mode selector for decreasing AGC response time.	Set mode selector to each of its positions. Use DVM for measurements.	Data mode: 11.0 ± 0.5 VDC Other modes: 0 ± 1.0 VDC
U (IF in)	IF input signal from FILTER 1A2A5	Receive mode Adjust RF generator to 0.5V Use oscilloscope.	AM mode: 20 ± 5 mVp-p SSB modes: 14 ± 4 mVp-p
W (AM AUDIO)	AM output signal to AUDIO 1A2A3	Select AM receive mode. Use oscilloscope.	350 ± 100 mVp-p at 1kHz
E (SSB AUDIO)	SSB output signal to AUDIO 1A2A3	Select SSB receive mode. Use oscilloscope.	700 ± 100 mV at 1kHz
I,O (AGC IF)	AGC voltage to module MIXER 1A2A1 in SSB mode	Select SSB receive mode. Vary RF generator output level from 10 microV to 0.5V. Use DVM.	Varies from 0.5 to 4.5 VDC
G (S METER)	Control voltage to CONT 1A7 for display of RF input level	See test points I,O.	S METER voltage changes from 0.1 to 8 VDC
X (TP AGC)	Test point for internal AGC voltage	Receive mode. Use DVM	Approx. 2.54 VDC

4-9. Module FILTER 1A2A5

a. Test Conditions.
(1) Transmit mode: 5mVAC at 1 kHz applied to the microphone input.

b. Recommended Test Equipment.
(1) Multimeter, Fluke model 8000A.
(2) Attenuator, Bird model 8321.
(3) Distortion analyzer, Hewlett-Packard Model 333A.
(4) Oscilloscope, Tektronix model 465B.
(5) Frequency counter, Hewlett-Packard model 5328A, opt 010.

Test Point	Function	Measurement Method	Result
B,C,D F,G,H J,K,L N,O,P (GND)	Ground	Use DVM	0 VDC
M (AM TUNE)	AM/tune control signal from PRE 1A2A4	Set mode selector to each of its position. Use DVM to measure DC voltage.	Tune and AM modes: 9.5 ± 1 VDC Other modes: 0 VDC
I (SSB CONT)	WCW, DATA, SSB control signal from CONT 1A7	Use DVM	SSB, WCW, DATA modes: 9.5 ± 1 VDC Other modes 0 VDC
E (NCW)	NCW control signal from CONT 1A7	Use DVM	NCW: 9.5 ± 1 VDC Other modes: 0 VDC
Q (IF MOD DET IN/OUT)	Input IF signal from IF 1A2A2	Sequentially set function selector to AM,SSB and NCW modes. Use oscilloscope and frequency counter for measurements in transmit mode.	AM: 450 ± 100 mVp-p at 5.25 MHz modulated by 1 kHz. SSB: 300 ± 50 mVp-p, 5.25MHz NCW: 270 ± 50 mVp-p, 5.25MHz 
A (MOD IN OUT/IN)	Output IF signal to MIXER 1A2A1	Same as for test point Q	AM: 430 ± 100 mVp-p at 5.25 MHz modulated by 1 kHz SSB: 120 ± 20 mVp-p, 5.25 MHz NCW: 120 ± 20 mVp-p, 5.25 MHz 

4-10. Module MIXER 1A2A1

a. Test Conditions.

(1) Receive mode: 3mV RF signal at (test frequency ± 1 kHz) applied to the DIPOLE connector (100 mV before attenuator).

(2) Transmit mode: 5mV at 1 kHz applied to the microphone input.

(3) SSB/USB operation mode.

b. Recommended Test Equipment.

(1) Multimeter, Fluke model 8010A.

(2) Attenuator, Bird model 8321.

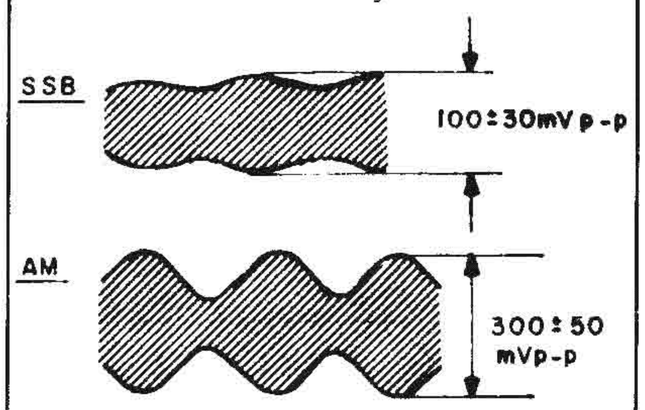
(3) Distortion analyzer, Hewlett-Packard Model 333A.

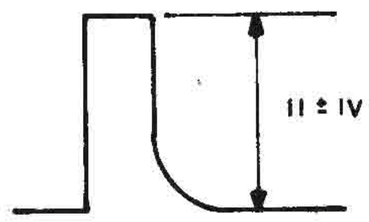
(4) Oscilloscope, Tektronix model 465B.

(5) RF signal generator, Hewlett-Packard model 8640B.

(6) Frequency counter, Hewlett-Packard model 5328A, opt 010.

(7) Spectrum analyzer, Hewlett-Packard 141T/8552B/8553B/8554B.

Test Point	Function	Measurement Method	Result
S (+6V)	6 VDC from PS 1A4	Use DVM	6 ± 0.2 VDC
C,Y (PTT 12V)	12 VDC from CONT 1A7 in transmit mode	Use DVM	Transmit: 11.5 ± 0.5 V Tune: 11.5 ± 0.5 V Receive: 0.4 ± 0.1 V
X (12V FIX)	12 VDC from PS1A4	Use DVM	12 ± 0.5 VDC
J22 (F2)	RF signal at 114.6 (USB) or 104.1 MHz (LSB) from USB 1A3A3	Set function selector to USB R/T and then to LSB R/T. Measure with spectrum analyzer.	USB mode: +2 to -4 dBm RF signal at 114.6 MHz LSB mode: +2 to -4dBm RF signal at 104.1 MHz
J21 (F1)	RF signal from VCP 1A3A1	Use spectrum analyzer.	+6 to -2 dBm RF signal at (test frequency +109.35MHz)
G (MOD IN)	Input IF signal from FILTER 1A2A5	Receive mode. Use oscilloscope.	SSB = 100 ± 30 mVp-p AM = 300 ± 50 mVp-p modulated by 1 kHz 
K (TX OUT)	Output RF signal	Measure in transmit mode. Check the amplification of the RF signal at operating frequency, relative to IF input.Use spectrum analyzer.	RF signal at operating frequency signal is amplified by 6 dB or more relative to IF input signal.

Test Point	Function	Measurement Method	Result
M (ALC)	ALC signal from SNF 1A5A3	Select DATA transmit mode. Change audio input from 0 to 1 V. Use DVM.	0.1 to 1 VDC
I (RFS)	Control signal from LORD 1A5A2 and from PS 1A4	Change frequency by 1 MHz or more by means of frequency selector. Use oscilloscope to observe short pulse at pin I, and spectrum analyzer to measure RF signal at pin K during the short pulse.	One short (approx. 10msec) pulse with amplitude +11 ± 1V RF signal at pin K is attenuated down to noise level 
T2/PIN 4	Output MIX No.1	Measure in transmit mode with spectrum analyzer.	-22 ± 2 dBm at 109.35 MHz
T2/PIN 1	Output MIX No.2	Measure in transmit mode with spectrum analyzer.	-22 ± 2 dBm at 109.35 MHz
J20 (RF in)	Input RF signal from SNF 1A2A5	Change output level of signal generator to achieve -60 dBm. Use spectrum analyzer.	
G (REC OUT)	Output RF signal to FILTER 1A2A5	Select SSB receive mode. RF input as for test point J20. Remove IF 1A2A2 to prevent AGC influence. Use spectrum analyzer.	IF signal at 5.25 MHz Amplitude: 13 ± 3 dBm
E (DC TP)	Test point for measurement of DC voltage in receive mode	Use DVM.	Receive: 9.2 ± 0.2 VDC Transmit: 0 VDC.
T6/PIN 1	Output MIX No.1	As for test point G	-45 ± 5 dBm at 109.35 MHz
T7/PIN 1	Input MIX No.2	As for test point G	-45 ± 5 dBm at 109.35 MHz
T10/2	F1 output amplifier	As for test point G	+2 ± 3 dBm at 111.35 MHz
T11/2	F2 output amplifier	As for test point G	-6 ± 3 dBm at 114.6 MHz

4-11. Module PA 1A6

a. Test Conditions.

(1) Transmit DATA/USB mode: with 0.775V at 1 kHz applied to the microphone line.

b. Recommended Test Equipment.

(1) Multimeter, Fluke model 8010A.
(2) Attenuator, Bird model 8321.
(3) Oscilloscope, Tektronix model 465B.
(4) AC voltmeter, Hewlett-Packard model 410C.

Test Point	Function	Measurement Method	Result
A	26 V unfiltered	Use DVM	26 VDC
B, D, F, H, Q, J, L, N	Ground	Use DVM	0 VDC
C	15 V	Use DVM	15 ± 0.5 VDC
I, G	34 V	Use DVM	33.6 ± 0.7 VDC
K, M	PTT 6 V	Use DVM	6 ± 0.2 VDC
P	RF PRE - RF input	Use oscilloscope	3.5 ± 1.5 Vp-p sinewave at 2 MHz
J26	RF OUT	Use oscilloscope	100 ± 15 Vp-p sinewave at 2 MHz
Q6(G)		Use DVM	4.3 ± 0.5 VDC
Q4(B), Q5(B)		In SSB mode. Audio generator disconnected. Use DVM.	0.6 ± 0.15 VDC
Q4(C), Q5(C)		As above	34 ± 0.5 V
C10, C11		Use oscilloscope	7 ± 1 Vp-p sinewave at 2 MHz
O	BP - bypass. RF input is connected to RF output by means of K1	On the panel, connect P3-56 to P3-66 (GROUND). Use DVM and oscilloscope.	0.7 VDC RF OUTPUT is equal to RF INPUT

4-12. Matching Network MN 1A5A1

a. Test Conditions.

(1) Transmit DATA/USB mode: with 0.775V at 1 kHz applied to the microphone line.

b. Recommended Test Equipment.

(1) Multimeter, Fluke model 8010A.
(2) Attenuator, Bird model 8321.
(3) Oscilloscope, Tektronix model 465B.
(4) AC voltmeter, Hewlett-Packard model 410C.

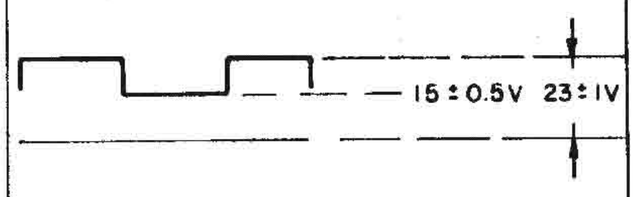
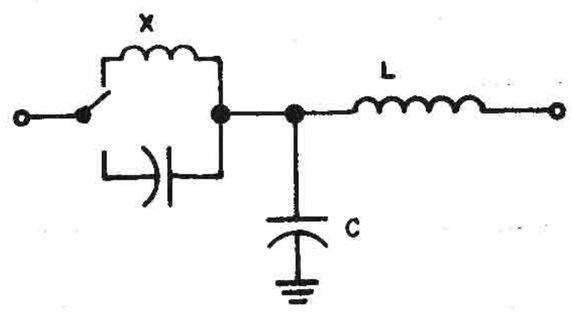
Test Point	Function	Measurement Method	Result
B VEN-2	Supply voltage for relays from PS 1A4	Select tune mode. Use oscilloscope.	Pulsed waveform with amplitude of 11±0.5Vp-p
D VEN-1	Supply voltage for latching relays from module PS 1A4	Select tune mode. Use oscilloscope.	Pulsed waveform, switching between two levels: 15±0.5V and 23±1V 
Various points on the module	Connection of different combinations of coils and capacitors in accordance with selected frequency	Connect whip simulator to the UUT. Change frequency and measure with DVM in position LO OHM the resistance of coils and its connections. Take into account that CD-8 is not shorted above 21 MHz (L-branch). Check connection of band-capacitors to ground (C-branch). 	1.L-branch: see Table 3 2.C-branch: see Table 1 TABLE 1 2 MHz - CB1 2.4 MHz - CB2 3.4 MHz - CB3 4.8 MHz - CB4 7.0 MHz - CB5 10.0 MHz - CB6 14.4 MHz - CB7 21.0 MHz - CB8 3.X-branch: The coils are connected at all frequencies, as in Table 2. TABLE 2 L2-1 - 60 mohm L2-2 - 46 mohm L2-3 - 30 mohm L2-4 - 19 mohm L2-5 - 9 mohm L2-6 - 5 mohm L2-7 - 3 mohm L2-8 - 1 mohm

TABLE 3

Coil	Resistance in mohm		Frequency Range (MHz)						
	Connected/ Disconnected	Shorted	2-2.3	2.4-3.3	3.4-4.7	4.8-6.9	7.0-9.9	10.0-14.3	14.4-29.9
L1-1	300	15	+	-	-	-	-	-	-
L1-2	250	19	+	+	-	-	-	-	-
L1-3	120		-	-	-	-	-	-	-

Test Point	Function	Measurement Method	Result

TABLE 3 (Cont'd)

Coil	Resistance in mohm		Frequency Range (MHz)						
	Connected/ Disconnected	Shorted	2-2.3	2.4-3.3	3.4-4.7	4.8-6.9	7.0-9.9	10.0-14.3	14.4-29.9
L1-4	110		+	-	+	-	-	-	-
L1-5	75		+	+	+	+	-	-	-
L1-6	80		-	+	+	-	-	-	-
L1-7	55	30	-	-	+	+	+	+	-
L1-8	32	20	+	+	-	+	+	+	-
L1-9	20	12	-	-	-	-	+	+	-
L1-10	14	12	-	-	+	-	+	+	+
L1-11	8	6	-	-	-	+	-	-	-
L1-12		1	-	-	-	-	-	-	-
L1-13	2	1	-	-	-	-	+	+	+

Note: + : coil connected into the network.
- : coil disconnected from the network or shorted.

4-13. Module SNF 1A5A3 and 6-dB Attenuator

a. Test Conditions.

(1) Transmit DATA/USB mode: 0.775V at 1 kHz applied to the microphone line.

b. Recommended Test Equipment.
(1) Multimeter, Fluke model 8010A.
(2) Attenuator, Bird model 8321.
(3) Oscilloscope, Tektronix model 465B.
(4) AC voltmeter, Hewlett-Packard model 410C.

Test Point	Function	Measurement Method	Result
P, X	Ground	Use DVM	0 VDC
H, L, C J, G	FL1 to FL5, respectively	See test points R, M, j, h, f (J3) of LORD 1A5A2.	
F, Q	X61 - control voltage from PANEL 1A1	Use DVM	9.5 ± 1 VDC
A	PTT 12 V	Use DVM	Transmit and tune: 12 ± 0.5 VDC Receive: 0 VDC
R	-10 VEN	Use DVM	Transmit and tune: -10 ± 0.5 VDC Receive: +3 to +11 VDC

Test Point	Function	Measurement Method	Result
Y	Φ - Phase detector output	Use oscilloscope	Tune: pulsed waveform, amplitude approx 12Vp-p Other modes: 6.5±0.5VDC
W	R - detector output	Use oscilloscope	Same as for test point Y
U	LT - VSWR - detector low threshold	Use oscilloscope	Tune: pulsed waveform, amplitude approx 12Vp-p Other modes: 1.2±0.7VDC
S	HT - VSWR - detector high threshold	Use oscilloscope	Same as for test point Y
B	RF signal output in receive to MIX 1A2A1	Receive mode. Adjust RF generator OUTPUT LEVEL to -20 dBm. Select frequency for test points R, M, j, h, f (J3) of LORD 1A5A2 and measure the RF level with spectrum analyzer (Range of FL6: 20 - 29.9 MHz)	-21 to -24 dBm
I	TUNE - control voltage from LORD 1A5A2	Use DVM.	Tune: 12 ± 0.5 VDC Other modes: 0 VDC
K	TX LEVEL	In DATA transmit mode, change audio input from 0 to 0.8VRMS. Use DVM.	Approx. 0.1 to 8.5 VDC
E	VEN 2	See test point G of PS 1A4	
V	PH-CONT control voltage from LORD	Select two frequencies: 1 - lower than 10 MHz, 2 - higher than 10 MHz. Use oscilloscope.	Tune: 1 - pulsed waveform switching between two levels: from 15V or 23V to approx. 0-2 VDC. Other modes: 14.5±0.5VDC
M	PTT PRE +12V	Use DVM.	Transmit and tune: 11.5 ± 0.5 VDC Other modes: 0 VDC
N	ALC - automatic level control	In DATA transmit mode, change audio input from 0 to 0.8 VRMS. Use DVM.	Approx. 0.1 to 0.9 VDC
P	BP - bypass	On the panel, connect P56 and P-66 (GND). Use DVM.	0 VDC

Test Point	Function	Measurement Method	Result
U2A/3	Input of ALC amplifier	Measure with DVM in transmit mode.	6.5 ± 0.5 VDC
U2B/10	Input of second stage of ALC amplifier	In transmit mode. Use DVM.	2.0 ± 0.3 VDC
P23, P24	6-dB attenuator connection	Use spectrum analyzer with divider AC probe	The difference between two levels is 6 ± 1.5dB.

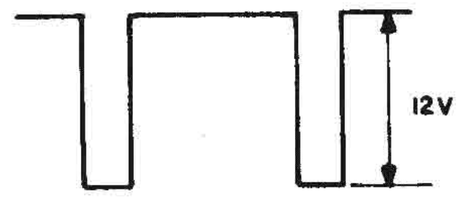
4-14. Module LORD 1A5A2

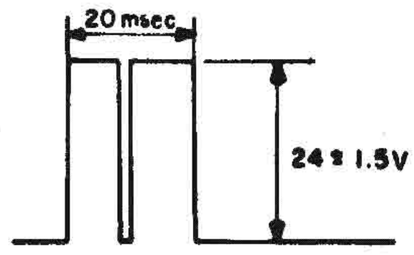
a. Test Conditions.

(1) Transmit DATA/USB mode: 0.775V at 1 kHz applied to the microphone line.

b. Recommended Test Equipment.

(1) Multimeter, Fluke model 8010A.
(2) Attenuator, Bird model 8321.
(3) Oscilloscope, Tektronix model 465B.
(4) AC voltmeter, Hewlett-Packard model 410C.

Test Point	Function	Measurement Method	Result
L (J3)	+12 VDC	Use DVM	12 ± 0.5 VDC
W (J3)	-10 VEN	Use DVM	Tune and transmit: -10 ± 0.5 VDC Receive: +3 to +11 VDC
F (J3)	ENC - control voltage to PS.	Use oscilloscope.	Tune: pulsed waveform with repetition rate of approx. 80 Hz and amplitude of 12 ± 0.5 Vp-p. Other modes: 0VDC 
P,A	VEN 1, VEN 2	See MN 1A5A1, D and B.	
B (J3)	LT - indication voltage from SNF 1A5A3	Use oscilloscope.	Tune: pulsed waveform with amplitude of approx. 12 Vp-p. Other modes: 1.2 ± 0.7 VDC 

Test Point	Function	Measurement Method	Result
D (J3)	HT - indication voltage from SNF 1A5A3	Use oscilloscope.	Tune: pulsed waveform of approx. 12 Vp-p Other modes: 6.5 ± 0.5 VDC
G (J3)	R - indication voltage from SNF 1A5A3	Use oscilloscope.	Same as test point D.
C (J3)	Indication voltage from SNF 1A5A3	Use oscilloscope.	As in T.P. G
E (J3)	Tune	Use DVM.	Tune: 12 ± 0.5 VDC Other modes: - 0 VDC
I	PH CONT	See test point V in SNF 1A5A3.	
S, U (J2)	DIP (D/W) Dipole or whip antenna selection latching relay	1. Whip simulator is connected 2. Whip simulator is disconnected. Measure with oscilloscope when turning the UUT on.	1. Single pulse of approx. 20 msec at 24 ± 1.5V at test point S (Y2), 0 VDC at test point U (X2). 2. As above, but the test point will be changed. 
e (J3)	PTT LORD 12 VDC from CONT 1A7	Measure with DVM in transmit mode.	11.0 ± 1 VDC
R,M,j,h, f (J3)	FL1, FL2, FL3, FL4, FL5 respectively	Change frequency. Measure with DVM.	2.0 to 2.9MHz - FL1 (11.5 + 1VDC) 3.0 to 4.9MHz - FL2 (11.5 + 1VDC) 5.0 to 7.9MHz - FL3 (11.5 + 1VDC) 8.0 to 11.9MHz - FL4 (11.5 + 1VDC) 12.0 to 19.9 MHz - FL5 (0VDC)

Test Point	Function	Measurement Method	Result
Test points at connector J1 or J2	Control voltage for MN 1A5A1 relays	Change frequency and check that appropriate connection of relays contacts is achieved (Refer to Table 1, Table 2, Table 3 of para 4-12 and fig. 4-37. For latching relays, observe the waveform when turning the UUT on. Use oscilloscope.	For non-latching relays: connected: 0.5 VDC disconnected: 14.5 ± 0.5 VDC For latching relays: connected: Pin Y2 (for half crystal can relays) and pin 10 (for TO-5 relays) - 0VDC Pin X2 (for half-crystal can relays) and pin 5 (for TO-5 relays) 20-msec pulse at 24 ± 1.5Vp-p disconnected: Pin Y2 and pin 10 - single 20-msec pulse at 24±1.5Vp-p. Pin X2 and pin 5 - 0VDC.
h, E (J1)	BP-control voltage to KBP in MN 1A5A1	Same as for test point U.	1. Single pulse of approx. 20 msec at test point E, 0 VDC - at test point h 2. Single pulse of approx. 20 msec at test point h, 0 VDC - at test point h

4-15. Module CONT 1A7

a. Test Conditions.

(1) Receive mode: 3mV RF signal at (test frequency +1 kHz) applied to the DIPOLE connector (100 mV before attenuator).

(2) Transmit mode: 5mV at 1 kHz applied to the microphone input.

(3) SSB/USB operation mode.

b. Recommended Test Equipment.

(1) Multimeter, Fluke model 8010A.

(2) Attenuator, Bird model 8321.

(3) Distortion analyzer, Hewlett-Packard model 333A.

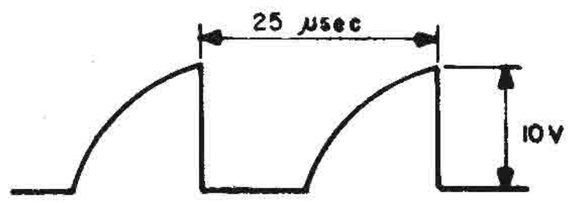
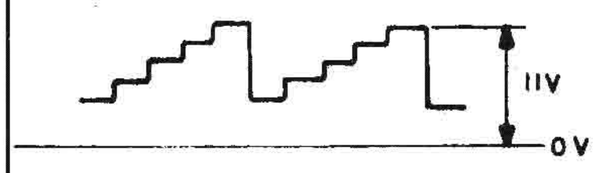
(4) Oscilloscope, Tektronix model 465B.

(5) AC voltmeter, Hewlett-Packard model 410C.

Test Point	Function	Measurement Method	Result
f,g (GND)	Ground	Use DVM	0 VDC
I (+26V)	26 VDC from PS 1A4	Use DVM	26.0 VDC

Test Point	Function	Measurement Method	Result
A (+12 VA)	12 VDC from PS 1A4	Use DVM	12 ± 0.5 VDC
a (+6V)	6 VDC from PS 1A4	Use DVM	6 ± 0.2 VDC
H (PTT HANG)	12 VDC from PRE 1A2A4 in receive mode	Use DVM	Receive: 11.8 ± 0.5 VDC Transmit: 0.5 VDC
J (R/T)	R/T control signal from function selector	Set function selector to each of its positions. Measure with DVM.	USB R/T, LSB R/T: 0.5VDC Other modes: 11.8±0.5VDC
L (SF)	High level from LORD 1A5A2 when turned on	Measure with DVM.	Turn on: 12 ± 0.5 VDC Other conditions: 0 VDC
R (FO, NL)	High level when synthesizer is unlocked or selected frequency is lower than 2.000 MHz	Select one frequency lower, and the other one higher than 2.0 MHz. Measure with Use DVM.	Selected frequency lower than 2.0 MHz: 11.5 ± 0.5 VDC. Other conditions: 0 VDC
U (PTT LORD)	12 VDC to LORD 1A5A2 in transmit mode	Use DVM	Receive: 0 VDC Transmit 11.8 ± 0.5 VDC
W (PTT +12V)	12 VDC to PANEL 1A1 and SNF 1A5A3 in transmit mode	Use DVM	Receive: 0 VDC Transmit: 10.8 ± 0.5 VDC
Y (PTT +6V)	12 VDC to PA 1A6 in transmit mode	Use DVM	Receive:0 VDC Transmit:+5.9 ± 0.2 VDC
C (PTT +15V)	15 VDC to PS 1A4, MIXER 1A2A1 and AUDIO 1A2A3 in transmit mode	Use DVM	Receive: 15 ± 0.5 VDC Transmit: 0 VDC
Q (PTT PRE)	12 VDC to 1A2A4, 1A2A1, 1A2A2, 1A5A3 in transmit mode	Use DVM	Receive: 0.4 VDC approx. Transmit: 11.6 ± 0.5 VDC
X (AM TUNE)	AM/tune control signal from PRE 1A2A4	Use DVM	AM and tune: 9.7±0.5 VDC Other modes: 0 VDC
V (NCW)	NCW control signal from mode selector	Use DVM	NCW: 11.4 ± 0.5 VDC Other modes: 0 VDC

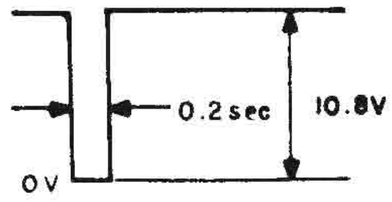
Test Point	Function	Measurement Method	Result
T (SSB CONT)	SSB/WCW/DATA control signal to FILTER 1A2A5	Use DVM	SSB,NCW, and DATA: 12 ± 0.5 VDC. Other modes: 0 VDC
b (INH F3)	Inhibit signal to AUDIO 1A2A3 and REF 1A3A6 in AM receive mode	Use DVM	AM receive mode: 0 VDC Other modes: 12 ± 0.5 VDC
M (TX LEVEL)	Control signal from module SNF 1A5A3 for display of RF output level in transmite mode	Use DVM	Transmit mode (AM,NCW) 7 V ± 2 V
S (S METER)	Control voltage from module IF 1A2A2 for display of RF input level in receive mode	Select receive mode. Vary RF input signal from 10 microV to 1.0 V and check that S METER voltage changes proportionally. Measure the voltage with DVM.	The voltage changes betweeen approx. 0.1 to 8V
B (IND)	IND control signal from battery control	Set battery control to each of its positions. Measure the voltage with DVM.	IND: 11.4±0.05VDC Other positions: 0 VDC
d (BAT CHK)	BAT CHK control signal from battery control	Set battery control to each of its positions. Measure the voltage with DVM.	BAT: 10.8 ± 0.5 VDC Other positions: 0 VDC
K (LOW BAT)	LOW BAT control signal output	Use DVM	12 ± 0.5 VDC when battery voltage is below 20 VDC, and 0VDC when above 21 VDC
N (TUNE)	Tune control signal from LORD 1A5A2	Use DVM	Tune: 11.2 ± 0.5 VDC Transmit: 0 VDC Receive: 0 VDC
P (NM)	"No matching" indication signal from LORD 1A5A2	Use DVM	11.4 ± 0.5 VDC when matching is not achieved, less than 0.7 VDC when matching is completed.
Z (SIGNALING)	Indication to AUDIO 1A2A3 during tuning	Use oscilloscope	Bursts of 1kHz tone during tuning at 3 ± 0.5 Vp-p

Test Point	Function	Measurement Method	Result
E,F,G D,C (L1,L2, L3,L4)	LED drivers	Use oscilloscope	Less than 0.1 VDC when corresponding LED should light. Approx. 4.7 VDC when LED should not light
U1B - pin 11		Set battery control to each of its positions. Measure with DVM	IND: 11.8 ± 0.5 VDC Other modes: 0 VDC
U3A-pin 3		Set battery control to each of its positions. Measure with DVM	SAVE: 0 VDC NORM: 0 VDC BAT: 11.8 ± 0.5 VDC TUNE or NO-MATCH: 0 VDC
U3B- pin 10		Use DVM	TUNE: 11.8 ± 0.5 VDC NO-MATCH: 11.8 ± 0.5 VDC Other modes: 0 VDC
U11- pin 11	BCD-to-decimal decoder	Use DVM	TUNE: 0V Other modes: 12 ± 0.5 VDC to 0 VDC
U5B-pin 9		Use DVM	FONL and NO-MATCH: 11.8 ± 0.5 VDC Other Modes: 0 V
U7A-pin 1	12.5-Hz oscillator	Measure level with oscilloscope. Measure frequency with frequency counter in NO-MATCH mode.	Waveform: approx. 10 Vp-p at 12.5 ± 2 Hz
U9A-pin 1	Clock oscillator	Measure level with oscilloscope. Measure frequency with frequency counter in IND and BAT mode.	Waveform: approx. 10Vp-p at 40 ± 5 kHz 
Q4/PIN 6	Step generator	Measure with oscilloscope in IND mode.	11 V max. Repetition rate approx. 4.5 kHz. 
P4/No.1, P3/No.30	FO, UNLOCK	Measure the DC voltage in the FONL mode	11.5 ± 0.5 VDC

4-16. Front Panel Assembly 1A1

The panel is tested by checking continuity of connections by an ohmmeter. The check is made with the panel separated from the receiver-transmitter chassis. Refer to fig. 2-80 for panel schematic diagram.

Test Point	Function	Measurement Method	Result
P4/No.2, P3/No.29	TUNE	Measure the DC voltage in the TUNE mode.	11.2 ± 0.5 VDC
P4/No.3, P3/No.56	BP (PA) INPUT	Check for continuity between P3/PIN 56 to J17/ PIN3 on the motherboard.	
P4/No.4, P3/No.40	USB	Set function selector to USB R/T and measure the DC voltage.	0 VDC.
P4/No.5	SAVE	Set battery control to SAVE and measure the DC voltage.	11.4 ± 0.5 VDC
P4/No.8, P3/No.53	+12V	Use DVM.	12 ± 0.5 VDC
P4/No.10	VOLUME	Rotate the VOLUME control from stop to stop and measure the DC voltage.	CCW 0 VDC CW 10.0 VDC min.
P4/No.11, P3/No.51	PHONE (OUT)	Measure in SSB receive mode.	Volume control fully CW: 2.45 VAC or more at 1 kHz.
P4/No.12 P3/No.52	PTT	Press PTT and measure the DC voltage.	0 VDC.
P4/No.13 P3/No.37	AM CONT	Set mode selector to AM and measure the DC voltage.	AM mode: 11.4 ± 0.5 VDC
P4/No.14, P3/No.49	MIC GND	Use DVM.	0 VDC
P4/No.15, P3/No.65	MIC (INPUT)	Connect audio generator to the input of audio junction box, adjust the signal to 100 mVp-p at 1 kHz and measure the voltage at J17/15 on the motherboard.	100 mVp-p

Test Point	Function	Measurement Method	Result
P4/No.16, P3/No.33	SSB (DATA)	Set mode selector to SSB and measure the DC voltage.	SSB mode: 11.4 ± 0.5 VDC
P4/No.17, P3/No.42	DIP	Use DVM	11.5 ± 0.5 VDC
P4/No.18, P3/No.19	TRANSIT	Change one of the first three digits of the frequency selector and measure the pulse levels.	Pulse width: 0.2 sec. During pulse, the voltage changes from 10.8 VDC to approx. 0 VDC. 
P4/No.19, P3/No.38	OFF CONT	Set function selector to OFF and measure the DC voltage.	0 VDC.
P4/No.20, P3/No.20	NCW	Set mode selector to NCW and measure the DC voltage.	11.4 ± 0.5 VDC
P4/No.21 P3/No.28	TX LEVEL (INPUT)	Check for continuity between P3/PIN 28 and J17/21	
P4/No.24 22 43 23 49	L1 L2 L3 L4 L5	Set battery control to BAT and vary power supply voltage from 21 to 29V.	The LEDs will light sequentially, in proportion to supply voltage.
P4/26, P3/54	ALC (INPUT)	Check for continuity between P3/PIN 54 and J17/26.	
P4/33, P3/41	R/T	Set the function selector to R/T and measure the DC voltage.	0.5 ± 0.2 VDC
P4/34, P3/21	WCW (CW)	Set mode selector to WCW and measure the DC voltage.	11.4 ± 0.5 VDC
P4/36, P3/22	DATA	Set mode selector to DATA and measure the DC voltage.	11.41 ± 0.5 VDC

Test Point	Function	Measurement Method	Result
P4/42, P3/16	+BAT IN	Use DVM.	26 VDC.
P4/44, P3/27	BAT CHK	Set battery control to BAT and measure the DC voltage.	11.4 ± 0.5 VDC
P4/45	+6V	Use DVM.	6 ± 0.2 VDC
P4/46, P3/55	PTT 12V	Measure the DC voltage in transmit mode.	10.8 ± 0.5 VDC
P4/52, P3/32	S-METER (OUTPUT)	Check for continuity between P3/PIN 32 and J17/52.	
P4/53, P3/48	NO-MATCH	Cause NO-MATCH and measure the DC voltage.	11.4 ± 0.5 VDC
P4/54, P3/66	GND	Use DVM.	0 VDC
P4/55, P3/14	GND	Use DVM.	0 VDC
P4/56, P3/57	FIX AUDIO (OUTPUT)	Measure at the connection between P3/pin 57 and pin A of AUDIO 1A2A3.	
P4/57, P3/13	IND	Set battery control to IND and measure the DC voltage.	11.4 ± 0.5 VDC
P4/58, P3/62	SQUELCH	Use DVM.	0 VDC
P4/59, P3/61	LT (M,N,BP)	Check for continuity between P3/61 and J17(59) on the motherboard.	
P4/62, P3/39	ON (CONT)	Set function selector to ON and measure the DC voltage.	0 VDC

Test Point	Function	Measurement Method	Result
P4/50, P3/5(X10) P4/35, P3/4(X11) P4/51, P3/12(X12) P4/6, P3/26(X13)	Bits of 100 Hz digit in BCD code, from frequency selector (X13-MSB)	Select each 100 Hz digit on the frequency selector. Check if appropriate BCD code is obtained. Measure with DVM. NOTE Logic "1": + 1 VDC Logic "0": less than 0.7VDC.	Digit X13 X12 X11 X10 0 0 0 0 0 1 0 0 0 1 2 0 0 1 0 3 0 0 1 1 4 0 1 0 0 5 0 1 0 1 6 0 1 1 0 7 0 1 1 1 8 1 0 0 0 9 1 0 0 1
P4/29, P3/34(X20) P4/7, P3/17(X21) P4/9, P3/16(X22) P4/30, P3/1(X23)	Bits of 1 kHz digit in BCD code, from frequency selector (X23-MSB)	Select each 10 kHz digit on the frequency selector. Check if appropriate BCD code is obtained. Measure with DVM.	Digit X23 X22 X21 X20 0 0 0 0 0 1 0 0 0 1 2 0 0 1 0 3 0 0 1 1 4 0 1 0 0 5 0 1 0 1 6 0 1 1 0 7 0 1 1 1 8 1 0 0 0 9 1 0 0 1
P4/31, P3/3(X30) P4/48, P3/11(X31) P4/47, P3/25(X32) P4/25, P3/45(X33)	Bits of 10 kHz digit in BCD code, from frequency selector (X33-MSB)	Select each 10 kHz digit on the frequency selector. Check if appropriate BCD code is obtained. Measure with DVM.	Digit X33 X32 X31 X30 0 0 0 0 0 1 0 0 0 1 2 0 0 1 0 3 0 0 1 1 4 0 1 0 0 5 0 1 0 1 6 0 1 1 0 7 0 1 1 1 8 1 0 0 0 9 1 0 0 1
P4/37, P3/58(X40) P4/39, P3/35(X41) P4/27, P3/18(X42) P4/32, P3/7(X43)	Bits of 100 kHz digit in BCD code, from frequency selector (X43-MSB)	Select each 10 kHz digit on the frequency selector. Check if appropriate BCD code is obtained. Measure with DVM.	Digit X43 X42 X41 X40 0 0 0 0 0 1 0 0 0 1 2 0 0 1 0 3 0 0 1 1 4 0 1 0 0 5 0 1 0 1 6 0 1 1 0 7 0 1 1 1 8 1 0 0 0 9 1 0 0 1
P4/28, P3/2(X50) P4/60, P3/10(X51) P4/40, P3/24(X52) P4/38, P3/44(X53)	Bits of 1 MHz digit in BCD code, from frequency selector (X53-MSB)	Select each 1 MHz digit on the frequency selector. Check if appropriate BCD code is obtained. Measure with DVM.	Digit X53 X52 X51 X50 0 0 0 0 0 1 0 0 0 1 2 0 0 1 0 3 0 0 1 1 4 0 1 0 0 5 0 1 0 1 6 0 1 1 0 7 0 1 1 1 8 1 0 0 0 9 1 0 0 1

Test Point	Function	Measurement Method	Result
P4/41, P3/36(X60) P4/61, P3/59(X61)	Bits of 10 MHz digit in BCD code, from frequency selector (X61-MSB)	Select each 10 MHz digit on the frequency selector. Check if appropriate BCD code is obtained. Measure with DVM.	Digit | X61 | X60 0 | 0 | 0 1 | 0 | 1 2 | 1 | 0

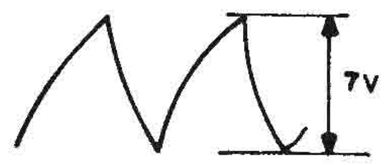
4-17. Module REF 1A3A6

a. Test Conditions

Equipment in receive mode.

b. Recommended Test Equipment

(1) Multimeter, Fluke model 8010A.
(2) Oscilloscope, Tektronix model 465B.
(3) Frequency counter, Hewlett-Packard model 5328, opt. 010.
(4) Spectrum analyzer, Hewlett-Packard 141T/8552B/8553B.

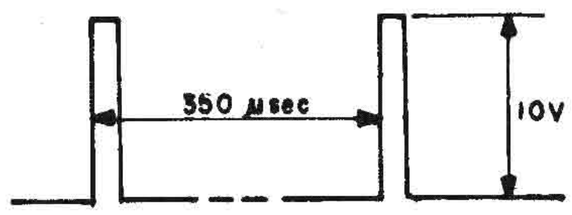
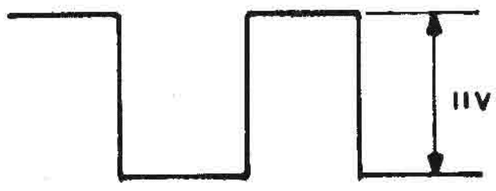
Test Point	Function	Measurement Method	Result
J,K,L (GND)	Ground	Use DVM	0 VDC
M (+12V)	12 VDC from PS 1A4	Use DVM	12 to 0.5 VDC
O (+15V)	15 VDC from PS 1A4	Use DVM	15 ± 0.5 VDC
Q (TP + 11)	Test point for checking internal 11 VDC	Use DVM	10.5 ± 0.5 VDC
N (TP TXCO)	Test point for checking TXCO output signal	Use oscilloscope with low capacitance probe to measure level, and frequency counter to measure frequency.	3.5MHz ± 3.5 Hz signal of approx. 7Vp-p 
G (INH F3)	Control signal from CONT 1A7 to inhibit generation of 5.25MHz	Set mode selector at each of its positions. Measure with DVM.	AM receive mode: less than 0.7 VDC. Other modes: 12 ± 0.5 VDC
E (5.25 MHz)	5.25MHz to IF 1A2A2	Use spectrum analyzer to measure level and frequency counter to measure frequency.	All modes except AM receive: 5.25MHz ± 10Hz sinewave at -13 to ± 3dBm

4-18. Module LOL 1A3A4

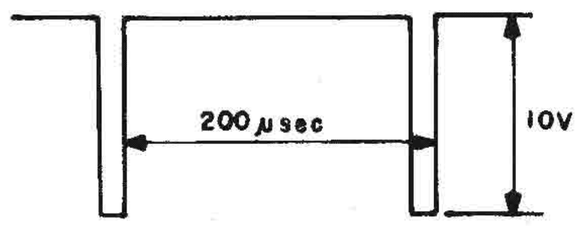
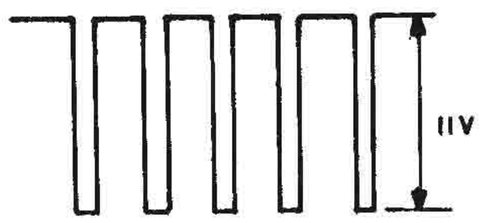
a. Test Conditions.
Equipment in receive mode.

b. Recommended Test Equipment.

(1) Multimeter, Fluke model 8010A.
(2) Oscilloscope, Tektronix model 465B.
(3) Frequency counter, Hewlett-Packard model 5328, opt. 010.

Test Point	Function	Measurement Method	Result
I (10.5MHz)	10.5MHz sinewave to USB 1A3A3	Use spectrum analyzer to measure level and frequency counter to measure frequency.	10.5 MHz ± 11 Hz sinewave at approx. -6 dBm.
F (20kHz)	20 kHz pulsed waveform to SUM 1A3A5	Observe waveform with oscilloscope. Check frequency with frequency counter.	Pulse waveform with repetition rate of 20kHz Pulse width: 350 nanosec. Peak amplitude: 10.5 ± 0.5 V 
A (5 kHz)	5 kHz square wave to LOL 1A3A4	Observe waveform with oscilloscope. Check frequency with frequency counter.	5 kHz square wave of approx. 11Vp-p
H (CW)	WCW/NCW control signal from mode selector	Use DVM	WCW, NCW modes: 10.5 ± 0.5 VDC Other modes: 0.7 VDC.
D (10kHz)	10 kHz square wave to PRE 1A2A4 in WCW/NCW modes	Observe waveform with oscilloscope. Check frequency with frequency counter.	WCW and NCW modes: 11 Vp-p square wave at 10 kHz. Other modes: no output signal 

Test Point	Function	Measurement Method	Result
L,M,N (GND)	Ground	Use DVM	0 VDC
Y (+15V)	15 VDC from PS 1A4	Use DVM	15 ± 0.5 VDC
X (+12V)	12 VDC from PS 1A4	Use DVM	12 ± 0.5 VDC
V (TEST +11V)	Test point for checking internal 11 VDC	Use DVM	10.5 ± 0.5 VDC
A (5K)	5kHz reference frequency from REF 1A3A6	Observe waveform with oscilloscope. Check frequency with frequency counter.	5 kHz square wave at approx. 11 Vp-p
P (X30)	LSB bit of 10kHz digit from frequency selector	Change the 10kHz digit on the frequency selector. Measure with DVM.	11.0 ± 0.5 VDC for each odd number. 0 VDC for each even number
R,S,O U (X23, X22,X21, X20)	Bits of 1kHz digit in BCD code from frequency selector (X23 - most significant bit)	Select each 1kHz digit on the frequency selector and check that appropriate BCD code is obtained	Digit R S O U 0 0 0 0 0 1 0 0 0 1 2 0 0 1 0 3 0 0 1 1 4 0 1 0 0 5 0 1 0 1 6 0 1 1 0 7 0 1 1 1 8 1 0 0 0 9 1 0 0 1 Logic "1":11 ± 1 VDC Logic "0":less than 0.7 VDC
K,I,E, G (X13, X12,X11, X10)	Bits of 100Hz digit in BCD code from frequency selector (X13 most significant bit)	Select each 100Hz digit On in the frequency selector and check that appropriate BCD code is obtained.	Digit K I E G 0 0 0 0 0 1 0 0 0 1 2 0 0 1 0 3 0 0 1 1 4 0 1 0 0 5 0 1 0 1 6 0 1 1 0 7 0 1 1 1 8 1 0 0 0 9 1 0 0 1

Test Point	Function	Measurement Method	Result
Q (LOF)	Pulsed waveform with repetition frequency between 30 and 49.9kHz to SUM 1A3A5	See test point C of SUM 1A3A5	
B (TEST VCO)	Test point for checking VCO signal. Pulsed waveform with repetition frequency between 1.5 and 2.495MHz	Change the last three digits of the frequency selector as above. Observe waveform with oscilloscope. Check frequency with frequency counter.	Repetition frequency exactly 50 times that of the LOF signal; amplitude approx. 4 Vp-p. For example, when the last 3 digits set on the frequency selector are 999, the frequency at test point Q is 49.9 kHz and that at test point B is 2495 kHz.
T (TEST P)	Test point for checking 5kHz pulsed waveform coming from the U4B	Check frequency with frequency counter.	Short negative pulses of approx. 10 Vp-p, with repetition rate of 5 kHz.
W (TEST Z)	Test point for checking 5kHz pulsed waveform coming from the variable divider	Observe amplitude with oscilloscope. Check frequency with frequency counter.	5 kHz pulsed waveform amplitude 10 Vp-p. Width of positive pulses is proportional to frequency increments 
C (TEST PHP)	Test point for checking output from phase comparator. High level indicates locked condition	Change frequency and observe short low level pulses while PLL is unlocked.	While PLL is unlocked: short 0 VDC pulse whose width is proportional to phase difference between output of variable divider and 5kHz reference. Locked condition: 11 VDC. 
D (TEST DC CONT)	Test point for checking DC control voltage to VCO	Use DVM	Changes in direct proportion to VCO frequency in the 0-11 VDC range.

4-19. Module USB 1A3A3

a. Test Conditions

Equipment in receive mode.

b. Recommended Test Equipment

(1) Multimeter, Fluke model 8010A.

(2) Oscilloscope, Tektronix model 465B.

(3) Frequency counter, Hewlett-Packard model 5328A, opt. 010.

(4) Spectrum analyzer, Hewlett-Packard model 141T/8552B/8554B.

Test Point	Function	Measurement Method	Result
K,M,I Q (GND)	Ground	Use DVM	0 VDC
H (+ 6 V)	6 VDC from PS 1A4	Use DVM	6 to 0.2 VDC
C (+12 V)	12 VDC from PS 1A4	Use DVM	12.0 ± 0.5 VDC
L (+26V)	26 VDC from PS 1A4	Use DVM	Approx. 26 V
B (TP + 5V)	Test point for checking internal 5 VDC	Same as for test point C.	5.2 ± 0.3 VDC
J (+17V)	17 VDC to VCP 1A3A1	Use DVM	17 ± 0.5 VDC
D (USB/LSB)	USB/LSB control signal from function selector	Set function selector to USB R/T and LSB R/T. Use DVM to measure the voltage.	USB : 1.2 ± 0.6 VDC LSB : 12.0 ± 0.5 VDC
E (10.5MHz)	10.5 MHz reference frequency from REF 1A3A6	Use spectrum analyzer to measure level, and frequency counter to check frequency.	10.5 MHz ± 11 Hz at +10 ± 3 dBm in USB mode
G 104.1 MHz	104.1 MHz sinewave to SUM 1A3A6	Use spectrum analyzer to measure level, and frequency counter to check frequency.	104.100 MHz ± 1.5 kHz at -16 ± 5 dBm in LSB mode
P18 (F2 OUT)	Sinewave at 114.6MHz (USB) or 104.1MHz (LSB) to MIXER 1A2A1	Use spectrum analyzer to measure level, and frequency counter to check frequency.	USB: 114.6 MHz ± 1.5 kHz LSB: 104.1 MHz ± 1.5 kHz Level: +2 to - 4 dBm

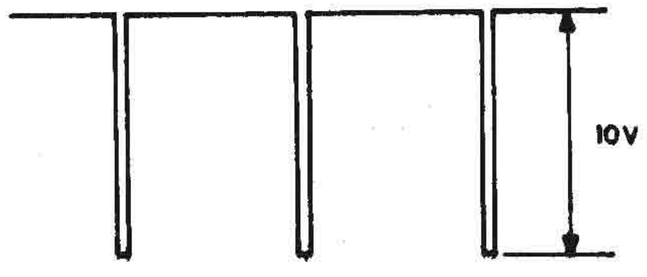
4-20. Module SUM 1A3A5

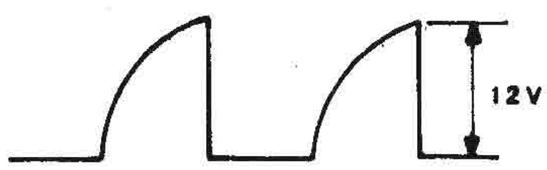
a. Test Conditions

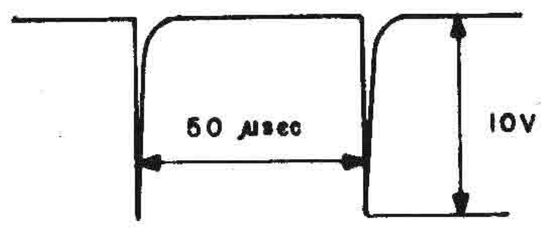
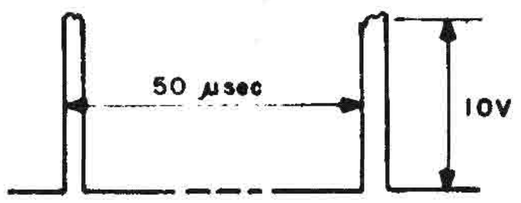
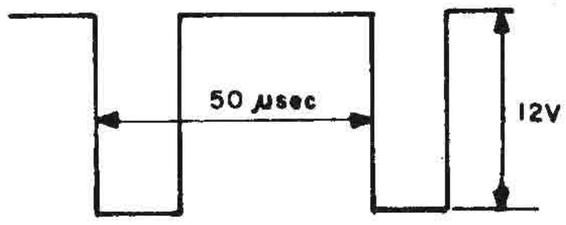
Equipment in receive mode.

b. Recommended Test Equipment

(1) Multimeter, Fluke model 8010A.
(2) Oscilloscope, Tektronix model 465B.
(3) Frequency counter, Hewlett-Packard model 5328A, opt. 010.
(4) Spectrum analyzer, Hewlett-Packard model 141T/8552B/8553B.

Test Point	Function	Measurement Method	Result
Y (GND)	Ground	Use DVM	0 VDC
G (+6V)	6 VDC from PS 1A4	Use DVM	6 ± 0.2 VDC
V (+12V)	12 VDC from PS 1A4	Use DVM	12 ± 0.5 VDC
O (+15V)	15 VDC from PS 1A4	Use DVM	15 ± 0.5 VDC
D (+5V-TEST)	Test point for checking internal 5 VDC	Use DVM	5 ± 0.2 VDC
K (+14V-TEST)	Test point for checking internal 14 VDC	Use DVM	14 ± 0.5 VDC
I (104.1 MHz)	104.1 MHz sinewave from USB 1A3A5	Use spectrum analyzer to measure level and frequency counter to measure frequency.	104.1 MHz ± 1.5 kHz at -16 ± 5 dBm
C (LOF)	Pulsed waveform with repetition rate between 30.0 and 49.9 kHz from LOL 1A3A4	Vary the last three digits of the frequency selector.	Pulsed waveform with repetition rate between 30 and 49.9 kHz. Pulse amplitude 10 Vp-p. See table below. 

Test Point	Function	Measurement Method	Result
C LOF (Cont'd)			Last Three Digits of Selected Frequency / LOF Frequency 000 30.000kHz 010 31.000kHz 020 32.000kHz 030 33.000kHz 040 34.000kHz 050 35.000kHz 060 36.000kHz 070 37.000kHz 080 38.000kHz 090 39.000kHz 100 40.000kHz 110 41.000kHz 120 42.000kHz 130 43.000kHz 140 44.000kHz 150 45.000kHz 160 46.000kHz 170 47.000kHz 180 48.000kHz 190 49.000kHz 191 49.100kHz 192 49.200kHz 193 49.300kHz 194 49.400kHz 195 49.500kHz 196 49.600kHz 197 49.700kHz 198 49.800kHz 199 49.900kHz
M (SUMF)	104.130 MHz sinewave to VCP 1A3A1	Use spectrum analyzer to measure level.	-4 to - 8 dBm
B (TEST DIFF FREQ.)	Test point for checking frequency difference between SUMF output and 104.1MHz input	Observe waveform with oscilloscope. Measure frequency with frequency counter.	Pulsed waveform with repetition rate from 30 to 49.9 kHz. Amplitude: approx. 12Vp-p 
F (TEST SUM PHASE PULSE)	Test point for checking phase comparator	Change frequency and observe short low level pulses while PLL is unlocked. Observe waveform with oscilloscope. Measure frequency with frequency counter.	Amplitude: +14 VDC for locked condition. Short pulses at 0 VDC while PLL is unlocked.

Test Point	Function	Measurement Method	Result
A (TEST DC CONTROL)	Test point for checking VCXO DC control voltage.	Use DVM	DC voltage in the 2 to 2 and 11 VDC, depending on VCXO frequency.
U (DEL VAD)	20kHz pulsed waveform from VCP 1A3A1	Observe waveform with oscilloscope. Measure frequency with frequency counter.	10Vp-p negative pulses at repetition rate of 20kHz and width of 50 microsec. 
S (20K)	20kHz pulsed waveform from REF 1A3A6	Observe waveform with oscilloscope. Measure frequency with frequency counter.	Pulsed waveform with repetition rate of 20kHz. Pulse width: 350 nsec. Peak to peak amplitude: approx. 10Vp-p. 
X (PHASE PULSE)	20kHz pulsed waveform from phase comparator	Change frequency and observe with oscilloscope.	About 12Vp-p at 20kHz. Duty cycle proportional to phase difference between rising edges of 20kHz and DEL VAD signals. 
W (UN-LOCKED)	Control signal to PANEL 1A1, CONT 1A7 and LORD 1A5A2	Change frequency. Use oscilloscope to observe waveform.	Locked condition: 0.7 VDC. Unlocked condition, shortly after frequency change: approx. 12 VDC.
Q3/pin b	Output filter: SUMF	Measure with spectrum analyzer.	-20 ± 5 dBm at 104.13 MHz
U1/pin 8	MIXER input	Measure with spectrum analyzer.	-16 ± 4 dBm at 104.13 MHz
Q5/pin b	MIXER output	Measure with oscilloscope.	0.4 ± 0.1 Vp-p sinewave

4-21. Module VAD 1A3A2

a. Test Conditions

Equipment in receive mode.

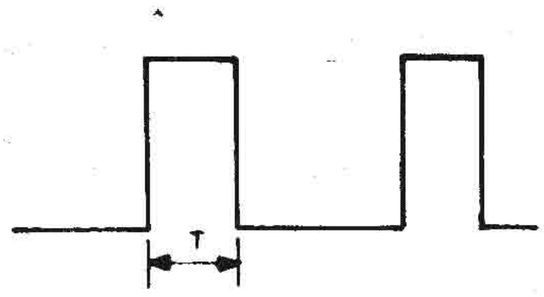
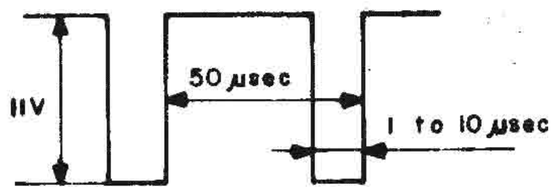
b. Recommended Test Equipment

(1) Multimeter, Fluke model 8010A.

(2) Oscilloscope, Tektronix model 465B.

(3) Frequency counter, Hewlett-Packard model 5328A, opt. 010.

Test Point	Function	Measurement Method	Result
P,L,N (GND)	Ground	Use DVM	0 VDC
0 +12V	12VDC from PS 1A4	Use DVM	12 ± 0.5 VDC
H (+6V)	6VDC from PS 1A4	Use DVM	6 ± 0.2 VDC
R (+6V SW)	Internal 6VDC to VCP 1A3A1	Use DVM	5 ± 0.2 VDC
T (DIF)	Sinewave from VCP 1A3A1 at frequency equal to difference between F1 and SUMF frequencies	Use spectrum analyzer to measure level, and frequency counter to check frequency.	7.22 to 35.20 MHz at +1 to -2 dBm. Frequency exact multiple of 20kHz. Frequency ratio is determined by frequency selector (see table for test point B).
C,E,G (X33,X32 X31)	Three most significant bits of 10 kHz digit in BCD code from frequency selector (X33-MSB)	Select each 10 kHz even digit on the frequency selector. Check if appropriate BCD code is obtained. Measure with DVM.	Freq C E G XXX00K 0 0 0 XXX20K 0 0 1 XXX40K 0 1 0 XXX60K 0 1 1 XXX80K 1 0 0 Logic "1": 10 to 12 VDC. Logic "0": less than 0.7 VDC.
K,I,Q,M (X43,X42 X41,X40)	Bits of 100 kHz digit in BCD code, from frequency selector (X43-MSB)	Select each 100kHz digit in the frequency selector. Check if appropriate BCD code is obtained. Measure with DVM.	Freq K I Q M XX000K 0 0 0 0 XX100K 0 0 0 1 XX300K 0 0 1 1 XX500K 0 1 0 1 XX700K 0 1 1 1 XX900K 1 0 0 1
O,S,Y,U (X53,X52 X51,X50)	Bits of 1 MHz digit in BCD code from frequency selector (X53-MSB)	Select each 1MHz digit in the frequency selector. Check if appropriate BCD code is obtained. Measure with DVM.	Freq O S Y U X0000M 0 0 0 0 X2000M 0 0 1 0 X3000M 0 0 1 1 X5000M 0 1 0 1 X7000M 0 1 1 1 X9000M 1 0 0 1

Test Point	Function	Measurement Method	Result
W,V (X60,X61)	Bits of 10MHz digit from frequency selector (X61-MSB)	Select each 10MHz digit on the frequency selector (0,1 or 2). Check if appropriate BCD code is obtained. Measure with DVM.	Freq V W 00XXX 0 0 10XXXM 0 1 20XXXM 1 0 X61 can be 9.5 ± 0.5 VDC
B (VAD PULSE)	20kHz to VCP 1A3A1	Change one or more of the first four digits on the frequency selector. Observe waveform with oscilloscope.	Width of positive pulse (T) is proportional to frequency increments. 
A (TP 10/11)	Test the point for checking the control line (PE2) of prescaler U1	Use oscilloscope. Select frequency and measure the pulse at A.	11 Vp-p pulsed waveform . Width varies between 1 to 10 microsec. Repetition: 50 microsec. 
X (TP PRS)	Test point for checking the output frequency of the prescaler	Set 2.0000 MHz on the frequency selector. Use counter and oscilloscope for measurements.	Frequency: 720 kHz Amplitude: 9.5 ± 0.5V p-p 

4-22. Module VCP 1A3A1

a. Test Conditions. Equipment in receive mode.

b. Recommended Test Equipment.

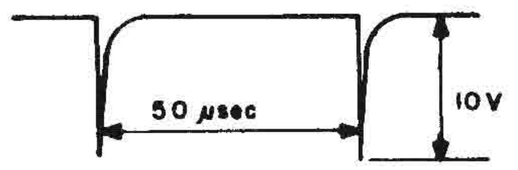
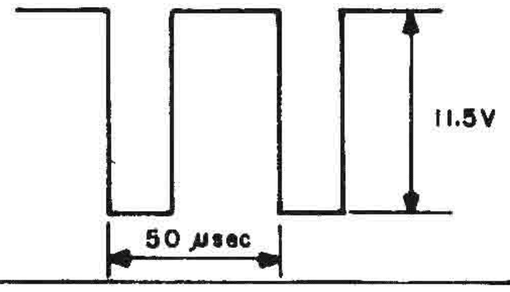
(1) Multimeter, Fluke model 8010A.

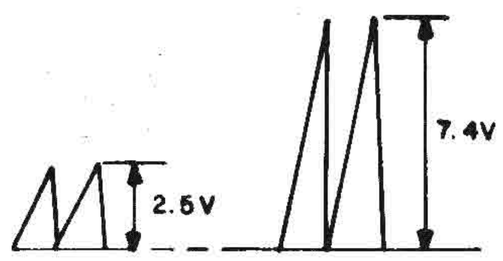
(2) Oscilloscope, Tektronix model 465B.

(3) Frequency counter, Hewlett-Packard model 532A, opt 010.

(4) Spectrum analyzer, Hewlett-Packard 141T8552B/8554B.

Test Point	Function	Measurement Method	Result
F,P,R,K,L, B,H,I	Ground	Use DVM	0 VDC

Test Point	Function	Measurement Method	Result
C (+15V)	15 VDC from PS 1A4	Use DVM	15 ± 0.5 VDC
O (+6V)	6 VDC from PS 1A4	Use DVM	6 ± 0.2 VDC
U (-10V)	-10 VDC from PS 1A4	Use DVM	-10 ± 0.5 VDC
Q (+17V)	17VDC from USB 1A3A3	Use DVM	17.0 ± 0.5 VDC
D (+6V SW)	6VDC from VAD 1A3A2	Use DVM	5 ± 0.2 VDC
J (SUMF)	104.130 to 104.149.9 MHz sinewave from module SUM 1A3A5	Spectrum analyzer	-4 to -8dBm
W (DELAYED VAD)	20 kHz pulsed signal to SUM 1A3A5	Oscilloscope	Approx. 10Vp-p negative pulses; repetition rate of 20 kHz. 
a (PHASE PULSE)	20 kHz pulsed signal from SUM 1A3A5, with duty cycle proportional to phase difference between DEL VAD and 20kHz reference.	Oscilloscope	Approx. 11.5Vp-p at 20 kHz. 
V,T,B,d (X53, X52, X51, X50)	Bits of 1 MHz digit in BCD code from frequency selector (X53 - most significant bit).	Select each 1-MHz digit on the frequency selector. Check if appropriate BCD code is obtained. Measure with DVM.	Approx. 12 VDC if bit is 1. 0 VDC if bit is 0.
Z,X (X61,X60)	Bits of 10 MHz digits from frequency selector X61 - (most significant bit).	Select each 10-MHz digit on the frequency selector. Check if appropriate BCD code is obtained.	Approx. 10 VDC if bit is 1. 0 VDC if bit is 0

Test Point	Function	Measurement Method	Result
F1 (Connector designated F1)	Sinewave signal to MIXER 1A2A1	Disconnect J21 and measure the frequency with counter. Measure level with spectrum analyzer.	Frequency exactly 109.35MHz higher than operating frequency (from 111.35MHz at 2MHz to 139.34MHz at 29.99MHz). Level -2 to +6 dBm.
F (DIF OUT)	Sinewave signal to VAD 1A3A2 at frequency equal to difference between F1 and SUMF frequencies.	Use spectrum analyzer to measure level and frequency counter to check frequency.	From 7.22 MHz (at 2MHz) to 35.2 MHz (at 29.99 MHz) level +1dBm to -7 dBm.
c (TEST RAMP)	Test point for checking ramp voltage on C7.	Change frequency and observe waveform with oscilloscope.	20 kHz truncated ramp, which rises from the appearance of each 20K pulse until the VAD pulse, and falls rapidly with each PHASE-PULSE pulse. 
S (TP PS CONTROL)	Test point for checking VCO DC control voltage to VCO	Change frequency. Measure with DVM.	2.8 to 8.5 VDC, depending on frequency.
E (TEST 5V)	Test point for checking 5 VDC.	Use DVM	5.1 ± 0.2 VDC
e (TEST V1)	Test point for checking 15 VDC	Use DVM	15.3 ± 0.7 VDC
g (TEST V2)	Test point for checking 13 VDC	Use DVM	13.5 ± 1 VDC

4-23. Alignment Following Replacement of Modules

a. Table 4-8 below lists the alignment procedures to be carried out on the RT-936/PRC-174 after replacement of modules as a result of troubleshooting.

Table 4-8. Alignment Procedures Following Replacement of Modules

Replaced Module	Alignment Procedure	Location
Mixer 1A2A1	ALC and AGC	Table 4-4, item 2
IF 1A2A2	AGC	Table 4-5, item 2
AUDIO 1A2A3	Squelch	Table 4-5, item 2
PRE 1A2A4	ALC	Table 4-4, item 5
SNF 1A5A3	ALC	Table 4-4, item 2
PA 1A6	ALC	Table 4-4, item 2